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A Fully Analog Implementation of Model Predictive Control With Application to Buck Converters

Simone Pirrera*, Lorenzo Calogero†, Francesco Gabriele‡, Diego Regruto*, Alessandro Rizzo§ and Gianluca Setti¶

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Abstract

This paper proposes a novel approach to design analog electronic circuits that implement Model Predictive Control (MPC) policies for dynamical systems described by affine models. Effective approaches to define a reduced-complexity explicit MPC are combined and applied to realize an analog circuit comprising a limited set of low-latency, commercially available components. The practical feasibility and effectiveness of the proposed approach are demonstrated through its application in the design of a novel controller for DC-DC Buck converters. We formally analyze the stability of the resulting system and conduct extensive numerical simulations to demonstrate the control system's performance in rejecting line and load disturbances.

Keywords: Model Predictive Control, Analog Implementation, DC-DC Buck Converters.

1 Introduction

Model predictive control (MPC) is one of the most widely adopted control techniques today, due to its flexibility to adapt to plants of diverse nature and, at the same time, to handling constraints [1]. Despite these desirable features, the practical implementation of MPC is not straightforward. First, the typical implementation of MPC imposes a significant overhead in terms of costs and circuit area due to the need to employ expensive digital hardware, including analog-to-digital converters (ADC), digital-to-analog converters (DAC), and a computing device, making the overall system too expensive for mass production, where a limited-budget design is often a primary requirement. Second, despite rapid advances in the development of novel algorithms for convex optimization [2, 3], the need to solve quadratic programming (QP) problems at each iteration renders the solution infeasible for systems exhibiting fast dynamics.

A widely adopted methodology, known for achieving significant computational efficiencies, involves the formulation of an explicit MPC (EMPC) control law. As demonstrated in [4, 5], a piecewise affine (PWA) function can be computed offline and used to define the MPC control input, obviating the need for online optimization. Although several algorithms have been proposed to efficiently compute the EMPC control law [6, 7, 8], the EMPC approach still raises criticalities in budget-constrained and fast-sampled applications. On the one hand, the need for digital hardware persists; on the other hand, when the PWA function is defined by several regions, its real-time evaluation may remain critical: the parameters defining the function may exceed the hardware storage capacity, and identifying the region containing the current parameter may be computationally expensive [9]. These issues are reported, e.g., in [10], which applies EMPC to Buck converters. A viable alternative is brought by custom hardware implementations. Notable results in this direction are [11] and [12]. In [11] the authors use a field-programmable gate array to implement an active-set algorithm to solve the QP, but its performance remains limited by the need to perform analog-to-digital and digital-to-analog conversions. On the other hand, [12] constructs an analog circuit that solves QP, thereby making it suitable for MPC implementations. However, the applicability of this method is limited by the resulting circuit complexity.

Here, we present a novel, general methodology for designing a fully analog electronic circuit that implements MPC controllers for affine systems. First, we derive an explicit MPC control law and apply state-of-the-art approaches to describe the controller in terms of a limited number of regions. Next, we define the circuit implementation using commercially available low-latency components: comparators, resistors, operational amplifiers (OP-AMPs), and one multiplexer (MUX).

Furthermore, the effectiveness and feasibility of our approach are validated through the application to the control of DC-DC Buck converters. Buck converters are devices that regulate a supply voltage to a lower, constant value. Buck converters are used in various applications, including the biomedical and renewable energy fields; see, e.g., [13, 14, 15]. Accurately regulating the output voltage in Buck converters is fun-

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damental for the proper operation of the devices supplied by the converter. However, the tracking accuracy of the converter is hindered by unpredictable and sudden variations of the input supply voltage (line disturbances) and of the current drawn by the load (load disturbances) [16, 17]. To improve tracking performance, several approaches have been considered. As to line disturbance attenuation, we mention the popular feedforwarding technique [18]. In contrast, the problem of attenuating the effects of load disturbances is more challenging. It has been addressed by methods based on the design of circuitry to modify either the feedback signal or the pulse width of the Pulse Width Modulated (PWM) signal in response to load variations; see [19, 20] for recent works in this direction. However, these solutions lack solid theoretical foundations. Other approaches aim at estimating the output current disturbance to apply a proper feedforward action. Among these, we mention the extended state observer [21], generalized proportional-integral observer [22], and the load estimator-compensator (LEC) [17] approaches. These solutions are often combined with optimal control design: [21] uses linear quadratic gaussian control in conjunction with the extended state observer, and [17] uses $\mathcal{H}_\infty$-optimal voltage mode control (VMC) in conjunction with the LEC.

For Buck converters, the MPC controller design approach is particularly compelling due to its ability to directly handle the limitation imposed by input duty-cycle saturation between 0% and 100%. The application of MPC to Buck converters has been explored in several contributions, e.g., [23, 24, 25, 26]. These works report successful results in practical implementations, but, in all cases, the sampling frequency must be kept low to ensure convergence of the optimization algorithm. More specifically, [23, 24], and [26] report switching frequencies limited to 10 kHz, 20 kHz, and 25 kHz, respectively. Similar considerations apply to [25], which implements the MPC using a field-programmable gate array.

To apply the proposed approach to DC-DC Buck converters, we first introduce a discrete-time (DT) mathematical model of the device and its linearization. Next, to ensure proper load-disturbance rejection performance, we use the load estimator proposed in [17], which enables a low-cost analog implementation. Finally, we apply the proposed analog EMPC design: thanks to the adopted region-reduction strategies, we observe a significant improvement over previous works on EMPC design for the Buck (see [10]), thus ensuring a low-cost circuit design and a faster implementation compared to the approach proposed in [12]. Furthermore, we provide a formal proof of the stability of the feedback control system's equilibrium point, robustly with respect to disturbances.

Our controller is validated through a comprehensive simulation study to demonstrate the feasibility and effectiveness of the proposed approach. We analyze system performance under parametric uncertainty in Buck component values using Monte Carlo simulations, considering both ceramic and electrolytic capacitor cases. Next, we perform an accurate low-level simulation utilizing the manufacturer's models of commercially available components, demonstrating the feasibility of the proposed method even in the presence of component non-idealities. The proposed analog implementation enables high-frequency sampling at 500 kHz, which is compatible with modern Buck designs and considerably improves upon previous solutions reported in [23, 24, 25, 26]. Our results indicate that the system exhibits outstanding disturbance-rejection performance, outperforming standard methods.

1.1 Outline

Sec. 2 reviews the standard formulation of the MPC problem. Sec. 3 expands on the proposed design method by proposing the EMPC formulation and its analog circuit implementation. In Sec. 4 we apply the proposed approach to the DC-DC Buck converter control problem: we model the system, detail how to estimate unmeasurable quantities, and provide stability guarantees. Sec. 5 depicts the obtained numerical results. Finally, Sec. 6 draws conclusions.

1.2 Notation

In the following, $x = [x_i]_{i=1}^N \in \mathbb{R}^{nN}$ is the vertical concatenation of the vectors $x_i \in \mathbb{R}^n$; $I_n \in \mathbb{R}^{n\times n}$ is the identity matrix; $\mathbf{0}_n, \mathbf{1}_n \in \mathbb{R}^n$ are the null and all-1 vectors, respectively; $\|x\|_M \doteq \|M^{1/2}x\|_2 = \sqrt{x^\top Mx}$ is the weighted norm of vector x, with weighting matrix M, and $\|A\|_M = \|M^{1/2}AM^{-1/2}\|_2$ is the induced weighted norm of matrix A; $\otimes$ is the Kronecker product; $e_n^{(m)} \in \mathbb{R}^n$ is the m-th vector of the standard Euclidean basis of $\mathbb{R}^n$; $E_n^{(m)} \in \mathbb{R}^{n\times n}$ is the matrix with 1s on the m-th subdiagonal and 0s elsewhere; $\odot$, $\oplus$, and $\overline{\star}$ are the Boolean (logic) AND, OR, and NOT operators, respectively.

2 MPC Problem Formulation

This section reviews the MPC formulation that we will consider throughout the remainder of the paper. Let us consider an n-dimensional discrete-time (DT) affine system, i.e.,

$$x_{k+1} = Ax_k + Bu_k + B_\nu\nu_k + b, \tag{1a}$$
$$y_k = Cx_k + Du_k + D_\nu\nu_k + d, \tag{1b}$$

where $x \in \mathbb{R}^n$, $u \in \mathbb{R}^{n_u}$, and $y \in \mathbb{R}^{n_y}$ are the state, input, and output vectors, respectively, $\nu \in \mathbb{R}^{n_\nu}$ is a vector of exogenous disturbances, $A \in \mathbb{R}^{n\times n}$, $B \in \mathbb{R}^{n\times n_u}$, $B_\nu \in \mathbb{R}^{n\times n_\nu}$, $C \in \mathbb{R}^{n_y\times n}$, $D \in \mathbb{R}^{n_y\times n_u}$, and $D_\nu \in \mathbb{R}^{n_y\times n_u}$ are matrices describing the system dynamics, $b \in \mathbb{R}^n$ and $d \in \mathbb{R}^{n_y}$ are constant affine terms.

We define, for each $k \geq 0$, the MPC optimal control problem for system (1) as:

$$\min_{\hat{x},\hat{u},\hat{y}} \sum_{i=0}^{N_p-1} \left(\|\hat{y}_i - y_r\|_Q^2 + \|\hat{u}_i - u_r\|_R^2\right) + \sum_{i=1}^{N_p-1} \|\hat{u}_i - \hat{u}_{i-1}\|_{R_\Delta}^2, \tag{2a}$$
$$\text{s.t.} \quad \hat{x}_0 = x_k, \quad \hat{x}_{i+1} = A\hat{x}_i + B\hat{u}_i + B_\nu\nu_k + b, \tag{2b}$$
$$\hat{y}_i = C\hat{x}_i + D\hat{u}_i + D_\nu\nu_k + d, \tag{2c}$$

$$H_x\hat{x}_i \le h_x, \quad H_u\hat{u}_i \le h_u, \quad i = 0, \dots, N_p - 1. \tag{2d}$$

Here, the decision variables are the predicted state trajectory $\hat{x} = [\hat{x}_i]_{i=1}^{N_p} \in \mathbb{R}^{nN_p}$, the predicted output trajectory $\hat{y} = [\hat{y}_i]_{i=0}^{N_p-1} \in \mathbb{R}^{n_y N_p}$, and the input sequence $\hat{u} = [\hat{u}_i]_{i=0}^{N_p-1} \in \mathbb{R}^{n_u N_p}$, where N_p is the prediction horizon.

The cost function (2a) is composed of three terms: $\|\hat{y}_i - y_r\|_Q^2$ and $\|\hat{u}_i - u_r\|_R^2$ serve as regulation terms for the predicted output $\hat{y}_i$ and input $\hat{u}_i$ towards the constant reference output $y_r \in \mathbb{R}^{n_y}$ and input $u_r \in \mathbb{R}^{n_u}$, respectively, while $\|\hat{u}_i - \hat{u}_{i-1}\|_{R_\Delta}^2$ penalizes the variation in time of the inputs to obtain smoother predicted trajectories (see, e.g., [27, 28]). $Q, R_\Delta \succeq 0$ and $R \succ 0$ are symmetric weighting matrices of suitable dimensions. We consider the following standard assumption on the reference (u_r, y_r):

Assumption 1. *The triple (u_r, x_r, y_r) is an equilibrium of the undisturbed system* (1)*, i.e., with $\nu_k = \mathbf{0}_{n_\nu}$ it holds that*

$$x_r = Ax_r + Bu_r + b, \tag{3a}$$
$$y_r = Cx_r + Du_r + d. \tag{3b}$$

The equality constraints (2b), (2c) serve as the MPC prediction model, which corresponds to model (1). Eq. (2d) imposes linear inequality constraints: $N_{c_x} \in \mathbb{N}$ on the states defined by $H_x \in \mathbb{R}^{N_{c_x}, n}$ and $h_x \in \mathbb{R}^{N_{c_x}}$, and $N_{c_u} \in \mathbb{N}$ on the input defined by $H_u \in \mathbb{R}^{N_{c_u}, n_u}$ and $h_u \in \mathbb{R}^{N_{c_u}}$. The considered MPC formulation is general and can incorporate additional features such as robustness and safety constraints. Importantly, these do not affect the proposed analog implementation.

By assuming that all states and disturbances are available for measurement, we define the control law by using the one-step receding horizon policy, i.e., at each time instant k, the first optimal input $u_k^* \doteq \hat{u}_0^*$ given by the MPC problem (2) is applied to the plant (1) over the time interval $I_k \doteq [kT, (k+1)T)$. This strategy implicitly defines a static state-feedback control policy $\pi : \mathbb{R}^{n_p} \to \mathbb{R}^{n_u}$, i.e.,

$$u_k^* = \pi(p_k), \tag{4}$$

where $p_k \doteq [x_k^\top,\ \nu_k^\top]^\top \in \mathbb{R}^{n_p}$ is the vector of variables acting as parameters in problem (2), with $n_p = n + n_\nu$.

The MPC problem (2) can be rewritten in a more compact QP form, comprising only $\hat{u}$ as decision variables, i.e.,

$$\min_{\hat{u}} \quad \frac{1}{2}\hat{u}^\top H\hat{u} + (Fp_k + c)^\top \hat{u} \tag{5a}$$
$$\text{s.t.} \quad G\hat{u} \le w + Kp_k, \tag{5b}$$

where $H \in \mathbb{R}^{n_u N_p \times n_u N_p}$, $F \in \mathbb{R}^{n_u N_p \times n_p}$, $c \in \mathbb{R}^{n_u N_p}$, $G \in \mathbb{R}^{q \times N_p n_u}$ and $w \in \mathbb{R}^q$. This transformation involves eliminating the constraints (2b), (2c), and rewriting Eqs. (2a) and (2d) as functions of $\hat{u}$ and p_k only; see, e.g., [4]. The corresponding development is reported in Appendix A.

As shown in [9], the positive definiteness of Q, R, and R_Δ implies $H = H^\top \succ 0$. Hence, for any p_k, the MPC problem (5) is strongly convex, thereby admitting a unique global optimum $\hat{u}^*$ (see, e.g., [29]). Consequently, the policy π is well-defined and uniquely maps p_k to the control input $u_k^* = \hat{u}_0^*$, according to the receding horizon scheme.

Proposition 1. *Given Assumption 1, assume that x_r and u_r satisfy the constraints* (2d)*, and let $p_k = [x_r^\top, \mathbf{0}_{n_\nu}^\top]^\top$. Then, problem* (5) *is uniquely solved by $\hat{u}^* = \mathbf{1}_{N_p} \otimes u_r$.*

Proof. By the equivalence of problems (2) and (5), they share the same unique solution $\hat{u}^*$. Then, $\hat{x}_{i+1} = x_r$, $\hat{u}_i = u_r$, $i = 0, \dots, N_p - 1$, is the global minimizer of problem (2) since, by assumption, it is a feasible trajectory under the constraints (2b) and achieves zero cost. Therefore, $\hat{u}^* = \mathbf{1}_{N_p} \otimes u_r$ uniquely solves problem (5) with $p_k = [x_r^\top, \mathbf{0}_{n_\nu}^\top]^\top$. □

Proposition 2. *The reference output y_r is an equilibrium of the closed-loop undisturbed system* (1)*,* (4)*, i.e.,*

$$x_r = Ax_r + B\pi([x_r^\top, \mathbf{0}_{n_\nu}^\top]^\top) + b, \tag{6a}$$
$$y_r = Cx_r + D\pi([x_r^\top, \mathbf{0}_{n_\nu}^\top]^\top) + d. \tag{6b}$$

Proof. This result is a direct consequence of Assumption 1 and Proposition 1. □

3 Proposed Design Approach

This section proposes a methodology for implementing MPC as a fully analog circuit. We first exploit the EMPC closed-form formulation and apply complexity-reduction, then describe the corresponding circuit implementation.

3.1 Reduced-Complexity EMPC Design

We start our design by explicitly representing the MPC policy (4) in closed form as stated in the following theorem.

Theorem 1 (Explicit MPC [5])**.** *Assume that the parameters p_k lie in a convex polytope $\mathcal{P} \subseteq \mathbb{R}^{n_p}$. Then, the optimal solution $u_k^* = \hat{u}_0^*$ of the MPC problem* (5)*, at each $k \ge 0$, is given by the policy π in Eq.* (4)*, where:*

(i) $\pi : \mathcal{P} \to \mathcal{U}$ is a continuous piecewise affine (PWA) function, defined over R regions $\mathcal{R}_i$, $i = 1, \dots, R$, i.e.,

$$u_k^* = \pi(p_k) = K_i p_k + l_i \quad \text{if} \quad p_k \in \mathcal{R}_i. \tag{7}$$

(ii) The regions $(\mathcal{R}_i)_{i=1}^R$ are full-dimensional polytopes with non-overlapping interiors, forming a partition of $\mathcal{P}$, i.e.,

$$\bigcup_{i=1}^R \mathcal{R}_i = \mathcal{P}, \quad \operatorname{int}(\mathcal{R}_i) \cap \operatorname{int}(\mathcal{R}_j) = \emptyset, \ \ i \ne j. \tag{8}$$

Replacing the MPC problem (5) with the EMPC policy (4) offers the significant advantage of being able to compute the optimal control input using a static function. As detailed in Sec. 3.2, the structure of Eq. (7) enables implementing the policy (4) using only static analog components, yielding quasi-instantaneous function evaluation.

Yet, the size and cost of the resulting analog circuit is directly influenced by the number of regions R describing Eq. (7). To minimize costs, it is essential to reduce them. As shown in [30], R equals the number of possible combinations of active constraints for problem (5). Thus, a bound on R is

$$R \leq \sum_{i=0}^{n_u N_p} \binom{q}{i}, \tag{9}$$

because at most $n_u N_p$ constraints can be active at the optimum. In most cases, R is much smaller, as most of the constraint combinations are never active at optimality. In the following, we illustrate how to reduce the number of regions using four complexity reduction strategies.

3.1.1 Move Blocking Strategy

The move blocking strategy [31] reduces the complexity of the MPC problem (5) by defining a linear map between the input sequence $\hat{u}$ and a smaller set of decision variables $u_c \in \mathbb{R}^{n_u N_c}$, $N_c < N_p$, as

$$\hat{u} = T u_c, \quad T \in \mathbb{R}^{N_p n_u \times N_c n_u}, \tag{10}$$

where the matrix T is a lower-trapezoidal design parameter. A popular choice is

$$T = \begin{bmatrix} I_{N_c-1} & \mathbf{0} \\ \mathbf{0} & \mathbf{1}_{N_p-N_c+1} \end{bmatrix} \otimes I_{n_u}, \tag{11}$$

so that the first $N_c - 1$ samples of $\hat{u}$ are independent, while the samples from N_c-1 to N_p-1 are bound to the same value. Eq. (10) can be directly replaced into the MPC problem (5), obtaining its reduced version with variables u_c, i.e.,

$$\min_{u_c} \quad \frac{1}{2} u_c^\top (T^\top H T) u_c + (T^\top F p_k + T^\top c)^\top u_c \tag{12a}$$

$$\text{s.t.} \quad G T u_c \leq w + K p_k. \tag{12b}$$

Notice that all the fundamental properties of the MPC formulation (5), such as its strong convexity, are preserved. Instead, the optimal solution is not. Still, T and N_c can always be tuned to ensure a negligible closed-loop performance decrease.

The move blocking strategy directly reduces the number of regions R in the EMPC policy (4). Indeed, the number of decision variables reduces from $N_p n_u$ in Eq. (5) to $N_c n_u$ in Eq. (12), yielding the tighter upper bound

$$R \leq \sum\nolimits_{i=0}^{n_u N_c} \binom{q}{i} < \sum\nolimits_{i=0}^{n_u N_p} \binom{q}{i}. \tag{13}$$

For more details on this aspect, we refer the reader to [32].

3.1.2 Optimal Merging of Regions

In the EMPC policy (4), regions sharing the same affine control law can be merged together, provided that such a merging produces a convex polytope [9]. To this end, [33] proposes an optimal merging algorithm named non-disjoint optimal merging, that yields the minimal number of merged regions while allowing for possible overlaps. This latter aspect poses no issue when evaluating the simplified EMPC policy, as overlaps always share the same affine function. Importantly, allowing non-disjoint polytopes leads to solutions with fewer regions and fewer facets (i.e., fewer inequalities defining the region) compared to the case where we restrict to disjoint polytopes [33]. The non-disjoint optimal merging algorithm is implemented in the Multi-Parametric Toolbox (MPT) for MATLAB [34].

3.1.3 Hyperplane Separation of Saturated Regions

The MPC formulation (2) typically accounts for lower and upper bounds on the input, i.e., Eq. (2d) includes constraints of the kind $u_{\text{lb}} \leq \hat{u}_i \leq u_{\text{ub}}$ for some $u_{\text{lb}}, u_{\text{ub}} \in \mathbb{R}^{n_u}$. In this case, the EMPC policy (4) naturally leads to several regions where the control law is constantly equal to either u_{lb} or u_{ub}. Henceforth, such regions are referred to as saturated regions; the other regions, in contrast, are called unsaturated regions.

Denoting with I_{lb} and I_{ub} the sets of indices of the regions saturated at the lower and upper bound, respectively, we define

$$\underline{\mathcal{S}} \doteq \bigcup\nolimits_{i \in I_{\text{lb}}} \mathcal{R}_i, \quad \overline{\mathcal{S}} \doteq \bigcup\nolimits_{i \in I_{\text{ub}}} \mathcal{R}_i. \tag{14}$$

It is worth noticing that the sets $\underline{\mathcal{S}}$ and $\overline{\mathcal{S}}$ are, in general, non-convex and, possibly, non-connected. Also, we define $I_{\text{unsat}} \doteq \{1, \dots, R\} \setminus (I_{\text{lb}} \cup I_{\text{ub}})$ as the set of indices of the unsaturated regions, and the union of unsaturated regions as

$$\mathcal{R}_{\text{unsat}} \doteq \bigcup\nolimits_{i \in I_{\text{unsat}}} \mathcal{R}_i. \tag{15}$$

By Theorem 1, the continuity of the EMPC policy ensures that $\underline{\mathcal{S}} \cap \overline{\mathcal{S}} = \emptyset$. Also, since by Theorem 1 the polytopes $\mathcal{R}_i$ do not overlap, it holds that $\mathcal{P} = \underline{\mathcal{S}} \cup (\mathcal{R}_{\text{unsat}}) \cup \overline{\mathcal{S}}$, $\text{int}(\mathcal{R}_{\text{unsat}}) \cap \text{int}(\underline{\mathcal{S}}) = \emptyset$, $\text{int}(\mathcal{R}_{\text{unsat}}) \cap \text{int}(\overline{\mathcal{S}}) = \emptyset$. With this notation, the MPC policy in Eq. (4) is rewritten as:

$$\pi(p_k) = \begin{cases} K_i p_k + l_i & \text{if } p_k \in \mathcal{R}_i,\ i \in I_{\text{unsat}}, \\ u_{\text{lb}} & \text{if } p_k \in \underline{\mathcal{S}}, \\ u_{\text{ub}} & \text{if } p_k \in \overline{\mathcal{S}}. \end{cases} \tag{16}$$

We reduce the complexity of Eq. (16) by removing the saturated regions. This is achieved by introducing a function $\sigma : \mathcal{P} \to \mathbb{R}$, called *separation function*, that separates the sets $\underline{\mathcal{S}}$ and $\overline{\mathcal{S}}$, according to its sign, i.e.,

$$\sigma(p) < 0, \ \forall p \in \underline{\mathcal{S}}, \quad \sigma(p) > 0, \ \forall p \in \overline{\mathcal{S}}. \tag{17}$$

Using σ, we can equivalently rewrite Eq. (16) as

$$\pi(p_k) = \begin{cases} K_i p_k + l_i & \text{if } p_k \in \mathcal{R}_i,\ i \in I_{\text{unsat}}, \\ u_{\text{lb}} & \text{if } p_k \notin \mathcal{R}_{\text{unsat}},\ \sigma(p_k) < 0, \\ u_{\text{ub}} & \text{if } p_k \notin \mathcal{R}_{\text{unsat}},\ \sigma(p_k) > 0. \end{cases} \tag{18}$$

The formulation (18) involves a reduced number of regions, thanks to the removal of saturated regions. Still, for analog circuital implementation, we must ensure that σ is sufficiently "simple". Thus, in the following, we seek an affine separation function, i.e., $\sigma(p) = a^\top p + b$, and we present the following theorem, concerning its existence and computation:

Theorem 2 (Affine separation)**.** *Let $\mathcal{S}_1$ and $\mathcal{S}_2$ be the unions of two sets of polytopes, such that $\mathcal{S}_1 \cap \mathcal{S}_2 = \emptyset$. Let V_1 and V_2 be the sets of vertices of $\mathcal{S}_1$ and $\mathcal{S}_2$, respectively. Finally, let $\sigma(x) = a^\top x + b$ be an affine function. Then, σ separates $\mathcal{S}_1$ and $\mathcal{S}_2$, i.e.,*

$$\sigma(x) < 0, \ \forall\, x \in \mathcal{S}_1, \quad \sigma(x) > 0, \ \forall\, x \in \mathcal{S}_2, \tag{19}$$

if and only if the following linear program (LP) is feasible:

$$\max_{a,b,\varepsilon} \ \varepsilon, \tag{20a}$$

$$\text{s.t.} \ \ \varepsilon > 0, \quad \|a\|_\infty \leq 1 \tag{20b}$$

$$a^\top v^{(1)} + b \leq -\varepsilon, \quad \forall\, v^{(1)} \in V_1, \tag{20c}$$

$$a^\top v^{(2)} + b \geq \ \ \varepsilon, \quad \forall\, v^{(2)} \in V_2. \tag{20d}$$

Moreover, the separation function is given by $\sigma(x) = a^{*\top} x + b^*$, where $(a^*, b^*, \varepsilon^*)$ is the global optimum of problem (20).

Proof. ($\Rightarrow$) Since $V_1 \subset \mathcal{S}_1$ and $V_2 \subset \mathcal{S}_2$, Eq. (19) directly implies the feasibility condition of problem (20).
($\Leftarrow$) For all positive ε, feasibility of (a, b) implies

$$\sigma(v) < 0, \ \forall\, v \in V_1, \quad \sigma(v) > 0, \ \forall\, v \in V_2. \tag{21}$$

Next, we drop the subscripts 1 and 2 to consider both polytopes at the same time. Consider $\lambda \in \mathbb{R}^{|V|}$ such that $\lambda \geq 0$ and $\sum_{i=1}^{|V|} \lambda_i = 1$. Then, by Eq. (21), we have that

$$\lambda_i (a^\top v_i + b) \gtreqless 0, \quad \forall\, i \in \{1, \dots, |V|\} \tag{22a}$$

$$a^\top \sum\nolimits_{i=1}^{|V|} \lambda_i v_i + b \sum\nolimits_{i=1}^{|V|} \lambda_i \gtrless 0 \tag{22b}$$

$$a^\top x + b \gtrless 0, \tag{22c}$$

where $x = \sum_{i=1}^{|V|} \lambda_i v_i \in \mathrm{conv}(V)$, by definition of convex hull. In Eq. (22b), we drop the equality because at least one term of the sum is surely not null by construction. Since $\mathcal{S} \subseteq \mathrm{conv}(V)$, it holds that $x \in \mathcal{S}$, yielding Eq. (19). □

Remark 1. *The LP feasibility problem (20) provides the maximal separation margin $\varepsilon^* > 0$ between the two regions $\mathcal{S}_1$ and $\mathcal{S}_2$, and the separation hyperplane σ, thereby enhancing the robustness to manufacturing tolerances of the components related to the implementation of σ. The variable ϵ in the LP (20) acts as a tolerance margin for the separating condition. In general, the EMPC formulation (18) may admit infinite affine separation functions. Solving (20) enhances the robustness to component tolerances of the subsequent analog implementation by looking for the separation function that maximizes the distance between the separation hyperplane and the sets $\mathcal{S}_1$ and $\mathcal{S}_2$.*

Remark 2. *If the LP problem (20) does not admit a feasible solution, then there exists no affine function able to separate $\mathcal{S}_1$ and $\mathcal{S}_2$. In such cases, it is possible to resort to more complex separating functions, e.g., polynomial ones [35], whose analog circuital implementation will be the subject of future research. Nevertheless, for the application considered in this paper, we could find an affine separator for the EMPC policy (18) as shown in Sec. 4.*

Hyperplane separation of saturated regions is most effective when a significant proportion of the regions are saturated. Tighter constraints on the input and a smaller magnitude of the input weighting matrix R result in more regions becoming saturated [30], thus enhancing the effectiveness of this method.

3.1.4 Removal of Trivial Inequalities

The EMPC policy (4) is defined over the polytopic domain $\mathcal{P}$, by Theorem 1. The set $\mathcal{P}$ is typically specified by the user, based on prior knowledge of the admissible values that p_k can take. Thus, any parameter p_k considered in practice always belongs to $\mathcal{P}$. As a result, in the EMPC policy, the inequalities associated with the facets of $\mathcal{P}$ are trivial (always satisfied) and, therefore, can be removed.

The four reduction techniques are applied sequentially from the highest to lowest abstraction level. Move blocking modifies the optimization problem, defining the initial region partition. Optimal merging and hyperplane separation then reduce the number of regions while preserving the MPC formulation. Finally, removing trivial inequalities refines the geometric description of the remaining regions at the lowest level.

The proposed procedure is key to an efficient EMPC hardware implementation. Since each region and inequality map to circuit components, the reduction strategies directly reduce the required hardware complexity, as detailed below.

3.2 Circuital Implementation

This section presents the circuit implementation of the complexity-reduced EMPC policy, using only commercially available low-latency analog components.

We start by introducing an alternative description of the EMPC policy. Without loss of generality, let the unsaturated regions be indexed first, i.e., $I_{\text{unsat}} = \{1, \dots, N_{\text{unsat}}\}$, with $N_{\text{unsat}} \doteq |I_{\text{unsat}}|$, and let them be described as

$$\mathcal{R}_j = \{p_k \in \mathbb{R}^{n_p} : H_j p_k \leq h_j\}, \quad j = 1, \dots, N_{\text{unsat}}, \tag{23}$$

where $H_j \in \mathbb{R}^{N_j \times n_p}$, $h_j \in \mathbb{R}^{N_j}$, and N_j is the number of scalar inequalities defining region $\mathcal{R}_j$. Accordingly, we define the Boolean variables associated with each unsaturated region as

$$r_j = \begin{cases} 1 & \text{if } H_j p_k \leq h_j, \\ 0 & \text{otherwise,} \end{cases} \quad j = 1, \dots, N_{\text{unsat}}. \tag{24}$$

Given these, we define variables $\beta_i \in \{0, 1\}$ as

$$\beta_i = \bigoplus\nolimits_{j \in \mathcal{I}_i} r_j, \quad i \in I_{\text{unsat}}^{\text{unique}} \tag{25}$$

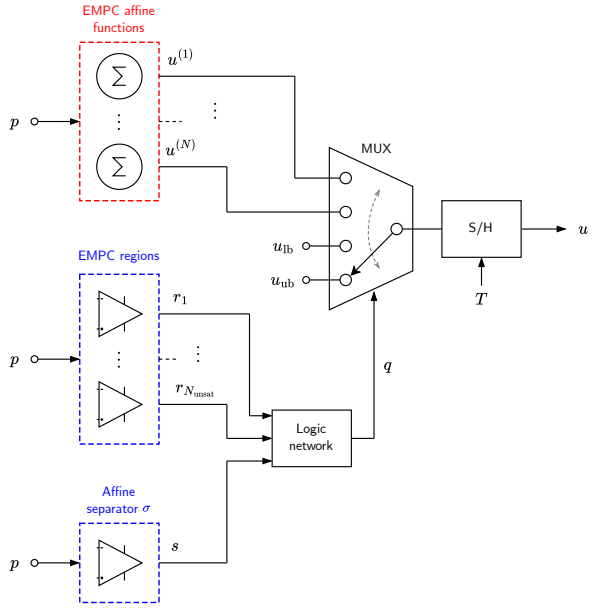


Figure 1. EMPC implementation: high-level schematic.

that assumes logical value 1 whenever the affine law $K_i p_k + l_i$ must be selected. In Eq. (25), $\mathcal{I}_i \subseteq I_{\text{unsat}}$ is the set of region indices sharing the law $K_i p_k + l_i$ and $I^{\text{unique}}_{\text{unsat}} \subseteq I_{\text{unsat}}$ is the set of indices of unsaturated regions that do not share the same law. We denote by $N \doteq |I^{\text{unique}}_{\text{unsat}}|$ the number of unique unsaturated affine functions. Finally, by defining the saturation signals

$$s = \begin{cases} 1 & \text{if } a^{*\top} p_k + b^* > 0, \\ 0 & \text{otherwise,} \end{cases} \qquad s_a = \bigodot_{i \in I^{\text{unique}}_{\text{unsat}}} \overline{\beta_i}, \tag{26}$$

the EMPC policy (18) is equivalent to

$$u_k = \pi(p_k) = \begin{cases} K_i p_k + l_i & \text{if } \beta_i, \ \ i \in I^{\text{unique}}_{\text{unsat}}, \\ u_{\text{ub}} & \text{if } s_a \odot s, \\ u_{\text{lb}} & \text{if } s_a \odot \overline{s}. \end{cases} \tag{27}$$

Remark 3. *The construction of the signals β_i in Eq. (25) takes into account the non-disjoint optimal merging strategy, described in Sec. 3.1. Specifically, in the case of an overlap between regions sharing the same i-th affine function, all the variables r_j with $j \in \mathcal{I}_i$ are combined using an OR operator so that the i-th affine function is selected if p_k belongs to $\bigcup_{j \in \mathcal{I}_i} \mathcal{R}_j$, i.e., the whole domain of the shared affine function.*

We implement the EMPC policy (27) using: (i) one multiplexer (MUX), (ii) a set of generalized adders, (iii) a set of comparators, and (iv) a small logic gate network, according to the circuit depicted in Fig. 1. A sample and hold (S/H) circuit is included after the MUX to ensure proper sampling and avoid inter-sample oscillations of the control input.

Below, we detail every stage of the design for the four main building blocks of the EMPC circuit.

3.2.1 Multiplexer

It is the main component in our EMPC circuit design. We use an analog multiplexer to implement the by-case PWA control policy in Eq. (27). Specifically, we use a multiplexer with $N + 2$ inputs: one for each unique unsaturated affine function, plus the two saturated input values u_{ub} and u_{lb}. While u_{ub} and u_{lb} are trivially imposed through a constant voltage, the inputs corresponding to the affine functions need to be computed online, given the current value of states and disturbances. To this end, we introduce generalized adders.

3.2.2 Generalized Adders

Generalized adders are a standard circuit in analog electronics [36] and their design is easily automated, as detailed in the following. We employ generalized adders to generate the control input $u^{(i)}$ given by each i-th unique unsaturated affine function in the EMPC policy (27),

$$u^{(i)} = K_i p + l_i, \quad i \in I^{\text{unique}}_{\text{unsat}}, \tag{28}$$

where, for notational convenience, we omit the explicit time dependence on k.

Without loss of generality, we consider the case $n_u = 1$ (i.e., $K_i \in \mathbb{R}^{1 \times n_p}$ and $l_i \in \mathbb{R}$). In this setting, being $u^{(i)}$ a scalar, each affine function requires a single generalized adder, so N in total. If $n_u > 1$, then a generalized adder is needed for each component $(u^{(i)})_j$, $j = 1, \dots, n_u$, resulting in n_u generalized adders for each affine function, so $n_u N$ in total.

For each generalized adder, the circuit inputs are the voltage measurements of the EMPC parameters p and a positive constant voltage V_0 to implement the constant offset l_i, which can be arbitrarily chosen; the circuit output is a voltage equal to $u^{(i)}$. Let us append V_0 to p, i.e., $p_{n_p+1} = V_0$. Also, let $K_{i,j} = (K_i)_j$ and append l_i to K_i, i.e., $K_{i,n_p+1} = l_i / V_0$. Then, we can equivalently rewrite Eq. (28) as follows:

$$u^{(i)} = \sum_{j=1}^{n_p+1} K_{i,j}\, p_j = \sum_{k=1}^{M_i} g^{(+)}_{i,k}\, p^{(+)}_{i,k} - \sum_{k=1}^{N_i} g^{(-)}_{i,k}\, p^{(-)}_{i,k}, \tag{29}$$

where, letting $M_i, N_i \in \mathbb{N}$ the number of inputs with positive and negative gains, respectively, we defined $g^{(+)}_{i,k} = K_{i,j} \geq 0$ for $k = 1, \dots, M_i$, $-g^{(-)}_{i,k} = K_{i,j} < 0$ for $k = 1, \dots, N_i$, and $p^{(+)}_{i,k}$, $p^{(-)}_{i,k}$ the inputs associated with gains $g^{(+)}_{i,k}$ and $g^{(-)}_{i,k}$, respectively. In the following, we omit the adder index i, except in N_i and M_i.

Let us define the total positive and negative gains, i.e.,

$$K^{(+)} = \sum\nolimits_{k=1}^{M_i} g^{(+)}_k, \quad K^{(-)} = \sum\nolimits_{k=1}^{N_i} g^{(-)}_k. \tag{30}$$

We identify two topologically distinct circuits for the considered design, depending on whether $K^{(+)} \geq K^{(-)} + 1$ or $K^{(+)} < K^{(-)} + 1$. Both topologies are reported in Fig. 2.

In the first case, with $K^{(+)} \geq K^{(-)} + 1$, the circuit includes the additional resistance $R^{(-)}_{N_i+1}$, connected to the inverting input of the OP-AMP OP^{add}, as shown in Fig. 2 (blue resistor) to increase the overall positive gain. In this case, if we ensure

$$G_f + \sum\nolimits_{k=1}^{N_i+1} G^{(-)}_k = \sum\nolimits_{k=1}^{M_i} G^{(+)}_k, \tag{31}$$

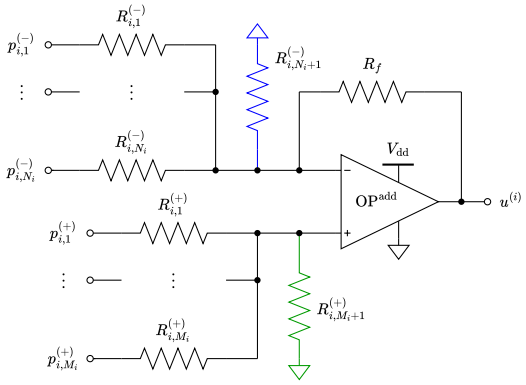


Figure 2. Generalized adder for the i-th affine function. The blue resistor is used if $K_i^{(+)} \geq K_i^{(-)} + 1$, while the green one is used otherwise.

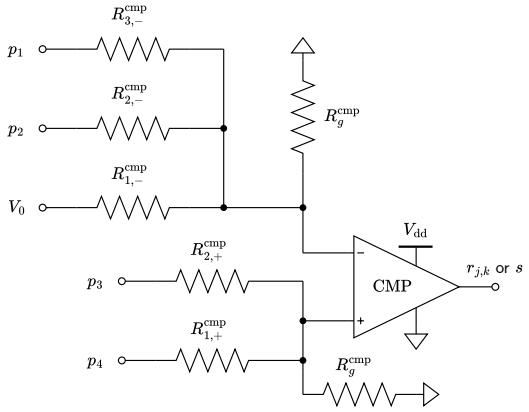


Figure 3. Comparator (case with $n_p = 4$, $|I_p| = 2$, and $|I_m| = 3$).

where $G_f = 1/R_f$, $G_k^{(-)} = 1/R_k^{(-)}$, and $G_k^{(+)} = 1/R_k^{(+)}$, we obtain the following:

$$g_k^{(-)} = G_k^{(-)} G_f^{-1}, \quad g_k^{(+)} = G_k^{(+)} G_f^{-1}. \tag{32}$$

Therefore, fixed a value for R_f, we can trivially obtain $R_k^{(-)}$ and $R_k^{(+)}$ from Eq. (32) and, next, $R_{N_i+1}^{(-)}$ from Eq. (31).

Similarly, in the second case, with $K^{(+)} < K^{(-)} + 1$, we reduce the overall positive gain by including the additional resistance $R_{M_i+1}^{(+)}$ to the positive input of $\mathrm{OP}^{\rm add}$, as shown in Fig. 2 (green resistor). In this case, if

$$G_f + \sum\nolimits_{k=1}^{N_i} G_k^{(-)} = \sum\nolimits_{k=1}^{M_i+1} G_k^{(+)}, \tag{33}$$

we obtain, as for the previous case, the design equations in Eq. (32), through which we can compute $R_k^{(-)}$ and $R_k^{(+)}$. Finally, $R_{M_i+1}^{(+)}$ is computed using Eq. (33).

Adders constitute the most expensive part of the device, as they require OP-AMPs. Still, the overall number of required adders is N, i.e., the number of unique unsaturated affine functions of the EMPC policy (27), which can be reduced through the techniques described in Sec. 3.1.

3.2.3 Comparators

We employ a set of comparators to obtain the Boolean signals $(r_j)_{j=1}^{N_{\rm unsat}}$ and s, as defined in Eqs. (24)–(26). For each r_j, let us define the auxiliary Boolean signal

$$r_{j,k} = \begin{cases} 1 & \text{if } -(H_j)_k\, p + (h_j)_k \geq 0, \\ 0 & \text{otherwise,} \end{cases} \tag{34}$$

where $(H_j)_k$ and $(h_j)_k$ are the k-th row of matrix H_j and the k-th element of vector h_j, respectively. Then, we have that $r_j = \bigodot_{k=1}^{N_j} r_{j,k}$, $j = 1, \ldots, N_{\rm unsat}$, which can be easily realized through logic AND gates.

Obtaining each of the Boolean signals $r_{j,k}$ and s requires evaluating a set of inequalities of the kind

$$[\alpha_1,\ \ldots,\ \alpha_{n_p}]\, p + \alpha_{n_p+1} V_0 \geq 0, \tag{35}$$

where V_0 is a positive constant voltage, which can be arbitrarily chosen (it is also employed in the generalized adders), and $(\alpha_i)_{i=1}^{n_p+1}$ are gains depending on $(H_j)_k$, $(h_j)_k$, a^*, and b^*, whose sign is not known a-priori. Let us append V_0 to p, i.e., $p_{n_p+1} = V_0$. We realize the comparison altogether with the sums in Eq. (35) through the circuit topology in Fig. 3. The selected circuit compares the voltage on the "+" terminal with that on the "−" terminal; these voltages are obtained through voltage dividers. To determine the resistance values, we rewrite Eq. (35) as

$$\sum\nolimits_{i\in I_p} \gamma_i\, p_i \geq \sum\nolimits_{i\in I_m} \gamma_i\, p_i, \tag{36}$$

where I_p, $I_m \subseteq \{1, \ldots, n_p + 1\}$ are the set of indices for which $\alpha_i > 0$ and $\alpha_i \leq 0$ in Eq. (35), respectively, and

$$\gamma_i = \frac{c\,|\alpha_i|}{\max_{j\in\{1,\ldots,n_p+1\}} |\alpha_j|}, \quad c \in (0, 1) \tag{37}$$

are normalized and rescaled versions of the gains α_i. In this way, the gains γ_i associated with each p_i are such that $0 < \gamma_i < 1$, for all $i = 1, \ldots, n_p + 1$. This enables the use of inexpensive voltage dividers for comparisons, eliminating the need for additional OP-AMPs.

Consider the networks of $|I_p| + 1$ and $|I_m| + 1$ resistors on the "+" and "−" terminal of the comparator, respectively. Let $R_g^{\rm cmp}$ be the resistor connected to ground, $R_i^{\rm cmp}$ the resistor associated with the input p_i, $G_g^{\rm cmp} = 1/R_g^{\rm cmp}$ and $G_i^{\rm cmp} = 1/R_i^{\rm cmp}$ the corresponding conductances. Then, the voltages on the two terminals are

$$v_+ = \sum_{i\in I_p} \frac{(G_g^{\rm cmp} + \sum_{j\neq i} G_j^{\rm cmp})^{-1}}{R_i^{\rm cmp} + (G_g^{\rm cmp} + \sum_{j\neq i} G_j^{\rm cmp})^{-1}} p_i \tag{38}$$

and similarly for v_-, with the sum over $i \in I_m$.

Imposing the gains match, i.e.,

$$\gamma_i = \frac{(G_g^{\rm cmp} + \sum_{j\neq i} G_j^{\rm cmp})^{-1}}{R_i^{\rm cmp} + (G_g^{\rm cmp} + \sum_{j\neq i} G_j^{\rm cmp})^{-1}}, \quad i \in I_p, \tag{39}$$

is equivalent to

$$\gamma_i \Big(G_g^{\rm cmp} + \sum\nolimits_{j\in I_p} G_j^{\rm cmp} \Big) = G_i^{\rm cmp}, \quad i \in I_p. \tag{40}$$

For any fixed resistor $R_g^{\rm cmp}$, Eq. (40) is a linear system

of $|I_p|$ equations in $|I_p|$ unknowns, whose matrix form is

$$\begin{bmatrix} \gamma_1 - 1 & \gamma_1 & \dots & \gamma_1 \\ \gamma_2 & \gamma_2 - 1 & \dots & \gamma_2 \\ \vdots & \vdots & \ddots & \vdots \\ \gamma_{|I_p|} & \gamma_{|I_p|} & \dots & \gamma_{|I_p|} - 1 \end{bmatrix} \begin{bmatrix} G_1^{\text{cmp}} \\ G_2^{\text{cmp}} \\ \vdots \\ G_{|I_p|}^{\text{cmp}} \end{bmatrix} = -G_g^{\text{cmp}} \begin{bmatrix} \gamma_1 \\ \gamma_2 \\ \vdots \\ \gamma_{|I_p|} \end{bmatrix}. \tag{41}$$

The matrix in Eq. (41) is always full-rank, thus admitting a unique solution for the conductances G_i^{cmp}. Then, resistors R_i^{cmp} are easily obtained by taking the inverse. The very same procedure applies to the network at the "$-$" terminal.

Overall, the number of comparators is upper-bounded by $1 + \sum_{j=1}^{N_{\text{unsat}}} N_j$, which is often effectively optimized through the complexity-reduction techniques described in Sec. 3.1, particularly the removal of trivial inequalities and the non-disjoint optimal merging strategy, which reduces both the number of EMPC regions and the number of facets. This number can be further reduced if different regions share the same inequality or use opposite ones (i.e., two or more regions have facets on the same hyperplane); in such scenarios, we may reuse comparators from other regions, eventually introducing a NOT logic gate.

3.2.4 Logic Network

A network of logic gates is needed to drive the selection signal q of the MUX, using the Boolean signals $(r_j)_{j=1}^{N_{\text{unsat}}}$ and s, according to Eqs. (25)–(27). Specifically, the signal $q = (q_i)_{i=1}^{\lceil \log_2(N+2) \rceil}$ is binary encoded to select each unsaturated affine function and the two saturated values u_{lb} and u_{ub}. The logic network implementing q can be easily designed using standard logic function optimization methods, such as Karnaugh maps.

3.3 Comparison with the literature

The proposed approach presents several structural differences with respect to existing MPC implementations. Compared to digital solutions (such as [23, 24] based on microcontrollers, or [11, 25] based on FPGA), it avoids the need for ADC and DAC interfaces, thereby reducing conversion-induced delays and hardware overhead. With respect to the prior analog implementation proposed in [12], all the circuit OP-AMPs operate in their linear region, thereby avoiding slew-rate limitations and enabling lower latency and higher achievable switching frequencies.

In addition, the proposed design links circuit complexity to the number of unsaturated regions in the EMPC law, which can be influenced through MPC parameters' choices. For instance, a shorter horizon, fewer constraints, and the use of move blocking directly reduce the number of regions as shown in Eq. (13), and the use of input regularization enhances the effectiveness of the hyperplane separation of saturated regions. This provides some flexibility in balancing closed-loop performance and implementation complexity. In contrast, in [12] the number of required OP-AMPs is directly tied to the number of constraints and, thus, cannot benefit from any of the proposed simplification strategies, directly limiting the overall design flexibility. Furthermore, in our design, fewer OP-AMPs are needed: we only require 1 OP-AMP per region, versus the 2 OP-AMPs per inequality in [12].

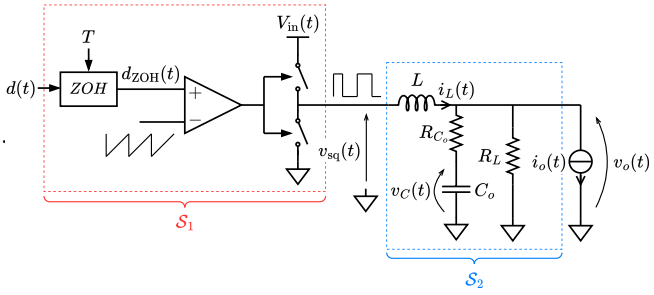


Figure 4. Buck converter circuit diagram.

4 Application to DC-DC Buck Converters

In this section, we apply the proposed approach to design a fully analog MPC-controlled DC-DC Buck converter.

4.1 Buck Converter Mathematical Model

We consider a Buck converter operating at a fixed switching frequency $f_{\text{sw}} = \frac{1}{T}$. With reference to the circuit diagram of the converter depicted in Fig. 4, we denote as $i_L(t)$ the inductor current, $v_C(t)$ the capacitor voltage, $d(t)$ the duty cycle of the square wave voltage $v_{\text{sq}}(t)$, $i_o(t)$ the drawn output current, $V_{\text{in}}(t)$ the supply voltage, and $v_o(t)$ the output voltage. We denote as $\overline{V}_{\text{in}}$ and $v_{\text{in}}(t)$ the nominal value and variation of $V_{\text{in}}(t)$, i.e., $V_{\text{in}}(t) = \overline{V}_{\text{in}} + v_{\text{in}}(t)$. The main control task is to regulate $v_o(t)$ at a reference $\overline{V}_o$.

We rely on the first principles of physics to relate the above quantities and derive the mathematical model of the Buck converter. Specifically, we describe the Buck converter as the cascade of two subsystems (see Fig. 4).

The first subsystem, $\mathcal{S}_1$, takes as inputs the duty cycle $d(t)$ in the form of a voltage signal ranging in $[0, 1]$ V, and the supply voltage $V_{\text{in}}(t)$. The output of $\mathcal{S}_1$ is the voltage $v_{\text{sq}}(t)$. This subsystem consists of three parts: a zero-order hold (ZOH), a comparator, and two switches. The ZOH samples $d(t)$ at each time instant $t = kT$, $k \in \mathbb{Z}_{\geq 0}$, and holds it constant at the value $d_k = d(kT)$ over the k-th switching period $I_k = [kT, (k+1)T)$. The ZOH output signal is given by $d_{\text{ZOH}}(t) = d_k$, for all $t \in I_k$. Then, $d_{\text{ZOH}}(t)$ is compared to a sawtooth wave, with fixed frequency f_{sw} and ranging in $[0, 1]$ V. This operation is performed by means of a comparator. When the sawtooth value is below $d_{\text{ZOH}}(t)$, the comparator outputs a voltage V_H; conversely, when the sawtooth value is larger than $d_{\text{ZOH}}(t)$, the comparator outputs a voltage V_L. The comparator output signal drives the two switches driven in anti-synchronized mode. One switch, called the high side, is connected to $V_{\text{in}}(t)$ and is open when the comparator outputs V_H; the other, called the low side, is connected to the ground and is open if the

comparator outputs V_L. As a result, the subsystem $\mathcal{S}_1$ outputs a square wave $v_{\text{sq}}(t)$ with duty cycle $d(t)$ and amplitude $V_{\text{in}}(t)$, according to:

$$\mathcal{S}_1(d(t), V_{\text{in}}(t)) \doteq \begin{cases} V_{\text{in}}(t), & t \in [kT, (k+d_k)T), \\ 0, & t \in [(k+d_k)T, (k+1)T). \end{cases} \tag{42}$$

The subsystem $\mathcal{S}_2$ is dynamical, linear and time-invariant (LTI). Its inputs are the square wave voltage $v_{\text{sq}}(t)$ from $\mathcal{S}_1$ and the output current $i_o(t)$. The output of $\mathcal{S}_2$ is the controlled output voltage $v_o(t)$. Following the standard approach in circuit theory, we define the state vector as $x(t) = [i_L(t),\ v_C(t)]^\top$. With this choice, we obtain the following state-space model for $\mathcal{S}_2$:

$$\mathcal{S}_2 : \begin{cases} \dot{x}(t) = A_c x(t) + B_{c,1} i_o(t) + B_{c,2} v_{\text{sq}}(t), \\ v_o(t) = C_c x(t) + D_1 i_o(t), \end{cases} \tag{43}$$

where

$$A_c = \begin{bmatrix} -\frac{R_L \| R_{C_o}}{L} & -\frac{R_L}{L(R_{C_o}+R_L)} \\ \frac{R_L}{C_o(R_{C_o}+R_L)} & -\frac{1}{C_o(R_{C_o}+R_L)} \end{bmatrix}, \tag{44a}$$

$$B_{c,1} = \begin{bmatrix} \frac{R_L \| R_{C_o}}{L} \\ -\frac{R_L}{C_o(R_{C_o}+R_L)} \end{bmatrix}, \quad B_{c,2} = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}, \tag{44b}$$

$$C_c = \begin{bmatrix} R_L \parallel R_{C_o} & \frac{R_L}{R_L+R_{C_o}} \end{bmatrix}, \quad D_{c,1} = -R_L \parallel R_{C_o}. \tag{44c}$$

We refer the reader to [16] for details.

Overall, the model of the entire plant is a nonlinear system described by the interconnection of $\mathcal{S}_1$ and $\mathcal{S}_2$:

$$v_o(t) = \mathcal{S}_2(i_o(t), \mathcal{S}_1(d(t), V_{\text{in}}(t))). \tag{45}$$

Notice that $v_o(t)$ depends on the $d(t)$, which we use as control input, but also on $i_o(t)$ and $\overline{V}_{\text{in}}$. The latter two quantities are external signals that we can not act upon; therefore, we shall consider their variations as disturbances to be compensated, i.e., $\nu_1(t) = i_o(t)$ and $\nu_2(t) = V_{\text{in}}(t) - \overline{V}_{\text{in}} = v_{\text{in}}(t)$.

According to the MPC formulation in Sec. 2, we need to describe the plant under control in Eq. (45) as a DT affine system, matching Eq. (1). To this end, we perform discretization and linearization of the model (45).

4.1.1 Model Discretization

We select the switching period T as the discrete time step for discretization. Henceforth, any quantity sampled at the switching time instants $t = kT$ will be denoted using the subscript k, i.e., $\star_k = \star(kT)$.

We address discretization by integrating Eq. (43) over the k-th switching period I_k. Thanks to the linearity of Eq. (43), we can evaluate the model prediction x_{k+1} in closed form using the following convolution integral:

$$x_{k+1} = e^{A_c T} x_k + \int_{kT}^{(k+1)T} e^{A_c((k+1)T-\tau)} (B_{c,1} i_o(t) + B_{c,2} v_{\text{sq}}(t)) d\tau. \tag{46}$$

By linearity, Eq. (46) is equivalent to

$$x_{k+1} = e^{A_c T} x_k + e^{A_c(k+1)T} \int_{kT}^{(k+1)T} e^{-A_c\tau} B_{c,1} i_o(t) d\tau + e^{A_c(k+1)T} \int_{kT}^{(k+1)T} e^{-A_c\tau} B_{c,2} v_{\text{sq}}(t) d\tau. \tag{47}$$

The integrals in Eq. (47) are solved in closed form. To this aim, we introduce the following assumption:

Assumption 2. *The input voltage $V_{\text{in}}(t)$ and the output current disturbance $i_o(t)$ remain constant over the switching periods, i.e., $V_{\text{in}}(t) = V_{\text{in},k}$ and $i_o(t) = i_{o,k}$ for all $t \in I_k$ and $k \geq 0$.*

Remark 4. *Note that, Assumption 2 is respected with a good approximation as long as: i) the input voltage $V_{\text{in}}(t)$ slowly varies (i.e., its bandwidth is much lower than f_{sw}); ii) the output current $i_o(t)$ is constant almost everywhere (i.e., it is well modeled by a piecewise-constant signal, since it only changes due to sudden load connections or removals).*

Under Assumption 2 and using $v_{\text{sq}}(t) = \mathcal{S}_1(d(t), V_{\text{in}}(t))$ as defined in Eq. (42), Eq. (47) simplifies to

$$x_{k+1} = e^{A_c T} x_k + e^{A_c(k+1)T} \int_{kT}^{(k+1)T} e^{-A_c\tau} B_{c,1} i_{o,k} d\tau + e^{A_c(k+1)T} \int_{kT}^{(k+d_k)T} e^{-A_c\tau} B_{c,2} V_{\text{in},k} d\tau. \tag{48}$$

Solving the integrals in Eq. (48) leads to the DT model

$$\begin{aligned} x_{k+1} &= f(x_k, d_k, i_{o,k}, V_{\text{in},k}) \\ &\doteq e^{A_c T} x_k + (e^{A_c T} - I) A_c^{-1} B_{c,1} i_{o,k} \\ &\quad + e^{A_c T} (I - e^{-A_c d_k T}) A_c^{-1} B_{c,2} V_{\text{in},k}. \end{aligned} \tag{49}$$

Proposition 3. *Let us consider constant disturbances $i_{o,k} = i_o$ and $v_{\text{in},k} = v_{\text{in}}$ for all $k \geq 0$. The system (49) admits a unique equilibrium point satisfying the output regulation task towards the desired constant reference $\overline{V}_o$, i.e., there exist unique $\overline{x} \in \mathbb{R}^n$ and $\overline{D} \in \mathbb{R}$ such that*

$$\overline{x} = f(\overline{x}, \overline{D}, i_o, V_{\text{in}}), \tag{50a}$$

$$\overline{V}_o = C\overline{x}. \tag{50b}$$

Proof. Solving Eq. (50a) for $\overline{x}$ and using Eq. (50b) yields

$$\overline{V}_o = C(I - A)^{-1}(A - A^{1-\overline{D}}) A_c^{-1} B_{c,2} V_{\text{in}} - \rho_1 i_o, \tag{51}$$

where $A = e^{A_c T}$ and $\rho_1 = C A_c^{-1} B_{c,1} \approx 0$ is the DC-gain of the linear subsystem $\mathcal{S}_2$ in Eq. (43) for input i_o. Existence is guaranteed by noting that the scalar function of $\overline{D}$ on the right-hand side of Eq. (51), defined over the interval $0 \leq \overline{D} \leq 1$, admits as image the interval $-\rho_1 i_o \leq \overline{V}_o \leq -\rho_1 i_o + \rho_2 V_{\text{in}}$, where $\rho_2 = C A_c^{-1} B_{c,2} \approx 1$ is the DC-gain of the linear subsystem $\mathcal{S}_2$ in Eq. (43) for input V_{in}. Uniqueness is a direct consequence of the fact that the function $\overline{V}_o(\overline{D})$ is monotonically strictly increasing. □

Remark 5. *The exact value of $\overline{D}$ can be computed, e.g., using Newton's method to solve the nonlinear equation* (51)*. Also, we notice that in the undisturbed case, i.e., $i_{o,k}=0$ and $V_{\text{in},k}=\overline{V}_{\text{in}}$, taking a linear approximation of the exponential function leads to $\overline{D}=\frac{\overline{V}_o}{\overline{V}_{\text{in}}}$, which is a good approximation in all our numerical tests and matches the classical assessment of steady-state duty-cycle as established in, e.g., [16].*

4.1.2 Model Linearization

We proceed with the linearization of the model in Eq. (49). Specifically, a nonlinearity in d_k and $V_{\text{in},k}$ arises from the presence of due to the presence of the term $e^{-A_c d_k T}V_{\text{in},k}$. We introduce the following assumption:

Assumption 3. *The sequences d_k, $V_{\text{in},k}$ are well-described by*

$$d_k=\overline{D}+\delta_k,\quad V_{\text{in},k}=\overline{V}_{\text{in}}+v_{\text{in},k},\tag{52}$$

where δ_k and $v_{\text{in},k}$ are small variations around the nominal values $\overline{D}$ and $\overline{V}_{\text{in}}$, respectively.

Remark 6. *Assumption 3, which is standard in set-point regulation for power converters (see, e.g., [37, Chapter 1]), is only used to construct the DT MPC prediction model* (2b), (2c)*, but not critical for stability; as we can formally guarantee stability of the closed-loop system considering the non-approximated nonlinear model in Eq.* (49)*; see Sec. 4.4.*

Let us consider the nonlinearity of model (49), i.e.,

$$g(\delta_k,v_{\text{in},k})\doteq e^{A_cT}(I-e^{-A_c(\overline{D}+\delta_k)T})A_c^{-1}B_{c,2}(\overline{V}_{\text{in}}+v_{\text{in},k}).\tag{53}$$

Under Assumption 3, we can linearize Eq. (53) around the point $(\delta_k,v_{\text{in},k})=(0,0)$ as follows:

$$\begin{aligned}g(\delta_k,v_{\text{in},k})\approx\ & g(0,0)+\frac{\partial g}{\partial\delta_k}(0,0)\,\delta_k+\frac{\partial g}{\partial v_{\text{in},k}}(0,0)\,v_{\text{in},k}\\ =\ & e^{A_c(1-\overline{D})T}TB_{c,2}\overline{V}_{\text{in}}\,\delta_k\\ &+e^{A_cT}(I-e^{-A_c\overline{D}T})A_c^{-1}B_{c,2}\,(\overline{V}_{\text{in}}+v_{\text{in},k}).\end{aligned}\tag{54}$$

Finally, using Eq. (54) to replace $g(\delta,v_{\text{in},k})$ in Eq. (49), we obtain a linearization matching Eq. (1), with $y_k=v_{o,k}$ and

$$A=e^{A_cT},\quad B=e^{A_c(1-\overline{D})T}TB_{c,2}\overline{V}_{\text{in}},\tag{55a}$$
$$B_{\nu_1}=(e^{A_cT}-I)A_c^{-1}B_{c,1},\tag{55b}$$
$$B_{\nu_2}=e^{A_cT}(I-e^{-A_c\overline{D}T})A_c^{-1}B_{c,2},\tag{55c}$$
$$b=e^{A_c(1-\overline{D})T}\left[\left(e^{A_c\overline{D}T}-I\right)A_c^{-1}-T\overline{D}\,I\right]B_{c,2}\overline{V}_{\text{in}},\tag{55d}$$
$$C=C_c,\quad D_{\nu_1}=D_{c,1}.\tag{55e}$$

Remark 7. *Note that, since the linearization is performed around the nominal values $\overline{D}$ and $\overline{V}_{\text{in}}$, the equilibrium point $(\overline{x},\overline{D},\overline{V}_o)$ of the nonlinear system* (49)*, is also an equilibrium of the linearized system in the undisturbed case. Thus, Assumption 1 is met.*

4.2 Output Current Disturbance and State Estimation

According to the setup in Sec. 2, both external disturbances and states must be either measured or estimated to apply EMPC design. This section describes a simple, low-complex design for devices that estimate $\nu(t)$ and $x(t)$.

4.2.1 Disturbances Estimation

The vector of disturbances is $\nu(t)=[i_o(t),v_{\text{in}}(t)]^\top$. Since $V_{\text{in}}(t)$ is available for measurement, $\nu_2(t)=v_{\text{in}}(t)$ is trivially obtained as $v_{\text{in}}(t)=V_{\text{in}}(t)-\overline{V}_{\text{in}}$ and does not need to be estimated. On the other hand, the output current drawn from the load, $\nu_1(t)=i_o(t)$, is not directly available for measurement; therefore, it must be estimated. In the remainder of this section, we describe how to design a device producing an estimate $\hat{i}_o(t)$ of $i_o(t)$. Specifically, we resort to the linear estimator proposed in [17], based on algebraic design. Given $v_o(t)$ and $i_L(t)$, the problem of estimating i_o is a linear algebraic problem. Indeed, it is obtained in [17] that $i_o(s)=-E_1(s)v_o(s)+i_L(s)$ where

$$E_1(s)\doteq\frac{P_{21}(s)}{P_{11}(s)}=\frac{C_o(R_L+R_{C_o})s+1}{R_L(1+C_oR_{C_o}s)}.\tag{56}$$

We refer the reader to [17] for the complete proof and a detailed discussion. Consequently, given the measured $v_o(t)$ and the measurement of the inductor current $i_{L,\text{sc}}(t)=g_{i_L}i_L(t)$ (where $g_{i_L}\in\mathbb{R}_{>0}$ is the corresponding sensor gain), the output current estimate $\hat{i}_o(t)$ is obtained by:

$$\hat{i}_o(s)=\mathcal{E}(s)\begin{bmatrix}v_o(s)\\ i_{L,\text{sc}}(s)\end{bmatrix},\quad \mathcal{E}(s)\doteq\begin{bmatrix}-E_1(s) & 1/g_{i_L}\end{bmatrix}.\tag{57}$$

Remark 8. *The design of the estimator is entirely conducted in continuous time (CT) and relies on signals involved in the linear subsystem only. Consequently, the problem is solved exactly by the CT LTI filter $\mathcal{E}(s)$.*

In ideal conditions, $\hat{i}_o(t)=i_o(t)$ for all $t\in\mathbb{R}_{\geq 0}$, but the presence of noise and modeling uncertainties in the plant description may hinder the quality of the estimate. Regarding noise, an appropriately designed printed circuit board (PCB) can minimize parasitic effects that perturb the measured signals before they are processed by $\mathcal{E}$. Regarding modeling uncertainties, we note that only R_L, C_o, and R_{C_o} are involved in the design; thus, uncertainties in any other components are irrelevant. We study the impact of the uncertainties on R_L, C, and R_{C_o} through the following sensitivity analysis:

$$S_C^{E_1}(s)\doteq\frac{\partial E_1}{\partial C}=\frac{1}{(CR_{C_o})^2}\frac{s}{(s+\frac{1}{CR_{C_o}})^2},\tag{58a}$$
$$S_{R_{C_o}}^{E_1}(s)\doteq\frac{\partial E_1}{\partial R_{C_o}}=-\frac{1}{R_{C_o}^2}\frac{s^2}{(s+\frac{1}{CR_{C_o}})^2},\tag{58b}$$
$$S_{R_L}^{E_1}(s)\doteq\frac{\partial E_1}{\partial R_L}=-\frac{1}{R_L^2}.\tag{58c}$$

As $s \to 0$, both $|S_C^{E_1}| \to 0$ and $|S_{R_{C_o}}^{E_1}| \to 0$, indicating that uncertainty on C and R_{C_o} poorly influence the estimate $\hat{i}_o$ at low frequencies. Instead, $|S_{R_L}^{E_1}|$ is non-zero, indicating that the uncertainty of R_L leads to some steady-state estimation error $|\hat{i}_o(t) - i_o(t)|$.

Let $\hat{C}_o$, $\hat{R}_{C_o}$, and $\hat{R}_L$ denote the nominal values of these components and $\hat{E}_1$ the transfer function E_1 in Eq. (56) when evaluated using $\hat{C}_o$, $\hat{R}_{C_o}$, and $\hat{R}_L$. To counteract the effect of the uncertainty on R_L, we propose a robust design of $\hat{E}_1$ to minimize the expected value of the steady-state estimation error $|\hat{i}_o(t) - i_o(t)|$. At steady state, since v_o is constant, $v_o(s) = \overline{V}_o/s$ and by the final value theorem, we obtain:

$$\begin{aligned}\lim_{t\to\infty}\left|\hat{i}_o(t) - i_o(t)\right| &= \lim_{s\to 0}\left|s\left(\hat{i}_o(s) - i_o(s)\right)\right| \\ &= \lim_{s\to 0}\left|s\left(\hat{E}_1(s) - E_1(s)\right)\frac{\overline{V}_o}{s}\right| = \overline{V}_o\left|\frac{1}{\hat{R}_L} - \frac{1}{R_L}\right|.\end{aligned} \tag{59}$$

First, we notice that such an error only depends on the uncertainty on R_L, and not on that on C_o, R_{C_o}, which only affects the error transient: for a frequency-dependent sensitivity analysis of the error, see the extended version of this manuscript[1]. Formally, we establish the following result:

Proposition 4 (Optimal estimator $\hat{R}_L^*$)**.** *Let R_L be a uniformly distributed random variable in $[R_{L,\min}, R_{L,\max}]$, i.e., $R_L \sim U([R_{L,\min}, R_{L,\max}])$. Then, the solution to*

$$\hat{R}_L^* = \underset{\hat{R}_L\in\mathbb{R}}{\arg\min}\,\mathbb{E}\left[\left|\frac{1}{\hat{R}_L} - \frac{1}{R_L}\right|\right], \tag{60}$$

is given by the mean resistance $\hat{R}_L^* = \frac{1}{2}(R_{L,\min} + R_{L,\max})$.

Proof. Consider the change of coordinates $a = 1/\hat{R}_L$ and $B = 1/R_L$. The probability density function of B is given by the change of variables formula [38, Sec. 2.3]:

$$f_B(b) = \begin{cases} \frac{1}{R_{L,\max} - R_{L,\min}} b^{-2} & \text{if } \frac{1}{R_{L,\min}} \le b \le \frac{1}{R_{L,\max}}, \\ 0 & \text{otherwise.}\end{cases} \tag{61}$$

After the change of variables, the problem takes the form

$$\hat{a}^* = \underset{a\in\mathbb{R}}{\arg\min}\,\mathbb{E}\left[|a - B|\right]. \tag{62}$$

It is a standard result that the optimum of such a problem corresponds to the median of the distribution of B [39, Chapter 1], i.e., a^* satisfies $\int_{-\infty}^{a^*} f_B(b)db = \frac{1}{2}$. Computing the integral, we get

$$\frac{1}{2} = \frac{1}{R_{L,\max} - R_{L,\min}}\left[-\frac{1}{b}\right]_{R_{L,\max}^{-1}}^{a^*} = \frac{R_{L,\max} - a^*}{R_{L,\max} - R_{L,\min}}. \tag{63}$$

Solving for a^* and taking its inverse yields the result. □

The estimator $\mathcal{E}(s)$, defined in Eq. (57), allows for a cheap circuit implementation as it is composed of a first-order filter $E_1(s)$ and a gain only.

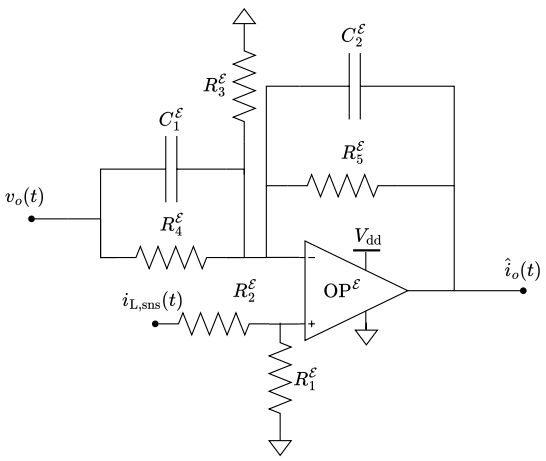


Figure 5. Estimator circuit.

We start from the definition of $E_1(s)$ in Eq. (56), which can be equivalently rewritten as

$$E_1(s) = \frac{1}{R_L}\frac{1 + sC_o(R_L + R_{C_o})}{1 + sC_oR_{C_o}} \tag{64}$$

$$= K_{\mathcal{E}}\frac{1 + s/z_{\mathcal{E}}}{1 + s/p_{\mathcal{E}}}, \tag{65}$$

where

$$K_{\mathcal{E}} = \frac{1}{R_L}, \quad z_{\mathcal{E}} = \frac{1}{C_o(R_L + R_{C_o})}, \quad p_{\mathcal{E}} = \frac{1}{C_oR_{C_o}}. \tag{66}$$

Since $R_{C_o} + R_L \gg R_{C_o}$, we have that $z_{\mathcal{E}} < p_{\mathcal{E}}$ and $E_1(s)$ is a high-pass filter. Consequently, we propose an analog implementation based on the circuital topology in Fig. 5 (highlighted in green in Fig. 6), which differs from the LEC implementation considered in [17] due to the absence of feedforward compensation. To avoid that the output of the OP-AMP $\text{OP}^{\mathcal{E}}$ exceeds the saturation limits, we scale the gain of $\mathcal{E}$ by a factor $g_{i_o} \in (0, 1)$, obtaining a scaled version of the current estimate $\hat{i}_{o,\text{sc}} = g_{i_o}\hat{i}_o$.

The transfer functions of the circuit in Fig. 5, from inputs v_o and $i_{L,\text{sns}}$ to output $\hat{i}_o$ are

$$\frac{\hat{i}_{o,\text{sc}}(s)}{v_o(s)} = -\frac{R_5^{\mathcal{E}}}{R_4^{\mathcal{E}}}\frac{1 + sR_4^{\mathcal{E}}C_1^{\mathcal{E}}}{1 + sR_5^{\mathcal{E}}C_2^{\mathcal{E}}}, \tag{67a}$$

$$\frac{\hat{i}_{o,\text{sc}}(s)}{i_{L,\text{sc}}(s)} = \frac{R_1^{\mathcal{E}}}{R_1^{\mathcal{E}} + R_2^{\mathcal{E}}}\frac{1 + R_5^{\mathcal{E}}(R_3^{\mathcal{E}} \parallel R_4^{\mathcal{E}})^{-1} + sR_5(C_1 + C_2)}{1 + sR_5C_2}. \tag{67b}$$

Matching Eq. (67) with the desired estimator transfer function in Eq. (57) requires imposing the conditions

$$g_{i_o}K_{\mathcal{E}} = R_5^{\mathcal{E}}/R_4^{\mathcal{E}}, p_{\mathcal{E}} = (R_5^{\mathcal{E}}C_2^{\mathcal{E}})^{-1}, z_{\mathcal{E}} = (R_4^{\mathcal{E}}C_1^{\mathcal{E}})^{-1} \tag{68}$$

to implement the $E_1(s)$ transfer function. Then, we select

$$R_4^{\mathcal{E}} = R_2^{\mathcal{E}}, \quad R_5^{\mathcal{E}} = g_{i_L}^{-1}g_{i_o}R_1^{\mathcal{E}} \tag{69}$$

and $R_3^{\mathcal{E}}$ such that

$$C_1^{\mathcal{E}}(R_3^{\mathcal{E}} \parallel R_4^{\mathcal{E}}) = C_2^{\mathcal{E}}R_5^{\mathcal{E}} \tag{70}$$

to ensure that $\hat{i}_o(s)/i_{L,\text{sns}}(s) = g_{i_L}^{-1}g_{i_o}$.

4.2.2 State Estimation

Since $i_L(t)$ can easily be sensed (see, e.g., [17]), but the capacitor voltage $v_C(t)$ is not accessible due to the presence of the capacitor equivalent series resistance (ESR), the estimation of $v_C(t)$ is needed. This section presents a simple algebraic estimator design for $v_C(t)$. Starting from Kirchhoff's current law on the output node of $\mathcal{S}_2$, we have

$$i_C = i_L - i_o - v_o/R_L = (v_o - v_C)/R_{C_o}. \tag{71}$$

Then, given the measurements of i_L and v_o and the estimate $\hat{i}_o$ of i_o, we define the estimator

$$\hat{v}_C = R_{C_o}(\hat{i}_o - i_L) + (R_{C_o}/R_L + 1)\, v_o. \tag{72}$$

With this procedure, $\hat{v}_C(t)$ is obtained using only weighted sums. Consequently, compared to the conventional observer-based strategy, the proposed approach streamlines the design and enables a low-cost analog implementation.

Remark 9. *In many practical applications, $R_{C_o} \ll R_L$. Under this assumption, Eq. (72) can be simplified to the straightforward relation $\hat{v}_C = v_o$, meaning that the controlled output voltage can be directly used as a reliable estimate of the state $v_C(t)$. This further simplifies the circuit design and reduces both the economic costs and the required board area.*

4.3 EMPC Design

We construct the EMPC policy according to Sec. 2 and 3.1, yielding the following expression:

$$\begin{aligned} u_k = d_k = \pi(p_k) &= \pi([i_{L,k},\ \hat{v}_{C,k},\ \hat{i}_{o,k},\ v_{\text{in},k}]^\top) \\ &= \pi\left(\left[\tfrac{1}{g_{i_L}} i_{L,\text{sc},k},\ \hat{v}_{C,k},\ \tfrac{1}{g_{i_o}}\hat{i}_{o,\text{sc},k},\ v_{\text{in},k}\right]^\top\right). \end{aligned} \tag{73}$$

Recalling Eq. (2d), we only impose upper-lower bound constraints on the input, i.e., the duty cycle d, since, by definition, it can only range between 0 (0%) and 1 (100%). This yields the constraint matrices $H_u = [1,\ -1]^\top$ and $h_u = [1,\ 0]^\top$.

We conduct MPC controller design according to Sec. 2 and 3.1. Specifically, within the MPC formulation in Eq. (2), we utilize the linearized Buck model described by matrices according to Eq. (55) and include input saturation limits $u_{\text{lb}} \le \hat{u}_i \le u_{\text{ub}}$ as polytopic constraints (2d), with limits u_{lb} =0 V and u_{ub} =1 V representing the PWM duty-cycle limits. The selected prediction horizon is $N_p = 5$. Regarding the weights Q, R, R_Δ, we employ a trial-and-error procedure to optimize the qualitative observation of load and line disturbance responses. Finally, to reduce the number of regions, we apply the strategies introduced in Sec. 3.1; specifically, in the selection of the move blocking strategy map in Eq. (11), we select control horizon $N_c = 2$.

4.4 Stability Analysis

In this section, we establish the existence and local stability of an equilibrium state $\overline{x} \in \mathbb{R}^2$ for the closed-loop system defined by the nonlinear DT Buck converter model (49) and the EMPC policy (73).

The following result establishes local stability robustly to the presence of bounded, constant load and line disturbances.

Theorem 3 (Local Stability)**.** *Let us consider constant disturbances $i_{o,k} = i_o$ and $v_{\text{in},k} = v_{\text{in}}$ for all $k \ge 0$. Then, the closed-loop system (49), (73) admits an equilibrium state $\overline{x}$.*

Further, let $Z = e^{A_c T(\overline{D}-\overline{u})} = A^{\overline{D}-\overline{u}}$, with $\overline{D}$ defined as in Eq. (51) for the undisturbed case, and $\overline{u} = \pi(\overline{p})$, with $\overline{p} = [\overline{x}, i_o, v_{\text{in}}]^\top$, according to Eq. (73). Assume there exists a matrix $P \in \mathbb{R}^{2\times 2}$ such that $\|A + BK_r\|_P \le 1 - \epsilon_s$ with $0 < \epsilon_s < 1$ and $K_r \in \mathbb{R}^2$ is the vector of the first two elements of the gain K_i of region $\mathcal{R}_i$ such that $[\overline{x}, 0, 0]^\top \in \mathcal{R}_i$. If the disturbances i_o and v_{in} are such that

$$\|Z - I\|_P + \epsilon_V \|Z\|_P \le \frac{\epsilon_s}{\|BK_r\|_P}, \tag{74}$$

where $\epsilon_V = v_{\text{in}}/\overline{V}_{\text{in}}$, then the equilibrium $\overline{x}$ is locally stable.

Proof. First, we prove the existence of the equilibrium state $\overline{x}$ satisfying

$$(A - I)\overline{x} + B_{\nu,2} i_o + g(\pi(\overline{p}), V_{\text{in}}) = 0. \tag{75}$$

As established in [40, Corollary 2.2.2], if $A - I$ is invertible and $g(\pi(\overline{p}), V_{\text{in}})$ is continuous and bounded, then Eq. (75) admits at least one solution. This holds since $0 \le u(x) \le 1$ implies that $g(u(\overline{x}), V_{\text{in}})$ remains bounded.

We now prove the local stability of $\overline{x}$. First, notice that in a neighbourhood of $\overline{p}$ the EMPC policy reduces to $\pi(x) = K_i[x, i_o, v_{\text{in}}]^\top + l_i = K_r x + l_r$ for $[x, i_o, v_{\text{in}}]^\top \in \mathcal{R}_i$, where $\mathcal{R}_i$ is the EMPC region containing $[x, 0, 0]^\top$, $K_r \in \mathbb{R}^2$ and $l_r = l_i + K_{i,3} i_o + K_{i,4} v_{\text{in}} \in \mathbb{R}$. Then, the closed-loop system is equivalently written as

$$x_{k+1} = F(x_k) = Ax + B_{\nu,2} i_o + g(K_r x_k + l_r, V_{\text{in}}). \tag{76}$$

We show that Eq. (76) locally defines a contraction in the P-norm, which is equivalent to the following condition (see, e.g., [41] for more details):

$$\|J(\overline{x})\|_P < 1, \quad J(\overline{x}) = \frac{\partial F}{\partial x}(\overline{x}). \tag{77}$$

For system (76), we obtain

$$J(\overline{x}) = A + e^{A_c(1 - K_r\overline{x} - l_r)T} T B_{c,2} V_{\text{in}} K_r. \tag{78}$$

Recalling that $B = e^{A_c(1-\overline{D})T} T B_{c,2} \overline{V}_{\text{in}}$ from Eq. (55a), we can rewrite

$$J(\overline{x}) = A + \Delta B K_r, \quad \Delta = e^{A_c(\overline{D}-\overline{u})T} \frac{V_{\text{in}}}{\overline{V}_{\text{in}}}. \tag{79}$$

A sufficient condition for $\|J(\overline{x})\|_P < 1$ is then

$$\begin{aligned} \|A + \Delta B K_r\|_P \le \|A + BK_r\|_P + \\ + \|\Delta - I\|_P \|BK_r\|_P < 1. \end{aligned} \tag{80}$$

Since, by assumption, $\|A + BK_r\|_P \le 1 - \epsilon_s$, we obtain

$$\|\Delta - I\|_P \le \frac{\epsilon_s}{\|BK_r\|_P}. \tag{81}$$

Then, recalling the expressions of Δ and Z, and requiring that $v_{\text{in}} = \overline{V}_{\text{in}}\epsilon_V$, yields

$$\begin{aligned}\|\Delta - I\|_P = \|Z(1+\epsilon_V) - I\|_P \leq \\ \leq \|Z - I\|_P + \epsilon_V \|Z\|_P .\end{aligned} \tag{82}$$

Finally, replacing Eq. (82) into Eq. (81), we obtain the condition in Eq. (74). □

The local feedback matrix K_r coincides with the standard linear quadratic regulator gain when a sufficiently long prediction horizon and no move blocking are considered. Under these ideal conditions, $A + BK_r$ is guaranteed to be Schur stable. Thus, the existence of a matrix P and a scalar $\epsilon_s > 0$ such that $\|A + BK_r\|_P = 1 - \epsilon_s$ is guaranteed. In our setting, the adopted move blocking strategy induces only mild perturbations compared to the unblocked formulation, so the resulting closed-loop matrix is expected to remain stabilizing. In practice, the Schur stability property of $A + BK_r$ can still be verified a posteriori.

Remark 10. *The Shur stability property of $A + BK_r$ serves only as a preliminary condition, and our local stability certificate is a stronger result. Beyond asymptotic stability, our analysis quantifies the admissible disturbance set for which the nonlinear closed-loop system remains stable, by computing ϵ_s, ϵ_V, and Z. Specifically, computing ϵ_s and ϵ_V is trivial, while $\|Z\|_P$ and $\|Z - I\|_P$ are monotone functions of $\overline{D} - \overline{u}$: we compute $\overline{D}$ from Eq.* (51) *and $\overline{u}$ from Eq.* (75) *using the worst-case value of the disturbances. For small disturbance amplitudes, we have $Z \approx I$ and $\epsilon_V \approx 0$, making the condition* (74) *trivially satisfied.*

5 Simulations and Results

In this section, we validate our circuital EMPC approach, applied to Buck converters, through extensive simulations. Specifically, we consider two simulation scenarios:

1) high-level Monte Carlo simulations performed in MATLAB® and Simulink® (ver. 2023b) to assess robust control performance in the presence of parametric uncertainty;

2) high-fidelity circuit-level simulations performed in LTSpice® [42] to assess the control performance under realistic operating conditions.

The relevant data, shared by all simulations, are as follows:

- General data: $T = 2$ µs, $f_{\text{sw}} = \frac{1}{T} = 500$ kHz.
- Buck converter: $\overline{V}_{\text{in}} = 50$ V (nominal), $V_{\text{in}} \in [25,\ 60]$ V (range); $\overline{V}_o = 5$ V; $I_{o,\max} = 15$ A; $R_L = 3.681\ \Omega$ (nominal), $R_L \in [0.333,\ 7.029]\ \Omega$ (range); $C_o = 250$ µF (nominal), $C_o \in 250\ \mu\text{F} \pm 10\% = [225,\ 275]$ µF (uncertainty); $L = 8.2$ µH (nominal), $L \in 8.2\ \mu\text{H} \pm 20\% = [6.56,\ 9.84]$ µH (uncertainty).
  - Ceramic capacitor: $R_{C_o} = 5\ \text{m}\Omega$ (nominal), $R_{C_o} \in 5\ \text{m}\Omega \pm 50\% = [2.5,\ 7.5]\ \text{m}\Omega$ (uncertainty).
  - Electrolytic capacitor: $R_{C_o} = 50\ \text{m}\Omega$ (nominal), $R_{C_o} \in 50\ \text{m}\Omega \pm 50\% = [25,\ 75]\ \text{m}\Omega$ (uncertainty).
- Estimators and sensors: $g_{i_L} = 0.2\ \text{V A}^{-1}$, $g_{i_o} = 0.1$.
- MPC: $N_p = 5$, $N_c = 2$, $Q = 10^2$, $R = 10^{-2}$, $R_\Delta = 1$.
- EMPC: $\mathcal{P} = \{p = (i_L, \hat{v}_C, \hat{i}_o, v_{\text{in}}) \in \mathbb{R}^4 : i_L \in [0,\ 80]\ \text{A},\ \hat{v}_C \in [0,\ 20]\ \text{V},\ \hat{i}_o \in [-5,\ 20]\ \text{A},\ v_{\text{in}} = [-35\ \text{V},\ 35\ \text{V}]\}$.

Concerning the capacitor ESR R_{C_o}, we highlight that a very large uncertainty is considered.

5.1 EMPC Design and Complexity Reduction

We derive the EMPC policy (73) following Sec. 3.1 and 4.3 by using nominal component values. Let us consider the case with the ceramic capacitor (i.e., $R_{C_o} = 5\ \text{m}\Omega$, analogous considerations apply to the electrolytic case). The resulting EMPC policy π is composed of $R = 19$ regions (7 unsaturated, 12 saturated), with 9 unique affine functions (7 unsaturated, 1 saturated to u_{lb}, 1 saturated to u_{ub}). We reduce the complexity of π by applying the four techniques reported in Sec. 3.1 in the following order:

1. move blocking strategy simplifies the EMPC policy to $R = 7$ regions (2 unsaturated, 5 saturated) with 4 unique affine functions (2 unsaturated, 2 saturated).
2. the non-disjoint optimal merging of regions leads to $R = 5$ regions (2 unsaturated, 3 saturated) with 4 unique affine functions (2 unsaturated, 2 saturated).
3. the hyperplane separation of saturated regions further reduces to only 2 unsaturated regions, with 2 unique unsaturated affine functions.
4. To remove trivial inequalities, we observe that the 2 unsaturated regions have 1 common facet and are delimited by 6 hyperplanes, 2 of which are given by the set $\mathcal{P}$. As a consequence, the unsaturated regions of the simplified EMPC policy can be defined by 4 non-trivial inequalities only, of which one is shared.

Overall, the number of regions to be checked (i.e., unsaturated) drops from 19 to 2, corresponding to a 89% reduction. Fig. 7 shows the EMPC policy before and after complexity reduction. The control law is projected onto a reduced two-dimensional state space with $\{(i_L, \hat{v}_C) \in \mathbb{R}^2 : i_L \in [0,\ 10]\ \text{A},\ \hat{v}_C \in [4,\ 5.5]\ \text{V}\}$, while holding $\hat{i}_o = 0$ A and $V_{\text{in}} = \overline{V}_{\text{in}} = 50$ V.

5.1.1 Comparison With the Literature

Compared to the recent work [10] on EMPC control with region elimination for Buck converters, we observe that our approach yields as few as 4 regions while considering a very fast switching frequency $f_{\text{sw}} = 500$ kHz; conversely, [10] reports an increase from 3 to 7 regions when increasing f_{sw} from 4 kHz to 10 kHz, potentially leading to an overly complex control law at the desired frequency of 500 kHz.

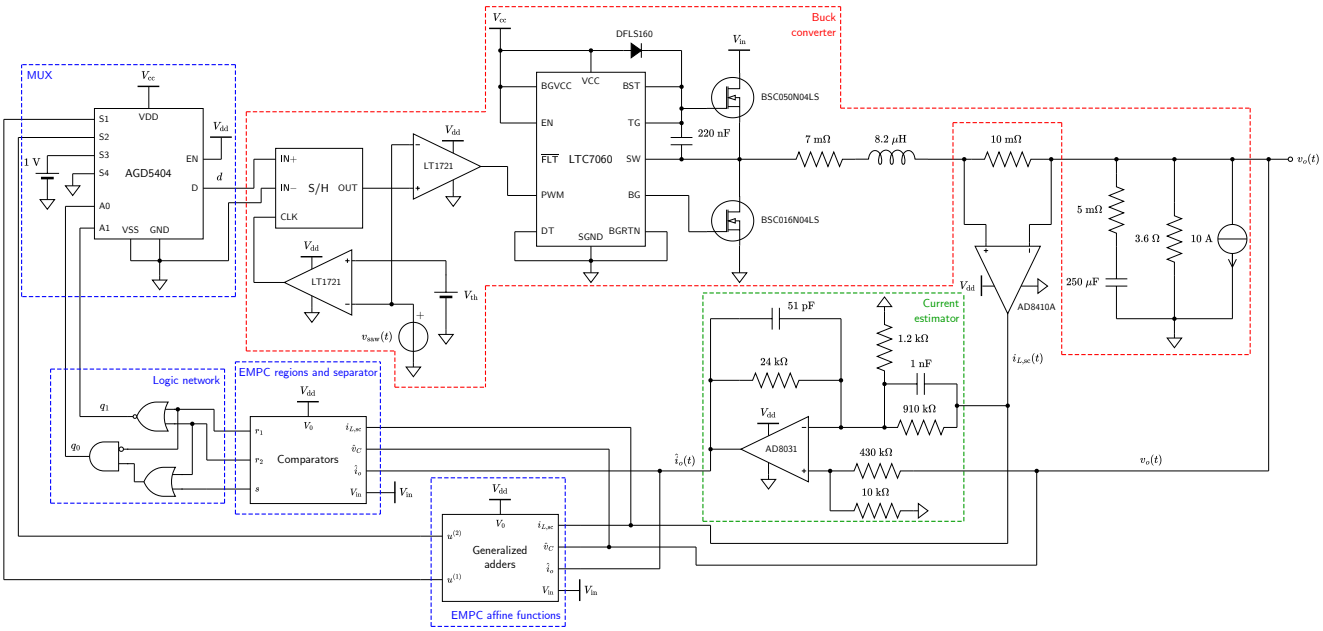


Figure 6. EMPC analog circuit controlling the Buck converter: complete schematic.

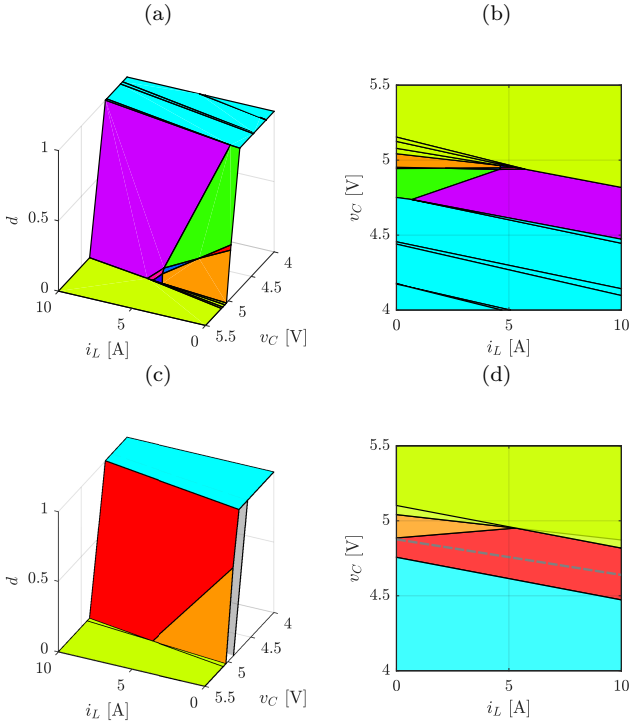


Figure 7. EMPC policy for the Buck converter, before (a, b) and after (c, d) complexity reduction. In (c) and (d), it is also reported the affine separation function σ ( ) and its zero-level set ( ). and denote regions saturated at 0 and 1, respectively.

5.2 Circuital Implementation

The analog circuit implementing the complexity-reduced EMPC policy is realized according to Sec. 3.2 and the estimator $\mathcal{E}$ is designed according to Sec. 4.2. For passive circuit components, we use values from the E-series standard. The overall circuit schematic is reported in Fig. 6.

The power stage of the Buck converter is implemented through the half-bridge gate driver `LTC7060`, which drives the high-side and low-side power MOSFETs of the half-bridge, which are the `BSC050N04LS` and `BSC016N04LS`, respectively, depending on the state of the logic signal provided on the PWM input pin. The Dickson's charge pump, including C_{pump}-D_{pump}, serves to drive the gate of the n-channel MOSFET `BSC050N04LS`, and it takes as input the voltage $V_{\text{cc}} = 12$ V. Both the load current estimator (Fig. 6, green box) and the generalized adders, which implement the EMPC affine functions (Fig. 2), utilize the `AD8031` OP-AMP: a rail-to-rail, single-supply OP-AMP characterized by 80 MHz gain-bandwidth product. The comparator used to implement the EMPC regions and the affine separator (Fig. 3) is the single-supply `LT1721`. The inductor current sensing is performed through a 10 mΩ shunt resistance R_{sense}, together with the current-sense amplifier `AD8410A`. The latter offers a 2.2 MHz bandwidth (four times f_{sw}) and is configured so that its voltage gain is $A_{\text{sense}} = 20$. Therefore, the overall gain is $g_{i_L} = R_{\text{sense}} A_{\text{sense}} = 0.2\ \text{V A}^{-1}$. The OP-AMPs, the current-sense amplifier, and the comparators are supplied with a voltage $V_{\text{dd}} = 5$ V. Also, within the generalized adders and comparators, we set the constant voltage $V_0 = V_{\text{dd}} = 5$ V (refer to Sec. 3.2). Finally, the 4-channel analog MUX is the `ADG5404`, which operates with the V_{cc} supply voltage.

5.2.1 Effect of Complexity Reduction on Circuital Implementation

After the four-fold complexity reduction carried out in Sec. 5.1, we draw conclusions on how many components are required to implement the analog EMPC circuit:

- A four-channel MUX, in order to select the control input from each of the 2 unsaturated affine functions, and the two saturated input values, $d_{\text{lb}} = 0$ and $d_{\text{ub}} = 1$.
- 2 generalized adders to implement the EMPC affine functions: 1 for each unique affine function.
- 5 comparators: 4 to implement the non-trivial inequalities describing the EMPC regions (3 for the first

s	r_1	r_2	q_1	q_0
0	0	0	1	0
0	0	1	0	1
0	1	0	0	0
0	1	1	-	-
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	-	-

TABLE 1
TRUTH TABLE FOR THE MUX SELECTION SIGNAL, IMPLEMENTING THE LOGIC FUNCTIONS (83). "-" STANDS FOR "DON'T CARE".

region and 2 for the second, with one shared), and 1 for the affine separator.

5.2.2 Logic Gate Network

In order to implement the network of logic gates in Sec. 3.2.4, which generates the selection signal $q = (q_0, q_1)$ for the four-channel MUX, we construct a truth table, relating the signals r_1, r_2, and s, according to the simplified EMPC policy and Eqs. (25)–(27). Table 1 shows the considered truth table, which correspond to the logic expressions:

$$q_0 = \overline{r}_1 \odot (s \oplus r_2), \quad q_1 = \overline{r_1 \oplus r_2}, \tag{83}$$

which are implemented using only 4 logic gates: 1 AND, 1 OR, 1 NOR, and 1 NOT; see Figure 6.

5.3 Robust Performance Assessment

In this section, we assess the robust control performance of the EMPC policy in the presence of uncertainties in the Buck converter model parameters through extensive Monte Carlo simulations. These simulations are performed in the MATLAB-Simulink environment due to its higher computational efficiency compared to other, more accurate, circuit simulators.

Within the Buck converter model (45), we introduce parametric uncertainty on the parameters of its passive components, i.e., R_L, L, C_o, and R_{C_o}. In the Monte Carlo simulations, these uncertain parameters are treated as random variables, with a uniform probability distribution within their respective uncertainty intervals. For R_{C_o}, we consider both the cases of ceramic and electrolytic capacitor. A total of 500 random runs are performed.

We study the response of the closed-loop system, i.e., the controlled output voltage $v_o(t)$, in presence of both load and line variations, i.e., injecting the disturbances $i_o(t)$ and $v_{\text{in}}(t)$, respectively. Fig. 8 reports the closed-loop system response $v_o(t)$ in presence of a step load disturbance $i_o(t)$ applied at time t_{i_o}, with amplitude equal to $I_{o,\max} - \frac{\overline{V}_o}{R_L}$; such an amplitude is chosen so that the total output current jumps exactly to the worst case value $I_{o,\max}$. Fig. 8a reports the ceramic capacitor case with $t_{i_o} = 2.4 \times 10^{-3}$ s; Fig. 8b reports the electrolytic capacitor case with $t_{i_o} = 2 \times 10^{-3}$ s. Fig. 9 reports the closed-loop system response $v_o(t)$ in presence of a step line disturbance $v_{\text{in}}(t)$ of amplitude to 10 V applied at time $t_{v_{\text{in}}}$; such an amplitude is significantly high compared to the nominal line voltage $\overline{V}_{\text{in}} = 50$ V. Fig. 9a reports the ceramic capacitor case with $t_{v_{\text{in}}} = 2.8 \times 10^{-3}$ s; Fig. 9b reports the electrolytic capacitor case with $t_{v_{\text{in}}} = 2.4 \times 10^{-3}$ s.

Overall, we observe that the EMPC policy (73), controlling the Buck converter with parametric uncertainty, achieves consistently good performance across the entire range of admissible component values, demonstrating the robustness of the adopted methodology. In general, we observe that parametric uncertainty leads to a slightly erroneous steady-state value, i.e., the reference output $\overline{V}_o = 5$ V is not exactly tracked. Still, the error is always lower compared to the ripple voltage, which is acceptable for most applications.

Regarding disturbance rejection, very small settling times are achieved across all simulations. Such a settling time is comparable to just a few cycles of the PWM modulation frequency: on average, three cycles are sufficient to restore steady-state cyclostationary operation. In the case of load disturbance, the undershoot/overshoot strongly depends on the disturbance amplitude and the capacitor ESR value R_{C_o}, being significantly larger for the electrolytic capacitor case. Specifically, we see that, when considering the electrolytic capacitor (i.e., higher R_{C_o}), the load disturbance undershoot becomes more pronounced, but the settling time improves. As concerns line disturbance, we observe, as expected, a small steady-state tracking error due to the linearized model nonlinearity involving V_{in}. However, this effect is always comparable to, or less than, the voltage ripple.

5.4 Circuital Simulations

We assess the control performance of the analog EMPC circuit controlling the Buck converter through circuit-level simulations. These simulations, carried out in LTSpice, are extremely accurate and allow us to demonstrate the practical feasibility of the proposed approach in real-world conditions. Through these simulations, we can also investigate the impact of circuit non-idealities on control performance.

In order to conduct the simulations, we select commercially-available components to implement the circuit (refer to Sec. 5.2 for more details). For each component, the manufacturer model has been imported into the LTSpice scheme. This enables accurate transistor-level simulation results, which include the non-idealities of the selected components. Among these, we have the finite gain-bandwidth product, the offset currents and voltages, and the slew-rate limitations for OP-AMPs, and the response delay for comparators, MUX, and logic gates. In particular, the non-ideal component dynamics and propagation delays accurately reflect real-time implementation conditions. Under these realistic constraints, the analog controller achieves a total latency of approximately 1 µs, which is strictly lower than the design sampling period and switching period $T = 2$ µs ($f_{\text{sw}} = 500$ kHz). This validates the circuit's real-time feasibility and demonstrates its capability for high-

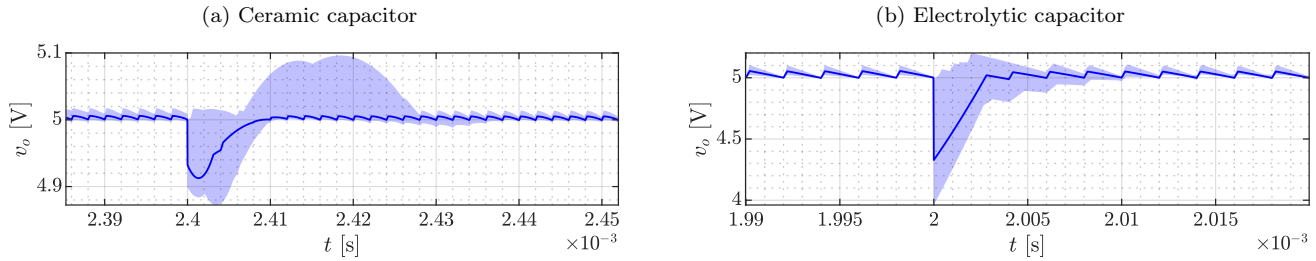


Figure 8. EMPC robust performance: closed-loop system response $v_o(t)$ (nominal ——, uncertainty ▬) to a step load disturbance $i_o(t)$.

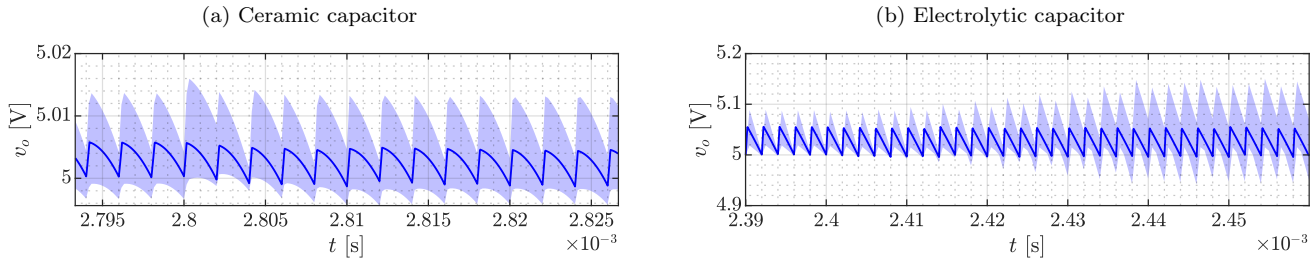


Figure 9. EMPC robust performance: closed-loop system response $v_o(t)$ (nominal ——, uncertainty ▬) to a step line disturbance $v_{\text{in}}(t)$.

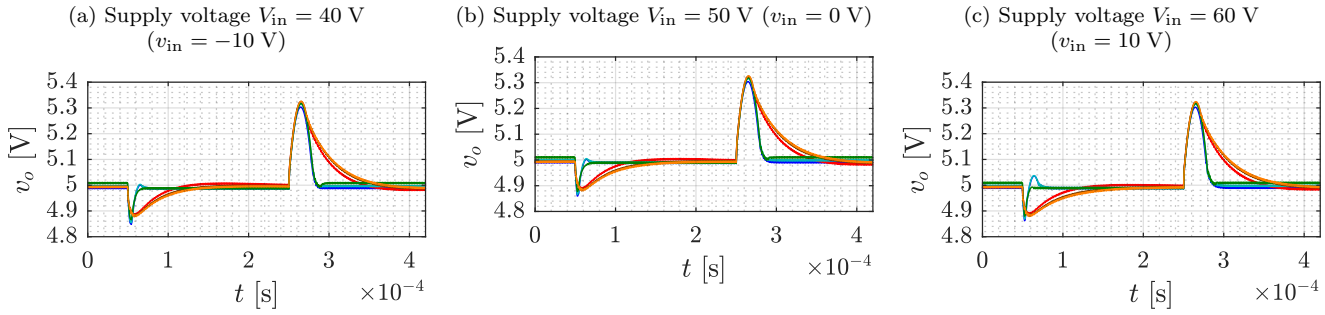


Figure 10. EMPC and VMC response $v_o(t)$ to a 10 A pulse load disturbance $i_o(t)$, under different constant line disturbance v_{in} and resistive loads R_L: EMPC with $R_L = 1\ \Omega$ ——, $R_L = 3\ \Omega$ ——, $R_L = 5\ \Omega$ ——; VMC with $R_L = 1\ \Omega$ ——, $R_L = 3\ \Omega$ ——, $R_L = 5\ \Omega$ ——).

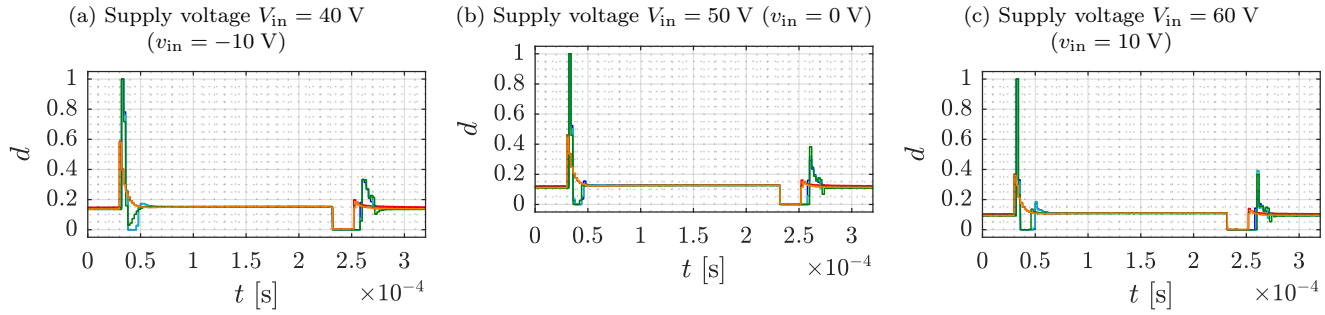


Figure 11. EMPC and VMC duty cycle d_k in response to a 10 A pulse load disturbance $i_o(t)$, under different constant line disturbance v_{in} and resistive loads R_L: EMPC with $R_L = 1\ \Omega$ ——, $R_L = 3\ \Omega$ ——, $R_L = 5\ \Omega$ ——; VMC with $R_L = 1\ \Omega$ ——, $R_L = 3\ \Omega$ ——, $R_L = 5\ \Omega$ ——.

frequency operation. Furthermore, this latency represents a substantial improvement over the 6 µs reported in [12] (enabled by the absence of slew-rate limitations; see Sec. 3.3) as well as existing digital MPC implementations for Buck converters [23, 24, 25, 26]. Finally, while implementing this controller using the approach in [12] would require 8 OP-AMPs, the proposed architecture achieves it with only 2 (see Sec. 3.3).

Alternative MPC implementation approaches, such as [11, 12] cannot operate at the target 500 kHz switching frequency. Simulations under the conditions in Sec. 5.3 at 100 kHz, a frequency compatible with the 6 µs propagation delay of [12], show that although transient performance is comparable to the 500 kHz case, the steady-state output voltage ripple quintuples, in accordance with the theory in [16]. As this elevated ripple is unacceptable for the target application, these lower-frequency waveforms are omitted. Instead, the quantitative comparison focuses on voltage-mode control (VMC), a well-established strategy compatible with

high-frequency operation.

To test different operating conditions, we conduct 9 simulations, considering 3 values for the resistive load $R_L \in \{1\ \Omega,\ 3\ \Omega,\ 5\ \Omega\}$ and 3 values for the supply voltage $V_{\text{in}} \in \{40\ \text{V},\ 50\ \text{V},\ 60\ \text{V}\}$. The latter model a constant line disturbance $v_{\text{in}} \in \{-10\ \text{V},\ 0\ \text{V},\ 10\ \text{V}\}$. To evaluate load disturbance rejection, we consider an output current pulse $i_o(t)$ with an amplitude 10 A and duration of 0.2 ms. Fig. 10 reports the closed-loop system response, i.e., the controlled output voltage $v_o(t)$. For each simulation, the response is compared with that obtained using standard VMC [16] implemented in LTSpice. Detailed VMC controller design, implementation, and component specifications can be found in [17], which utilizes the same case study. Results indicate that, with the selected components, the impact of circuit non-idealities is negligible, as the circuit-level system responses are mostly overlapping with those obtained through the high-level simulations in Sec. 5.3. In terms of load disturbance rejection, the analog EMPC circuit significantly outperforms standard VMC. At $t = 0.5 \times 10^{-4}$ s (i_o rising edge), the undershoot is comparable between EMPC and VMC, being 2.4% for VMC and 2.6% for EMPC; instead, the settling time is 2.5 µs for EMPC, significantly lower than the 10 µs of VMC. Similarly, during the recovery phase at $t = 2.5 \times 10^{-4}$ s (i_o falling edge), we observe identical average overshoots of 6.2% and the settling time is 42 µs for EMPC, while VMC exceeds 200 µs. These results are consistent across the various considered supply voltages and load configurations.

Fig. 11 shows the duty cycle response to the pulse load disturbance. As expected, EMPC saturates the duty command to rapidly reject the disturbance, whilst the VMC response is more conservative across all considered operating conditions.

In all simulations, both EMPC and VMC exhibit a small steady-state tracking error, which, in either case, is at most 10 mV. For EMPC, this error arises from the joint effects of the uncertain load value R_L, the model linearization error, and the approximation introduced by rounding the resistors used to implement the MPC to standard E-series values. Conversely, VMC benefits from an inherent integral action that theoretically ensures zero steady-state error, but the finite gain of the OP-AMP used in its implementation leads to a small non-zero steady-state error.

6 Conclusions

This paper introduced a general methodology for implementing explicit model predictive control policies as fully analog electronic circuits. The proposed approach leverages the piecewise-affine structure of the control policy to map the control law into an analog architecture and employs tailored complexity-reduction strategies to minimize the number of components. This enables real-time operation within fast sampling rates and avoids the overhead associated with digital implementations.

Our approach was applied to the control of DC-DC Buck converters, achieving effective rejection of load and line disturbances. We theoretically analyzed the robustness of closed-loop stability to bounded disturbances, leveraging contraction theory. The EMPC analog circuit was validated through extensive Monte Carlo and circuit-level simulations, demonstrating excellent disturbance rejection performance across a wide range of uncertainties.

Future work will explore the application of the approach to other plants that require fast sampling, such as different DC-DC converter topologies.

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A Reformulation of the MPC problem in standard QP form

This section shows how the MPC problem (2) can be rewritten in a standard and more compact QP form, comprising only $\hat{u}$ as decision variables. The adopted procedure follows along the same lines as in [4].

We eliminate the constraints (2b), (2c) and rewrite Eq. (2a) as a function of $\hat{u}$ and p_k only. First, to eliminate the variables $\hat{x}$ and $\hat{y}$ from problem (2), by recursively applying Eq. (2b), we have

$$\hat{x}_i = A^i x_k + \sum_{j=0}^{i-1} A^{i-j-1}(B\hat{u}_i + B_\nu \nu_k + b). \tag{84}$$

Then, $\hat{x}$ is expressed as a function of $\hat{u}$ and p_k by

$$\hat{x} = \begin{bmatrix}\Phi & \Gamma_\nu\end{bmatrix} p_k + \Gamma\hat{u} + \gamma, \tag{85}$$

where

$$\Phi = \begin{bmatrix} I_n \\ \sum_{i=1}^{N_p} e_{N_p}^{(i)} \otimes A^i \end{bmatrix}, \tag{86a}$$

$$\Gamma = \begin{bmatrix} \mathbf{0}_{n\times N_p n_u} \\ I_{N_p}\otimes B + \sum_{i=1}^{N_p-1} E_{N_p}^{(i)} \otimes A^i B \end{bmatrix}, \tag{86b}$$

$$\Gamma_\nu = \begin{bmatrix} \mathbf{0}_{n\times n} \\ \sum_{i=1}^{N_p} \left(e_{N_p}^{(i)} \otimes \sum_{j=0}^{i-1} A^j \right) \end{bmatrix} B_\nu, \tag{86c}$$

$$\gamma = \begin{bmatrix} \mathbf{0}_{n\times n} \\ \sum_{i=1}^{N_p} \left(e_{N_p}^{(i)} \otimes \sum_{j=0}^{i-1} A^j \right) \end{bmatrix} b. \tag{86d}$$

By Eq. (2c), we can also rewrite

$$\hat{y} = \overline{C}\hat{x} + \overline{D}\hat{u} + \overline{D}_\nu \nu_k + \overline{d}, \tag{87}$$

where

$$\overline{C} = \begin{bmatrix} I_{N_p}\otimes C & \mathbf{0}_{n_y N_p \times n} \end{bmatrix}, \quad \overline{D} = I_{N_p}\otimes D, \tag{88a}$$

$$\overline{D}_\nu = I_{N_p}\otimes D_\nu, \qquad \overline{d} = \mathbf{1}_{N_p}\otimes d. \tag{88b}$$

Next, by defining

$$\begin{aligned} &\overline{Q} = I_{N_p}\otimes Q, \\ &\overline{R} = I_{N_p}\otimes R, \quad \overline{R}_\Delta = M \otimes R_\Delta, \\ &M = \operatorname{diag}([1, 2\cdot \mathbf{1}_{N_p-2}^\top, 1]^\top) - E_{N_p}^{(1)} - E_{N_p}^{(1)\top}, \\ &\overline{y}_r = \mathbf{1}_{N_p}\otimes y_r, \end{aligned} \tag{89}$$

we rewrite the cost function $J(\hat{y},\hat{u})$ in Eq. (2a) in the following compact form:

$$J(\hat{y},\hat{u}) = \|\hat{y}-\overline{y}_r\|_{\overline{Q}}^2 + \|\hat{u}\|_{\overline{R}+\overline{R}_\Delta}^2. \tag{90}$$

Replacing Eqs. (85) and (87) into Eq. (90) yields

$$J(\hat{y},\hat{u}) = J_u(\hat{u}) = \frac{1}{2}\hat{u}^\top H\hat{u} + (Fp_k + c)^\top \hat{u}, \tag{91}$$

where

$$H = (\overline{C}\Gamma + \overline{D})^\top \overline{Q}(\overline{C}\Gamma + \overline{D}) + \overline{R} + \overline{R}_\Delta, \tag{92a}$$

$$F = (\overline{C}\Gamma + \overline{D})^\top \overline{Q}\,\overline{C}\begin{bmatrix}\Phi & \overline{C}\Gamma_\nu + \overline{D}_\nu\end{bmatrix}, \tag{92b}$$

$$c = (\overline{C}\Gamma + \overline{D})^\top \overline{Q}(\overline{C}\gamma + \overline{d} - \overline{y}_r). \tag{92c}$$

Finally, we also express the linear constraints (2d) as a function of $\hat{u}$ and p_k only. First, we compact Eq. (2d) as

$$\overline{H}_x\hat{x} \le h_x, \quad \overline{H}_u\hat{u} \le h_u \tag{93}$$

where

$$\overline{H}_x = \begin{bmatrix} I_{N_p}\otimes H_x & \mathbf{0}\end{bmatrix}, \quad \overline{h}_x = \mathbf{1}_{N_p}\otimes h_x, \tag{94a}$$

$$\overline{H}_u = I_{N_p}\otimes H_u, \qquad \overline{h}_u = \mathbf{1}_{N_p}\otimes h_u. \tag{94b}$$

Then, replacing Eq. (85) into Eq. (93) yields the constraints

$$G\hat{u} \le w + Kp_k, \tag{95}$$

where

$$\begin{aligned} G &= \begin{bmatrix}\overline{H}_x\Gamma \\ \overline{H}_u\end{bmatrix}, \quad w = \begin{bmatrix}\overline{h}_x - \overline{H}_x\gamma \\ \overline{h}_u\end{bmatrix}, \\ K &= \begin{bmatrix}-\overline{H}_x\Phi & -\overline{H}_x\Gamma_\nu \\ \mathbf{0} & \mathbf{0}\end{bmatrix}. \end{aligned} \tag{96}$$

Overall, the original MPC problem (2) is equivalent to the following QP:

$$\min_{\hat{u}} \quad \frac{1}{2}\hat{u}^\top H\hat{u} + (Fp_k + c)^\top \hat{u} \tag{97a}$$

$$\text{s.t.} \quad G\hat{u} \le w + Kp_k. \tag{97b}$$