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Operation control for green data centers supplied by two-terminal voltage source converter with bipolar DC bus

Jianquan Liao [a], Jiameng Cai [a], Yiyao Zhou [b,*], Junzhi Ren [c], Tao Huang [d]

[a] School of Electrical Engineering, Sichuan University, Chengdu 610065, China
[b] School of Electrical Engineering and Electronic Information, Xihua University, Chengdu 610039, China
[c] Key Laboratory of Smart Grid of Ministry of Education, Tianjin University, Tianjin 300072, China
[d] Energy Department "Galileo Ferraris", Politecnico di Torino, Turin 10129, Italy

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ABSTRACT

A two-terminal bipolar DC distribution network (Bi-DCDN) offers a highly reliable power supply and flexible voltage-level configuration, making it well-suited to the operational requirements of data centers. However, fluctuations in large computing loads and inherent parameter asymmetries in Bi-DCDNs can degrade voltage quality, i.e., violations of voltage unbalance and deviation limits, thereby affecting the economic operation of data centers. To address this issue, this paper proposes a voltage quality enhancement strategy for data centers powered by two-terminal voltage source converter (VSC) with bipolar bus based on DC electric springs (DCESs). First, the influence mechanism of DCESs on the voltage quality of data center power supply networks is analyzed, and the optimal installation node of DCESs in the two-terminal VSC with bipolar DC bus is determined through electrical distance-guided configuration method. Then, an equivalent model of the two-terminal system with bipolar DC bus incorporating adaptive droop control of the VSC is derived. Next, the equivalent impedance parameters are identified offline using the least squares method, and a voltage quality compensation equivalent model of the bipolar DC bus is established. Based on the identified parameters, adaptive VSC droop control is implemented to form a coordinated voltage control strategy that includes neutral-line voltage compensation, thereby jointly improving voltage unbalance and deviation. Finally, both MATLAB/Simulink simulations and hardware platform experiments are carried out to verify the effectiveness of the proposed voltage quality enhancement strategy.

1. Introduction

1.1. Background and Motivation

The rapid development of artificial intelligence, particularly the rise of large language models, has triggered a surge in computing power demand [1,2], which prompted data centers to become the core infrastructure of Smart Cities[3]. However, the massive and fluctuating power consumption of data centers poses significant challenges to the efficiency and reliability of their power supply systems.

Bipolar DC distribution networks (Bi-DCDNs) offer a promising solution by eliminating the AC/DC conversion stage and enabling direct power access for data centers [4,5]. Bi-DCDNs feature two voltage levels, enhanced controllability of power quality, high reliability, and large transmission capacity, making them particularly suitable for energy-intensive scenarios such as data center clusters [6,7]. In a Bi-DCDN, the two poles operate independently, allowing one pole to maintain power supply to the data center even if the other fails [8,9]. And bidirectional power flow between the two data centers improves energy utilization, fault tolerance and system resilience [10].

Despite these advantages, Bi-DCDNs face voltage unbalance between the positive and negative poles [11–13], which arises from coupling effects between the poles and asymmetries in power supply, transmission line parameters, and load distribution [14]. Consequently, unbalanced power [15] generates an unbalanced current at the neutral line, leading to voltage deviations and increased losses, which may violate the stringent voltage quality requirements of data centers. Therefore, mitigating voltage unbalance is essential for the reliable and efficient operation of data centers.

* Corresponding author.
E-mail address: yiyaozhou@xhu.edu.cn (Y. Zhou).

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1.2. Literature review

Given the challenges posed by voltage quality of Bi-DCDNs, researchers have concentrated their efforts on two primary areas, i.e., data center energy management and power supply network operation control.

The first stream focuses on the data center level, aiming to make the load more compatible with the power supply. Advances include hierarchical optimization [16], spatio-temporal task redistribution [17,18], thermal energy storage [19], and stochastic co-optimization of energy and workload [20].

The second stream concentrates on mitigation techniques within the Bi-DCDNs to directly suppress voltage unbalance and deviation. Existing studies can be broadly classified into several categories:

Converter-level methods focus on power converter topology optimization. Ref. [21] suppresses voltage unbalance by optimizing the structure or control strategies of voltage balancers, while Ref. [22] proposes a bidirectional dual-input dual-output converter that simultaneously performs independent bidirectional power control and voltage balancing control. Additionally, Refs. [23,24] utilize DCESs to regulate non-critical loads for indirect voltage balancing via power redistribution.

Load-side reconfiguration strategies mitigate node-level unbalances. Refs. [25,26] propose automatic polarity switching, allowing upstream and downstream unbalanced currents to partially cancel each other out. While effective in theory, this method increases complexity and cost due to the extensive switching hardware.

Droop control techniques enhance system-level regulation. Ref. [27] adjusts VSC droop coefficients to suppress the voltage unbalance and deviation, which is equivalent to adding virtual impedance. However, this method is mainly suited to single-terminal radial networks and lacks adaptability in more complex topologies such as two-terminal or multi-terminal networks.

Ref. [28] adopts a communication-based centralized control scheme, which minimizes DC voltage deviation as the optimization objective to solve for the optimal power flow. However, its system performance is highly dependent on the communication system, whose failure may lead to voltage quality deterioration or loss of system control.

A comparative summary of aforementioned methods is presented in Table 1.

1.3. Research gaps and main contribution

While existing research has covered multiple aspects of voltage quality improvement in Bi-DCDNs, significant challenges persist when the networks are deployed to supply data centers:

(1) **Lack of system-level coordinated control:** existing approaches often treat source-side (e.g., VSC) and load-side (e.g., DCES) measures in isolation, failing to orchestrate them as a unified whole for coordinated optimization.

(2) **The absence of DCES installation principle:** although DCES has been applied to some extent, its optimal configuration method based on electrical distance guidance has not been established.

(3) **Lack of self-adaptability:** existing studies typically rely on fixed system parameters for controller design. Their performance degrades when system operating conditions or network topology change, revealing a lack of self-adaptability.

To bridge these critical gaps, this paper develops a novel joint improvement strategy for two-terminal VSC with bipolar DC bus. Distinguished from prior studies, our approach establishes a unified framework (shown in Fig. 1) that coordinates source-side and load-side voltage control devices.

The main contributions are as follows:

(1) **A system-level joint improvement strategy:** this paper develops a novel system architecture for data center power supply. This strategy significantly enhances voltage quality by jointly mitigating voltage unbalance and deviation, ensuring high power quality for critical data center loads.

(2) **The impact mechanism of DCESs and its configuration method:** this paper elucidates the impact mechanism of DCESs on two-

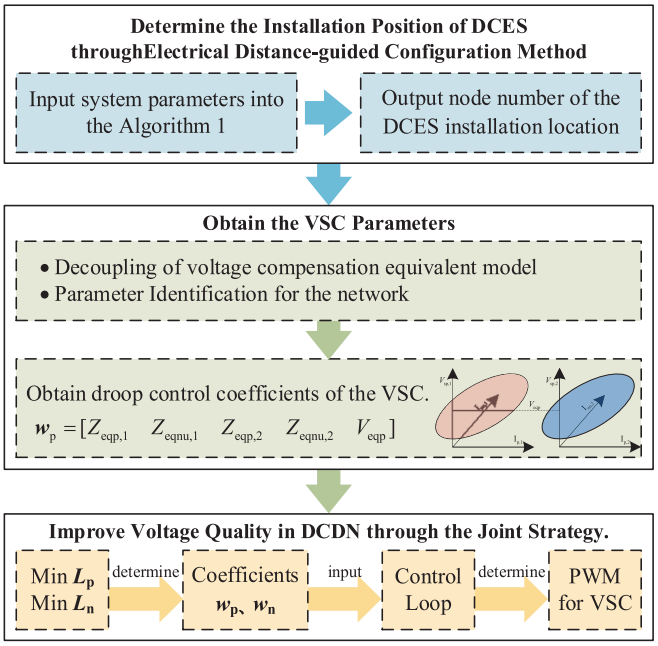


Fig. 1. Research framework.

Table 1
Summary of literature review.

Level	Ref.	Method Category	Advantages	Limitations
Data center	[16]	System parameter optimization	• Large global optimization potential	• High computational complexity • High implementation difficulty
	[17,18]	Spatio-temporal load transfer	• High flexibility • Low implementation cost	• Limited regulation capacity • Dependency on load flexibility
	[19]	Thermal energy management	• Long system lifespan • Significant energy savings	• Geographical constraints • High initial investment
	[20]	Coordinated energy-workload management	• Balances economy and sustainability • Handles Uncertainty	• Reliance on forecasting accuracy • Increases system complexity
Bi-DCDNs	[21,22]	Voltage balancer optimization	• Direct and effective control	• Requires structural changes
	[23,24]	Power redistribution through DCESs	• Flexible regulation and utilization of NCLs	• Load-dependent
	[25,26]	Load-side reconfiguration	• Mitigates node-level unbalances	• High cost and system complexity
	[27]	Droop control techniques	• Simple and high reliability	• Limited to single-terminal networks
	[28]	Communication-based control	• Enables system-wide coordination	• Relies on communication • Less robust

terminal VSC with bipolar DC bus, establishes an electrical distance-guided configuration method for optimal DCES placement.

(3) **An adaptive VSC droop control method:** this paper employs the least squares method for offline impedance identification to establish an equivalent model for voltage compensation. Subsequently, based on this model, an online control strategy is formulated to jointly improve voltage quality, enabling adaptive adjustment of droop coefficients for superior regulation performance.

The overall research framework is illustrated in Fig. 1.

2. The impact mechanism of DCESs on enhancing the voltage quality for data center

2.1. Architecture of a green data center supplied by two-terminal VSC with bipolar DC bus

As shown in Fig. 2 (a), the green data center eliminates fossil-fuel-based backup sources (e.g., diesel generators) and instead relies on on-site energy storage systems for both backup supply and energy buffering. Regarding the power consumption strategy, the data center prioritizes self-consumption of on-site PV generation. PV power first supplies the IT equipment and auxiliary facilities. Any remaining PV power that is not self-consumed is first directed to charge the energy storage system. The excess power will be fed into the AC grid only when the storage is full and there is still surplus PV power.

Fig. 2 (a) also shows the complete system and the interconnections relationships among its various parts. Specifically, the AC bus is interfaced with the DC bus via the VSC, while the DC bus is further connected to renewable generation units and the data center power supply units.

To fully leverage the green potential of the above architecture, two different operating modes are defined. (1) Grid-connected mode with renewable maximization: under normal conditions, the DC system operates connected to the AC grid. The two-terminal VSC regulates the bipolar DC bus voltages while the green sources operate at their maximum power point. Excess green energy is stored in energy storage. (2) Islanded mode using local storage: when the AC grid is unavailable, the DC system is disconnected from the grid and relies solely on green sources and energy storage. The VSC operates in grid-forming mode to maintain stable bipolar DC voltages, ensuring uninterrupted power supply to the data center.

Compared with traditional AC-fed data centers, the proposed DC architecture reduces conversion stages, avoiding cumulative AC-DC-AC losses to improve efficiency and lower cooling demand. Moreover, the bipolar DC bus directly integrates PV and storage without extra inversion, simplifying green power use. Overall, it offers superior long-term environmental and economic returns.

The bipolar DC bus consists of the positive, neutral and negative line, denoted by p, nu and n as shown in Fig. 2 (b). The equivalent circuit is shown in Fig. 2 (c). Nodes can be classified into power and load nodes in the data center power supply system. Power nodes correspond to the converter outlets connecting bipolar DC bus to the AC power network. Load nodes are responsible for distributing electricity to the users, among which those supplying data centers constitute our primary focus. Loads can be categorized into constant power load (CPL), constant resistance load (CRL) and constant current load (CCL) according to their characteristics [29]. There are N load nodes (numbered 1-N) and 2 power nodes (numbered 0, $N+1$) in the network. Data centers can be located at any one or multiple nodes from 1 to N. Within this power supply structure, data centers benefit from multiple power feed paths, resulting in enhanced fault ride-through capability.

In Fig. 2 (c), $V_{sp,1}$, $V_{sn,1}$ represent the positive and negative pole-to-ground voltages at power node 0, respectively. $V_{sp,2}$, $V_{sn,2}$ represent the corresponding voltages at power node $N+1$. The line impedances between node i and node $i+1$ are defined as $R_{p,i}$, $R_{n,i}$ and $R_{nu,i}$ for the positive, negative and neutral lines, respectively. Additionally, $R_{Lp,i}$ and $R_{Ln,i}$ represent the load impedances across the positive-to-neutral and negative-to-neutral paths at node i, respectively.

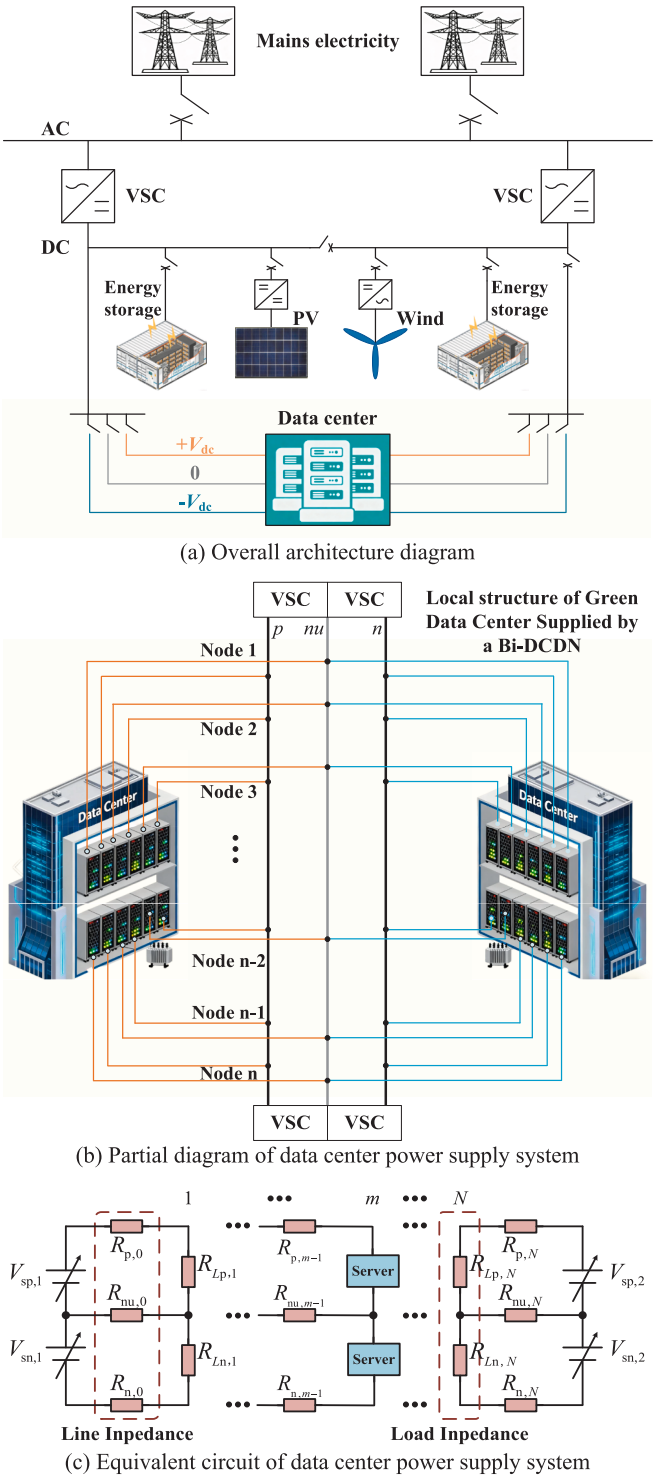


Fig. 2. Data centers supplied by two-terminal VSC with bipolar DC bus.

2.2. Voltage quality Assessment indices

Voltage unbalance is a critical index for assessing the voltage quality of Bi-DCDNs. Excessive voltage unbalance may affect the normal operation of DC loads, increase operational losses in the distribution network, and reduce the economy of the system. To ensure both the stability and economic efficiency of the bipolar DC bus, this paper adopts the definition for voltage unbalance factor (VUF) in [30], as

expressed in (1).

$$U_{\mathrm{uf},i} = \frac{2 \times \left| V_{\mathrm{p},i} - V_{\mathrm{n},i} \right|}{V_{\mathrm{p},i} + V_{\mathrm{n},i}} \times 100\% \tag{1}$$

where $U_{\mathrm{uf},\,i}$ represents the VUF at node i of bipolar DC bus; $V_{\mathrm{p},i}$ and $V_{\mathrm{n},i}$ are the voltage at the positive and negative ports of node i, respectively.

According to the definition of VUF in (1), the cumulative VUF of the multi-node system over multiple time periods can be calculated, as shown in (2).

$$U_{\mathrm{uf}} = \sum\nolimits_{t=1}^{24} \sum_{i=1}^{N} \frac{2 \times \left| V_{\mathrm{p},i}(t) - V_{\mathrm{n},i}(t) \right|}{V_{\mathrm{p},i}(t) + V_{\mathrm{n},i}(t)} \tag{2}$$

where U_{uf} represents the total VUF over 24 h in the entire system; N denotes the total number of the nodes in the system; t denotes the time series; the variables involving t in (2) follow the same definitions as those in (1) and are therefore not repeated.

Eq. (3) presents the index for evaluating voltage deviation factor (VDF) as defined in [27].

$$U_{\mathrm{df},i} = \left(V_{\mathrm{p},i} - V_{\mathrm{pm},i}\right)^2 + \left(V_{\mathrm{n},i} - V_{\mathrm{nm},i}\right)^2 \tag{3}$$

where $U_{\mathrm{df},\,i}$ represents the VUF at node i of bipolar DC bus; $V_{\mathrm{pm,i}}$ and $V_{\mathrm{nm},\,\mathrm{i}}$ represent the rated voltage at positive and negative ports of node i, respectively.

Similarly, the cumulative VDF of the multi-node system over multiple time periods can be reformulated from (3), as shown in (4).

$$U_{\mathrm{df}} = \sum\nolimits_{t=1}^{24} \sum_{i=1}^{N} \left(V_{\mathrm{p},i}(t) - V_{\mathrm{pm},i}\right)^2 + \left(V_{\mathrm{n},i}(t) - V_{\mathrm{nm},i}\right)^2 \tag{4}$$

where U_{df} represents the total VDF over 24 h in the entire system. A higher value of U_{df} indicates a more severe deviation of each node in the distribution network from the rated voltage.

To analyse the VUF and VDF of the network and establish the DC current calculation model, the ZIP load equivalent model is employed to linearize the CPL. Taking the positive CPL $P_{\mathrm{Pp},i}$ at node i as an example, the voltage and current at the port of the CPL conform to the relationship given in Eq. (5):

$$I_{\mathrm{Pp},i} = \frac{P_{\mathrm{Pp},i}}{V_{\mathrm{pnu},i}} \tag{5}$$

where $I_{\mathrm{Pp},i}$ represents the positive CPL current at node i; $V_{\mathrm{pnu},i}$ represents the voltage at the positive port of node i.

During normal operation of the distribution network, the port voltage fluctuation of the CPL remains within the defined operational interval [31]. As a result, $1/V_{\mathrm{pnu},i}$ can be linearly expressed by a first-order Taylor approximation, as shown in (6).

$$\frac{1}{V_{\mathrm{pnu},i}} \approx \frac{1}{V_{\mathrm{pnum},i}} - \left(\frac{1}{V_{\mathrm{pnum},i}}\right)^2 \left(V_{\mathrm{pnu},i} - V_{\mathrm{pnum},i}\right) \tag{6}$$

where $V_{\mathrm{pnum},i}$ represents the rated voltage at the positive port of node i.

A CPL can be linearized into (7) by substituting (6) into (5). Eq. (7) means that the CPL can be equivalently replaced by a parallel structure of a CRL and a CCL, as shown in Fig. 3.

$$I_{\mathrm{Pp},i} = P_{\mathrm{Pp},i}\left[\frac{2}{V_{\mathrm{pnum},i}} - \left(\frac{1}{V_{\mathrm{pnum},i}}\right)^2 V_{\mathrm{pnu},i}\right] \tag{7}$$

Due to the effect of line impedance in the three lines, there exist two points, A and B, with the lowest voltage on the positive and negative poles of bipolar DC bus, respectively. As a result, the line voltage gradually decreases from the power nodes on both sides to these two points, as illustrated in Fig. 4.

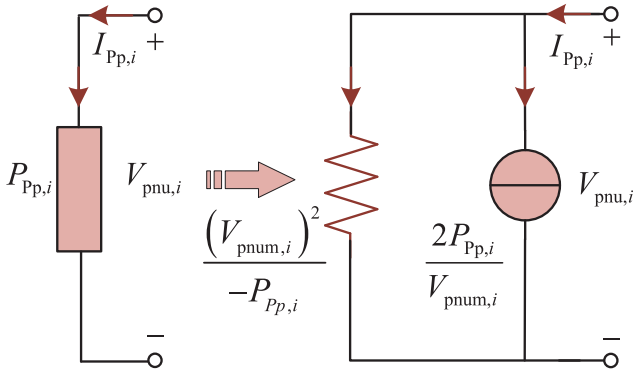


Fig. 3. Linearized equivalent model of CPL.

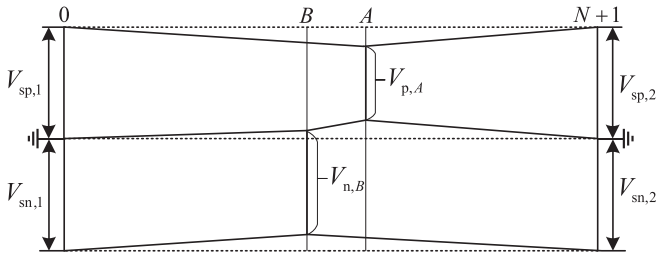


Fig. 4. Influence of line impedance on positive and negative voltages.

2.3. The model of DCESs and considerations for the installation locations

DCES contributes to stabilizing the fluctuating critical load (CL) voltage [32]. Its structures can generally be classified into series and parallel configurations, among which the series-type DCES has received the most research attention [33]. In a series-type DCES, the device is connected in series with the resistive NCLs, collectively forming a smart load. The smart load adjusts the output voltage of the energy storage device, based on port characteristics, allowing it to modify the voltage at both ends of the NCLs. This process helps transfer the power fluctuation from the nodes to the NCLs, ultimately stabilizing the port voltage of the CL. Smart loads are installed at the same node as the CLs to be protected, ensuring that the port voltage of smart load matches that of the CL.

When bipolar DC bus is in a steady state, no power fluctuation needs to be transferred to NCLs. At this time, the voltage across the electric spring remains constant, allowing the DCES to be equivalently modelled as a voltage source [34]. The equivalent model is shown in Fig. 5. In this model, V_{ES} is the voltage of the equivalent controlled voltage source of the electric spring. V_{bus} is the port voltage at the node where the DCES is installed, and I_{bus} is the current flowing into this node. R_{NL} is the resistance of the NCL.

The selection of installation locations for the DCES is determined using electrical distance, which is evaluated through sensitivity analysis. The sensitivity indices used in this analysis are defined in (8). Electrical distance quantifies the strength of the electrical coupling between two buses in a power system. The sensitivity-based method provides an

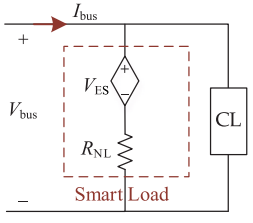


Fig. 5. Equivalent model of DCES.

effective means of computing this index by assessing the similarity of voltage variations between an observed node and a disturbed node under small perturbations [35]. Accordingly, based on this relationship and Equation (8), the corresponding indices can be defined as shown in (9).

$$\begin{cases} VDSI_i = \dfrac{U_{\mathrm{df}}(V_i + \Delta V_i) - U_{\mathrm{df}}(V_i)}{\Delta V_i} \\ VISI_i = \dfrac{U_{\mathrm{uf}}(V_i + \Delta V_i) - U_{\mathrm{uf}}(V_i)}{\Delta V_i} \end{cases} \tag{8}$$

$$\begin{cases} D_{m,i} = \ln(VDSI_i) + \ln(VISI_i) \\ S_m = \sum_{i \neq m} D_{m,i} \end{cases} \tag{9}$$

where the U_{df} and the U_{uf} are the defined indices for VDF and VUF; V_i indicates the voltage of the bus i where a DCES is installed; ΔV_i indicates the voltage promoted by the DCES of the bus i; $VDSI_i$ and $VISI_i$ are the sensitivity indices for the VDF and VUF related to the voltage promotion for bus i respectively; $D_{m,i}$ indicates the electrical distance, representing the comprehensive impact at node i after installing a DCES at node m, with $i \neq m$; and S_m indicates the global impact on the entire system following the installation of a DCES at node m. A larger value of S_m indicates that the regulatory effect of the DCES installed at node m can cover and influence a greater number of nodes across the network.

Therefore, through traversal calculations across all candidate nodes, the node that maximizes the global impact index S_m is selected as the DCES installation location. This process is illustrated in Algorithm 1.

Algorithm 1 Optimal DCES Installation Node Selection

Input: system parameters, N
Output: DCES installation node

$m = 1$
$S_{\max} = 0$
$m_optimal = 1$
While $m<=N$ **Do**
  Calculate the system parameters at this moment
  $S_m = 0$
  For $i = 1$ to N **Do**
    If $i!=m$ **Then**
      Calculate the electrical distance $D_{m,i}$
      $S_m = S_m + D_{m,i}$
    End if
  End for
  If $S_m > S_{\max}$ **Then**
    $S_{\max} = S_m$
    $m_optimal = m$
  End if
  $m = m + 1$
End While
Return $m_optimal$

In practice, DCES deployment faces several constraints. Physical integration is limited by available space in existing data center cabinets, often requiring compact or modular designs. Thermal management becomes critical under high-frequency compensation: forced air cooling may suffice for smaller units, while larger installations may need liquid cooling. Economically, DCES hardware requires a primary investment, but it can reduce server power loss and minimize downtime by improving voltage quality. For data center operators, even a slight reduction in downtime can translate into significant economic value. These considerations, while not the focus of this work, are acknowledged for real-world applications.

This paper investigates the issues of steady-state voltage unbalance and deviation, assuming that the network is resistive. The simplified equivalent circuit of bipolar DC bus is shown in Fig. 6.

After the DCES is deployed, the voltage profile across the system nodes is illustrated in Fig. 7. Compared with Fig. 4, the voltage drop is significantly mitigated.

In Fig. 7, $V_{\mathrm{p},A}$ and $V_{\mathrm{p},A}$' represent the voltage at the positive port of

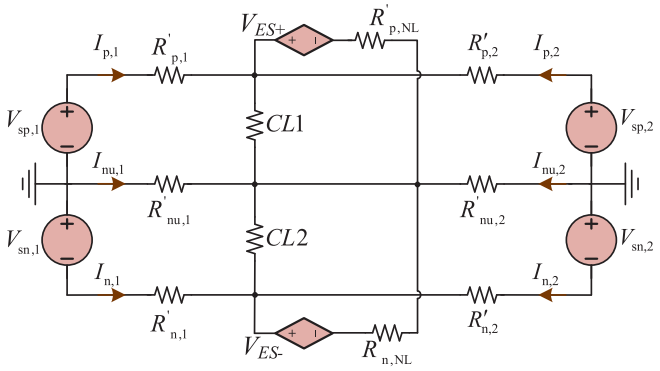


Fig. 6. Simplified equivalent circuit of bipolar DC bus.
where *CL1* and *CL2* represent the positive and negative load impedance of the equivalent circuit, respectively; $R'_{\mathrm{p,1}}$, $R'_{\mathrm{n,1}}$ and $R'_{\mathrm{nu,1}}$ represent the positive, negative, and neutral line impedance of the equivalent circuit on the left side of the installation nodes, respectively; Similarly, $R'_{\mathrm{p,2}}$, $R'_{\mathrm{n,2}}$ and $R'_{\mathrm{nu,2}}$ represent the corresponding impedance on the right side of the installation nodes.

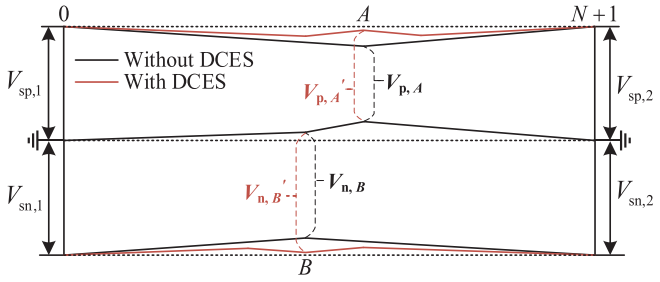


Fig. 7. Voltage variations on positive and negative voltage with DCES.

node A before and after deploying DCES, respectively; $V_{\mathrm{n},B}$ and $V_{\mathrm{n},B}$' denote the corresponding voltages at node B.

2.4. Power flow model incorporating adaptive droop control of VSC

Since the currents flowing into both sides of the power division points in bipolar DC bus are minimal, the network can be approximately decoupled from points A and B (as shown in Fig. 7). For an N-node network, the relationship between the supply voltage and the load currents can be expressed in (10)-(11), with the involved parameters defined in (12)-(18). The current reference direction is set as flowing out of the node.

$$\begin{aligned} \boldsymbol{V}_{\mathrm{ps}} = {} & \boldsymbol{K}_{\mathrm{pa}}\left[\boldsymbol{I}_{\mathrm{Ip}} + \boldsymbol{I}_{\mathrm{Ib}} + \boldsymbol{Y}_{\mathrm{Rp}}\boldsymbol{V}_{\mathrm{pnu}} + \boldsymbol{Y}_{\mathrm{Rb}}\boldsymbol{V}_{\mathrm{pn}}\right] \\ & + \boldsymbol{K}_{\mathrm{pb}}\left[\boldsymbol{I}_{\mathrm{In}} - \boldsymbol{I}_{\mathrm{Ip}} + \boldsymbol{Y}_{\mathrm{Rn}}\boldsymbol{V}_{\mathrm{nun}} - \boldsymbol{Y}_{\mathrm{Rp}}\boldsymbol{V}_{\mathrm{pnu}}\right] + \boldsymbol{K}_{\mathrm{pc}} \end{aligned} \tag{10}$$

$$\begin{aligned} \boldsymbol{V}_{\mathrm{ns}} = {} & \boldsymbol{K}_{\mathrm{na}}\left[\boldsymbol{I}_{\mathrm{In}} + \boldsymbol{I}_{\mathrm{Ib}} + \boldsymbol{Y}_{\mathrm{Rn}}\boldsymbol{V}_{\mathrm{nun}} + \boldsymbol{Y}_{\mathrm{Rb}}\boldsymbol{V}_{\mathrm{pn}}\right] \\ & + \boldsymbol{K}_{\mathrm{nb}}\left[\boldsymbol{I}_{\mathrm{In}} - \boldsymbol{I}_{\mathrm{Ip}} + \boldsymbol{Y}_{\mathrm{Rn}}\boldsymbol{V}_{\mathrm{nun}} - \boldsymbol{Y}_{\mathrm{Rp}}\boldsymbol{V}_{\mathrm{pnu}}\right] + \boldsymbol{K}_{\mathrm{nc}} \end{aligned} \tag{11}$$

$$\begin{cases} \boldsymbol{I}_{\mathrm{Ip}} = \left[I_{\mathrm{Ip},1} \quad I_{\mathrm{Ip},2} \quad \ldots \quad I_{\mathrm{Ip},A} \quad \ldots \quad I_{\mathrm{Ip},N}\right]^{\mathrm{T}} \\ \boldsymbol{I}_{\mathrm{Ib}} = \left[I_{\mathrm{Ib},1} \quad I_{\mathrm{Ib},2} \quad \ldots \quad I_{\mathrm{Ib},A} \quad \ldots \quad I_{\mathrm{Ib},N}\right]^{\mathrm{T}} \\ \boldsymbol{I}_{\mathrm{In}} = \left[I_{\mathrm{In},1} \quad I_{\mathrm{In},2} \quad \ldots \quad I_{\mathrm{In},A} \quad \ldots \quad I_{\mathrm{In},N}\right]^{\mathrm{T}} \end{cases} \tag{12}$$

$$\boldsymbol{K}_{\mathrm{pa}} = \begin{bmatrix} k_{\mathrm{pa},1} & k_{\mathrm{pa},2} & \ldots & k_{\mathrm{pa},A} & \ldots & 0 \\ 0 & 0 & \ldots & k_{\mathrm{pa},N-A} & \ldots & k_{\mathrm{pa},N} \end{bmatrix} \tag{13}$$

$$\boldsymbol{K}_{\mathrm{pb}} = \begin{bmatrix} k_{\mathrm{pb},1} & k_{\mathrm{pb},2} & \ldots & k_{\mathrm{pb},A} & \ldots & 0 \\ 0 & 0 & \ldots & k_{\mathrm{pb},N-A} & \ldots & k_{\mathrm{pb},N} \end{bmatrix} \tag{14}$$

$$\boldsymbol{K}_{\mathrm{na}}=\begin{bmatrix} k_{\mathrm{na},1} & k_{\mathrm{na},2} & \cdots & k_{\mathrm{na},B} & \cdots & 0 \\ 0 & 0 & \cdots & k_{\mathrm{na},N-B} & \cdots & k_{\mathrm{na},N} \end{bmatrix} \tag{15}$$

$$\boldsymbol{K}_{\mathrm{nb}}=\begin{bmatrix} k_{\mathrm{nb},1} & k_{\mathrm{nb},2} & \cdots & k_{\mathrm{nb},B} & \cdots & 0 \\ 0 & 0 & \cdots & k_{\mathrm{nb},N-B} & \cdots & k_{\mathrm{nb},N} \end{bmatrix} \tag{16}$$

$$\begin{cases} \boldsymbol{K}_{\mathrm{pc}}=\begin{bmatrix} k_{\mathrm{pc},1} & k_{\mathrm{pc},2} \end{bmatrix}^{\mathrm{T}} \\ \boldsymbol{K}_{\mathrm{nc}}=\begin{bmatrix} k_{\mathrm{nc},1} & k_{\mathrm{nc},2} \end{bmatrix}^{\mathrm{T}} \end{cases} \tag{17}$$

$$\begin{cases} \boldsymbol{V}_{\mathrm{ps}}=\begin{bmatrix} V_{\mathrm{sp},1} & V_{\mathrm{sp},2} \end{bmatrix}^{\mathrm{T}} \\ \boldsymbol{V}_{\mathrm{ns}}=\begin{bmatrix} V_{\mathrm{sn},1} & V_{\mathrm{sn},2} \end{bmatrix}^{\mathrm{T}} \end{cases} \tag{18}$$

where $\boldsymbol{V}_{\mathrm{ps/ns}}$ is the voltage at the positive and negative ports of power nodes, respectively, both being 2-dimensional column vectors. $\boldsymbol{I}_{\mathrm{Ip/Ib/In}}$ denotes the N-dimensional current column vectors for the positive, bipolar and negative CCLs, respectively. $\boldsymbol{V}_{\mathrm{pnu/pn/nun}}$ is the voltage matrices at the load nodes from positive to neutral, positive to negative, and neutral to negative, respectively, all being N-dimensional column vectors. $\boldsymbol{Y}_{\mathrm{Rp/Rb/Rn}}$ denotes the admittance of the constant impedance components in positive, bipolar and negative load, respectively, all being N-dimensional square matrices with elements only on the diagonal line. $\boldsymbol{K}_{\mathrm{pa/pb}}$ represents the pole-current parameter matrix and the neutral-line current parameter matrix for the adaptive droop control of the positive VSC, respectively, both of which are 2 N-dimensional matrices. In $\boldsymbol{K}_{\mathrm{pa/pb}}$, the first A columns of the first row contain identical non-zero elements, and the last N-A columns of the second row contain another identical non-zero elements, respectively representing positive parameters of power node 0 and $N+1$. Similarly, $\boldsymbol{K}_{\mathrm{na/nb}}$ is the corresponding negative parameters with B replacing A. $\boldsymbol{K}_{\mathrm{pc/nc}}$ represents the constant parameter matrices for the positive and negative VSC, respectively.

Furthermore, the loads connected to the lines are treated as current sources. By decoupling the positive, neutral, and negative lines, the node equations for the three lines are formulated, as shown in (19)-(22):

$$\boldsymbol{V}_{\mathrm{port}}=\begin{bmatrix} \boldsymbol{V}_{\mathrm{pnu}} \\ \boldsymbol{V}_{\mathrm{nun}} \\ \boldsymbol{V}_{\mathrm{pn}} \end{bmatrix}=\boldsymbol{D}\boldsymbol{V}_{\mathrm{pole}}=\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 1 & 0 & -1 \end{bmatrix}\begin{bmatrix} \boldsymbol{V}_{\mathrm{p}} \\ \boldsymbol{V}_{\mathrm{nu}} \\ \boldsymbol{V}_{\mathrm{n}} \end{bmatrix} \tag{19}$$

$$\boldsymbol{I}_{\mathrm{p}}=-\boldsymbol{I}_{\mathrm{Ip}}-\boldsymbol{I}_{\mathrm{Ib}}+\boldsymbol{Y}_{\mathrm{ps}}\boldsymbol{V}_{\mathrm{ps}}-\boldsymbol{Y}_{\mathrm{Rp}}\boldsymbol{V}_{\mathrm{pnu}}-\boldsymbol{Y}_{\mathrm{Rb}}\boldsymbol{V}_{\mathrm{pn}}=\boldsymbol{Y}_{\mathrm{p}}\boldsymbol{V}_{\mathrm{p}} \tag{20}$$

$$\boldsymbol{I}_{\mathrm{nu}}=\boldsymbol{I}_{\mathrm{Ip}}-\boldsymbol{I}_{\mathrm{In}}+\boldsymbol{Y}_{\mathrm{Rp}}\boldsymbol{V}_{\mathrm{pnu}}-\boldsymbol{Y}_{\mathrm{Rn}}\boldsymbol{V}_{\mathrm{nun}}=\boldsymbol{Y}_{\mathrm{nu}}\boldsymbol{V}_{\mathrm{nu}} \tag{21}$$

$$\boldsymbol{I}_{\mathrm{n}}=\boldsymbol{I}_{\mathrm{In}}+\boldsymbol{I}_{\mathrm{Ib}}-\boldsymbol{Y}_{\mathrm{ns}}\boldsymbol{V}_{\mathrm{ns}}+\boldsymbol{Y}_{\mathrm{Rn}}\boldsymbol{V}_{\mathrm{nun}}+\boldsymbol{Y}_{\mathrm{Rb}}\boldsymbol{V}_{\mathrm{pn}}=\boldsymbol{Y}_{\mathrm{n}}\boldsymbol{V}_{\mathrm{n}} \tag{22}$$

where $\boldsymbol{V}_{\mathrm{p/nu/n}}$ is N-dimensional column vectors representing the node-to-ground voltage of positive, neutral, negative nodes. $\boldsymbol{Y}_{\mathrm{ps/ns}}$ represents the connection admittance matrices between positive/ negative load nodes and power nodes, respectively, both being 2 N-dimensional matrices. For example, the element $\boldsymbol{Y}_{\mathrm{ps}}(i,j)$ represents the connection admittance between the load node i and the power node j. Given the symmetry of the positive/ negative poles and identical cable parameters, the admittances satisfy $\boldsymbol{Y}_{\mathrm{ps}}=\boldsymbol{Y}_{\mathrm{ns}}=\boldsymbol{Y}_{\mathrm{s}}$. The node admittance matrices $\boldsymbol{Y}_{\mathrm{p/nu/n}}$ (each N*N) correspond to the three networks after removing the power nodes. Due to the symmetry of the lines, it can also be assumed that $\boldsymbol{Y}_{\mathrm{p}}=\boldsymbol{Y}_{\mathrm{nu}}=\boldsymbol{Y}_{\mathrm{n}}=\boldsymbol{Y}_{\mathrm{L}}$.

Substituting Eqs. (10)-(19) into Eqs. (20)-(22) and performing pairwise subtraction yields the relationship between port voltage and load current, as given in Eq. (23), where $\boldsymbol{A}$ and $\boldsymbol{B}$ are 3 N-dimensional square coefficient matrices corresponding to the load current and port voltage, respectively, and $\boldsymbol{C}$ is a 3 N-dimensional column vector. These matrices and vector are directly constructed from the network parameters defined in Eqs. (10)-(18). The specific forms of $\boldsymbol{A}$, $\boldsymbol{B}$, and $\boldsymbol{C}$ are provided in the Appendix A.

$$\boldsymbol{A}\begin{bmatrix} \boldsymbol{I}_{\mathrm{Ip}} & \boldsymbol{I}_{\mathrm{In}} & \boldsymbol{I}_{\mathrm{Ib}} \end{bmatrix}^{\mathrm{T}}+\boldsymbol{C}=\boldsymbol{B}\boldsymbol{V}_{\mathrm{port}} \tag{23}$$

3. Voltage quality compensation equivalent model and parameter identification

3.1. Voltage quality compensation equivalent model

Voltage quality at the load nodes can arise due to source-side control and load fluctuations. To improve power quality, it is essential to implement control measures.

To compensate for the voltage drop across the line impedance, adaptive droop control is introduced into the VSC. As discussed in Section 2.2, all loads viewed from bipolar DC bus can be transformed into a combination of CCLs and CRLs through the ZIP load linearization model. From the perspective of the power supply port, the CCL component remains unchanged over time, whereas the CRL component varies proportionally with system conditions. Consequently, the droop control equations for each supply voltage should contain both primary and constant terms related to the neutral-line current and pole line current. The specific formulation is given in Eq. (24):

$$\begin{cases} V_{\mathrm{sp},j}=Z_{\mathrm{eqp},j}I_{\mathrm{p},j}+Z_{\mathrm{eqnu},j}I_{\mathrm{nu},j}+V_{\mathrm{eqp}} \\ V_{\mathrm{sn},j}=Z_{\mathrm{eqn},j}I_{\mathrm{n},j}+Z_{\mathrm{eqnu},j}I_{\mathrm{nu},j}+V_{\mathrm{eqn}} \end{cases} \tag{24}$$

where, j is equal to 1 or 2, representing the power node 0 or $N+1$; $V_{\mathrm{sp},j}$ and $V_{\mathrm{sn},j}$ denote the VSC reference voltages of positive and negative after compensation, respectively; $Z_{\mathrm{eqp},j}$ and $Z_{\mathrm{eqn},j}$ are the parameters used to compensate for the voltage drop of the positive and negative lines, respectively; $Z_{\mathrm{eqnu},j}$ is the parameter used to compensate for the potential fluctuation in the neutral line; V_{eqp} and V_{eqn} are fixed parameters related to the voltage compensation of the positive and negative, respectively.

3.2. Parameter identification based on the least squares method

For the adaptive droop control mechanism for VSC, the droop coefficient serves as the key control parameter. Based on the defined indices U_{uf} and U_{df}, an optimization model is established with the following objective:

$$\mathrm{Min}\ f=\alpha U_{\mathrm{uf}}+(1-\alpha)U_{\mathrm{df}} \tag{25}$$

where α is a weight coefficient.

Subsequently, the total load power at each bus is set to follow a typical daily load curve, while the load ratio (positive: negative) varies between 1 and 1.5. This yields a dataset of load power scenarios. For each scenario, the optimal VSC voltage and the corresponding output current are obtained by solving the established objective function and the power flow model.

Based on this dataset, the parameters of the voltage compensation equivalent model are identified using the Least Squares Method. As the coefficients are derived from data spanning a broad range operating conditions, the resulting model exhibits strong robustness, thereby enabling the droop control strategy to adapt effectively to varying load states. Taking the adaptive droop control parameter identification for the positive-pole VSC as an example, the loss function is defined in matrix form as follows:

$$\boldsymbol{L}_{\mathrm{p}}=\frac{1}{N}(\boldsymbol{Y}-\boldsymbol{X}\boldsymbol{w}_{\mathrm{p}})^{\mathrm{T}}(\boldsymbol{Y}-\boldsymbol{X}\boldsymbol{w}_{\mathrm{p}}) \tag{26}$$

where

$$\boldsymbol{w}_{\mathrm{p}}=\begin{bmatrix} Z_{\mathrm{eqp},1} & Z_{\mathrm{eqnu},1} & Z_{\mathrm{eqp},2} & Z_{\mathrm{eqnu},2} & V_{\mathrm{eqp}} \end{bmatrix} \tag{27}$$

$$\boldsymbol{X}=\begin{bmatrix} \boldsymbol{I}_{\mathrm{p1}} & \boldsymbol{I}_{\mathrm{nu1}} & \boldsymbol{I}_{\mathrm{p2}} & \boldsymbol{I}_{\mathrm{nu2}} & \boldsymbol{2} \end{bmatrix} \tag{28}$$

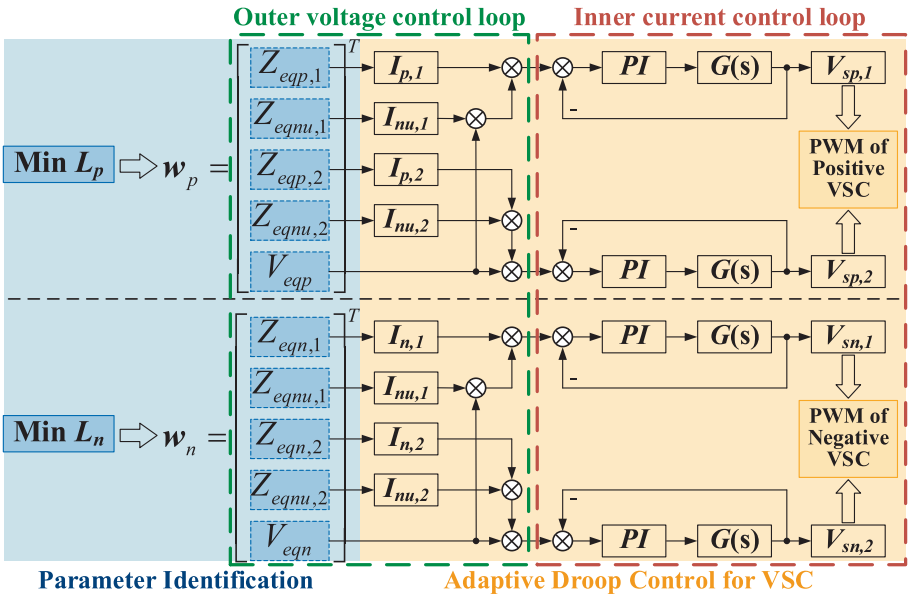


Fig. 8. VSC control loop.

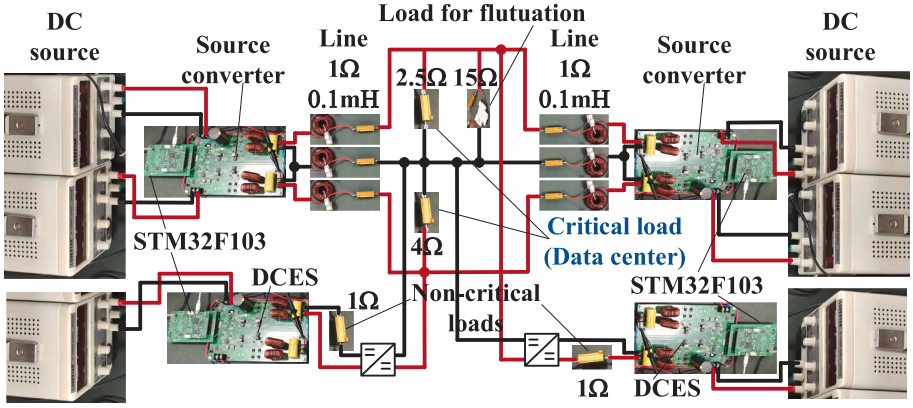


Fig. 9. Hardware connection diagram.

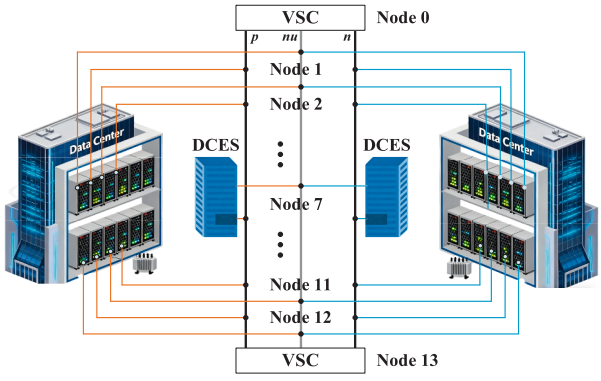


Fig. 10. 14-node two-terminal Bi-DCDN model.

$$\boldsymbol{Y} = \boldsymbol{V}_{sp,1} + \boldsymbol{V}_{sp,2} \tag{29}$$

where $\boldsymbol{w}_p$ is the parameter vector of the power supply voltage compensation equivalent model to be solved; $\boldsymbol{X}$ is the current matrix of the operational data; $\boldsymbol{I}_{p1/nu1/p2/nu2}$ is the positive current of node 0, the neutral-line current of node 0, the positive current of node $N+1$, and the neutral-line current of node $N+1$, respectively, all of which are 24-dimensional vectors; $\boldsymbol{2}$ is a 24-dimensional vector of all twos; $\boldsymbol{Y}$ is the voltage matrix of historical operational data; $\boldsymbol{V}_{sp,1}$ and $\boldsymbol{V}_{sp,2}$ are the voltage vector at the positive port of node 0 and node $N+1$,

Table 2
Parameter of the two-terminal VSC with a 14-bus Bi-DCDN.

Starting node	Ending node	Line impedance/ Ω	Load power at the ending node		
			L_p/ kW	L_n/ kW	L_b/ kW
0	1	0.037	20.8	16	0
1	2	0.032	11.7	9	0
2	3	0.038	9.1	7	0
3	4	0.037	10.4	8	0
4	5	0.033	15.6	12	0
5	6	0.016	16.9	13	0
6	7	0.036	10.4	8	0
7	8	0.037	15.6	12	0
8	9	0.033	16.9	13	0
9	10	0.033	9.1	7	0
10	11	0.026	20.8	16	0
11	12	0.027	11.7	9	0
12	13	0.019	–	–	–

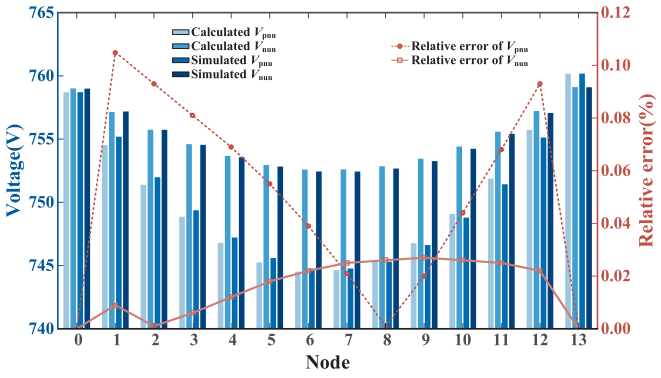


Fig. 11. Comparison of simulation results of voltage calculation.

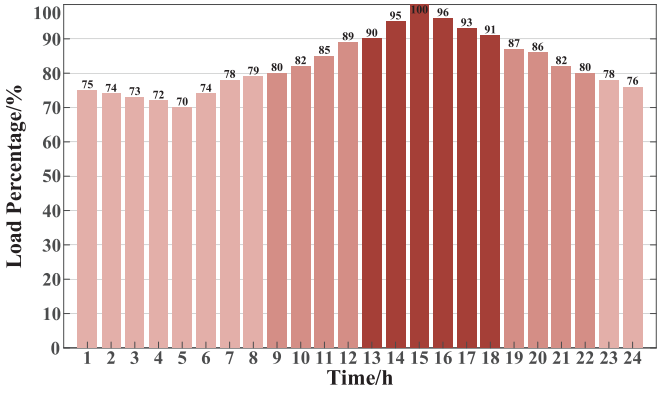


Fig. 12. Daily load change curve of the DCDN.

Table 3
Proportion of positive and negative load in each case.

Load ratio (Positive: Negative)	Load unbalance degree
1.0	0.0%
1.1	9.5%
1.2	18.2%
1.3	26.1%
1.4	33.3%
1.5	40.0%

respectively, both of which are 24-dimensional vectors.

To minimize the loss function, set the partial derivative of $\boldsymbol{L}_{\mathrm{p}}$ equal to zero:

$$\frac{\partial \boldsymbol{L}_{\mathrm{p}}}{\partial \boldsymbol{w}_{\mathrm{p}}} = \frac{2}{N}\boldsymbol{X}^{T}\boldsymbol{X}\boldsymbol{w}_{\mathrm{p}} - \frac{2}{N}\boldsymbol{X}^{T}\boldsymbol{Y} = 0 \tag{30}$$

The solution is obtained as:

$$\boldsymbol{w}_{\mathrm{p}} = \left(\boldsymbol{X}^{T}\boldsymbol{X}\right)^{-1}\boldsymbol{X}^{T}\boldsymbol{Y} \tag{31}$$

Since the output characteristics of the VSC are highly sensitive to its droop coefficients, the accuracy of least squares identification is critical. The loss function $\boldsymbol{L}_{\mathrm{p}}$ quantifies the sum of squared residuals between $\boldsymbol{Y}$ and the product term $\boldsymbol{X}\boldsymbol{w}_{\mathrm{p}}$ over 24 h. Minimizing $\boldsymbol{L}_{\mathrm{p}}$ yields the parameter vector $\boldsymbol{w}_{\mathrm{p}}$ that best fits the data within the expected operating range. According to least squares theory [36], the wide coverage of operating conditions ensures persistent excitation of the input data matrix, thereby guaranteeing the accuracy and robustness of the identified parameters. Therefore, the identified $\boldsymbol{w}_{\mathrm{p}}$ can meet the engineering accuracy requirements for adaptive droop control.

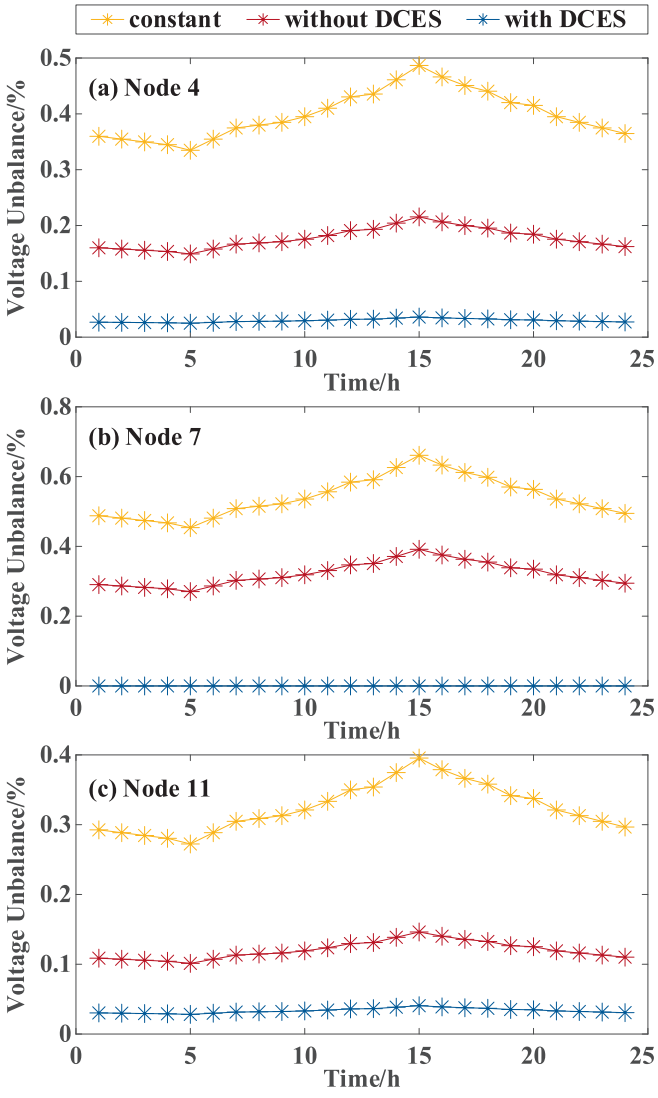


Fig. 13. Voltage unbalance variation curve.

4. The joint improvement strategy of voltage quality based on voltage compensation equivalent model

4.1. Power supply voltage unbalance suppression

When the load distribution is seriously uneven, the voltage unbalance of power supply after adaptive droop control compensation may exceed the permissible range. In such case, unbalance suppression is necessary. According to Eq. (1), when the positive and negative voltages just meet the maximum allowable voltage unbalance, the supply voltage is shown in (32).

$$V_{\mathrm{sp},j} = \frac{200 + (2x-1)\varepsilon}{200 - (2x-1)\varepsilon} V_{\mathrm{sn},j} \tag{32}$$

where ε represents the maximum allowable VUF; the variable $x \in \{0, 1\}$ is determined by voltage relationship: $x = 1$ if $V_{\mathrm{sp},j} > V_{\mathrm{sn},j}$, and $x = 0$ otherwise.

When the supply voltage after adaptive droop control compensation falls within the allowable unbalance range, no further regulation is required. If the compensated supply voltage remains outside the allowable unbalance range, additional suppression measures is necessary to meet the minimum unbalance requirement. In scenarios where suppression is required, the objective function F, which quantifies the

difference in power supply voltage before and after unbalance suppression, is defined in (33).

$$F = \left(V_{\mathrm{Osp},j} - V_{\mathrm{sp},j}\right)^2 + \left(V_{\mathrm{Osn},j} - V_{\mathrm{sn},j}\right)^2 \tag{33}$$

where $V_{\mathrm{Osp},j}$ and $V_{\mathrm{Osn},j}$ represent the positive and negative supply voltages after unbalance suppression, respectively.

By substituting Eq. (32) into Eq. (33) and minimizing the objective function F, the results are obtained ad shown in (34)-(35), where the variable x is defined as in Eq. (32).

$$\begin{cases} V_{\mathrm{Osp},j} = \dfrac{\alpha^2 V_{\mathrm{sp},j} + \alpha V_{\mathrm{sn},j}}{\alpha^2 + 1} \\ V_{\mathrm{Osn},j} = \dfrac{\alpha V_{\mathrm{sp},j} + V_{\mathrm{sn},j}}{\alpha^2 + 1} \end{cases} \tag{34}$$

$$\alpha = \frac{200 + (2x-1)\varepsilon}{200 - (2x-1)\varepsilon} \tag{35}$$

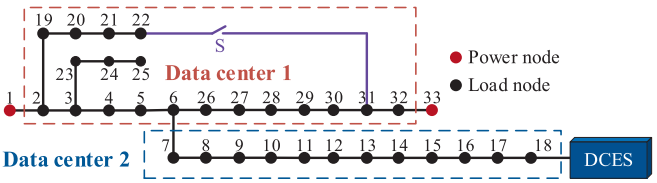


Fig. 15. Modified IEEE 33-bus Test System with DCES.

4.2. Joint improvement strategy

The control scheme based on the voltage compensation equivalent model is shown in Fig. 8, where $\boldsymbol{L}_{\mathrm{p/n}}$ is the loss functions for the positive and negative poles, respectively; $\boldsymbol{w}_{\mathrm{p/n}}$ is the corresponding derived parameter vectors of the voltage compensation equivalent model. The green dashed box in the figure represents the voltage outer loop, and the DC voltage reference value at its output is calculated using Eq. (24). The red dashed box represents the current inner loop, which adopts a

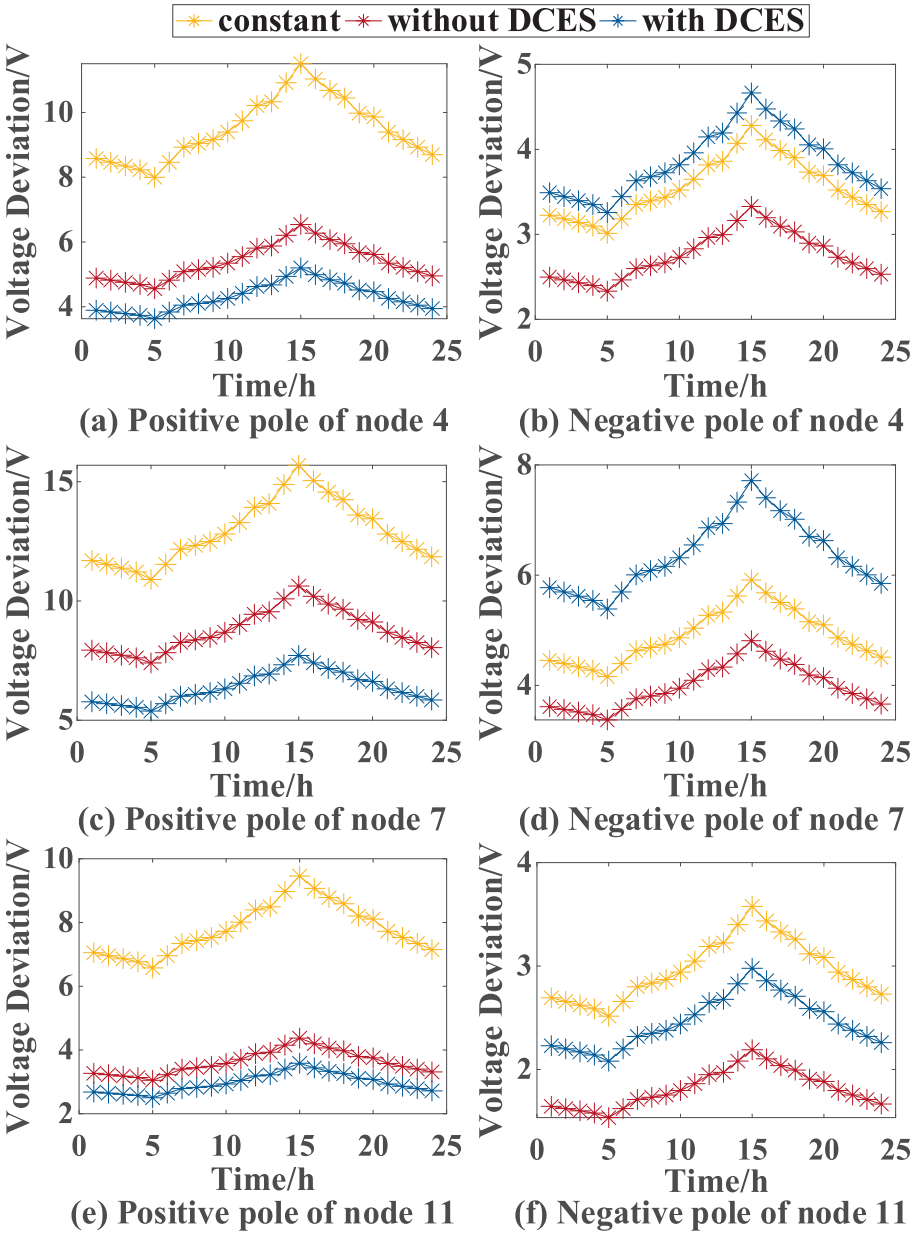


Fig. 14. Voltage deviation variation curve.

Table 4
Comparison of indices of three strategies.

Strategy	U_{uf} (%)	U_{df} (V^2)
Constant	108.1782	3.0783×10^4
Droop without DCES	53.4174	1.2468×10^4
Droop with DCES	11.3969	1.1063×10^4

conventional current control scheme and is not elaborated further.

Algorithm 2 provides the complete voltage quality improvement strategy.

Algorithm 2 Voltage Control with DCES and Compensation from VSC

Initialize system parameters
Construct power flow model considering voltage compensation and DCES
Obtain the operational data of the power flow model
Calculate control parameters:
  $I_{p/n/nu,\ 1}$, V_{eqp}, $Z_{eqp/eqn/eqnu,\ 1}$
  $I_{p/n/nu,\ 2}$, V_{eqn}, $Z_{eqp/eqn/eqnu,\ 2}$
Perform VSC droop control
For $j = 1$ to 2 **Do**
  If $2|\ V_{sp,\ j} - V_{sn,\ j}\ |/(V_{sp,\ j} + V_{sn,\ j}) >= \varepsilon$ **Then**
    $V_{Osp,\ j} = (\alpha^2 \times V_{sp,\ j} + \alpha \times V_{sn,\ j})/(\alpha^2 + 1)$
    $V_{Osn,\ j} = (\alpha \times V_{sp,\ j} + V_{sn,\ j})/(\alpha^2 + 1)$
  End if
End for
Return

5. Simulation analysis and verification

To validate the proposed strategy for jointly mitigating voltage unbalance and deviation, a series of cases are conducted, progressing from software simulations to hardware experiments. The simulation environment is conducted in MATLAB/Simulink based on a 14-node Bi-DCDN model, as illustrated in Fig. 10, with parameters detailed in Table 2. The subsequent cases are performed: Case 1 verifies the accuracy of the proposed power flow calculation model; Case 2 and Case 3 independently evaluate the suppression effect on voltage unbalance and voltage deviation, respectively, within the 14-node system; Case 4 tests the strategy's scalability in a modified IEEE 33-node system shown in Fig. 15; and Case 5 demonstrates its feasible verification in a 14-node Simulink model. Finally, Case 6 involves experiments on a hardware platform, with the experimental setup and circuit connections shown in Fig. 9, where the critical loads represent data center servers.

Case 1. Verification of the power flow calculation model.

The line impedance parameters between nodes, as given in Table 2, are kept constant. To verify the power flow calculation model, the power flow of the DCDN without DCES is computed using two approaches: (1) software simulation methods and (2) the power flow calculation method incorporating the adaptive droop control of VSC. The results are presented in Fig. 11.

As the chart demonstrates, the correctness of the power flow model has been verified.

Case 2. Verification of Voltage Unbalance Suppression

From the historical operational data of the power flow model, the average daily load variation curve of the network is obtained as shown in Fig. 12. The bar chart illustrates a typical daily load profile, showing the ratio of node load power to a base value over 24 h. The load remains relatively stable and low during the early morning hours, gradually increases after 7 a.m., and reaches its peak around 14:00. It then slowly declines in the late afternoon and evening hours. This trend reflects a typical "valley-rise-peak-decline" pattern in daily electricity demand.

Table 3 [37] presents six different load distribution cases for the two-terminal Bi-DCDN model. The load unbalance degree is defined as twice the absolute load difference between poles divided by the total load. In Table 3, the loads connected to the negative pole line of the network remain consistent with those in Table 2. By changing the load ratio between positive and negative, the load unbalance of the network is simulated.

Case 2 maintains the model parameters in Table 2 and selects the load ratio of 1.2 in Table 3. The simulation compares and verifies the voltage unbalance under three strategies: constant power supply voltage

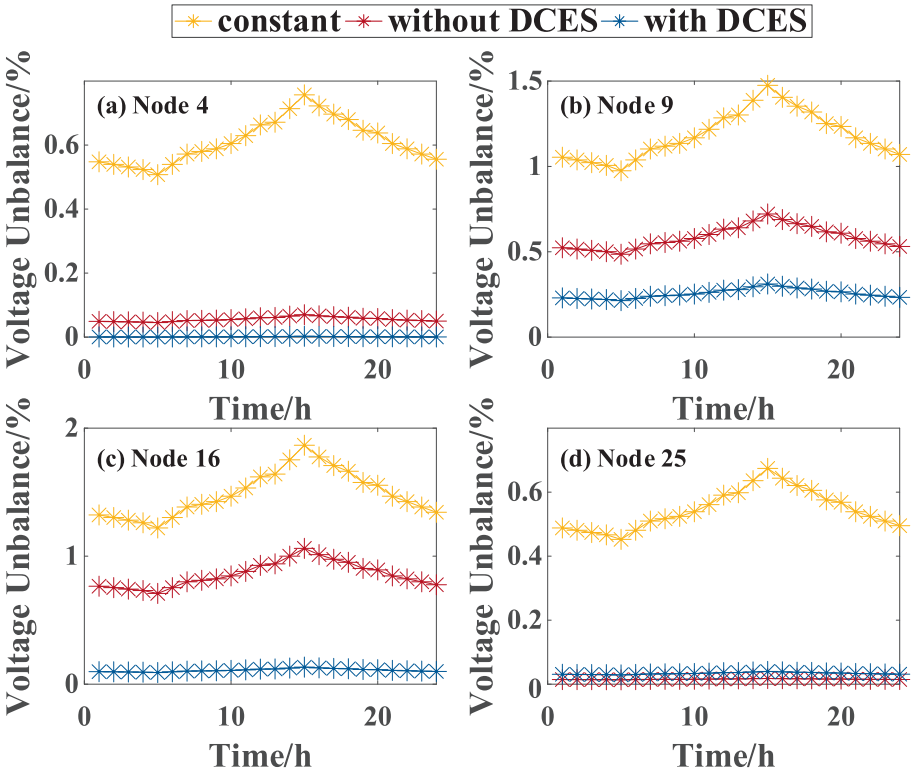


Fig. 16. Voltage unbalance variation curve.

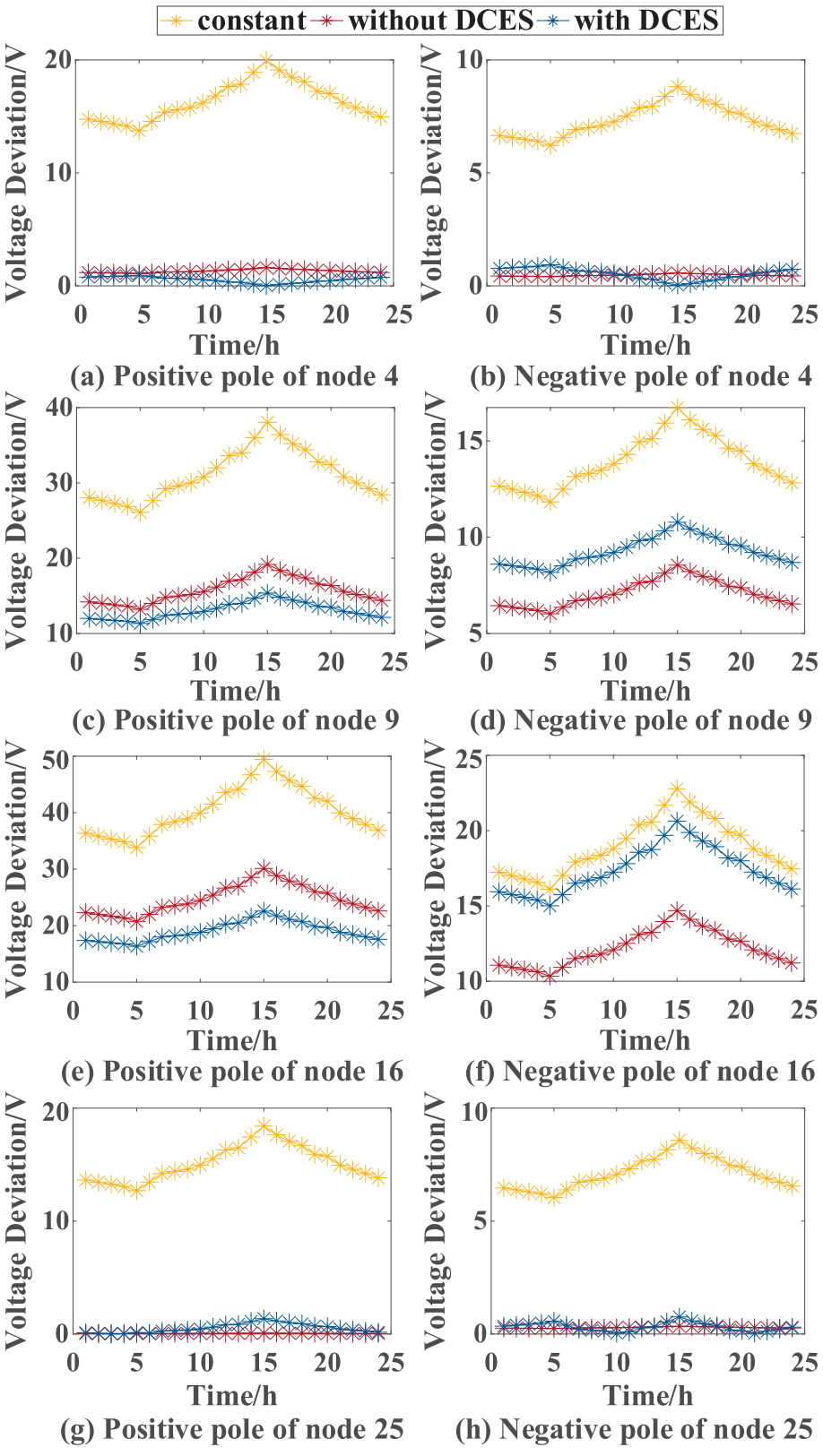


Fig. 17. Voltage deviation variation curve.

(Strategy 1: constant), droop control [27] of VSC (Strategy 2: droop without DCES), and adaptive droop control of VSC along with DCES (Strategy 3: droop with DCES) installed at node 7.

It is worth noting that droop control is the most widely adopted VSC control method in DC systems. Strategy 2 adopts the conventional droop control from Ref. [27] as a representative benchmark. Strategy 3 further integrates the proposed adaptive droop control with DCES. More advanced methods (e.g., communication-based coordinated control or AI-driven optimization) rely on fundamentally different assumptions (e.g., high-speed communication or global information) and are therefore

Table 5
Comparison of indices of three strategies.

Strategy	U_{uf} (%)	U_{df} (V^2)
Constant	607.2120	5.7482×10^5
Droop without DCES	275.9111	1.6723×10^5
Droop with DCES	103.8816	1.4643×10^5

not comparable under the same problem setting. Hence, the comparison between Strategy 2 and Strategy 3 constitutes a fair and meaningful evaluation of the proposed strategy.

Fig. 13 shows the curves of voltage unbalance variation over time at nodes 4, 7 and 11, respectively. The comparison shows that the constant voltage strategy results in the highest voltage unbalance, while the droop with DCES strategy achieves the lowest overall level.

From the yellow curves in Fig. 13, under the constant voltage strategy, nodes farther from the power supply exhibit larger voltage unbalance at the same time instant due to accumulated line impedance effects. As the load varies, the voltage unbalance fluctuates significantly, ranging from 0.27% to 0.66%, indicating weak robustness against load variations.

When droop control without DCES is applied, the voltage unbalance at all nodes is significantly reduced. The variation becomes smoother, with values ranging from 0.10% to 0.39%, demonstrating improved voltage regulation capability. At node 7, the average unbalance is reduced by more than 40% compared with the constant voltage strategy.

When the droop with DCES strategy is employed, a distinct enhancement effect is observed. At the installation node (node 7), the DCES provides direct and fast power compensation, resulting in a near-zero voltage unbalance, as shown by the blue curve in Fig. 13 (b). For nodes away from node 7 (nodes 4 and 11), although the improvement is obvious, it is not as close to zero as node 7. This is because the compensation effect of DCES attenuates with electrical distance, due to network impedance and coupling between nodes. Consequently, the voltage unbalance reduction is weaker at remote nodes.

Overall, the results indicate that the proposed strategy can significantly improve voltage quality at critical nodes while maintaining acceptable performance across the network. This behavior is consistent with the design objective of prioritizing voltage quality at key load nodes in data center applications.

Case 3. Verification of Voltage Deviation Suppression

Case 3 maintains the model parameters in Table 2 and selects the load ratio of 1.2 in Table 3. The simulation compares and verifies the voltage deviation under three strategies: constant, droop without DCES, and droop with DCES. Fig. 14 shows the curves of the voltage deviation variation over time at nodes 4, 7 and 11, respectively. Deviations in the figures are expressed as absolute values.

Two phenomena can be observed from the figure. First, the positive deviation with DCES is smaller than that without DCES. Second, the negative voltage deviation with DCES is larger than that without DCES. The reason for this phenomenon lies in the setup of the case study, where the positive load is consistently greater than the negative load. Therefore, without DCES, the deviation of the negative voltage from its rated value is smaller than that of the positive voltage. After DCES is installed, in order to suppress the voltage unbalance, it brings the positive and negative voltages toward an equal target. This results in a decrease in positive deviation and an increase in negative deviation compared with the droop strategy without DCES. However, the deviations always remain within the acceptable range, i.e., below 1% of the rated voltage.

Table 4 intuitively presents the aggregated performance indices of the system under different control methods using specific data, where U_{uf} is calculated by Eq. (2), representing voltage unbalance, and U_{df} is

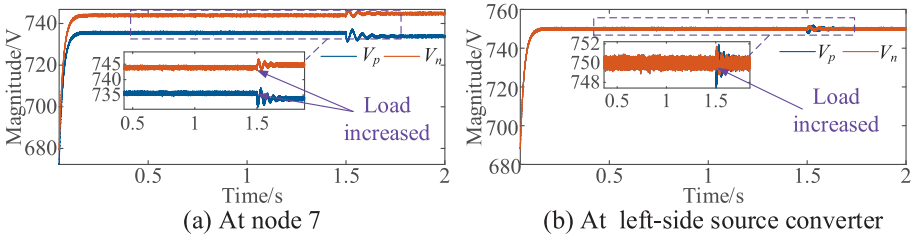


Fig. 18. Voltage variation under the strategy of constant.

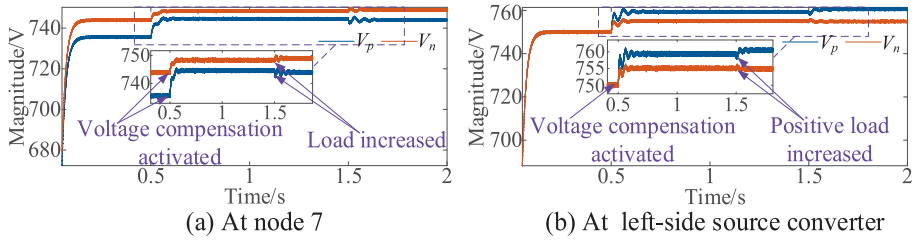


Fig. 19. Voltage variation under the strategy of droop without DCES.

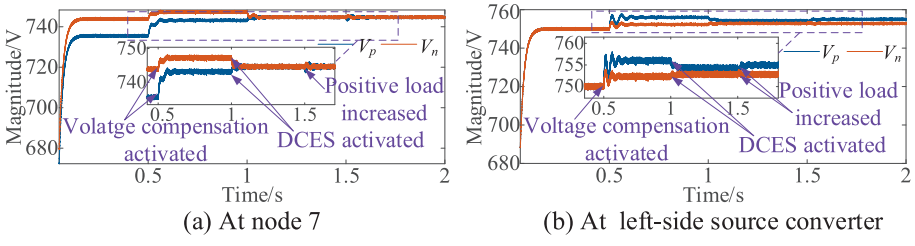


Fig. 20. Voltage variation under the strategy of droop with DCES.

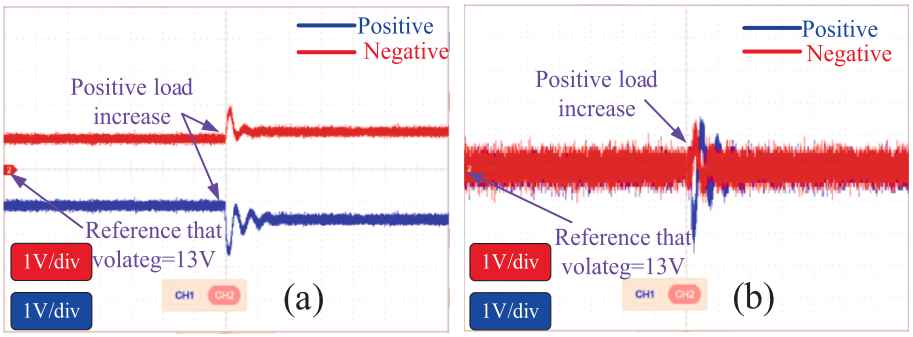


Fig. 21. Voltage variation under the strategy of constant at (a) load (b) source converter.

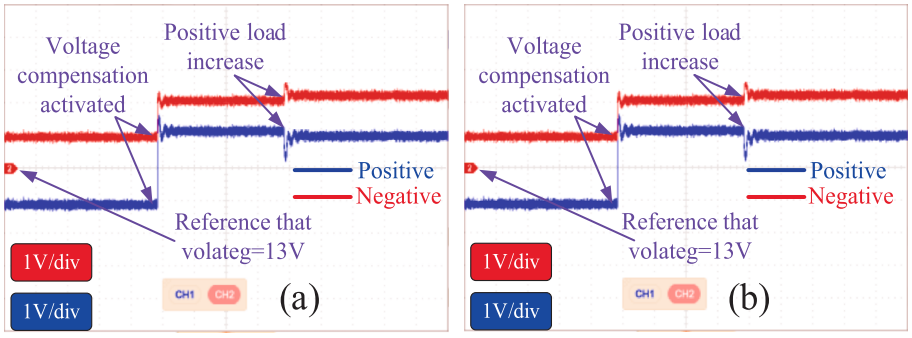


Fig. 22. Voltage variation under the strategy of droop without DCES at (a) load (b) source converter.

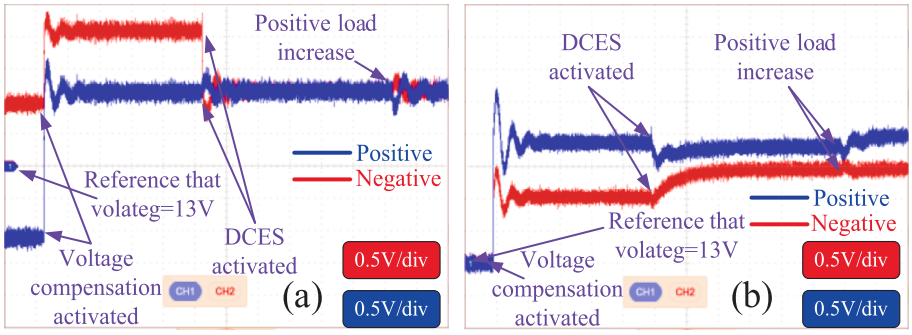


Fig. 23. Voltage variation under the strategy of droop with DCES at (a) load (b) source converter.

calculated by Eq. (4), representing voltage deviation.

The data provide a more effect of the joint improvement strategy. The indices of the three strategies are decreasing in turn. Compared with the strategy of constant power supply voltage, the strategy of droop with DCES reduces U_{uf} by 89% and U_{df} by 64%.

Case 4. Modified IEEE 33-node Test System.

To verify the effectiveness of the proposed method on a more complicated system, a case study is conducted on a modified IEEE 33-bus test system [38]. Topology of the test system is illustrated in Fig. 15, where S is a switch. The line inductance and reactive load power are ignored. Base value of total load power for each node equal is half of the active power in the original test system. Based on the electrical distance-guided configuration method, the node 18 is selected to install a DCES.

When the ratio of positive and negative load is 1.5:1.0, the simulation verifies the voltage unbalance and deviation in three conditions: constant power supply voltage, droop without DCES, and droop with DCES.

Fig. 16 shows the curves of the voltage unbalance variation over time at nodes 4, 9, 16 and 25, respectively. It can be seen from the figure that, in IEEE 33-bus system, overall, the voltage unbalance corresponding to the three strategies shows a decreasing law, which is consistent with the conclusion validated in the 14-node system.

Fig. 17 show the curves of the positive and negative voltage deviation variation over time at nodes 4, 9,16 and 25, respectively. Deviations in the figures are expressed as absolute values.

As illustrated in Fig. 17, two phenomena similar to those observed in the 14-node system again appear. First, the positive deviation with DCES is smaller than that without DCES. Second, the negative voltage deviation with DCES is larger than that without DCES. The reasons are also the same as those in the 14-node system, primarily because the positive load is consistently larger than the negative load, and because the system aims to minimize the weighted sum of voltage unbalance and voltage deviation.

Table 5 more intuitively compares the final indices under three strategies through specific data, where U_{uf} is calculated by Eq. (2), representing voltage unbalance, and U_{df} is calculated by Eq. (4), representing voltage deviation.

The data provide a more effect of the joint improvement strategy. The indices of the three strategies are decreasing in turn. Compared with the strategy of constant power supply voltage, the strategy of droop with DCES reduces U_{uf} by 82% and U_{df} by 74%.

Through the comparison of the above four examples, it's obvious that DCES is effective in reducing voltage fluctuations and ensuring stable operation of the Bi-DCDN. By strategically deploying DCES at critical nodes, the system achieves better voltage regulation, thereby enhancing power quality and reliability of data center.

Case 5. Feasible verification in Simulink.

To evaluate the feasibility of the proposed method, a simulation based on the system shown in Fig. 10 is conducted using Simulink. In Fig. 18, under the control strategy where the source voltage is maintained constant, the voltage curves of node 7 and the left-side source converter are presented. Using the same system configuration, Fig. 19 and Fig. 20 illustrate the voltage curves for the same locations under the control strategies with source voltage compensation—without and with joint DCES, respectively.

From Fig. 19 and Fig. 20, it can be observed that once the voltage compensation control is activated, the voltages are effectively improved and stabilized, despite some initial oscillations. This result demonstrates the feasibility of the proposed strategy. Furthermore, as shown in Fig. 20, after the activation of the DCESs, the positive and negative voltages of bus 7 are ultimately balanced and stabilized. Even when subjected to load power fluctuations, the system maintains voltage balance after a brief period of oscillation. These results further validate the effectiveness of the joint voltage compensation and DCES strategy for Bi-DCDNs.

Case 6. Experiments Carried out on the Hardware Platform.

The physical experiment in Fig. 9 was carried out. Fig. 21, Fig. 22, Fig. 23 present the oscilloscope results after subtracting 13 V from the port voltage curves of the load and source converter under the three strategies. A comparison of these figures reveals that the voltage curves of both the loads and source converters exhibit trends similar to those observed in the simulation results shown in Fig. 18- Fig. 20, thereby demonstrating the hardware feasibility of the proposed method.

6. Conclusions

This paper proposes a joint voltage improvement strategy for mitigating voltage unbalance and deviation in data centers supplied by two-terminal VSC with bipolar DC bus. The strategy integrates adaptive droop control on both the VSC and the DCES to enhance voltage levels and minimize voltage losses, thereby realizing coordinated voltage control across the entire power supply system of the data center. The main conclusions are as follows:

(1) Simulation results from both the 14-node and 33-node test systems demonstrate the strategy's superior performance, achieving a maximum reduction of 89% in voltage unbalance and 74% in voltage deviation compared to conventional methods. This outcome validates the proposed system-level control strategy and confirms its high effectiveness in achieving comprehensive voltage quality improvement.

(2) The strategic deployment of DCES, guided by the electrical distance principle, effectively reduced voltage unbalance at critical nodes, even approaching zero. This result not only validates the configuration method but also demonstrates the powerful capability of DCES in executing precise node-level voltage compensation.

(3) The consistent performance observed across both feasible verification in Simulink and experiments in hardware platform, including stable voltage recovery under load fluctuations, confirms the strategy's robustness. This close agreement between simulation and experimental results strongly indicates its high feasibility for practical engineering applications.

In summary, this research provides a validated solution for voltage quality improvement in next-generation data center power supplies.

CRediT authorship contribution statement

Jianquan Liao: Writing – review & editing, Methodology, Investigation. **Jiameng Cai:** Writing – original draft, Software, Investigation, Formal analysis. **Yiyao Zhou:** Writing – review & editing, Validation, Methodology, Formal analysis. **Junzhi Ren:** Writing – review & editing, Validation. **Tao Huang:** Resources, Formal analysis, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A

Supplement to Equa**tion (23)**

$$\boldsymbol{A} = [\boldsymbol{A}_1 \quad \boldsymbol{A}_2 \quad \boldsymbol{A}_3] \tag{A1}$$

$$\boldsymbol{A}_1 = \begin{bmatrix} -2\boldsymbol{E} + \boldsymbol{Y}_{ps}\boldsymbol{K}_{pa} - \boldsymbol{Y}_{ps}\boldsymbol{K}_{pb} \\ \boldsymbol{E} - \boldsymbol{Y}_{ns}\boldsymbol{K}_{nb} \\ -\boldsymbol{E} + \boldsymbol{Y}_{ps}\boldsymbol{K}_{pa} - \boldsymbol{Y}_{ps}\boldsymbol{K}_{pb} - \boldsymbol{Y}_{ns}\boldsymbol{K}_{nb} \end{bmatrix} \tag{A2}$$

$$\boldsymbol{A}_2 = \begin{bmatrix} \boldsymbol{E} + \boldsymbol{Y}_{ps}\boldsymbol{K}_{pb} \\ -2\boldsymbol{E} + \boldsymbol{Y}_{ns}\boldsymbol{K}_{na} + \boldsymbol{Y}_{ns}\boldsymbol{K}_{nb} \\ \boldsymbol{Y}_{ps}\boldsymbol{K}_{pb} - \boldsymbol{E} + \boldsymbol{Y}_{ns}\boldsymbol{K}_{na} + \boldsymbol{Y}_{ns}\boldsymbol{K}_{nb} \end{bmatrix} \tag{A3}$$

$$\boldsymbol{A}_3 = \begin{bmatrix} -\boldsymbol{E} + \boldsymbol{Y}_{ps}\boldsymbol{K}_{pa} \\ -\boldsymbol{E} + \boldsymbol{Y}_{ns}\boldsymbol{K}_{na} \\ -2\boldsymbol{E} + \boldsymbol{Y}_{ps}\boldsymbol{K}_{pa} + \boldsymbol{Y}_{ns}\boldsymbol{K}_{na} \end{bmatrix} \tag{A4}$$

$$\boldsymbol{B} = [\boldsymbol{B}_1 \quad \boldsymbol{B}_2 \quad \boldsymbol{B}_3] \tag{A1}$$

$$\boldsymbol{B}_1 = \begin{bmatrix} \boldsymbol{Y}_L + \boldsymbol{Y}_{ps}\boldsymbol{K}_{pb}\boldsymbol{Y}_{Rp} - \boldsymbol{Y}_{ps}\boldsymbol{K}_{pa}\boldsymbol{Y}_{Rp} + 2\boldsymbol{Y}_{Rp} \\ -\boldsymbol{Y}_{Rp} + \boldsymbol{Y}_{ns}\boldsymbol{K}_{nb}\boldsymbol{Y}_{Rp} \\ -\boldsymbol{Y}_{ps}\boldsymbol{K}_{pa}\boldsymbol{Y}_{Rp} + \boldsymbol{Y}_{ps}\boldsymbol{K}_{pb}\boldsymbol{Y}_{Rp} + \boldsymbol{Y}_{Rp} + \boldsymbol{Y}_{ns}\boldsymbol{K}_{nb}\boldsymbol{Y}_{Rp} \end{bmatrix} \tag{A5}$$

$$\boldsymbol{B}_2 = \begin{bmatrix} -\boldsymbol{Y}_{\mathrm{Rn}} - \boldsymbol{Y}_{\mathrm{ps}}\boldsymbol{K}_{\mathrm{pb}}\boldsymbol{Y}_{\mathrm{Rn}} \\ \boldsymbol{Y}_L + 2\boldsymbol{Y}_{\mathrm{Rn}} - \boldsymbol{Y}_{\mathrm{ns}}\boldsymbol{K}_{\mathrm{na}}\boldsymbol{Y}_{\mathrm{Rn}} - \boldsymbol{Y}_{\mathrm{ns}}\boldsymbol{K}_{\mathrm{nb}}\boldsymbol{Y}_{\mathrm{Rn}} \\ -\boldsymbol{Y}_{\mathrm{ps}}\boldsymbol{K}_{\mathrm{pb}}\boldsymbol{Y}_{\mathrm{Rn}} - \boldsymbol{Y}_{\mathrm{ns}}\boldsymbol{K}_{\mathrm{na}}\boldsymbol{Y}_{\mathrm{Rn}} - \boldsymbol{Y}_{\mathrm{ns}}\boldsymbol{K}_{\mathrm{nb}}\boldsymbol{Y}_{\mathrm{Rn}} + \boldsymbol{Y}_{\mathrm{Rn}} \end{bmatrix} \tag{A6}$$

$$\boldsymbol{B}_3 = \begin{bmatrix} \boldsymbol{Y}_{\mathrm{Rb}} - \boldsymbol{Y}_{\mathrm{ps}}\boldsymbol{K}_{\mathrm{pa}}\boldsymbol{Y}_{\mathrm{Rb}} \\ -\boldsymbol{Y}_{\mathrm{ns}}\boldsymbol{K}_{\mathrm{na}}\boldsymbol{Y}_{\mathrm{Rb}} + \boldsymbol{Y}_{\mathrm{Rb}} \\ \boldsymbol{Y}_L - \boldsymbol{Y}_{\mathrm{ps}}\boldsymbol{K}_{\mathrm{pa}}\boldsymbol{Y}_{\mathrm{Rb}} + 2\boldsymbol{Y}_{\mathrm{Rb}} - \boldsymbol{Y}_{\mathrm{ns}}\boldsymbol{K}_{\mathrm{na}}\boldsymbol{Y}_{\mathrm{Rb}} \end{bmatrix} \tag{A7}$$

$$\boldsymbol{C} = \begin{bmatrix} \boldsymbol{Y}_{\mathrm{ps}}\boldsymbol{K}_{\mathrm{pc}} \\ \boldsymbol{Y}_{\mathrm{ns}}\boldsymbol{K}_{\mathrm{nc}} \\ \boldsymbol{Y}_{\mathrm{ps}}\boldsymbol{K}_{\mathrm{pc}} + \boldsymbol{Y}_{\mathrm{ns}}\boldsymbol{K}_{\mathrm{nc}} \end{bmatrix} \tag{A8}$$

$$\boldsymbol{E} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{A9}$$

Data availability

Data will be made available on request.

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