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Wideband 3-W GaAs MMIC Doherty PA with Stacked Devices and Load Variation Tolerance under 2.5:1 VSWR

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***Abstract* — This paper presents a 3-W GaAs fully integrated multi-stage Doherty power amplifier designed for wideband 5G FR1 applications. The amplifier utilizes a balanced configuration of two Doherty cells, with stacked devices implemented in both the driver and final stages. Experimental results show a saturated output power exceeding 34.7 dBm across the 3.3–5.0 GHz frequency range, maintaining a gain of 20 dB. The amplifier achieves a power-added efficiency greater than 25% at 6 dB output back-off and over 30% at saturation across the entire band. The performance well compares with the state of the art, both in continuous wave and with wideband modulated signals. Tolerance to load variations is demonstrated under 2.5:1 VSWR.**

***Keywords* — Doherty, efficiency, gallium arsenide, power amplifiers, wideband, VSWR.**

I. Introduction

The Doherty power amplifier (DPA) [1] has emerged as a favored solution for enhancing efficiency in Output power Back Off (OBO) conditions due to its relative simplicity. However, the wide modulation bandwidths required by 5G systems, particularly those spanning multiple frequency bands, pose a significant challenge to PA design [2]. In the case of DPAs, ensuring consistent load modulation and phase alignment over such bandwidths is particularly demanding [3]. Ensuring power amplifier resilience to load mismatches is critical for phased array and MIMO systems, where dynamic beam steering and varying load conditions can lead to significant impedance variations that degrade overall system performance [4].

While Gallium Nitride (GaN) technology is often the preferred choice for medium-power-level PAs due to its high power density, systems operating with lower voltage supplies can benefit from Gallium Arsenide (GaAs) as a viable alternative. GaAs offers advantages such as reduced cost, enhanced reliability, and competitive performance, making it a practical solution for achieving high efficiency and functionality under such constraints. However, achieving several watts of output power requires with GaAs the use of devices with considerably larger periphery compared to GaN [5]. This constraint can be mitigated by employing advanced configurations, such as stacked architectures [6], [7] and balanced designs [8], which also improve the tolerance to load variations.

The aim of this work is to develop a fully integrated DPA with 3 W saturated output power adopting a GaAs technology. The target is to cover simultaneously the n77 (3.3–4.2 GHz) and n79 (4.4–5 GHz) bands of the 5G FR1 and to operate efficiently with 100-MHz bandwidth modulations and under significant load mismatch. The developed DPA achieves 34.7 dBm of saturated output power and more than 20 dB of linear gain while maintaining a power-added efficiency (PAE) exceeding 25% across a 6-dB OBO range, with excellent load insensitivity, proving that GaAs can be competitive to GaN for such power targets.

II. Design

A. Architecture definition

The choice of the architecture is a result of a delicate trade-off among the selected technology and the requirements in terms of saturated power, gain, resilience to load variations and wideband operation.

The 150-nm-gate-length high-power GaAs pHEMT process (PPH15X-20) by UMS is adopted, which features a power density around 0.8 W/mm at the nominal 6 V supply and is almost static at the target operating frequencies.

The target output power of 3 W cannot be achieved by a DPA featuring single devices in the Main and Auxiliary branches, as each of these devices should have a periphery around 2 mm: there is no foundry model available for such size, and the optimum load would be extremely low, hampering the design of the Doherty combiner. The combination of several transistors is called for; among the available ones, the combination of 8 transistors in the final stage is selected.

Furthermore, a standard DPA has a significant performance degradation under load mismatch [9]. Load variation tolerance without the insertion of circulators or statically tunable elements [10] has been demonstrated for limited instantaneous bandwidth (IBW) [11]. A balanced architecture is typically required to achieve this for wider IBW. Therefore, two individual DPAs are designed on 50 Ω load and then combined through quadrature couplers.

Achieving wideband operation requires minimizing the output impedance transformation. Therefore, in each DPA, the parallel combination of transistors is avoided as it lowers the optimum output impedance, which is detrimental for wideband operation especially for load modulated PAs. On the contrary, transistor stacking is employed to combine power while increasing the optimum load [6], thus reducing the step to the 50 Ω output. Stacking has the additional feature of increasing the gain as well as the power, which has a positive effect on the overall PAE. Stacking two transistors allows to employ the GaAs technology with a doubled drain supply voltage (12 V).

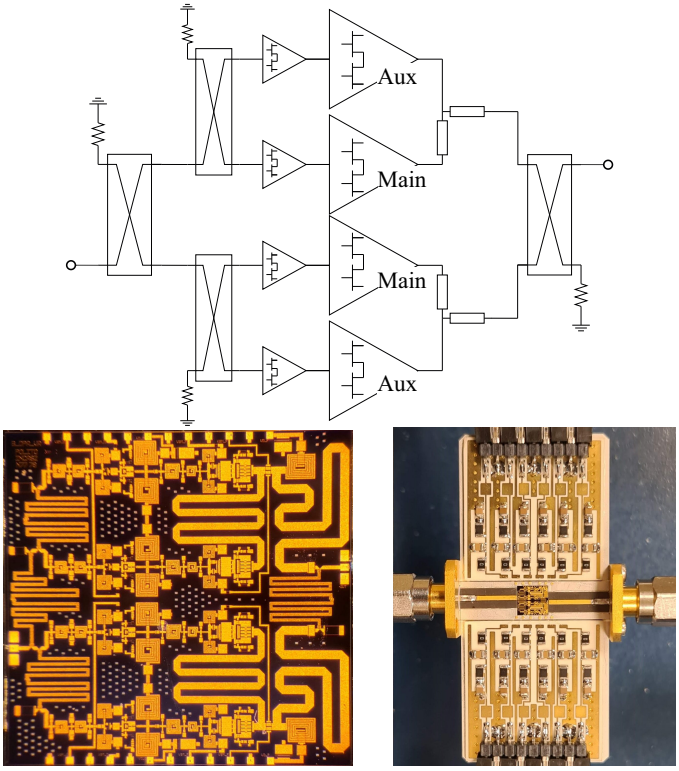


Fig. 1. Scheme of principle (top), and photographs of the MMIC ($5\times5\,\mathrm{mm}^2$) and its assembly in jig (bottom).

The scheme of the architecture and the photographs of the realized DPA are shown in Fig. 1.

B. Doherty combiner

Since the operating frequency is much lower than the cutoff frequency of the selected process, the transistors have very limited reactive parasitic effects. Therefore, the design of the combiner is performed directly at the current generator planes targeting real optimum loads, which for the $2\times(8\times150\,\mu\mathrm{m})$ stacked cell is of $33\,\Omega$.

Despite the quarter-wavelength is roughly 6 mm at these frequencies, a distributed combiner is preferred due to its wideband behaviour. A lumped implementation of the impedance inverter would be more compact but also more narrowband and lossy. The selected topology, shown in Fig. 2 together with the simulated load modulation, consists of a 33-Ω impedance inverter on the Main branch, a DC feed inductor at the common node, a 29-Ω impedance inverter as post-matching element and a DC blocking capacitor at the output. It aims at minimizing the element count and the losses, which are maintained within 0.3 dB in back-off and 0.2 dB at saturation. This type of combiner provides a wideband matching for the Auxiliary, but it does not allow to simultaneously achieve a wideband matching of the Main stage both in back-off and at saturation. Therefore, the load modulation trajectories are such as to achieve a reasonable trade-off between a uniform saturated output power and a good back-off efficiency.

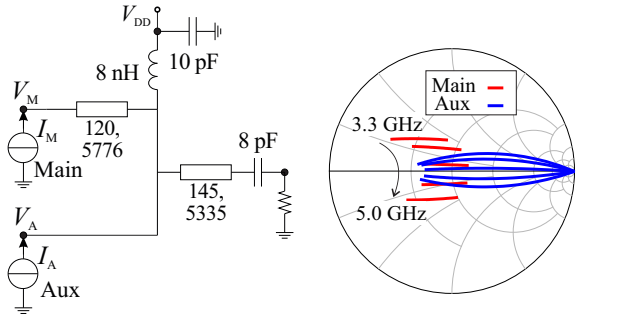


Fig. 2. Schematic of the Doherty combiner (left) and synthesized loads (right). Microstrip dimensions are reported as W (μm), L (μm).

C. Drivers

To achieve a gain compatible with real applications while preserving PAE, drivers should be inserted in the Doherty architecture. To reduce the complexity and avoid different drain supply voltages in the MMIC, the drivers are also stacked cells, of periphery $2\times(2\times100\,\mu\mathrm{m})$.

Since the selected process can provide gain up to around 40 GHz and there are no low-pass elements in the Doherty combiner, the inter-stage (ISMN) and input (IMN) matching networks are designed as high-order band-pass filters, aiming at maintaining good matching over the operating band and cutting off sharply the out-of-band signal. Due to area constraints, these are entirely made of lumped components (MIM capacitors and spiral inductors).

D. Couplers

Quadrature couplers are used both to implement the balanced architecture and as even power splitters for the individual DPAs, to also embed the required phase delay on the Auxiliary path. The design of integrated 90° couplers able to cover the target bandwidth is challenging both in terms of size and losses, due to the relatively low frequency. Considering that the distributed implementations are very area consuming but the lumped ones are typically narrowband, the choice falls on interdigitated Lange couplers, which can be bent to fit in the available space. As shown in Fig. 1, they have to be tightly folded, which is not optimal in terms of coupling among folds and consequent performance. They feature an insertion loss of about 1 dB, which corresponds to a drop in the passive efficiency of the output section of 20%. While this limits the maximum achievable efficiency, it allows to provide the DPA with a good tolerance to load mismatch.

III. Characterization

The MMIC DPA has been fully characterized on-wafer, in small and large signal conditions, before being assembled in a test jig for system level characterization.

The simulated and measured scattering parameters are shown in Fig. 3. The agreement is quite good, apart from a shift of the measured data towards higher frequencies of about 100 MHz. This has been ascribed to the effect of a passivization layer that was not accounted for during the

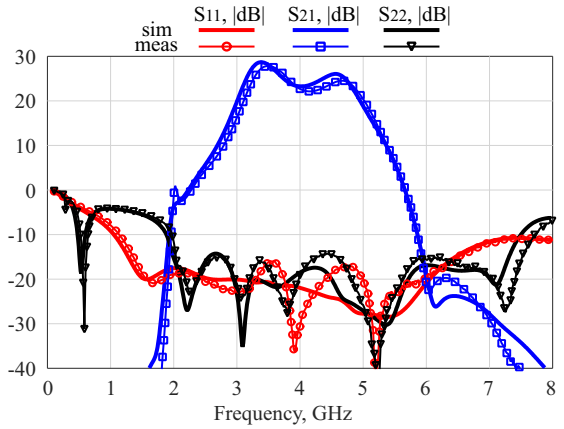


Fig. 3. Simulated (solid) and measured (symbols) scattering parameters.

design. The small-signal gain ($|S_{21}|$) is higher than 20 dB over the whole 3.3-5 GHz range, where the input and output return losses are below -15 dB.

The large signal performance is tested in continuous wave (CW) conditions. Fig. 4 reports the comparison of simulated and measured performance versus frequency, at saturation and at 6 dB OBO. The measured saturated power and PAE are higher than 34.7 dBm and 27% over the whole 3.3–5 GHz range, with the lower (n77) band featuring slightly higher PAE at the expense of lower output power compared to the higher (n79) band. At 6 dB OBO, the PAE is higher than 25%. The measured gain ranges from 15–20 dB at saturation to 20–25 dB in back-off. The simulations predict the output power and gain quite accurately, apart from the slight gain shift that was already observed in the scattering characterization. The PAE is also very well predicted by simulations until the 6 dB OBO point, whereas at saturation the measured one is higher. This is not uncommon in DPAs, due to the difficulty of developing a nonlinear model able to accurately predict the behaviour of the Auxiliary when it dynamically moves from class C to class A. In this case, an additional factor may be the difficulty of correctly modelling the stacked structure, which requires an *ad hoc* three-terminal transistor model and often must rely on the use of non-calibrated ports for the EM simulations of the passive elements connecting the transistors in the stack [12].

The load variation tolerance is then estimated by testing the amplifier under terminations corresponding to a VSWR of 2.5. An example of the resulting performance compared to the one under nominal loading conditions is shown in Fig. 5 at 4.7 GHz, which is the centre of the high band. The saturated output power drops by 2 dB in the worst case, and the PAE at 6 dB OBO reduces by 5 points, from 28% to 23%.

The system level characterization has been performed on the in-jig DPA with a Keysight N5242B PNA-X. The adopted signal has a 4.15 GHz carrier and a 64-Quadrature Amplitude Modulation (QAM) with 100 MHz instantaneous bandwidth and 6.1 dB PAPR. Without digital predistortion (DPD), the DPA achieves Adjacent Channel Power Ratio (ACPR) of -26 dBc and Error Vector Magnitude (EVM) of 8.7% at

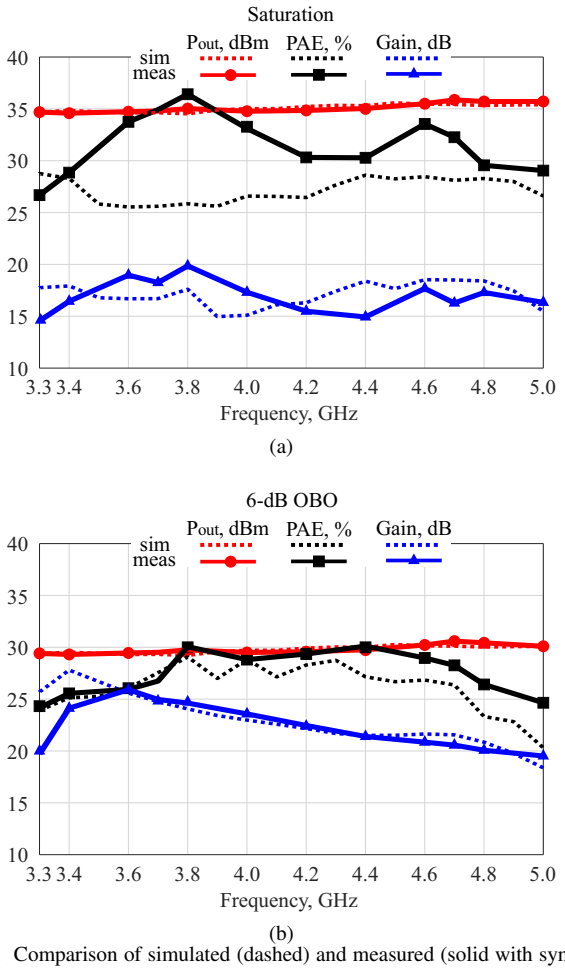


Fig. 4. Comparison of simulated (dashed) and measured (solid with symbols) CW performance: at (a) saturation and (b) 6-dB OBO.

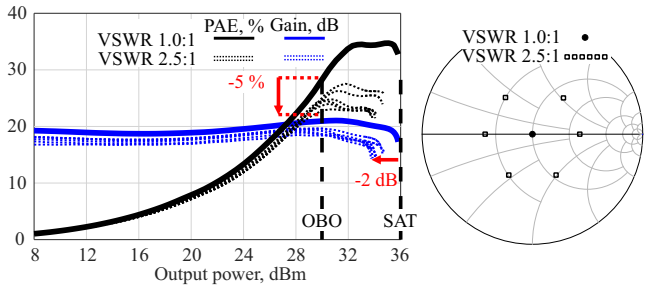


Fig. 5. Measured power sweeps at 4.7 GHz, under no load mismatch and with VSWR=2.5, and corresponding synthesized loads.

an average output power of 30 dBm, with a corresponding efficiency of 26%. After DPD, the ACPR and EVM are reduced to -43 dBc and 1.4%, respectively, with a negligible impact on output power and efficiency. The measured output constellation after DPD is shown in Fig. 6.

The performance of the DPA is compared to the state of the art at similar frequencies in Table 1. Most of the watt-level DPAs are developed in GaN technologies, and despite this the proposed GaAs DPA can achieve competitive power and PAE performance, especially considering the presence of drivers on chip and the wide operating band. In fact,

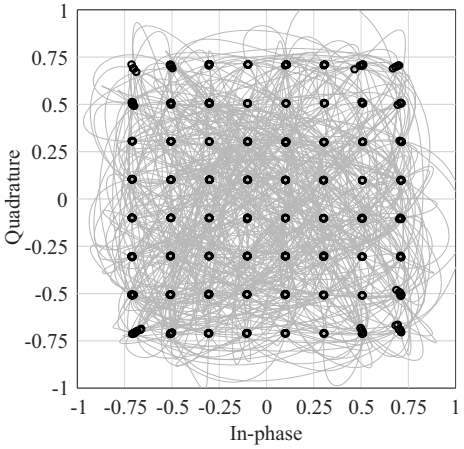


Fig. 6. Measured output constellation at 4.15 GHz: 64-QAM modulation with 100-MHz bandwidth after DPD.

very few examples can cover both the n77 and n79 bands simultaneously. The performance is also very competitive under wideband modulated signals excitation, both without and with DPD.

Table 1. State-of-the-art DPAs for sub-6 GHz communications.

	T.W.	[13]	[14]	[15]	[16]
Technology	**GaAs**	GaAs	GaN	GaN	GaN
Freq.(GHz)	**3.3-5.0**	3.3-3.5	4.5-6.0	3.2-4.7	3.3-5.0
BW(%)	**41**	6	29	31	41
V_{DD}(V)	**12**	5	28	9, 18	28
P_{sat}(dBm)	**34.7**	38	35	29	37
$\mathrm{PAE}_{\mathrm{sat}}$(%)	**30**	47	32	37	25
$\mathrm{PAE}_{\mathrm{6dB}}$(%)	**25**	30	23	30	20
G_{ss}(dB)	**20**	34	8	11	19
Degradation VSWR=2.5	**2dB P_{sat} 5% PAE**	-	-	-	-
Modulation	**64-QAM**	LTE	64-QAM	64-QAM	256-QAM
BW(MHz)	**100**	20	100	100	50
PAPR(dB)	**6.1**	8	8	7.5	7.2
Carrier(GHz)	**4.15**	3.5	5.0	4.3	4.15
$\mathrm{P}_{\mathrm{ave}}$(dBm)	**30**	30	29	22	33
$\mathrm{PAE}_{\mathrm{ave}}$(%)	**26**	30	25.7	-	23
EVM(%)	**8/1.4***	-	3	9.6/3.4*	4.5/1.2*
ACLR(dBc)	**-26/-43***	-30/-50*	-35	-23/-36*	-32/-46*

* After DPD

IV. Conclusion

This work has presented the design and experimental characterization of a fully integrated balanced DPA developed on a commercial GaAs power pHEMT technology. Thanks to the transistor stacking, the MMIC DPA can achieve an output power comparable to that of GaN with a very dense on-chip transistor combination, while also achieving a high gain and a PAE always higher than 25% over a 6-dB back-off range, from 3.3 GHz to 5 GHz. Furthermore, the balanced DPA features excellent load variation tolerance under 2.5:1 VSWR.

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