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Original
High-Frequency Doherty Versus Class-AB Power Amplifiers: What Is the Gain? / Piacibello, A., Camarchia, V.. - In: IEEE MICROWAVE MAGAZINE. - ISSN 1527-3342. - 27:3(2026), pp. 69-80. [10.1109/MMM.2025.3617917]

Availability:
This version is available at: 11583/3017507 since: 2026-11-04T08:30:15Z

Publisher:
IEEE

Published
DOI:10.1109/MMM.2025.3617917

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19 November 2026

High-frequency Doherty vs. Class-AB Power Amplifiers: what is the gain?

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October 1, 2025

Introduction

The Doherty power amplifier (Doherty PA) is a popular back-off efficiency enhancement architecture proposed by W.H. Doherty in 1936 [1, 2] for vacuum tubes and later adapted to solid-state transistor technology. Across the years the Doherty PA has evolved into various configurations which include asymmetric and multi-way topologies to meet the stringent linearity and efficiency requirements of high Peak-to-Average Power Ratio (PAPR) communication standards. Recent research efforts are focused on extending the Doherty concept toward millimeter-wave frequencies and monolithic integration. In this framework critical design trade-offs emerge: at frequencies where transistor gain is limited, the gain penalty intrinsic to the Doherty architecture, often overlooked in favor of efficiency metrics, becomes particularly severe and also impacts the overall achievable efficiency, especially if multi-stage architectures are mandatory. Bandwidth further constrains design choices, often forcing trade-offs between peak performance and wideband behavior. This also reduces the available design space to optimize linearity together with efficiency, which ultimately determines whether Doherty PAs provide sufficient advantages to justify deployment in place of non load-modulated class-AB PAs, generally more wideband, robust to process variations and simpler in terms of bias and architecture design.

The Doherty principle

The Doherty PA basic form, shown in Fig. 1, includes a Main and an Auxiliary amplifier connected to a common load. Its operation is based on the load modulation principle: the Main amplifier al-

ways contributes to the output power, while the Auxiliary amplifier is only active at high input power, where it modulates the load impedance presented to the Main through an impedance inverter in such a way to keep it maximally efficient [3].

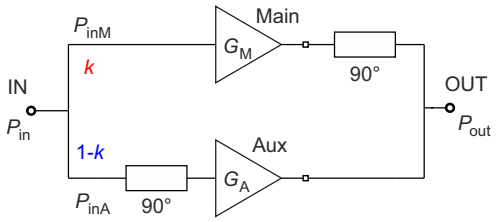
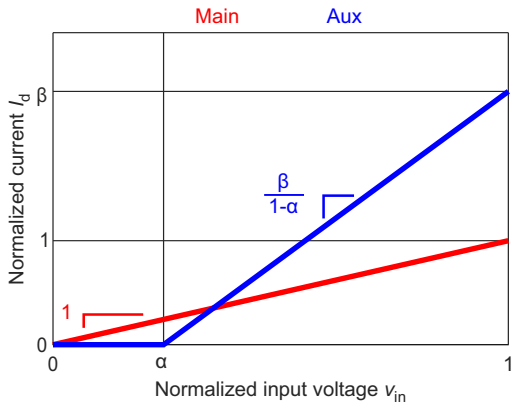


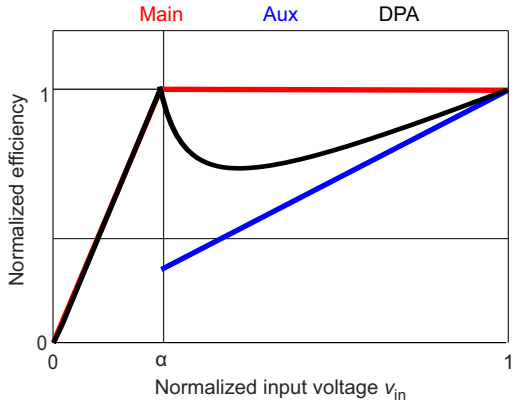
Fig. 1: Scheme of principle of the basic Doherty PA architecture.

For historical reasons as well as for ease of analytical formulation, the Doherty PA is often studied considering both Main and Auxiliary as tuned-load class-B amplifiers, driven in such a way to produce the fundamental drain current profiles shown in Fig. 2(a), leading to the efficiency profiles of Fig. 2(b), where $\alpha = 10^{(-N/20)}$ is the position of the desired back-off efficiency peak in linear voltage units. In the following, the analysis is carried out at the center frequency, where the analytical formulation is exact. When extended to a finite bandwidth, deviations from the ideal case arise, reducing the theoretical advantages of the technique and requiring appropriate corrective measures and design trade-offs. A comprehensive discussion on bandwidth limitations and compensation strategies can be found in [4].

In the conventional implementation, the Main



(a)



(b)

Fig. 2: Profiles versus normalized input voltage of (a) fundamental drain current and (b) efficiency.

and Auxiliary deliver the same maximum power ($\beta = 1$) and the Auxiliary turns on when the Main reaches half of its dynamics ($\alpha = 1/2$), thus leading to a highly efficient Doherty PA over a 6-dB Output Back-Off (OBO) range. With the advent of modern wireless communication standards that adopt high-PAPR signals, the Doherty PA has been extended to provide highly efficient signal amplification over wider N-dB OBO. There are essentially two ways of achieving this: asymmetric Doherty PAs with

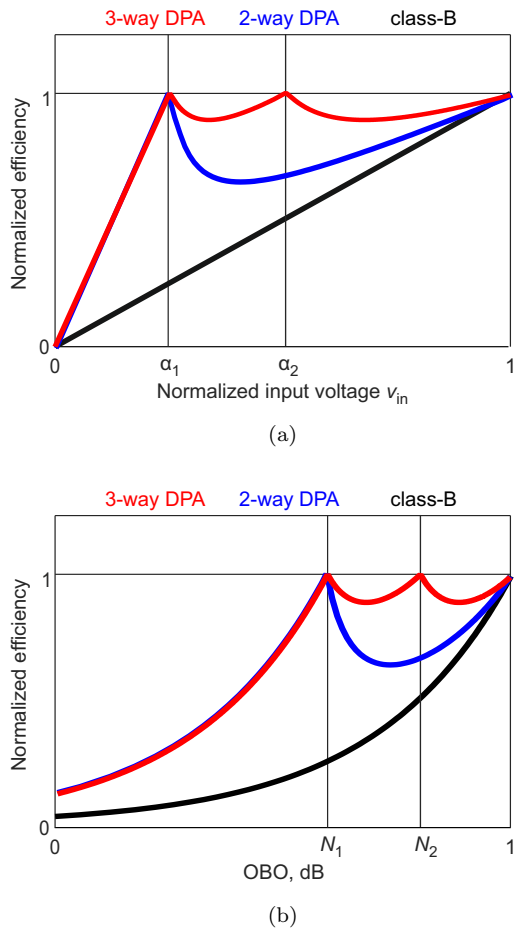


Fig. 3: Normalized efficiency profiles of class-B, 2-way and 3-way Doherty PAs versus (a) normalized input voltage and (b) OBO.

a smaller Main and a larger Auxiliary that delivers higher maximum power ($\beta > 1$) and turns on earlier ($\alpha < 1/2$)[5], and multi-way Doherty PAs where there are several Auxiliary PAs that turn on at different points of the dynamics and contribute to different amounts of the output power, creating multiple back-off efficiency peaks [6, 7]. The ideal efficiency curves of the various Doherty PA types are summarized in Fig. 3, where they are compared to the efficiency of a class-B PA.

The gain penalty issue

Reaching several watts of output power requires the adoption of monolithic microwave integrated circuit (MMIC) based on compound semiconductors such as GaAs and GaN. However, in processes featuring gate lengths smaller than 150 nm that are suitable for applications above 6 GHz, the gain of individual devices alone cannot ensure the amplification required to the entire amplifier, thus making multi-stage architectures imperative. This challenge particularly impacts on the Doherty architecture (and its derivatives) due to its inherent additional gain penalty compared to corporate amplifiers.

Despite extensive research on dual-input and digitally driven Doherty PAs, the architectures implemented in practice are very often single-input. In such cases, the Auxiliary stage typically operates in class C to turn on at the desired input power level and realize the efficiency enhancement at output back-off. Even in digital Doherty configurations, the Auxiliary is frequently biased in class C, although often with a less pronounced bias depth. This causes a gain reduction in small signal due to the static input splitter delivering power to both branches while only the Main is contributing to the output power. This issue, already significant in symmetric 2-way Doherty configurations,

becomes even more critical in asymmetric or multi-way topologies, which have larger overall Auxiliary periphery.

While there are several ways to quantify this effect, with different trade-offs between analytical complexity and accuracy, it is often useful to adopt a simplified estimation method that assumes class-B operation for the devices, corresponding to the drain current profiles shown in Fig. 2(a), and extend its validity to the case where the Main stage is biased in class AB (thus having non-zero linear gain) and the Auxiliary is in class C. While this is strictly speaking inconsistent, it provides results that are comparable to more accurate formulations [8]. The small-signal gain penalty K of the Doherty PA depends on the back-off N as derived in [9] and shown in Fig. 4. It is interesting to note that K is almost equal to N, with the dependence becoming linear with increasing N. In particular, the gain penalty for a 6-dB Doherty PA is of 7 dB and it becomes 12 dB for a 12-dB Doherty PA.

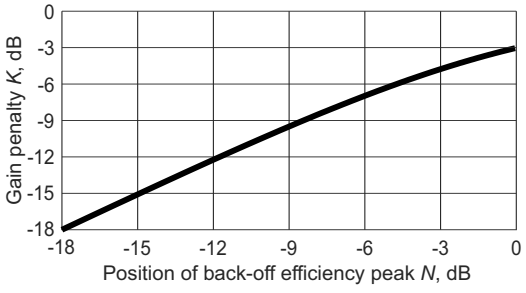
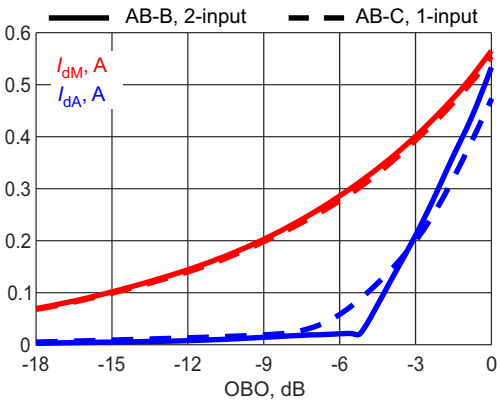


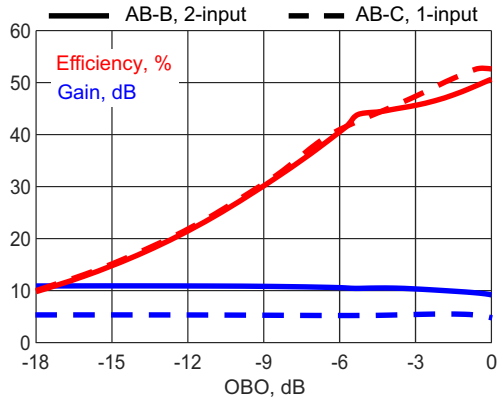
Fig. 4: Gain penalty K of an N-dB 2-way Doherty PA.

A practical example of this issue can be observed by implementing an ideal and lossless Doherty combiner and driving it with real nonlinear transistor models. Let us consider for instance a 6-dB Doherty PA designed according to the topology in Fig. 1 for operation at 18.8 GHz adopting two identical transistors in a 100-nm GaN-Si technology. Fig. 5 reports the profiles versus normalized input voltage of (a) fundamental drain current and (b) efficiency and gain, for class-AB-B 2-input (solid) and a class-AB-C 1-input (dashed) DPAs. The inclusion of the input splitter and the necessity to bias the auxiliary device in class C causes a gain penalty around 6 dB, very close to the theoretical prediction. While the efficiency remains similar in the 2- and 1-input cases, the back-off peak is less pronounced when a 1-input class-AB-C architecture is implemented, due to the smoother turn-on of the Auxiliary.

For the common case of a 6-dB 2-way Doherty PA, a different approach to synthesize the same response consists in adopting an even input splitter and doubling the Auxiliary active periphery. In this way, the Auxiliary presents an equivalent transconductance that is twice than the Main and can therefore achieve the same maximum current in half of the input voltage dynamics. The advantage of this approach is that the gain penalty reduces from 7 dB to 3 dB, at the price of under-utilizing the Auxiliary device, whose periphery is only half exploited. Conversely, in deep-OBO Doherty architectures, it



(a)



(b)

Fig. 5: Simulated profiles of (a) fundamental drain current and (b) efficiency and gain, for class-AB-B 2-input (solid) and class-AB-C 1-input (dashed) DPAs at 18.8 GHz.

is uncommon to under-utilize the Auxiliary stages to achieve the target current profile. This is because the periphery ratio between the Auxiliary and Main paths is typically chosen such to produce the desired load modulation when all Auxiliary stages are fully utilized. Reducing the utilization of the Auxiliary would generally compromise the achievable efficiency enhancement and is therefore rarely adopted in practice [10, 11].

There are other techniques to mitigate the gain penalty issue, such as the adoption of a higher supply voltage for the Auxiliary [12]. In the case drivers are embedded in the Doherty PA architecture, which is often the case especially for applications beyond 6 GHz [13], the desired load modulation can be achieved with a reduced asymmetry in the input power splitter, while also enhancing the Power-Added Efficiency (PAE).

Efficiency, gain and multi-stage architectures

Considering the small-signal gain penalty just described and the limited gain that most of the solid-state transistor technologies offer at high frequency, Doherty PAs often need embedded drivers for their efficiency enhancement to be effective. A simplified estimation of the Doherty PA efficiency in a two-stage architecture like the one of Fig. 6 is instructive to understand the trade-offs. The scheme describes an N-dB OBO Doherty PA with drivers embedded in its branches, designed to fully saturate the respective final stage while operating well within its linear region across the entire power swing, thus ensuring negligible contribution to the overall distortion and preserving the intended Doherty load modulation.

It is assumed that the whole Auxiliary branch

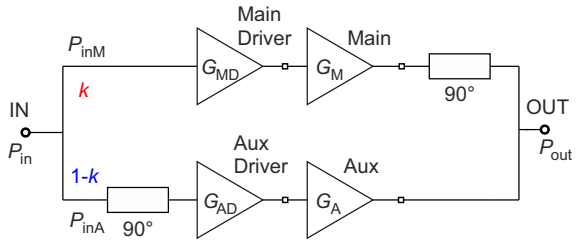


Fig. 6: Scheme of principle of a 2-stage Doherty PA with embedded drivers.

does not consume any dc power in OBO, which amounts to either class-B operation (if separate control of the inputs is available) or class-C operation of Auxiliary Driver (AD) and Auxiliary (A) in a conventional single-input Doherty PA. Despite the potential difference in operating class, for a first approximate estimation it is acceptable to assume that the efficiency at saturation of the driver and final stages of both Main and Auxiliary are the same $\eta_{\mathrm{MD,sat}} = \eta_{\mathrm{AD,sat}}$ and $\eta_{\mathrm{M,sat}} = \eta_{\mathrm{A,sat}}$, as well as the saturation gain of the final stages $G_{\mathrm{M,sat}} = G_{\mathrm{A,sat}}$. The output combiner has a passive efficiency η_{c} accounting for the losses due dissipation and mismatch. Under such assumptions, one can derive simple analytical expressions for the Doherty PA efficiency in the OBO and saturation conditions (1),(2).

The assumptions that are made allow obtaining analogous expressions for $\eta_{\mathrm{DPA,obo}}$ and $\eta_{\mathrm{DPA,sat}}$, which enables a unified discussion of the main impacting quantities. While their absolute value will differ, the trend is analogous and is shown for the normalized $\eta_{\mathrm{DPA,obo}}$ in Fig. 7. The values considered for the independent variables are based on realistic cases: the Main stage gain $G_{\mathrm{M,obo}}$ ranges from 5 dB to 20 dB, which in linear units corresponds to roughly 3 to 100, the driver efficiency $\eta_{\mathrm{MD,obo}}$ is derived assuming the dependence of efficiency on OBO for a class-B amplifier ($\eta_{\mathrm{MD,obo}} = \eta_{\mathrm{MD,sat}} \cdot \sqrt{10^{(-\mathrm{OBO}/10)}}$), where the efficiency at saturation ranges from 20% to 50%.

It is evident from the 3D plot of Fig. 7 that the gain of the final stage has a much greater impact than the efficiency of the driver for most of the considered ranges. If the gain is lower than 10 (10 dB), the Doherty PA efficiency is strongly reduced even if the driver has a fairly good efficiency. On the other side, if the gain is sufficiently high (>50, i.e., 17 dB), the impact of the drivers efficiency is neg-

$$\eta_{\mathrm{DPA,obo}} = \frac{P_{\mathrm{out,obo}}}{P_{\mathrm{DC,M}} + P_{\mathrm{DC,A}}} = \frac{P_{\mathrm{out,obo}}}{\frac{P_{\mathrm{out,M,obo}}}{\eta_{\mathrm{M,obo}}} + \frac{P_{\mathrm{out,M,obo}}}{G_{\mathrm{M,obo}}\eta_{\mathrm{MD,obo}}}} = \frac{\eta_{\mathrm{c}}}{\frac{1}{\eta_{\mathrm{M,obo}}} + \frac{1}{G_{\mathrm{M,obo}}\eta_{\mathrm{MD,obo}}}} \tag{1}$$

$$\eta_{\mathrm{DPA,sat}} = \frac{P_{\mathrm{out,sat}}}{P_{\mathrm{DC,M}} + P_{\mathrm{DC,A}} + P_{\mathrm{DC,MD}} + P_{\mathrm{DC,AD}}} = \\ = \frac{P_{\mathrm{out,sat}}}{\frac{P_{\mathrm{out,M,sat}}}{\eta_{\mathrm{M,sat}}} + \frac{P_{\mathrm{out,A,sat}}}{\eta_{\mathrm{A,sat}}} + \frac{P_{\mathrm{out,M,sat}}}{G_{\mathrm{M,sat}}\eta_{\mathrm{MD,sat}}} + \frac{P_{\mathrm{out,A,sat}}}{G_{\mathrm{A,sat}}\eta_{\mathrm{AD,sat}}}} = \frac{\eta_{\mathrm{c}}}{\frac{1}{\eta_{\mathrm{M,sat}}} + \frac{1}{G_{\mathrm{M,sat}}\eta_{\mathrm{MD,sat}}}} \tag{2}$$

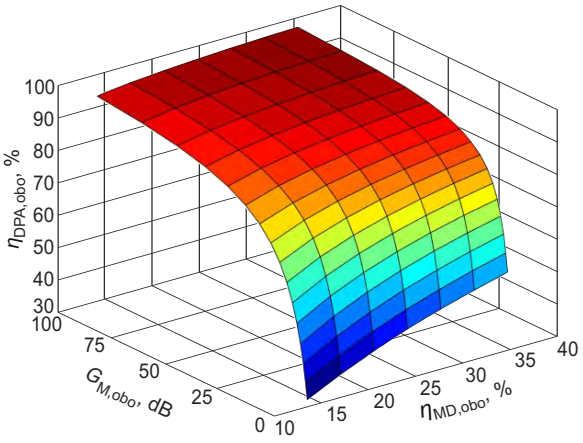


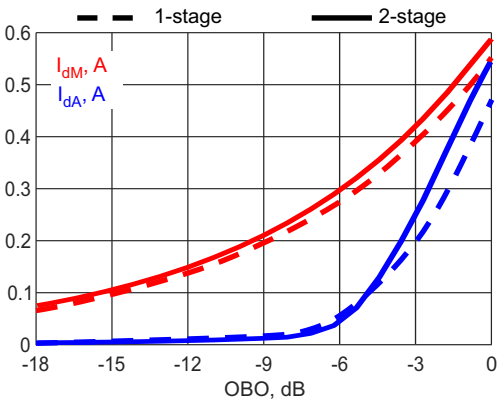
Fig. 7: 3D plot of the efficiency of a Doherty PA in OBO as a function of the final stages' gain and of the drivers' efficiency.

ligible. However, for most solid state implementations, the power gain of the individual transistor (after stabilization) is seldom higher than 10–12 dB, which makes the design of efficient drivers essential and calls for trade-offs with the linearity. Another aspect that strongly affects the achievable gain is targeting broadband operation, which typically implies higher mismatch and thus lower effective gain.

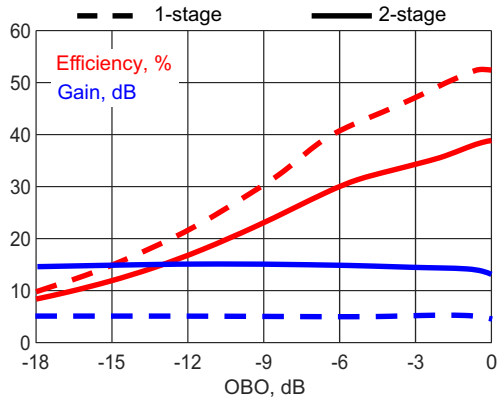
The effect of embedding drivers in the Doherty PA architecture is shown on the realistic example of Fig. 5, focusing on the 1-input architecture. Two identical drivers are inserted in front of the Main and Aux power devices, designing suitable input Matching Networks (IMNs) and Inter Stage Matching Networks (ISMNs), which are lossless and achieve optimal matching at single frequency. Thanks to symmetry, the input splitter parameters are unchanged. Fig. 8 compares the performance of the 1- and 2-stage architectures. While the shapes of the profiles are very similar, the 2-stage architecture shows an increase in gain of around 10 dB, at the expense of 10–15 efficiency percentage points reduction. In fact, the gain of the final stage is not high enough to minimize the sensitivity to the drivers' performance. The absolute value of the simulated efficiency is in line with the prediction of (1), (2) when the following set of parameters is used: $N = 6$, $\eta_{\mathrm{M,sat}} = \eta_{\mathrm{M,obo}} = 0.55$, $\eta_{\mathrm{c,obo}} = 0.79$, $\eta_{\mathrm{c,sat}} = 0.93$, $\eta_{\mathrm{MD,sat}} = 0.31$, $G_{\mathrm{M,obo}} = 11$. Note that the values of η_{c} are different at saturation and OBO as they account for reflections due to mismatch, which are typically higher in back-off.

Despite the deviations from the ideal efficiency performance, the Doherty architecture shows potential at these frequencies. However, for a possible application at Ka band such as wireless communication in the satellite downlink, even higher gain as well as wideband operation is required. The works in [14] and [15, 16] implement state-of-the-art Doherty PAs based on this architecture, but with one extra driver stage and a wideband combiner topology.

Even more challenging from the gain perspective are the prototypes in [7] and [17], which are among the first GaN MMIC 3-way Doherty PAs for the Frequency Range 2 (FR2) bands of 5G and explore the capabilities of both the architecture and of the technology, still under pre-commercial development



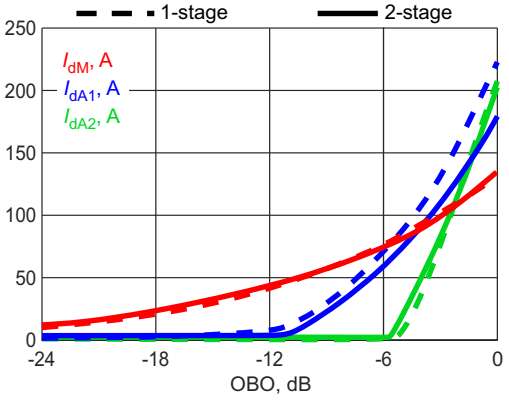
(a)



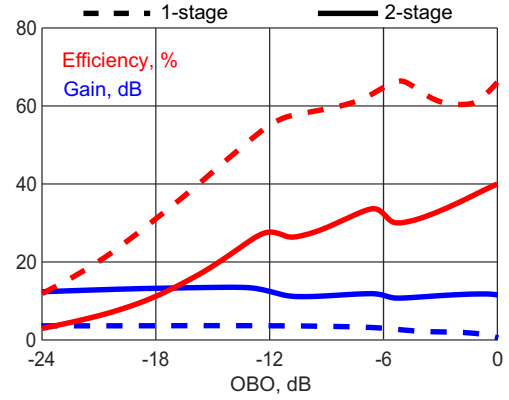
(b)

Fig. 8: Simulated profiles of (a) fundamental drain current and (b) efficiency and gain, for 1-stage (dashed) and 2-stage (solid) class-AB-C 2-way DPAs at 18.8 GHz.

at the time of the design. In [7] we propose an analytical formulation to assess the available design space for a 3-way Doherty PA combiner and then discuss the implementation challenges at FR2 frequencies. By extending the formulation that holds for two-way Doherty PAs, the required input power splitting results of $k = 1/14$, which corresponds to a small signal gain reduction of 11.5 dB for the overall Doherty PA. Indeed, with a 150-nm gate-length technology that provides a transistor power gain around 10 dB at 28 GHz, for a class-AB bias (100 mA/mm) on the optimum load, a single-stage Doherty PA architecture is unfeasible.



(a)



(b)

Fig. 9: Simulated profiles of (a) fundamental drain current and (b) efficiency and gain, for a 1-stage (dashed) and a 2-stage (solid) class-AB-C 2-input 3-way DPA at 28 GHz.

Fig. 9 shows the simulated performance of the 1- and 2-stage 3-way DPA architectures at 28 GHz, adopting the PDK nonlinear device models, loss-

less combiner and ideal input splitter. The transistors are biased in class AB-C-C to provide the desired turn on of the Auxiliaries. In the 1-stage case the efficiency profile clearly shows three peaks as predicted by theory, but the gain is indeed quite low. It is therefore necessary to embed drivers in each branch to achieve a final gain higher than 10 dB, as shown in Fig. 9(b). For the 2-stage architecture, all passive networks are lossless and the parameters of the ideal power splitting are unchanged. The gain and efficiency profiles are still in agreement with theory, although change shape slightly due to the effect of matching and phasing. The gain increase brings about a significant efficiency drop due to the power consumption of the drivers, and the impact of the drivers on the back-off efficiency peak is stronger than on the one at saturation. Also in this case, the simulations agree with the estimate provided by (1), (2) with the following set of parameters: $N = 12$, $\eta_{\mathrm{M,sat}} = \eta_{\mathrm{M,obo}} = 0.65$, $\eta_{\mathrm{c,obo}} = 0.78$, $\eta_{\mathrm{c,sat}} = 0.93$, $\eta_{\mathrm{MD,sat}} = 0.27$, $G_{\mathrm{M,obo}} = 10$. Note that the val-

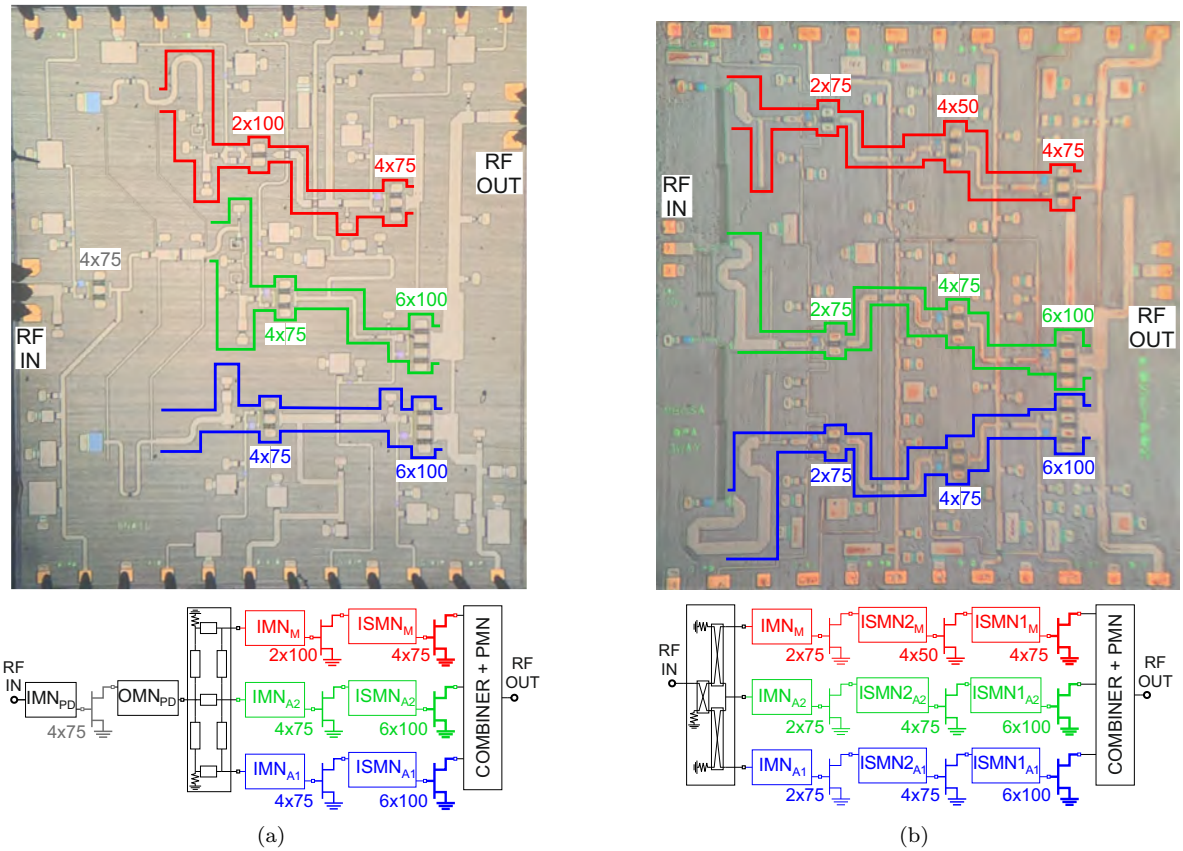


Fig. 10: Chip photographs and functional block diagrams of the 3-way Doherty PAs: (a) from [7], and (b) from [17].

ues of η_c are in line with those reported in Fig. 8 of [7], which are slightly lower as they also include ohmic losses. Another aspect worth noting is that the values of $\eta_{\mathrm{MD,sat}}$ and $G_{\mathrm{M,obo}}$ include the power loss due to mismatch, which is estimated around 1.5-2 dB due to the MNs being optimized over a 1-GHz bandwidth and thus cannot be neglected.

Despite the strong impact of low gain and losses, the demonstrator presented in [7] shows performance competitive with the state of the art, with a 12-dB OBO PAE of 15% and consistent operation over 1 GHz. In [17] we then expand on the previous work and propose some design techniques to improve the performance (especially gain) and widen the bandwidth. These act on both the architecture (a second level of drivers is included in the Doherty PA branches, substituting the single pre-driver at the input) and the design of the functional blocks (the combiner is based on the same theory but optimized differently, and the input splitter adopts a different topology). Fig. 10 summarizes the two architectures, highlighting the different input splitter as well as the number and position of the drivers.

Power splitting

Several options are available to design a 2-way input splitter for a Doherty PA (Wilkinson, branchline, Lange, coupled lines), the selection among which is guided by desired phase relation, bandwidth, size and losses. On the other hand, the synthesis of a 3-way input splitter that simultaneously achieves the desired power division and frequency response is considerably more challenging. Often, two 2-way splitters are cascaded, but for integrated architectures this solution may not be compact enough.

In [7], a double branchline structure is adopted to implement a compact asymmetric 3-way splitter, whose schematic and performance are reported in Fig. 11. Although this structure does not provide an exact solution that ensures matching and isolation at all ports and the desired power splitting ratio, it can be optimized so as to provide the desired performance over the 27–29 GHz band. However, since the phase relationship between the output ports (0°, +90°, 0°) is not the one needed by a 3-way Doherty PA (0°, 0°, +90°), additional delay lines are needed on two ports, which have been implemented in lumped form due to area constraints.

In [17] we propose a different topology, consisting in a cascade of back-to-back Lange couplers centered at different frequencies. The latter is both more compact and uniform over a wider band, which makes the architecture more robust to frequency shifts. Additionally, it also provides better port matching and isolation, as shown in Fig. 12. The working principle exploits two level of Lange couplers, both providing an asymmetric signal splitting. The asymmetry of first level (L1)

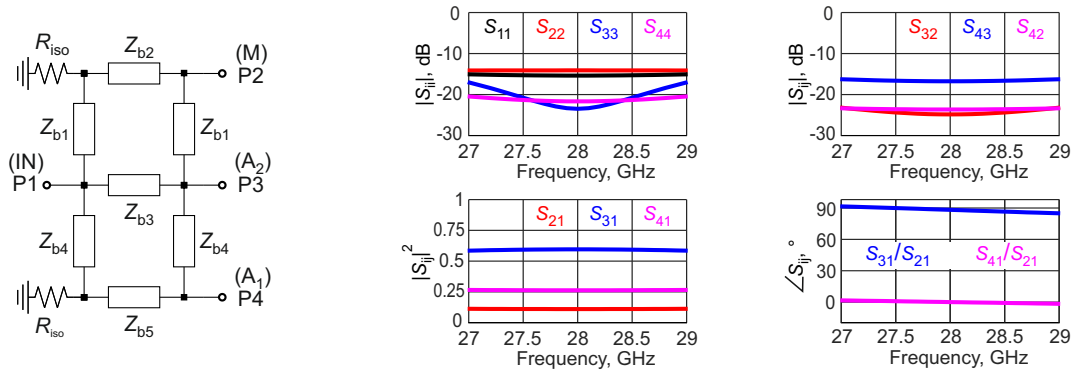


Fig. 11: Schematic and simulated scattering parameters of the input splitter of [7].

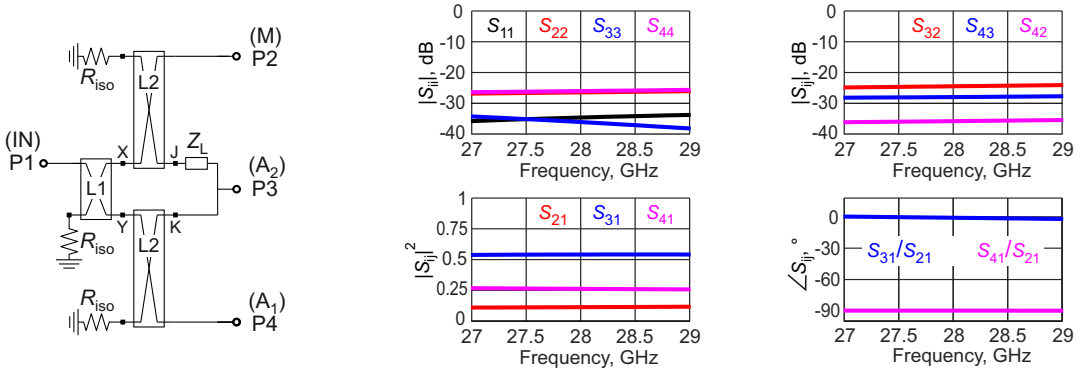


Fig. 12: Schematic and simulated scattering parameters of the input splitter of [17].

is more pronounced, for which reason its center frequency is $f_1 > f_0$, whereas the second level (L2) is composed by two identical Lange couplers that are only slightly asymmetric (over-coupled) and are centered at the design frequency f_0. The power of the internal ports of the second layer are then combined (after re-phasing), to provide the largest fraction of power to the Auxiliary A2. Also in this case the phase relationship between the output ports (0°, 0°, -90°) is not the optimal one, thus requiring a 180° phase delay on branch A1.

The work in [18] provides a comparison with a 2-way Doherty PA for the same bands and OBO level, in the same technology. Although both architectures present bandwidth limitations that are also partially due to the preliminary PDK available at the time of the design, the 2-way Doherty PA shows better peak performance, both in terms of gain (8 dB higher) and PAE (almost 10% higher). On the other side, the 3-way Doherty PA in [17] has better intrinsic linearity under modulated signal excitation (64-Quadrature Amplitude Modulation, 50-MHz Instantaneous Bandwidth, 10-dB PAPR), which can result in advantageous line-up

performance when the linearizer is also considered. In fact, it can maintain Adjacent Channel Power Ratio <-28 dBc and Error Vector Magnitude <8% over the whole dynamic range in the band 27–29 GHz, while operating at an average efficiency ranging from 15% to 21% at the maximum average output power of 28 dBm, which makes it compatible with the 3GPP standard without the need of additional linearization.

All in all, these first deep-OBO Doherty PAs *Ka*-band demonstrators evidenced a potential benefit in terms of efficiency enhancement for OBO levels higher than 9 dB, but also a strong sensitivity of the architectures to many parameters (technology and design related, such as the devices' threshold voltage, their intrinsic capacitive effects, etc.) which made a robust design hard to implement in MMIC form at that time. The evolution of the technology has surely an important role in advancing their performance. At the same time, the market has so far evolved in a direction that makes deep OBO especially attractive for FR1 -and possibly FR3- bands [19, 20], while deployment in FR2 is limited and does not heavily necessitate high-PAPR signals yet.

Linearity

Although originally conceived for efficiency enhancement, the Doherty PA has also been adopted as a linearity improvement technique in communication systems with wideband modulated signals and stringent in-band and adjacent-channel distortion requirements [21, 22]. The impact of nonlinear effects like AM/AM distortion and AM/PM conversion on the linearity or "linearizability" of PAs is a topic of great interest among the research community. While the AM/AM distortion can be managed in very effective ways by powerful linearizers, the AM/PM conversion is still more difficult to handle, especially over wide bandwidths [23].

Popular techniques to adopt the Doherty PA for linearity enhancement are to either use the driver stage as an integrated analogue phase predistorter for the final stage minimizing the total AM/PM [24] or exploit the class-C Auxiliary to compensate for the phase distortion introduced by the class-AB Main when undergoing load modulation [25]. Ideally, this should be achieved without compromising the achievable efficiency, which may or may not be possible depending on the degrees of freedom available for the design of the combiner and of the amplifying chain, including all its matching networks. In this complex scenario, an added complexity may be given by the necessity to combine several transistors on chip to achieve the desired output power level. While this is uncommon when using GaN-SiC, the adoption of GaN-Si or GaAs technologies may easily call for on-chip power combination to achieve multi-watt output power.

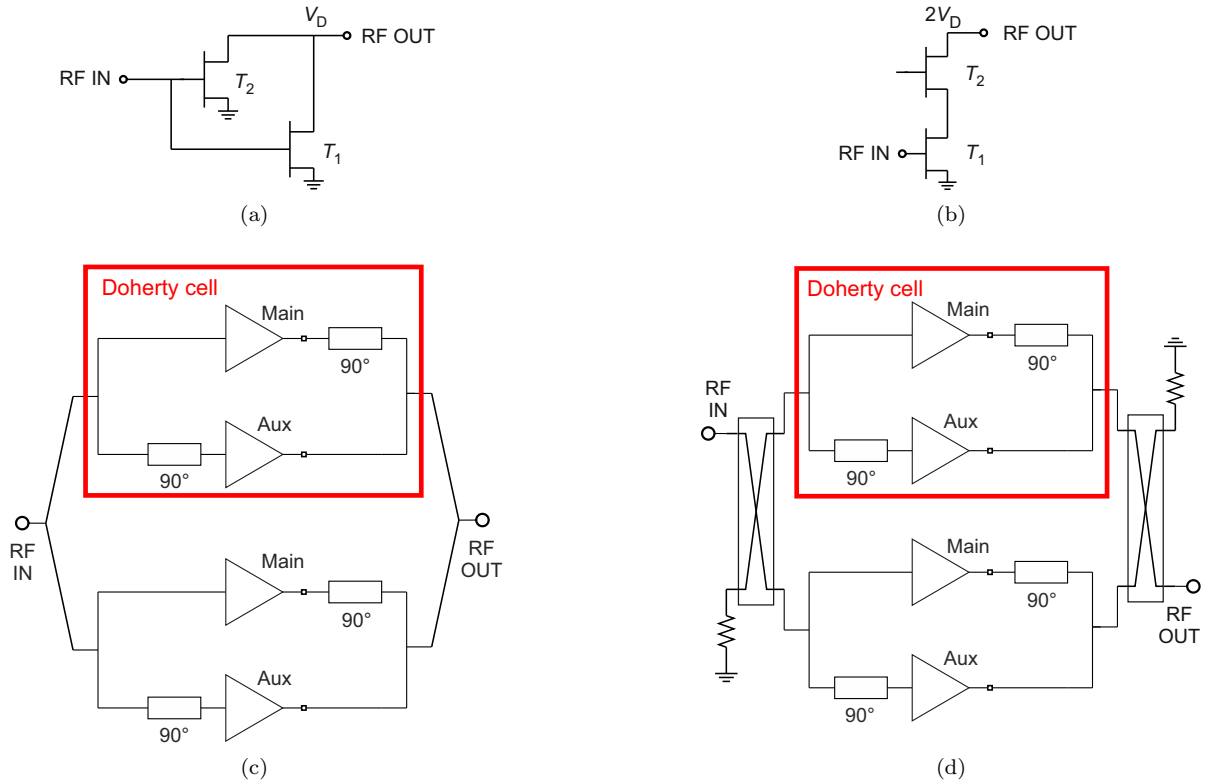
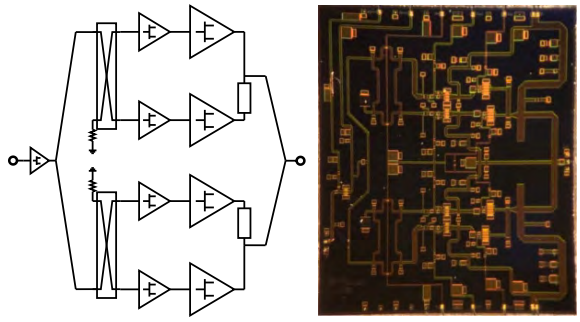


Fig. 13: Schemes of principle of power combination strategies: at device level (a) in parallel or (b) stacking, and at PA level with (c) parallel combination or (d) balanced combination.

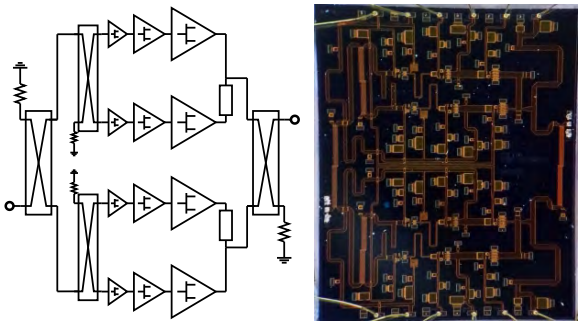
In [26], different on-chip power combination strategies are discussed, which are summarized in Fig. 13. They can be subdivided into two categories, namely at the transistor level, where two individual transistors can either be paralleled (a) or stacked (b), and at the PA level, where Doherty PA cells can be combined in parallel (c) or balanced (d). These cases imply different impedance scaling: in (a) the optimum load of the combined devices halves compared to the one of the individual transistor, whereas in (b) it doubles [27, 28]. In (c), similarly to (a) the load impedance of the Doherty PA cell halves, and finally in (d) there is no impedance scaling between the Doherty PA cell and the overall input/output, if the quadrature couplers are designed on the same reference impedance as the cell.

Concerning the latter case, impedance levels are not the only consideration that guides the choice: non-isolating power splitters and combiners may lead to higher efficiency, since they minimize losses, especially at the output, but they are less robust in terms of stability and input/output return loss.

The design of highly linear Doherty PAs adopt-



(a)



(b)

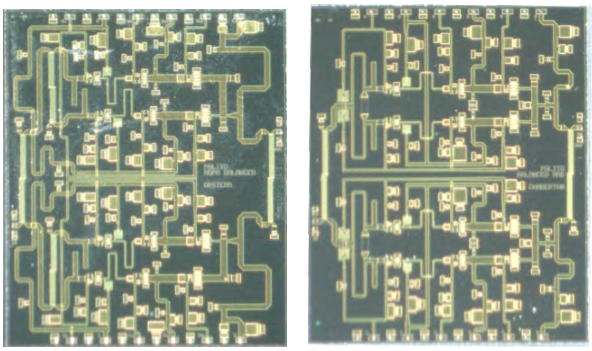
Fig. 14: Functional block diagrams and chip photographs of the Doherty PAs: (a) combined, from [14] and (b) balanced, from [16].

ing on-chip power combination at Doherty PA-cell level is presented in [14] (combined Doherty PAs, Fig. 14(a)) and in [15, 16] (balanced Doherty PAs, Fig. 14(b)). These MMIC Doherty PAs are developed in the 100 nm GaN-Si technology of OMMIC (D01GH) and target 5-W output power and high intrinsic linearity to be used for Ka-band satellite downlinks. The linearity metric often used for such applications is the Noise-to-Power Ratio (NPR), which measures the amount of noise and distortion that fall into an unused channel of a (wideband) multi-channel system when there is a random signal on the others [29]. The minimum requirement set for these Doherty PAs is 15 dB. However, the NPR is strongly influenced by the test conditions, such as signal statistics, instantaneous bandwidth of the test signals, and the waveform characteristics of the baseband signal, which makes it hard to compare linearity performance among PAs designed for satellite applications and calls for a standardized NPR measurement methodology [30]. The Doherty PA of [14] was characterized with 100-MHz bandwidth uniformly distributed modulated signals and showed an sufficient linearity (NPR>17 dB) under these conditions. However, the main challenge in SatCom applications is to adopt modulations with higher PAPR and wider bandwidth than the current one, driving the PAs with full-band modulated signals. Therefore, a further linearity enhancement is needed, which is achieved in [15, 16] by exploiting the features of balanced amplifiers to minimize the odd intermodulation products, improving the gain flatness, and most importantly optimizing the transistors' terminations at baseband frequencies as well as synthesizing a linear amplifying chain and an output combiner that shapes the phase distortion of the Auxiliary to compensate that of the Main. This Doherty PA achieves state-of-the-art performance both in terms of efficiency and linearity, also under very wideband (2.9-GHz instantaneous bandwidth) modulated signal excitation. Thanks to a design strategy that relies on single- and two-tone metrics, we demonstrated a success-

ful Doherty PA which maintains a PAE of at least 25% at the target 15-dB NPR point under all excitation conditions and with no bias tuning after the CW characterization.

Class-AB vs. Doherty PA

Is the Doherty architecture truly competitive in real-world applications compared to conventional class-AB power amplifiers? This question is legit, given concerns around the Doherty PA's architectural complexity, the increased number of bias lines, potential reductions in robustness, and especially the risk that linearity degradation could reduce the expected efficiency benefits.

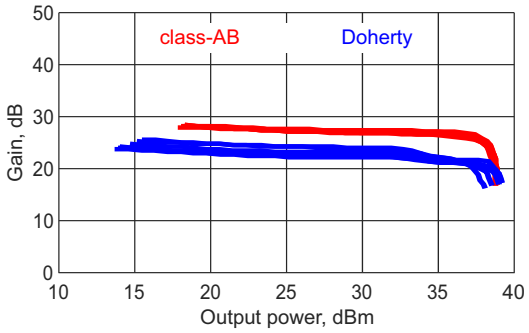


(a) (b)

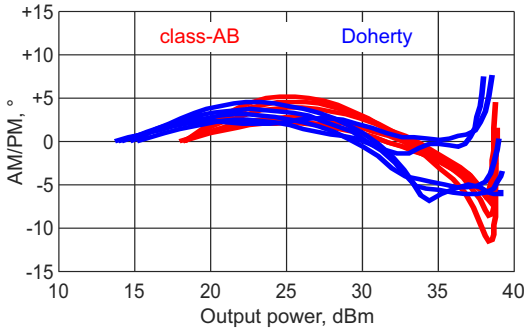
Fig. 15: Chip photographs of the balanced PAs: (a) Doherty and (b) class-AB.



(a)



(b)



(c)

Fig. 16: Comparison of large signal power sweeps of the balanced PAs, class-AB (red) and Doherty (blue), from 17.3 GHz to 20.3 GHz, with 0.5 GHz steps: (a) PAE, (b) gain, and (c) AM/PM.

To try and answer this question, it is interesting to compare the performance of two analogous PA architectures designed in the same technology. For instance, the balanced Doherty PA presented in [15, 16] can be compared to the corresponding balanced class-AB PA, designed adopting identical devices and replacing the Doherty combiner in each cell with an in-phase power combiner. The microscope

photographs of the two chips are shown in Fig. 15.

Fig. 16 compares their performance in terms of simulated CW power sweeps in their operating range, from 17.3 GHz to 20.3 GHz. While the class-AB offers slightly higher small-signal gain (by approximately 3 dB), both architectures achieve similar saturated output power and gain and peak efficiency. As expected, the Doherty PA demonstrates a clear advantage in back-off efficiency, exceeding the class-AB by over 10 percentage points at 6 dB output back-off.

Archit.	$\eta_{\mathbf{MAX}}$ (%)	$\eta_{\mathbf{6\,dB}}$ (%)	$\mathbf{G_{ss}}$ (dB)	**AM/PM** (°)
Class-AB	36	18	28	±10
Doherty	37	32	23	±7

Table 1: Class-AB vs. Doherty PA performance summary over the 17.3 GHz-20.3 GHz band.

Notably, this efficiency gain does not come at the expense of linearity. The Doherty PA maintains linearity performance comparable to, or even slightly better than, its class-AB counterpart, see Table 1. This supports the feasibility of the Doherty architecture for systems with moderate PAPR (≈ 6 dB), such as multi-carrier or variable-envelope applications. Additionally, the inclusion of isolated input and output splitters/combiners contributes to improved robustness under load variations.

That said, Doherty implementation does involve higher cost and design complexity compared to classical class-AB PAs. The use of asymmetric device chains, additional biasing requirements, and the need for accurate modeling, particularly for class-C operation, introduce challenges. These factors may limit its adoption in applications where cost or maximum robustness is critical, such as certain satellite communication systems.

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