Novel GaN-Based Digital Class-E Doherty PA with High 12dB OBO Efficiency

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***Abstract*— This paper presents a novel GaN-based 3-chip digital class-E Doherty power amplifier (PA) module designed to extend the back-off capabilities of the digital Doherty to deep back-off. Three identical class-E PA chips with digital input driving are combined off-chip in a two-way Doherty configuration for high efficiency in the 5G FR1 frequency band. For a single-tone input signal, the measured final-stage drain efficiency at 3.5 GHz peaks at 68% at 12 dB back-off, with a saturated output power of 33 dBm. Under a 20 MHz, 9 dB-PAPR digital OFDM input, the PA module delivers a drain efficiency of 55% at the same frequency.**

***Keywords*— amplifier, class-E, digital, digital driving, doherty, GaN, OBO, power back-off, PWM, 5G.**

I. Introduction

With the advancement of 5G and 6G wireless communication systems, increasingly complex modulation schemes with high peak-to-average power ratio (PAPR) have become common. This trend requires the design of energy-efficient power amplifiers (PAs) capable of maintaining high performance over a wide output power back-off (OBO) of 9 dB or more [1].

The class-E amplifier [2] is a widely used switching-mode PA due to its capability to achieve theoretically up to 100% efficiency, with practical implementations reaching values of 80% [3]. However, class-E PAs operate with an overdriven input and therefore cannot be effectively used to amplify amplitude-modulated signals.

In the analog domain, the Doherty technique [4] has been used for decades to enhance OBO efficiency, improving the performance of amplifiers when used with modern modulated signals. In recent years, increasing research efforts have focused on non-analog Doherty PA (DPA) implementations as a step toward fully digital transmitters [3].

This paper presents a digital class-E Doherty architecture that extends the high efficiency of class-E operation into power back-off and demonstrates its compatibility with modern modulation schemes that include amplitude modulation.

II. Design Process

Given the interest in enhancing efficiency at deep back-off levels in digital amplifiers operating with amplitude-modulated signals, an architecture analogous to an asymmetric DPA is implemented. Three identical chips, fabricated on a 250 nm GaN-HEMT process, are combined: while a single one constitutes the Main amplifier, two are combined to form an Auxiliary amplifier which double power capability. According to the conventional DPA theory, this configuration corresponds to a 9-dB OBO efficiency peak.

A. Class-E Chip

Fig. 1 presents a photograph of the digital PA chip used, along with the ideal class-E output network (L_1, C_1, L_2, C_2). The class-E shunt capacitance (C_2) is absorbed in the final-stage transistor drain-to-source capacitance (C_{ds}). A series capacitance of 1.25 pF (C_1) is integrated on-chip at the output of the transistor to be used as an element of the class-E output network. L_1 and L_2 inductances are partially implemented by the gold bond-wires necessary to connect the chip to the board; a value of about 1 nH / mm is estimated through previous measurements. Larger values are reached by using high-precision SMD inductors from Coilcraft.

The optimum loads for the class-E chip are determined through load-pull simulations at the intrinsic drain of the transistor ($Z_{d,int}$ in Fig. 1), using pulse-width modulated (PWM) signals at the input. For this purpose, the class-E output network components C_2 and L_2 are initially removed, and the class-E resonator tuned to the fundamental frequency, formed by C_1 and L_1, is replaced with an ideal network to ensure proper class-E operation during the load-pull process.

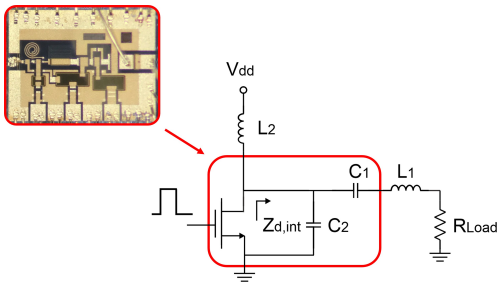


Fig. 1. Ideal class-E PA with GaN digital class-E chip highlighted. Chip area is 1.71 x 1.18 mm^2. Saturated output power (Psat) is 29 dBm.

The Microwave Monolithic Integrated Circuits (MMICs) include two on-chip driver stages intended solely to ensure proper excitation of the final-stage transistor. Accordingly, all

reported efficiency values refer only to the final-stage drain efficiency (η_{drain}).

B. Combiner Design

An analog Doherty strategy [5] is employed to implement a combiner with a 9 dB OBO. However, since the Doherty combiner must be driven by digitally operated class-E amplifiers, both the load conditions and the driving signals require redefinition. This section presents the selection of the required load impedances and driving currents, while the following section explains how these driving currents can be obtained from PWM input signals with varying duty cycles.

Although the switching operation of the class-E devices generates multiple harmonics at their drain, the class-E resonator (C_1, L_1 in Fig. 1), tuned to the fundamental frequency, filters these components so that only the fundamental reaches the load. Downstream of the resonator, the fundamental current is assumed to be proportional to that at the intrinsic drain. Accordingly, the analog combiner theory is applied by modeling each transistor and its output network as an ideal single-frequency current source.

Fig. 2 shows the implemented combiner. The Doherty topology employs one quarter-wavelength transformer in the Main branch (TL_M) and one quarter-wavelength transformer for post-matching (TL_{PMN}). The characteristic impedance of the lines is selected according to the desired OBO.

To achieve a 9 dB OBO , the Auxiliary device must deliver twice the fundamental current of the Main at saturation. This is realized by combining the outputs of two identical chips on-board, forming an effective Auxiliary device with double the size. Accordingly, the ideal topology is optimized to include short transmission lines on the Auxiliary branch (TL_{A1} and TL_{A2}) to combine the two Auxiliary chips and interface them with the Main line.

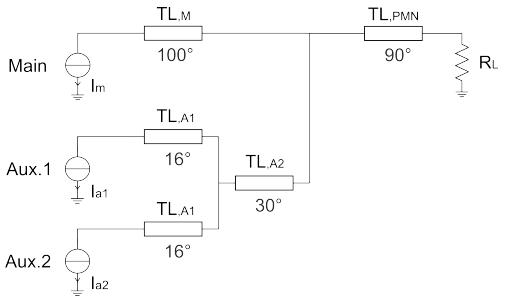


Fig. 2. . Implemented Doherty combiner topology.

The class-E chip optimum loads are evaluated at the fundamental frequency of 3.5 GHz at simulation level through load-pull at the transistor intrinsic drain ($Z_{d,int}$ in Fig. 1). For the saturation condition, at a final-stage drain supply voltage (V_{DD}) of 10 V, the chip presents a maximum efficiency of 70% with a P_{sat} of 29 dBm on a (77 + j25) Ω load, when a 60% input duty cycle is applied.

To target a 9 dB OBO, an optimum load corresponding to about 5 dB of power back-off must be selected for the Main. The single class-E MMIC PA is designed to maximize

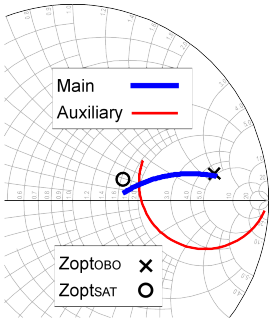


Fig. 3. Load modulation trajectories at 3.5 GHz, with optimum saturation ($Z_{opt,SAT}$) and back-off ($Z_{opt,OBO}$) loads highlighted.

efficiency performance for duty cycles lower than 50%. When a 30% input duty cycle is applied, it shows an efficiency of 75% and an output power of 24 dBm, i.e., at 5 dB back-off, on a (230 + j150) Ω load.

The class-E output network components (L_1, C_1, L_2, C_2 in Fig. 1) are initially selected in a single class-E PA simulation, following the class-E formulas in [6], so that the intrinsic drain of the transistor sees the optimum OBO load, (230 + j150) Ω. The components values are then refined through simulation optimization to ensure that the combination of the class-E output network and the Doherty combiner synthesize the correct loads at both OBO and saturation. Fig. 3 shows the simulated load modulation trajectories for the Main and Auxiliary amplifiers, for the implemented combiner at 3.5 GHz frequency, with the target loads highlighted.

C. Digital Driving

For digital class-E amplifiers, by varying the input duty cycle it is possible to vary the drain current and output power delivered by the device [2], [6]. For the implemented digital Doherty, the input duty cycles for the Main and Auxiliary are varied to obtain current profiles, analogous to the one of the analog examples, as shown in Fig. 4b.

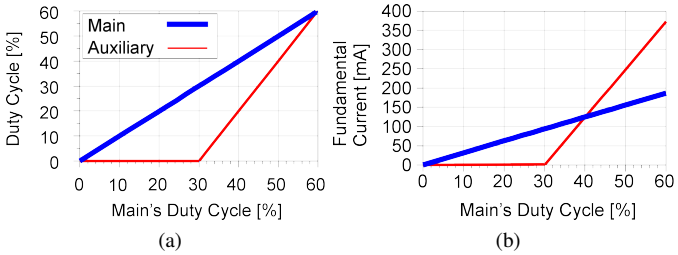


Fig. 4. Imposed duty cycle sweep for the Main (red) and Auxiliary (blue) devices (a); corresponding ideal fundamental current magnitude increase (b).

As shown in Fig. 4a, the Main's duty cycle is increased from 0 to 60%. For the Auxiliary device, implemented with two identical chips, the driving duty cycle is set for both to 0% up to the break point corresponding to 30% duty cycle, so that the chips will be turned ON just after this point. After that, the duty cycle is increased up to a value that makes the sum of the current of the Auxiliary chips reach about twice

the maximum Main current. Fig. 4a shows the imposed duty cycle for Main and Auxiliary chips and Fig. 4b shows the corresponding fundamental current magnitude increase.

D. Board Integration

The Doherty combiner, along with the input and biasing circuitry, was fabricated on a Rogers 4003C PCB laminate with a thickness of 0.305 mm. The board is mounted on a copper heatsink, and the complete demonstrator has an overall size of 49 × 38 mm^2. Fig. 5 shows the fabricated module. The three class-E MMICs are mounted in dedicated cut-outs on the board, soldered onto the copper carrier to ensure a common ground, and wire-bonded to the DC and RF lines on the PCB.

Three RF connectors provide the digital inputs (PWMin) to the MMICs: one for the Main chip and two for the Auxiliary chips, which are driven separately. Each connector is routed to its corresponding MMIC input through a 50 Ω transmission line. Fig. 5 also shows the topology of one of the MMIC bias lines. It includes four levels of decoupling capacitors, ranging from 43 pF to 10 μF, and a feed inductor. It is connected to the DC supply through a bias connector.

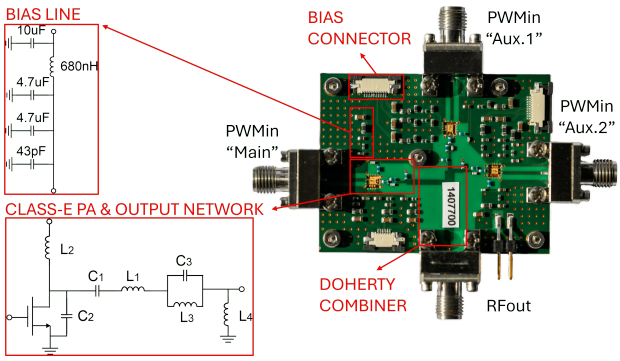


Fig. 5. Fabricated digital class-E Doherty module including three GaN PA MMICs, class-E output networks and Doherty combiner; size: 49 x 38 mm^2.

At the chip outputs, the class-E output network is implemented as described in Section II-A: components C_1 and C_2 are integrated on-chip, while inductors L_1 and L_2 are realized partly through chip-to-board bondwires and partly with on-board lumped elements. As shown in Fig. 5, additional high-precision SMD components (L_3, C_3, and L_4) are added to the class-E network on board, following Sokal's approach [2], providing additional flexibility to synthesize the required intrinsic loads. Downstream of the class-E network, the Doherty combiner is implemented using microstrip lines and connects to the RF output (RFout).

III. CHARACTERIZATION

The measurement setup employs a Keysight M8195A Arbitrary Waveform Generator (AWG) and three external broadband preamplifiers to ensure proper on/off switching of the final-stage GaN transistors in the digital class-E MMICs, driving them below and above threshold from –5 V to 1 V. The V_{DD} is set to 11 V, to match the load-pull simulation performance while slightly increasing the output power. At the output of the module, a 20 dB attenuator is connected to the Tektronix DPO70000SX real-time oscilloscope.

All the reported efficiency values correspond to the drain efficiency of the final-stage transistor only. In fact, this work aims to demonstrate the effectiveness of the combining strategy for achieving high efficiency over an extended output power back-off range, larger than 9 dB, rather than focusing on the maximum performance of the digital class-E amplifier as a stand-alone PA. All measured characteristics presented are extracted from the recorded real-time data.

A. 1-Tone Characterization

The digital class-E DPA has been initially characterized using single-tone PWM input signals, to prove the effectiveness of the digital Doherty combination strategy. The back-off behaviour is investigated by setting reduced duty cycles for the input signals of the Main and Auxiliary chips, as shown in Fig. 4a.

For the two chips implementing the Auxiliary branch, the PWM inputs ("PWMin Aux.") are phase-equalized. To ensure that the drive levels are also matched in magnitude, cables and preamplifiers from the same manufacturer and of the same type are used. Any residual mismatch is further mitigated by the overdrive characteristic of the class-E input.

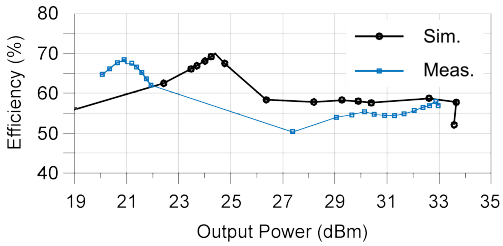


Fig. 6. η_{drain} vs. output power 1-tone performance @ 3.5 GHz, with V_{DD}=11 V: (black) simulated results; (blue) measured results.

Fig. 6 shows the simulated and measured 1-tone η_{drain} vs. output power at 3.5 GHz, with a V_{DD} of 11 V for all the chips. The measured saturated output power is 33 dBm, only 0.5 dB below the simulated value. The measured maximum efficiency is 68% at 12 dB OBO and 57% at saturation, within 2% of the simulated results. Across the OBO range, however, the measured efficiency decreases more than predicted, reaching a value of 50%.

The main discrepancy between simulations and measurements is in the OBO range, which is of 9 dB and 12 dB respectively. Because the OBO peak occurs where only the Main amplifier is active, as confirmed by drain current measurements, the discrepancy is attributed to differences between the simulated and implemented loads. Given the high simulated OBO load of (230 + j150) Ω and the low corresponding output power in the order of 20 dBm, even small variations in the implemented circuit can significantly affect the OBO power level.

Overall, the results show that efficiencies above 50% are maintained across the entire output power range, with a peak efficiency of 68% achieved at a remarkably high 12 dB OBO.

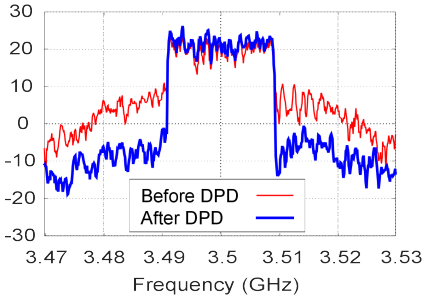


Fig. 7. System level characterization @ 3.5 GHz with 20 MHz 9 dB PAPR OFDM signal before (blue) and after (red) DPD. After DPD -28 dBc of ACPR and 6% EVM obtained, with 48% and 23 dBm of average efficiency and average power respectively.

B. System Level Characterization

The PA module has been tested at 3.5 GHz with OFDM input signals having 9 dB PAPR with 20 MHz bandwidth. All input signals are generated using a digital modulator that includes an inline linearization technique which does not require any additional power for the DPD.

During system-level characterization, an issue is observed in reproducing short pulses. Due to the limited time resolution (16 ps) and 8-bit amplitude quantization of the AWG, some short pulses may be lost, resulting in reduced signal power. This limitation is particularly relevant for modern modulation schemes with low average power, where the digital signal contains many short pulses that are likely to be affected by amplitude attenuation.

To mitigate these limitations, the digital Doherty drive is optimized to produce low output power in OBO, while still being driven by large, reproducible duty cycles on the AWG. The OFDM results at 3.5 GHz with a 20 MHz signal bandwidth show 55% average efficiency and 22 dBm average power, with -16 dBc recorded ACPR. After linearization, the module achieves -28 dBc of ACPR and 6% EVM, with a partially reduced efficiency of 48% and 23 dBm of average power. Fig. 7 presents the signal spectrum before and after linearization.

Due to the novelty of the topology, further investigations and improvements are needed to achieve effective linearization. Nevertheless, the results demonstrate that the proposed digital class-E Doherty solution can efficiently handle modern modulation schemes.

IV. Conclusion

The paper presents a GaN-based digital class-E Doherty module designed to extend the back-off capabilities of digital Doherty amplifiers to deep OBO. At 3.5 GHz, the measured final-stage drain efficiency reaches a peak of 68% at 12 dB OBO in single-tone measurements, with a maximum saturated output power of 33 dBm. At 3.5 GHz, the PA module achieves 55% drain efficiency for a 20 MHz 9 dB PAPR digital OFDM input signal. The system level characterization results prove the big potential of the proposed digital class-E Doherty architecture for future 5G base station applications.

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