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(Article begins on next page)

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GaN-Based Digital Class-E Doherty Power Amplifier for 5G FR1 Frequency Band

Giulia Bartolotti[#1], Anna Piacibello[#2], Vittorio Camarchia[#3], Deguang Sun[$4], Thomas Hoffmann[$5], Andreas Wentzel[$6]

[#]Politecnico di Torino, Italy

[$]Ferdinand-Braun-Institut (FBH), Berlin, Germany

{[1]giulia.bartolotti, [2]anna.piacibello, [3]vittorio.camarchia}@polito.it,

{[4]deguang.sun, [5]thomas.hoffman, [6]andreas.wentzel}@fbh-berlin.de

***Abstract* — This paper presents for the first time a GaN-based digital class-E Doherty power amplifier module (PA) for the 5G FR1 frequency band. Two identical class-E PA MMICs with digital pulse-width modulated (PWM) input driving are combined in a two-way Doherty configuration for high efficiency over an extended output back-off (OBO) range up to 9 dB. A wideband Doherty combiner design strategy is adapted to the class-E capabilities of the PAs to achieve high-efficiency for low power levels leading to an extended back-off range. At 7.5 dB OBO, the measured final-stage drain efficiency (η_{drain}) peaks at 68% for 3.4 GHz PWM single-tone input signal. Over a 3.2-3.6 GHz frequency range the prototype achieves a minimum of 52% η_{drain} at 9 dB OBO. The maximum saturated output power is 32.8 dBm. At 3.3 GHz, the PA module achieves 60% and 59% η_{drain} for a 20 MHz and 100 MHz 9 dB PAPR digital OFDM input signal, respectively.**

***Keywords* — Back-off, Class-E, Digital, Doherty, GaN, PWM.**

I. Introduction

The power amplifier (PA) is crucial in the RF front-end of transmitters, and its high efficiency is essential for effective data transmission. The class-E amplifier [1] is a widely used switching-mode PA due to its capability to achieve, in principle, 100% efficiency at maximum saturated output power (P_{out}), with practical efficiency values of 80% in the sub-6 GHz range at Watt-level [2].

With the advancement of 5G and 6G wireless communication systems, there has been a rise in data rates and the adoption of more complex modulation schemes that exhibit a high peak-to-average power ratio (PAPR). This shift makes it essential to design energy-efficient power amplifiers that deliver strong performance across a wide range of output power back-off (OBO) up to 9 or even 12 dB.

In the past, the different combination of switching PAs has been attempted to achieve high efficiencies in back-off conditions. The half-bridge, sequential, and outphasing configurations have shown either low OBO (6 dB) or low frequency of operation up to now (e.g., [2]).

The Doherty load modulation technique [3] is a popular method for improving efficiency in back-off. Extensively studied in the analog domain due to its simplicity, it offers also the possibility to achieve high OBO, larger than 6 dB, with either using different device size which may limit the achievable bandwidth, or more complex topologies as 3-way Doherty [4]. In contrast, a digital implementation offers greater flexibility and compactness significantly simplifying communication systems as, e.g., no DACs are required any more. This leads to a more sustainable, greener ICT. Due to this, fully digital transmitters and PA architectures [2] are gaining more and more attention. In [5] an analog driven class-E Doherty has been presented with the focus of wideband behavior. The concept of integrating the Doherty advantage for enhanced back-off efficiency with the high-efficiency performance of digital class-E PAs is mostly unexplored in existing literature. To the authors' best knowledge, the paper presents for the first time a GaN-based digital class-E Doherty power amplifier for 5G sub-6 GHz applications.

II. Design Process

Two identical digital class-E PA Monolithic Microwave Integrated Circuits (MMIC) [2] which have been fabricated on the FBH 250 nm GaN-HEMT process line, are combined off-chip in a two-way Doherty configuration through a microstrip wideband combiner implementation. Due to the digital design approach the frequency of operation (f_{s}) is only determined by the (class-E) output network. As no narrowband reactive matching is applied one can flexibly choose the f_{s}. This is one of the major advantages of digital PAs. Moreover, the chips become very compact.

A. Class-E Chip

Fig. 1 shows the schematic of the used digital class-E PA chips exhibiting an area of $1.71\times1.18\,\mathrm{mm}^2$. A common-source final-stage 8×62.5 µm GaN-HEMT (V1) is fed by two integrated driver stages (V01, V03). The class-E shunt capacitance is absorbed in the final-stage transistor drain-to-source capacitance (C_{ds}). An on-chip series capacitance of 1.25 pF (C1) is integrated at the output of the circuit to be used as an element of the class-E output resonator. More details of the design and a photo of the MMIC can be found in [2].

B. Class-E Load-Pull

The maximum performance of the individual class-E chip are investigated in terms of load pull in Keysight's ADS^{TM} environment with the schematic shown in Fig. 2.

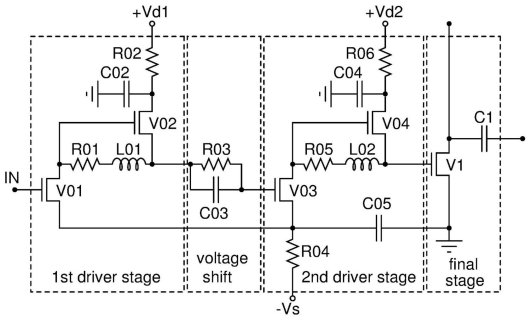


Fig. 1. Schematic of the digital class-E GaN PA MMICs used [2].

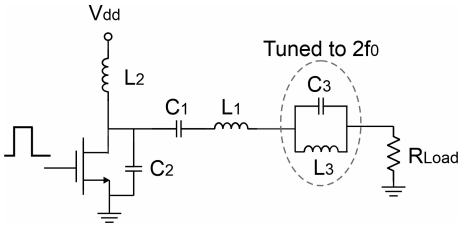


Fig. 2. Class-E ideal output matching network and resonator. Additional resonant network tuned at the second harmonic discussed in Section II.D.

First, the basic class-E output matching network and resonator (L1, C1, L2, C2 of Fig. 2) are implemented with ideal components. A simplified switch model is used to emulate the chip final-stage transistor V1 (see Fig. 1). The design equations of Sokal [1] are applied to determine the components' starting values. The optimum complex impedance at the device drain is estimated and used as initial condition to perform a load-pull analysis on the chip circuit level model. For this an ideal resonator at the selected f_s of 3.4 GHz is inserted at the output reproducing an ideal class-E output with a single-tone signal. The circuit is then loaded with a complex load, to be implemented at a later stage with the lumped components.

The maximum efficiency for different power levels is evaluated in order to choose the proper load targets for the load modulation of the Doherty. Different power levels are set by varying the duty cycle of the digital input signal. Table 1 presents the maximum efficiency of the chip at various power back-off levels with a 10 V drain supply V_{DD}. It indicates a saturated output power of 29 dBm and an efficiency greater than 75%, down to 5 dB OBO.

Table 1. Loads for maximum efficiency at different power back-off levels.

Load (Ω)	**Power** (dBm)	**OBO** (dB)	**Efficiency** (%)
$77 + j25$	29	-	70
$117 + j111$	25	4	78
$230 + j150$	24	5	75

The reported efficiency values correspond to the drain efficiency of the final-stage transistor only (cp. V1 in Fig. 1). This work aims to demonstrate the effectiveness of the combining strategy for achieving high efficiency over an extended OBO range, rather than focusing on the maximum performance of the digital class-E amplifier as a stand-alone PA. Therefore, the estimations of dissipated power and the efficiency performance do not account for the drivers, indicated as V01 and V03 in Fig. 1.

The preliminary investigation shows a low impact of the duty cycle on the efficiency performance of the class-E PA, as suggested by the investigations presented in [6]. In fact, the single-chip class-E PA configuration can provide high efficiency, in excess of 75%, over a 5 dB back-off range.

C. Combiner Design Strategy

A Doherty combiner strategy [7] is adapted to the class-E capabilities of the PAs of achieving high-efficiency for low power levels to obtain an extended back-off range. The strategy foresees equal device size for the Main and Auxiliary power amplifiers. One quarter-wavelength transformer is present on the Main branch and one half-wavelength line on the Auxiliary branch. A shunt high-precision SMD inductor is inserted on each branch for parasitic compensation. Fig. 3 shows the combiner topology.

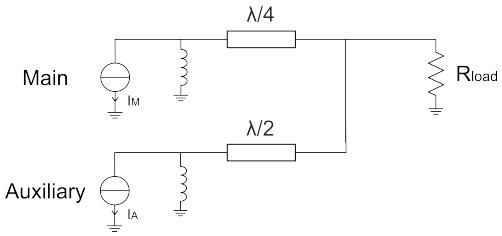


Fig. 3. Simplified circuit topology of the designed Doherty combiner: one quarter-wavelength transformer on the Main branch and one half-wavelength line on the Auxiliary branch.

This topology has proven in analog Doherty configurations to allow for OBO larger than 6 dB when used in combination with different drain biases for the Main and Auxiliary PA. Furthermore, the additional line on the Auxiliary branch can improve the Doherty wideband behaviour.

The digital implementation provides greater flexibility in adjusting the PA's turn-on and the current increase slope by properly setting the input duty cycle. Fig. 4 shows the Main and Auxiliary load modulation trajectories when simulated in a small-signal environment with ideal current generators. The target saturation and 5dB back-off loads of $(77 + j25)\,\Omega$ and $(230 + j150)\,\Omega$ respectively are highlighted.

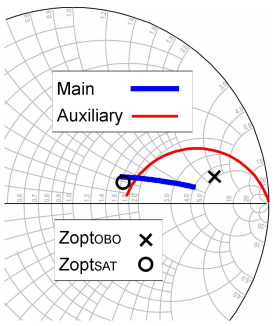


Fig. 4. Load modulation trajectories for the Main (blue) and Auxiliary (red) amplifiers at 3.4 GHz center frequency. Optimum saturation (ZoptSAT) and back-off (ZoptOBO) loads are highlighted.

D. Resonator and Output Matching Network

The implementation of the output matching network and resonator must take into account the fixed values for the fabricated FBH PA MMICs: the embedded drain-to-source capacitance C_{ds} of the final-stage transistor acting as C_2 and the integrated series capacitance acting as C_1. Also, the gold bond-wires necessary to connect the chip to the board contribute to the value of L_1 and L_2 inductors with a value of about 1 nH / mm, estimated through previous measurements. In case of higher inductance values, high-precision lumped SMD inductors from Coilcraft are selected to reach the necessary values.

Fig. 2 shows that a resonator tuned to the second harmonic is added to the topology. Sokal [1] has shown that this configuration can reduce the transistor peak voltage for a given output power. Here, the topology has the additional advantage of increasing the design space limited by the MMIC fixed integrated capacitor value.

E. Board Integration

The optimized Doherty combiner as well as input and biasing circuitry have been fabricated on a Rogers 4003C PCB laminate with 0.305 mm thickness. The board is mounted on a copper heatsink and the developed demonstrator has an overall size of 39 × 42 mm^2. Fig. 5 shows the fabricated module.

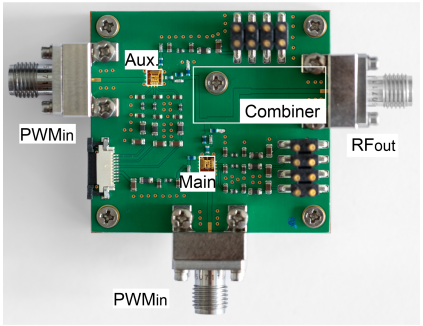


Fig. 5. Fabricated digital class-E Doherty PA module including two GaN PA MMICs and the Doherty combiner; size: 39 × 42 mm^2.

Two RF connectors (PWMin) for the digital inputs are connected with 50 Ω line to the input of the two MMIC class-E chips. The chips are soldered on the Cu carrier (see Fig. 5, two cutouts in PCB) for a common ground connection, and bonded to the DC and RF lines on the board. At their output there is the resonator implemented with lumped components presented in Section II-D and the Doherty combiner implemented with microstrip lines, connected to the RF output (RFout). The remaining lumped elements are decoupling capacitors and feeding inductors of the drivers and final stage bias lines. Flat connectors and pin header connectors are present for DC biasing.

III. Characterization

The digital class-E Doherty PA has been initially characterized using single-tone PWM input signals to prove the effectiveness of the digital Doherty combination strategy. The back-off behavior is investigated by setting reduced duty cycles for the input signals. Fig. 6 illustrates the used measurement setup.

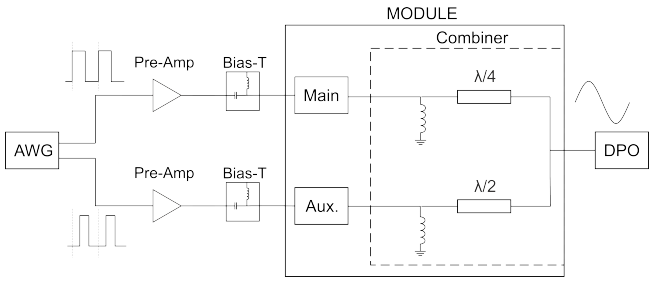


Fig. 6. Block diagram of used measurement setup.

It includes a Keysight Arbitrary Waveform Generator (AWG) M8195A to generate the two digital input signals, and two external broadband preamplifiers to ensure a 6 V peak-to-peak input voltage swing for the class-E MMICs. Two bias-Ts are required since the inputs of the module are connected to the input of the chips which coincide with the gate of the driver transistor (Fig. 1). The bias-Ts adjust the DC value of the digital input signal, which varies based on the input signal's duty cycle. At the output, a 20 dB attenuator is used to limit the input power of the utilized Tektronix DPO70000SX real-time oscilloscope. All measured characteristics presented in the following are extracted from the recorded real-time data.

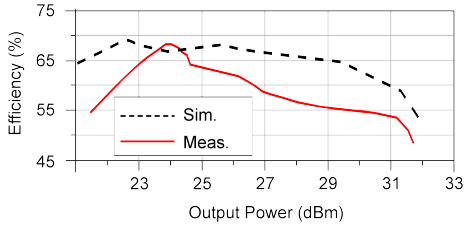


Fig. 7. η_{drain} vs. output power performance @ f_s=3.4 GHz with V_{DD}= 10 V: (dashed) simulated and (continuous) 1-Tone measured results.

By taking into account only the chip final-stage drain efficiency, Fig. 7 compares measured with simulated η_{drain} vs. output power at 3.4 GHz at a final-stage drain supply voltage (V_{DD}) of 10 V. The saturated P_{out} reaches 31.6 dBm and maximum efficiencies of 68% and 61% at 7.5 dB OBO and 9 dB OBO are achieved, respectively. The measured and simulated performance results are comparable at saturation and in the efficiency level of back-off peak, while some discrepancies are noted in the saturated efficiency levels and the power back-off. This variation is partially attributed to the fact that the simulated results are derived from time-domain circuit-level simulations, then adding the Doherty combiner losses estimated through electromagnetic simulations. Although direct time-domain simulations of the electromagnetic version of the circuit could be more precise, they have shown convergence issues. The measured output power peaks at 32.8 dBm at a V_{DD} of 12 V. It must be mentioned here that according to class-E theory the maximum voltage swing across the transistor is 3.6* V_{DD}. To stay in the safe region, all measurements shown were conducted at

10 V. The efficiency curves show that there is no performance reduction between the two efficiency peaks, unlike in most analog Doherty PAs. The high efficiency of the Auxiliary amplifier is due to its digital class-E implementation. As discussed at the end of Section II-B, a single class-E PA can achieve high efficiencies at low power levels. When two class-E devices are combined, the Auxiliary amplifier can maintain high efficiency immediately after its turn-on, which prevents a drop in overall efficiency. This is a major advantage compared to all previous Doherty realizations so far.

The performance over the 3.2-3.6 GHz frequency range are then investigated. Fig. 8 shows a minimum saturated power of 31 dBm and a power variation lower than 1 dB over the band. The graph also reports the maximum efficiency recorded in the power sweeps, with minimum value of 65% over the bandwidth and peak value of 71% at 3.2 GHz.

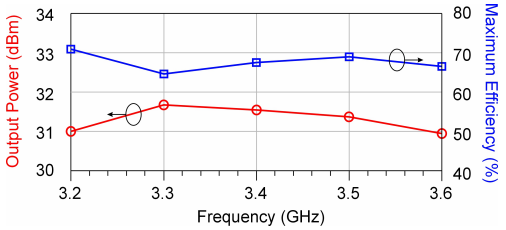


Fig. 8. 1-Tone measured performance with V_{DD}= 10 V: (red) saturated output power and (blue) maximum η_{drain}.

Fig. 9 reports the efficiency performance over the band for fixed 7 dB, 8 dB, and 9 dB OBO levels. Minimum values of 60%, 55%, and 52% respectively are recorded. Specifically, a remarkable 52% minimum efficiency at 9 dB OBO over a 400 MHz frequency range represents a record value for a digital Doherty.

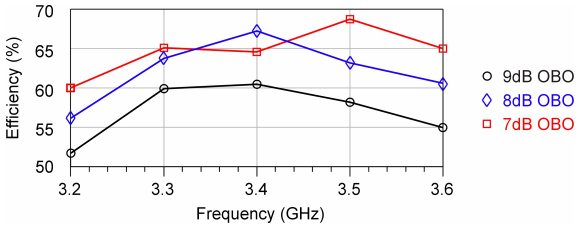


Fig. 9. 1-Tone measured η_{drain} performance with V_{DD}= 10 V over 3.2-3.6 GHz band at 7, 8, and 9 dB OBO.

Finally, the PA module has been tested from 3.2-3.6 GHz with OFDM input signals having 9 dB PAPR encoded. All input signals are generated using the digital modulator concept presented in [8]. It includes an inline linearization technique which does not consume any additional power required for the DPD. The best results are registered at 3.3 GHz with a 20 MHz signal bandwidth, 60% average efficiency and 21.6 dBm average power with -20 dBc ACPR are recorded. For 100 MHz bandwidth, 59% average efficiency and 21.4 dBm average power with -15 dBc ACPR are registered. After the linearization, the 20 MHz bandwidth signal achieves -31 dBc of ACPR and 4.2% EVM, but with reduced efficiency of 47% and 19 dBm of output power. Due to the novelty of the topology and the respective input signal constellation further investigations and improvements are required for effective linearization. Nevertheless, the achieved results prove the big potential of the proposed digital class-E Doherty architecture for future 5G base station applications.

IV. Conclusion

The paper presents for the first time a GaN-based digital class-E Doherty power amplifier for 5G sub-6 GHz applications. The implemented PA shows maximum performance under 1-Tone measurements, with 68% drain efficiency at 7.5 dB OBO at 3.4 GHz and 52% drain efficiency over the (3.2-3.6) GHz bandwidth at 9 dB OBO. Moreover, the very compact module shows high potential for future 5G base-station applications when tested with modulated (OFDM) input signals with bandwidths up to 100 MHz and efficiencies close to 60%.

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