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(Article begins on next page)

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Broadband Integrated Doherty Power Amplifier Module using Advanced GaN-on-Si HEMT Technology for 5G mMIMO Base Stations

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***Abstract*—In this paper, a broadband integrated GaN Doherty power amplifier (PA) module for 5G massive MIMO base stations is reported. Benefiting from the dual-driver Doherty structure and the optimal biasing scheme, the lineup efficiency has been boosted without compromising the linearity. The adopted passive networks, including the combiner, interstage and input matching network, have been developed for broadband operation and eventually have been miniaturized into $12\times8\,\mathrm{mm}^2$ laminate. The PA module features compact dimensions and lightweight characteristics for the 5G base station scenario. It achieves an efficiency higher than 45.8 % and a gain of more than 31 dB across the 3.6–4.0 GHz band under a 100-MHz LTE signal with 8-W average output power. Linearized adjacent channel power ratio of -54.5 and -50.5 dBc, is achieved through digital pre-distortion for 20- and 100-MHz signals, respectively.**

***Index Terms*—Gallium Nitride, Doherty power amplifier, 5G mobile communication, Digital pre-distortion**

I. Introduction

Global mobile network data traffic has experienced a surge of growth in recent years, boosted by the high demand for data transformation on various media platforms. To expand the system capability, innovative techniques like massive MIMO (mMIMO) have been widely deployed in the 5G base stations transceivers [1]. As multiple PAs are adopted before each antenna in the RF transceiver, power amplifier modules (PAMs) become a predominant solution, providing high integration with sufficient output power. At the same time, 5G communication systems adopt complex modulation schemes, generating signals with a high peak-to-average ratio (PAPR), typically in the range of 8 to 14 dB. This requires the PA to operate with high efficiency over a broad range of back-off power levels. While the Chireix outphasing architecture has shown potential especially in its native dual-input form [2], [3], when targeting on extended back-off operation and high-level integration the Doherty PA (DPA) has become a popular choice due to its ability to enhance back-off efficiency with a simple single-input architecture, which can also be minimized into a small footprint.

Nevertheless, the conventional one-stage DPA normally has a limited gain, which is not able to meet the requirement from the real 5G base station scenario. One or more driver stages are essential to increase the gain of the circuit. Due to the extra DC power consumption of the drivers, the lineup efficiency is deemed to be reduced. Previous works have investigated the impact of driver stage on the gain and the lineup efficiency of DPA design [4], [5]. The single-driver and dual-driver DPA can exhibit quite distinct lineup efficiency while achieving a similar gain. This is strongly dependent on the gain of the final PA stage and the selection of the driver size. In the case of a final PA stage featuring a low gain, the dual-driver DPA offers a higher lineup efficiency, even though the complexity of the design increases contemporaneously. In GaN-on-Si technologies, where the lower thermal conductivity of the silicon substrate imposes stricter thermal constraints, high-efficiency operation is also beneficial to mitigate heat dissipation, especially in compact implementations [6].

This work is developed based on the Infineon 28 - V 0.25 - μm RF GaN-on-Si heterostructure field-effect transistor technology, with the feature of a high gain and a high efficiency. A relatively low drain capacitance from this technology provides the potential to design a broadband DPA with low frequency dispersion. The design and characterization of a fully integrated dual-driver DPA module are presented. The DPA module illustrated in Fig. 1 is constituted of a fully integrated dual-driver DPA and an on-board biasing control integrated circuit.

II. Doherty PA module design

A. Asymmetrical Structure and Biasing Scheme

To extend the back-off range in a DPA, the main and auxiliary amplifiers are requested to deliver different maximum out-

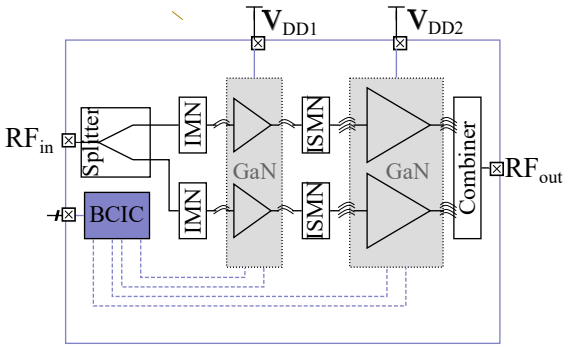


Fig. 1: Block diagram of the dual-driver DPA, including splitter, input matching networks (IMN), interstage (ISMN), combiner, and an embedded biasing control integrated circuit (BCIC).

put powers to form asymmetrical operation. Originally, both the main and auxiliary device utilize the same drain voltage supply to simplify the complexity of the DC power supply circuitry. Considering the unavoidable gain compression in GaN DPAs, the periphery ratio between main and auxiliary devices is determined as 1:2 to provide an 8 -9 dB back-off power level.

The driver transistor sizes are selected to sufficiently drive the PA final stage at a certain gain compression level. The requested output power for each device is listed in Table I. A gain compression of 5 dB at saturation is expected, consisting of 4 dB for the PAs and 1 dB for the drivers. Nevertheless, the calculated periphery of the main driver is too small to realize and also further increases the optimal load impedance for the main driver, therefore complicating the interstage matching network. To overcome these issues, the symmetrical driver strategy is adopted, where the main driver is slightly oversized but has proven to have a negligible impact on the lineup efficiency [7]. The gain compression of the driver can be limited at saturation, which would potentially benefit the linearity.

TABLE I: Estimated power budget

Amplification Stage	Main PA	Auxiliary PA	Main Driver	Auxiliary Driver
Pout [W]	19.7	46.1	7.4	7.4

Both the driver and the output power device on the main branch operate in Class-AB, which gives the best trade-off between the efficiency and linearity. Meanwhile, both the driver and the output power device on the auxiliary branch are biased in Class-C to ensure the minimum power consumption before the auxiliary device turns on, therefore boosting the lineup efficiency. In single-stage 9 - dB DPAs, an uneven input splitter is required, which reduces the linear gain and results in lower line-up efficiency. However, the dual-driver architecture has additional degrees of freedom, which allows for an even input splitter with negligible impact on the load modulation.

B. DPA Combiner Design

For the asymmetric structure, a larger impedance transformation ratio and a normally larger parasitic capacitance from the auxiliary device together put constraints on the desired broadband operation [8], [9]. The inverted topology illustrated in Fig. 2 is considered as a suitable topology for creating broadband operation in asymmetrical DPA [10]. Nevertheless, a transmission line with an electrical length of $\lambda/2$ or a $\lambda/4$ at center frequency f_0 is hard to meander into a small footprint in a PAM.

In [11], the inverted combiner is realized by Tee-type transmission line network with parasitic capacitance absorption in favor of the compactness and wideband operation. In this work, the quasi-lumped $\lambda/4$ transmission line-based inverted combiner is adopted to enhance the circuit compactness.

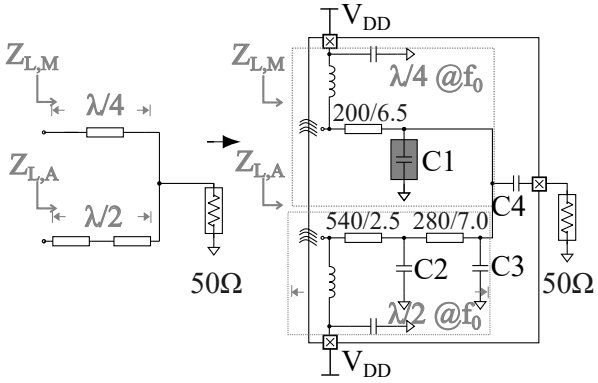


Fig. 2: Topology of the inverted combiner (left) and circuit schematic of the adopted DPA combiner (right). The dimensions of microstrip components are reported in width (μm)/ length (mm) format.

The circuit schematic is shown in Fig. 2 and the related details have been presented in the author's previous work [12], [13]. The length of each transmission line is reduced from a standard $\lambda/4$ by inserting capacitors C1, C2, being suitable to wind on board. Despite the compactness, the quasi-lumped $\lambda/4$ section is optimized up to the second harmonic to enhance the efficiency. Benefiting from the highlighted capacitor C1, the impedance at the combination node is enforced towards short at the second harmonic range. From the system point of view, this compact DPA combiner additionally provides the insensitive harmonic loads, avoiding the potential efficiency deterioration due to the interference from the PA's output termination.

C. Interstage and Input Matching Design

To mitigate linearity degradation caused by intermodulation products near the RF band, the ISMN and IMN are developed to enhance band insensitivity. This design targets a 100 MHz bandwidth margin extended from each side of the operational band.

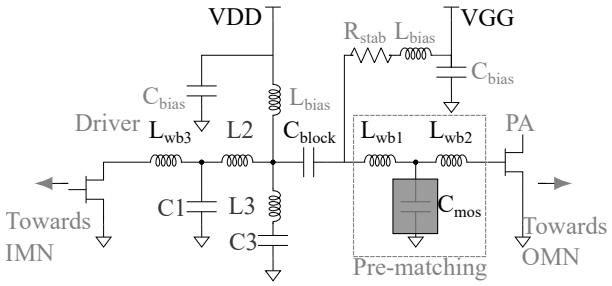


Fig. 3: Circuit schematic of the realized ISMN.

The ISMN is based on a broadband topology analytically derived from [14], trading off the simplicity and wideband feature, offering an impedance transformation of 1:25 over 3.5 - 4.1 GHz. Meanwhile, the topology of IMN is highly focusing on the simplicity. The realized ISMN is illustrated in Fig. 3, a highlighted capacitor C_{mos} is inserted to control the second harmonic, together with the bondwires L_{wb} providing the pre-matching. While the bandpass feature is established by the ISMN, the IMN equalizes the transistor gain roll-off by increasing the high-frequency loss and mismatching at lower frequencies, resulting in lower gain ripple within the target band. Moreover, the same topology is adopted on both main and auxiliary branches to preserve the symmetry to control the phase deviation.

III. Demonstrator and Experimental Results

The designed PAM is implemented in a product environment using a 339 - μm five-layer coreless laminate substrate illustrated in Fig. 4, maintaining a compact dimension and lightweight characteristics. Copper thermal bar-via structures allocate underneath the dies to enhance mechanical stability and reduce the thermal resistance path. A programmable smart BCIC integrated circuit is implemented for biasing function, temperature monitoring, and TDD switching of the PAM.

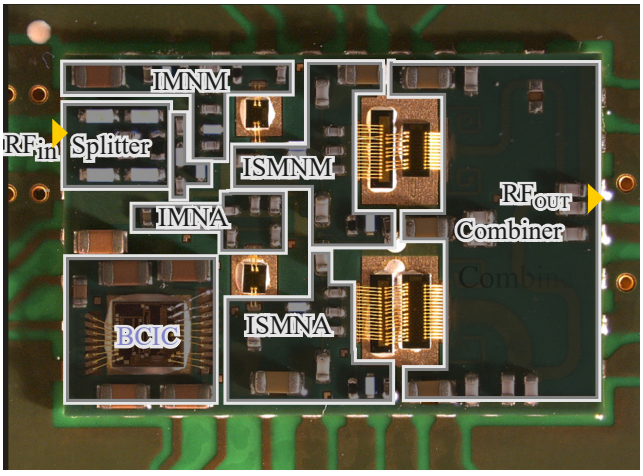


Fig. 4: Photograph of the designed Doherty PAM (12×8 mm^2 footprint).

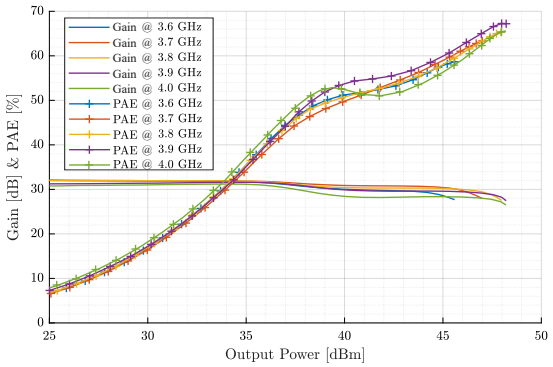
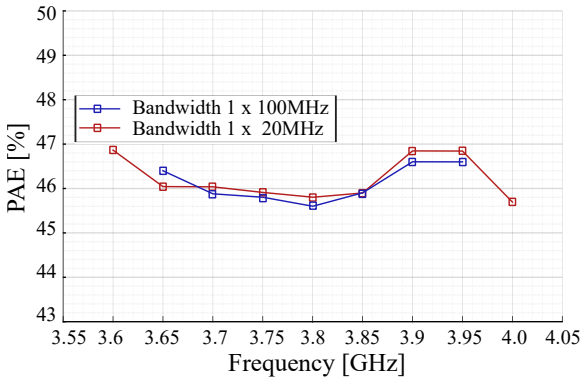
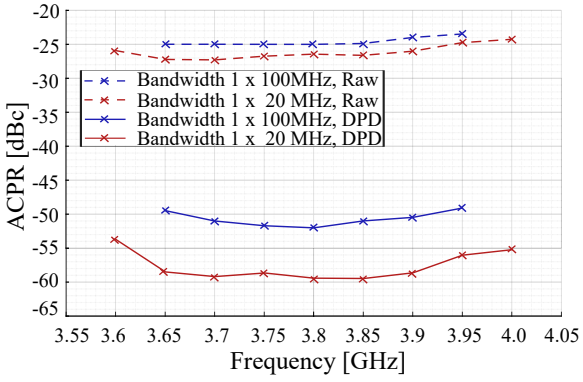


Fig. 5: Measured gain and PAE versus output power with pulsed-CW signals, from 3.6 GHz to 4.0 GHz.



(a)



(b)

Fig. 6: Modulation measurement using signal with NR FDD OFDM 265-QAM scheme and a PAPR of 7.5 dB at 39 dBm: (a) average PAE and (b) ACPR, from 3.6 GHz to 4.0 GHz.

The PA has been characterized in large-signal Continuous-Wave (CW) conditions by using the power measurement bench setup by Infineon. The measured gain and PAE for each operational frequency, as a function of the output power, are displayed in Fig. 5, respectively. The measured PAE is higher than 50% at an average output power of 39 dBm. The obtained gain is higher than 31 dB with a ripple lower than 1 dB over

TABLE II: Performance comparison with State-Of-The-Art DPAs for 3-4 GHz band

References	Freq [GHz]	iBW [MHz]	PAPR [dB]	Pave [dBm]	Line-up Gain [dB]	Mod. PAE [%]	ACLR before DPD [dBc]	ACLR after DPD [dBc]	Area PCB [mm^2]
[15] (2016)	3.0 - 3.6	20	7.5	34.2	12	45.9	-40	-50	$>>10^3$
[16] (2017)	3.4 - 3.6	20	7.2	35	26.2	41.5	-24	-50	400
[7] (2024)	3.5 - 3.7	20/100	8	40	25.7	47.9	-25/-25	-53/-45	$>>10^3$
[11] (2022)	3.4 - 4.1	20/200	7.5	40.3/43.3	30	42.0/43.3	/	-47/-45.1	76
[17] (2024)	3.4 - 3.8	200	8.5	39	29	48.5	-27.1	-47	96
This Work	3.6 - 4.0	20/100	7.5	39	31	45.9/45.8	-25.5/-25.5	-54.5/-50.5	96

the band.

For the modulation measurement, a test signal with a New Radio (NR) Frequency Domain Division (FDD) Orthogonal Frequency-Division Multiplexing (OFDM) 256-Quadrature Amplitude Modulation (QAM) scheme and a PAPR of 7.5 dB has been adopted. The measured PAE and ACPR with the signal bandwidth of 20 MHz, 100 MHz are shown in Fig. 6, respectively. The decomposed vector rotation (DVR) model is used for the Digital Pre-distortion (DPD) with a total coefficient vector size of 189.

Finally, a comparison with other state-of-the-art Doherty PAs is shown in Table II. The lineup efficiency and operational bandwidth of this design align with other state-of-the-art works, whilst a relatively higher gain is achieved. A good raw ACLR of -25.5 dBc is achieved before DPD and eventually is improved to -50.5 dBc after DPD, meeting the linearity requirement of the base station. The circuit's linearizability and compact feature are highlighted, making it suitable for mMIMO 5G base station applications.

IV. Conclusion

The design and characterization of a multi-stage Doherty PAM is presented. The dual-driver DPA design leverages advanced GaN-on-Si technology with high gain and power density. A broadband combiner implemented with miniaturized transmission lines and shunt capacitors enhances the circuit's compactness and favors the insensitivity of the harmonic loads. Eventually, the PAM illustrates a PAE of 45.8% and a gain of more than 31 dB across the 3.6 - 4.0 GHz band under 100 - MHz LTE signal with 8 - W average output power. An ACLR of -25.5 and -50.5 dBc before and after DPD, respectively, showing a good linearizability of the circuit.

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