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27 November 2026

Dead Time Losses Comparison of GaN FET Versus Si MOSFET in Inverter Switching Leg

S. Musumeci, *Member, IEEE*, F. Stella. *Member, IEEE*, V. Barba, *Student Member, IEEE* F. Mandrile, *Member, IEEE* and M. Palma, *Senior Member, IEEE*

***Abstract*—Optimal dead-time selection in switching converters is a critical design consideration for minimizing reverse conduction losses and enhancing output current quality. The minimum achievable dead time strongly depends on the device technology. In recent years, low-voltage AC motor drive applications, such as those in light e-mobility and humanoid robotics, have grown rapidly. While traditional Silicon (Si) MOSFETs remain widely used, they are increasingly being complemented or replaced by Gallium Nitride (GaN) devices, which continue to improve in performance and cost competitiveness. This paper deals with the comparison of the dead time requirements for GaN devices and Si MOSFETs used in inverter switching leg applications. The study focuses on low-voltage enhancement-mode GaN FETs and Si MOSFETs with similar current ratings, emphasizing the different reverse conduction mechanisms exhibited during dead time. The influence of dead time at different load currents, which are typical in inverter operation, is investigated through both simulations and experimental measurements. Additionally, device temperature measurements are used to assess the impact of dead time on the losses, further highlighting the differences between Si MOSFETs and GaN FETs from a thermal point of view. Based on the results, a methodology is proposed to select the optimal dead time duration to prevent cross-conduction, minimize power losses, and improve output current waveform quality.**

***Index Terms*—GaN FET, MOSFET, Dead Time, Switching Leg, Inverter, Parasitic Capacitances, Reverse Conduction.**

I. INTRODUCTION

Silicon-based power devices are approaching their theoretical performance limits, driving the industry to explore alternative technologies such as silicon carbide (SiC) and, more recently, GaN [1]. GaN power devices offer several advantages over their Si counterparts, particularly in terms of faster switching speeds and reduced switching losses, making them increasingly attractive for high-efficiency power conversion applications [2]. A key limitation of Si MOSFETs lies in the inherent trade-off between on-resistance and die size: reducing on-resistance typically requires a larger die, which in turn increases parasitic capacitance and associated switching losses. This trade-off makes it difficult to optimize both conduction and switching performance simultaneously in Si-based devices [3]. In pulse-width modulation (PWM) motor drive applications, GaN technology enables achieving higher switching frequencies, thus reducing current ripple and enhancing output waveform quality. However, to prevent cross-conduction in voltage source inverters (VSIs), a dead time must be introduced between the switching transitions of the high-side and low-side devices [4]. While essential for safe operation, dead time introduces waveform distortion, contributing to output voltage errors. This distortion arises not only from the dead time itself but also from device-specific characteristics such as turn-on/off delays and voltage drops across the switches and their body or reverse diodes.

GaN FET technology is becoming increasingly attractive for power electronics applications due to its high power density, low on-resistance, and capability to operate efficiently at high switching frequencies. At present, low-voltage applications below 100V are a significant, domain for GaN technology [5], while silicon MOSFETs remain dominant in certain low-cost, lower-frequency areas [6]. GaN technology's advantages like higher efficiency, smaller size, and faster switching are beneficial in low-voltage applications such as portable chargers, humanoid robots, and server power supplies [5], [7]. For example, in low-voltage motor drives, GaN-based inverters operating at high switching frequencies (e.g., ≥100 kHz) and reduced dead times (≤50 ns) have been proposed to lower the size of passive components (i.e., DC-link capacitors) and minimize motor torque ripple [8]. However, the associated high dV/dt rates require careful consideration of switching node transients and potential impacts on motor insulation and EMI performance [9]. The choice and optimization of dead time are therefore tightly linked to the switching device technology. Understanding the dynamic behavior of reverse conduction during dead time and its contribution to power losses is critical for setting an appropriate dead time duration in both GaN and Si-based converters. Additionally, analyzing the energy exchanged between high-side (HS) and low-side (LS) devices during both hard- and soft-switching transitions provides valuable insights into switching loss mechanisms. This study aims to optimize dead time settings to improve overall efficiency and performance in low-voltage motor drive inverters using either Si or GaN semiconductor technologies.

Several authors have investigated the loss mechanism of dead time in DC-DC converters [10], [11], [12]. The impact of dead time in inverter application for motor drive with GaN FETs is deeply examined in [13], [14]. In particular, the reference [13] investigates the impact of dead time on current THD and torque,

S. Musumeci, F. Stella,V. Barba and F. Mandrile. are with Department of Energy ‘‘Galileo Ferraris’’, Politecnico di Torino, 10129 Turin, Italy.

M. Palma is with Efficient Power Conversion (EPC), Volpiano, 10088 Turin, Italy.

demonstrating that the dead time reduction strongly diminishes the harmonic content of the inverter current. Voltage source inverters (VSIs) current harmonics due to the nonlinear effects for Si MOSFETs and GaN FETs are further investigated in [15]. In [16], a software compensation strategy is discussed to mitigate the distortion effect using a complex adaptive control method. Furthermore, the design process of optimal dead-time selection for the SiC MOSFET-based three-phase converter is evaluated in [17]. Collectively, these works provide a solid foundation for understanding dead time management and optimization in both GaN FET and Si MOSFET inverter systems, offering valuable insights for enhancing efficiency and performance in power electronics.

Furthermore, this paper provides a detailed experimental comparison between GaN FETs and Si MOSFETs in low-voltage switching leg for inverter devoted to motor drive applications, with particular emphasis on commutation transients occurring during dead time. The study presents a comprehensive analysis of key performance metrics, including switching losses, reverse conduction behavior, and dead time effects. Experimental tests conducted over a range of load current values (typical of AC motor drives) reveal distinct switching characteristics under varying operating conditions. The investigation also analyzes the effects of both hard and soft-switching transitions on energy losses, highlighting the fundamental differences in performance between GaN FETs and Si MOSFETs. A validated simulation model complements the experimental results, enabling quantitative estimates of switching energy and losses. These results demonstrate that GaN FETs can outperform Si MOSFETs in terms of efficiency at shorter dead times, despite their higher reverse conduction voltage drop. Therefore, this study provides both qualitative and quantitative insights into optimal dead time selection, offering practical guidelines tailored to the characteristics of each device technology and application scenario. This article represents an extended version of [4], with particular attention on the causes of switching losses during dead time, as mentioned above, considering the role of devices' parasitic output capacitances in a half-bridge connection. The study of the impact of these parasitic capacitances allows for accurate identification and distinction of different energy contributions. Furthermore, the paper examines the correlation between energy losses, dead time duration, and transistor temperature rise, demonstrating that the temperature is lower for a given combination of current and dead time. The thermal evaluation features an optimal choice of dead time for a given output current. with the addition of a detailed thermal analysis evaluating how dead time duration affects the temperature (i.e., losses) behavior of switching-leg devices.

The paper is organized as follows:

Section II presents a comparison of dead-time commutation behavior for GaN FETs and Si MOSFETs using two inverter boards with identical layouts. The analysis includes different switching current directions and different dV/dt. Section III introduces a validated simulation model used to evaluate energy losses and switching dynamics during dead time events. Section IV presents experimental thermal measurements, examining how dead time influences device temperature in both technologies. Section V concludes the paper with a summary of key results and design recommendations.

II. GaN FET And Si MOSFET Commutation Transients in Inverter Switching Leg

In an AC motor drive, each inverter leg operates with a sinusoidal phase current of varying amplitude. These currents either flow from the inverter leg's switching node to the motor phase or in the reverse direction.

To analyze commutation transients in switching legs using Si MOSFET and GaN FET devices, two half-bridge experimental PCB boards, differing only in device technology, were employed. This setup ensured a similar layout with homogenous parasitic effects from the PCB, thus enabling a reasonable comparison. However, differences in package design between GaN FETs and Si MOSFETs remain unavoidable, as each technology introduces its inherent parasitic elements, such as different stray inductances based on the different device packaging [18]. All tests were conducted under similar operating conditions for GaN FET and Si MOSFET-based boards to ensure a comparable and reliable evaluation. The GaN FET board houses two EPC2065 GaN FETs [19] in a half-bridge configuration, while the Si MOSFET one houses two Onsemi FDMS2D5N08C [20] in the same half-bridge setup. The main device characteristics are provided in Table I. The gate voltage level for driving the devices is 5 V for the GaN FETs and 10 V for the Si MOSFETs. The schematic of the switching leg is depicted in Fig. 1a. The experimental boards housing the GaN FETs and Si MOSFETs used in the tests are shown in Fig. 1b. The devices are tested at ambient temperatures (25°C) with a DC input voltage $V_{DC} = 48\ V$.

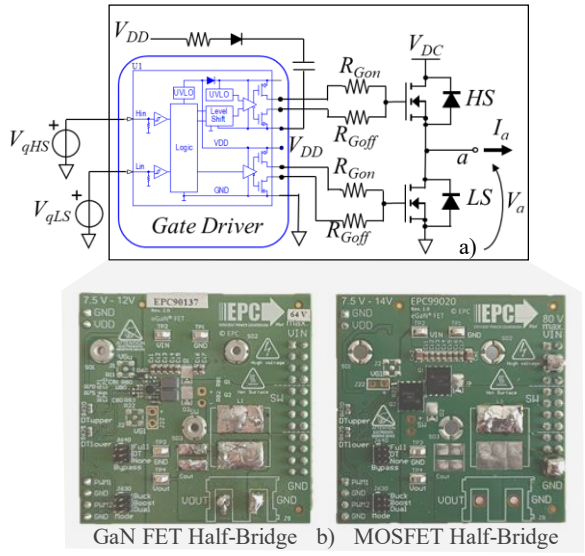

Fig. 1. a) Functional schematic of the half-bridge switching leg boards used for the experimental testing of the devices, mounting GaN transistors or Si MOSFETs in high-side (HS), and low-side (LS) positions. b) GaN FET (left) and Si MOSFET (right).

The gate resistors in the two switching boards are chosen so that, under the same conditions, the positive dV/dt turn-on overshoot in buck mode is the same [21]. The phase current I_a is controlled by a Si MOSFET-based inverter interfaced with an LCL filter to the switching node (node *a* of Fig. 1a) of the half-bridge. A STM32H7 microcontroller is used for generating the two PWM signals required to drive the two switches of the board under test. This MCU features an integrated high-resolution timer, enabling precise dead-time control with a time resolution of 200 ps. The experimental measurement setup is shown in Fig. 2. In Fig. 2a, the functional schematic of the proposed experimental setup is depicted, while Fig. 2b shows the main components of the physical test bench. During testing, the PWM switching frequency was set to $f_{sw} = 20\ kHz$ with a duty-cycle of 0.1 chosen to minimize the current ripple. The switching frequency for the experimental switching tests is based on the accessible switching frequency for Si MOSFET devices The highest possible switching frequencies for GaN FETs are not helpful for the dead-time analysis we wish to focus on. Since the tests involve switching during dead time, they are the same both at 20 kHz and at higher frequencies, more suitable for GaN FETs. Particular attention is given to the dead time, during which both GaN FETs and Si MOSFETs operate in reverse conduction mode.

TABLE I
SI MOSFET AND GAN FET PARAMETERS

Parameter	Symbol	Si MOSFET	GaN FET
Breakdown voltage	BV_{DSS}	80V	80V
Conduction resistance	R_{DSon}	2.7mΩ	3.6mΩ
Driving gate voltage	V_{GS}	10V-0V	5V-0V
Nominal rate current @T_a=25°C	I_{Dnom}	68A	60A
Output parasitic capacitances, max	C_{oss}	2070pF	801pF
Gate Charge	Q_G, Q_{GD}	54nC, 12nC @ V_{DS} = 40 V, V_{GS} =10 V, I_D = 68 A	12nC, 1.7nC @ V_{DS} = 40 V, V_{GS} = 5 V, I_D = 25 A
Reverse conduction Voltage, @T_a=25°C	V_F	1.2V	2.6V

While Si MOSFETs include an intrinsic body diode that conducts during reverse current flow in the dead time interval, GaN FETs do not have a physical body diode. Instead, they exhibit reverse conduction behavior through the channel itself, mimicking a diode. In AC motor drive applications, the amplitude and polarity of the sinusoidal phase current strongly influence the voltage slew rate (dV_a/dt) across the inverter legs during switching events. To preserve the quality of the output waveform and minimize phase voltage and current distortion, the dead time duration t_{dt} must be kept as short as possible [5], [22]. In the current setup, a dead time of $t_{dt} = 150\ ns$ is preliminarily applied to both boards, representing a balanced choice that meets the requirements of both GaN FET and Si MOSFET technologies.

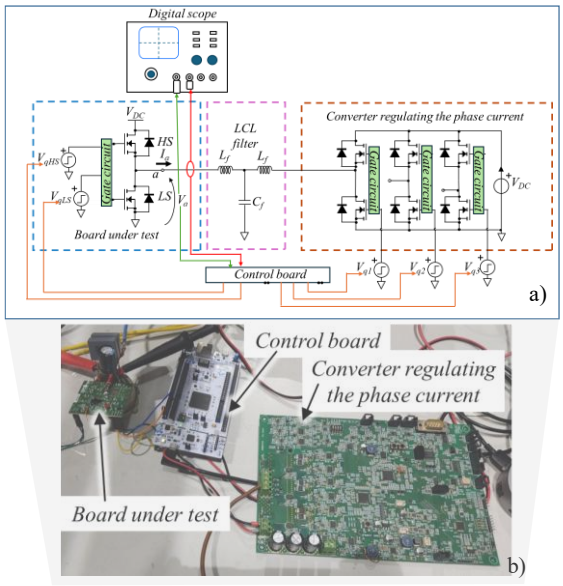

Fig. 2. Experimental setup with the half-bridge board under test (GaN FET and Si MOSFET), the inverter imposing the phase current, and the STM32H7 microcontroller. a) Block diagram of the experimental setup. b) Overview of the experimental setup.

The experimental analysis focuses on specific levels of phase current I_a, considering both positive and negative polarities. Positive I_a, corresponds to current exiting from the switching node *a*, while negative I_a refers to current flowing in the opposite direction. The tested current values include: 0.5 A, 1 A, 1.5 A, 2 A, 5 A, 7.5 A, and 10 A.

Two key commutation events are examined with positive values of I_a:

1. **High-side Turn-Off, Low-side Turn-On**: This event is characterized by a negative voltage slew rate ($dV_a/dt < 0$), as the phase voltage (V_a) decreases.
2. **Low-side Turn-Off, High-side Turn-On**: This event shows a positive voltage slew rate ($dV_a/dt > 0$), as the phase voltage (V_a) rises to V_{DC}.

A. Switching transients with $dV_a/dt < 0$ and positive I_a

During the commutation event involving the turn-off of the High Side (HS) switch and turn-on of the Low Side (LS) switch, the switching node voltage V_a decreases from V_{DC} to ground, thus resulting in a negative voltage slew rate ($dV_a/dt < 0$). This transient behaviour is influenced by both the instantaneous phase current I_a and the total output capacitance at the switching

node, defined as, $C_{OSS}=C_{GD}+C_{DS}$. The current paths during this transition for $I_a > 0$ and $dV_a/dt < 0$ are depicted in Fig. 3a. When HS is in on-state, the current flows through HS as shown in the red current path of Fig. 3a. As HS turns off, V_a falls, charging the C_{OSS} of HS and discharging the C_{OSS} of LS. The current path is depicted in purple in Fig. 3a.

In scenarios with low current values, as depicted in Fig. 3b, the voltage slew rate (dV_a/dt) during commutation is low due to the long C_{OSS} discharging time. The body diode does not conduct in this situation, avoiding associated conduction losses. On the contrary, high I_a causes a fast V_a variation, as depicted in Fig. 3b. In this case, the equivalent diode of LS conducts during part of the dead time, and the current follows the blue path of Fig. 3a. This reverse conduction time t_{rc} is always shorter than t_{dt}. At the end of the dead time, HS is in off-state, and the current is provided by LS (green path) turned on. In Fig. 3c the gate voltages V_{GS} are reported to highlight the different gate circuit voltage amplitudes required. Fig. 3b shows that the behaviour of the switching node voltage V_a is influenced by the duration of the dead time t_{dt} and the magnitude of the phase current I_a.

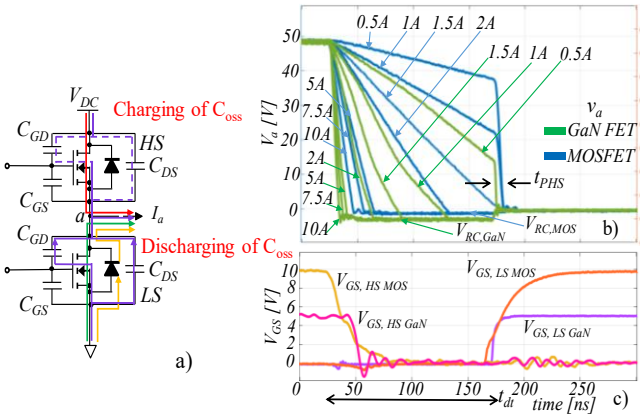

Fig. 3. a) Switching leg circuit model with current paths. b) Phase voltages V_a measured on GaN FET and Si MOSFET during the HS device turn-off and LS device turn-on commutation with $I_a > 0$ A and t_{dt} = 150 ns. c) Gate-source voltages V_{GS}. (V_a = 10 V/div, V_{GS} = 2 V/div, time = 50 ns/div)

Three types of switching events can occur:

1. **Zero Voltage Switching (ZVS):** ideal case where the switch turns on at zero V_{DS}.
2. **Partial Hard Switching (PHS):** the switch turns on with a reduced V_{DS}, thus resulting in moderate losses.
3. **Reverse Conduction (RC):** occurs when the reverse conduction path carries current during the dead time, before LS turn-on.

When HS commutates to the off state, the phase voltage V_a starts to decrease. This reduction occurs more rapidly at higher I_a due to the combined effect of the parasitic output capacitances C_{OSS} of the device. C_{OSS} value is not constant with the voltage, therefore, an equivalent capacitance C_{eq} is used to represent the behavior of V_a. Furthermore, the C_{eq} taking into account the contribution of the output parasitic capacitances as well as the node switching capacitances due to the load (such as the capacitance of the winding in the case of motor coils) [22]. The value of C_{eq} is calculated from the observed rate of change in V_a at different I_a levels as:

$$C_{eq} = \frac{V_{DC}}{t_{Vfall} \cdot I_a} \quad (1)$$

Where t_{vfall} is the voltage fall time required for V_a to drop to 0 V from V_{DC} when HS device turns off.

The value of C_{eq} can be computed considering an experimental waveform obtained in conditions of ZVS and using the basic relation of the capacitor current related to $\Delta t=t_{Vfall}$ at a fixed current I_a. ZVS occurs when the LS switch turns on precisely as V_a reaches 0 V, which is when the equals t_{dt}. Looking at the Si MOSFET waveforms of Fig. 3b, ZVS occurs at a phase current I_a=1.5 A. On the other hand, GaN FETs exhibit ZVS for I_a between 0.5 A and 1 A. This difference in ZVS's current level is due to the lower GaN FET C_{OSS} (801 pF) compared to the Si MOSFET (2070 pF), thus resulting in a shorter t_{vf} and allowing ZVS at lower I_a levels.

PHS occurs for I_a below the ZVS level. As shown in Fig. 6b, Si MOSFETs display PHS events at I_a of 0.5 A and 1 A, while GaN FETs exhibit PHS only at I_a of 0.5 A. The conditions of PHS event obtained with the GaN FET switching at I_a = 0.5 A is shown in Fig. 4a. The soft switching commutation obtained with the GaN FET switching at I_a = 2 A is depicted in Fig. 4b.

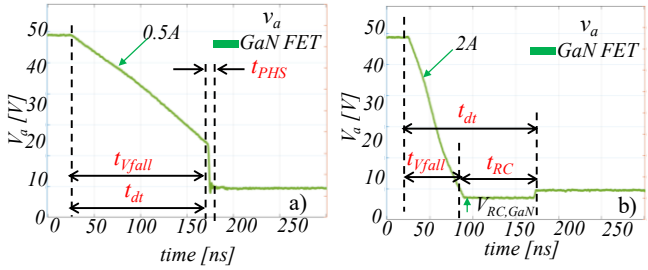

Fig. 4. Switching node voltages measured on GaN FET during the HS turn-off and LS turn-on commutation: a) PHS event at I_a = 0.5 A. b) RC event at I_a = 2 A. (V_a = 10 V/div, timestep = 50 ns/div)

In Fig. 4a, the LS device turns on before V_a drops completely to 0 V, leading to PHS losses after t_{dt}. For higher I_a values than those required for ZVS, a soft-switching event with a reverse conduction phenomenon appears (t_{rc}). In Fig. 4b, V_a reaches 0 V before t_{dt} ends ($t_{v\,fall} < t_{dt}$), and LS device operates in reverse conduction (RC). Therefore, V_a becomes negative and equal to the reverse conduction voltage V_{rc}. GaN FETs feature V_{rc}, significantly greater than the Si MOSFET, thus resulting in higher RC losses for GaN FET during dead time reverse condition. RC stops as the HS device turns on and lasts:

$$t_{rc} = t_{dt} - t_{Vfall} \quad (2)$$

Moreover, after t_{dt}, there are no additional losses as the HS transistor turns on.

B. Switching transients with $dV_a/dt > 0$ and positive I_a

While the LS device is in the on-state, the current is conducted following the red current path of Fig. 5a. When the LS transistor is turned off, the current flows through the diode of the LS device for the time t_{dt} (see the blue current path of Fig. 5a). The reverse conduction voltage drop V_{rc} appears and elapses in $t_{rc} = t_{dt}$, regardless of the I_a amplitude, as illustrated in Fig. 5b. After t_{dt}, the HS device is turned on, and the I_a current flow is associated with the red current path of Fig. 5a.

The phase voltages V_a, measured in the switching leg boards during commutation with $dV_a/dt > 0$ at several values of I_a are shown in Fig. 5b. Fig. 5c shows the gate-source voltages ($V_{GS,LS}$ for LS transistor and $V_{GS,HS}$ for HS device).

As shown in the results of Fig. 5b, reverse conduction appears immediately as LS device turns off and lasts until the end of t_{dt}. During this time, V_a equals the reverse conduction voltage drop of the GaN FET ($V_{rc,GaN}$) or the Si MOSFET ($V_{rc,MOS}$). The hard switching event (HSW) happens after t_{dt}. As shown in Fig. 5b, V_a rises more steeply than in the commutation shown at $dV_a/dt < 0$ (Fig. 3b). The V_a slope does not change with the I_a amplitude. The HSW duration t_{HSW} is longer for the Si MOSFET than for the GaN FET because of the higher C_{OSS} value of the Si MOSFET. The time t_{HSW} can be estimated by circuit parameters by means of equation (3).

$$t_{HSW} = C_{oss} \cdot \frac{V_{DC}}{I_a} \tag{3}$$

Finally, V_a stabilizes at V_{DC} after the HS switch turn-on transient ends.

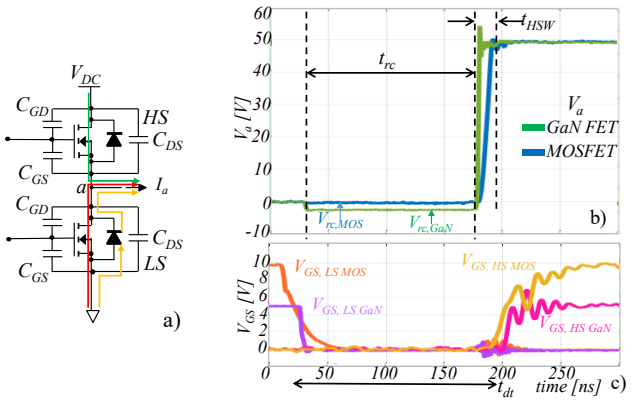

Fig. 5. a) Switching leg circuit model with current paths. b) Phase voltages V_a measured on GaN FET and Si MOSFET during the LS device turn-off and HS device turn-on commutation with $I_a > 0$ A and $t_{dt} = 150$ ns. c) Gate-source voltages V_{GS}. ($V_a = 10$ V/div, $V_{GS} = 2$ V/div, time = 50 ns/div)

C. Switching transients with negative I_a

For $I_a < 0$ A, the results are similar to those observed with $I_a > 0$ A in the commutation with a different sign of dV_a/dt. When $I_a < 0$ A and $dV_a/dt < 0$, the commutation exhibits a RC event that lasts for the duration of $t_{rc} = t_{dt}$ as shown in Fig. 6a. During this phase, the reverse conduction voltage drop of the GaN FET ($V_{rc,GaN}$) or the Si MOSFET ($V_{rc,MOS}$) causes the phase voltage to stabilize at $V_a = V_{rc} + V_{DC}$ during t_{dt}. Subsequently, as LS turns on, HSW event occurs, and V_a falls quickly to 0 V. The hard switching transient t_{HSW} lasts shorter for the GaN FET than the Si MOSFET due to the lower C_{OSS} featured by GaN FET. The findings discussed for $dV_a/dt > 0$ and $I_a > 0$ A are also valid for the scenario of $dV_a/dt < 0$ and $I_a < 0$ A.

The results of the commutation with $dV_a/dt > 0$ and $I_a < 0$ are presented in Fig. 6b. In particular, the results shown in Fig. 6b are obtained testing with I_a = -1.5 A, -2 A, -5 A, -7.5 A, -10 A.

In the commutation with $dV_a/dt > 0$ and $I_a < 0$, the dynamics are affected by the current amplitude I_a and the charging and discharging time of the system's parasitic capacitances. As a result, the commutation can exhibit ZVS, PHS, and RC phenomena.

This commutation behaves similarly to the commutation with $dV_a/dt < 0$ and $I_a > 0$. At low values of I_a, the voltage rise time t_{vr} lasts longer as the dead time t_{dt} and partial hard switching event appear. Conversely, reverse conduction occurs during t_{PHS} when the level of I_a is higher than the level causing ZVS.

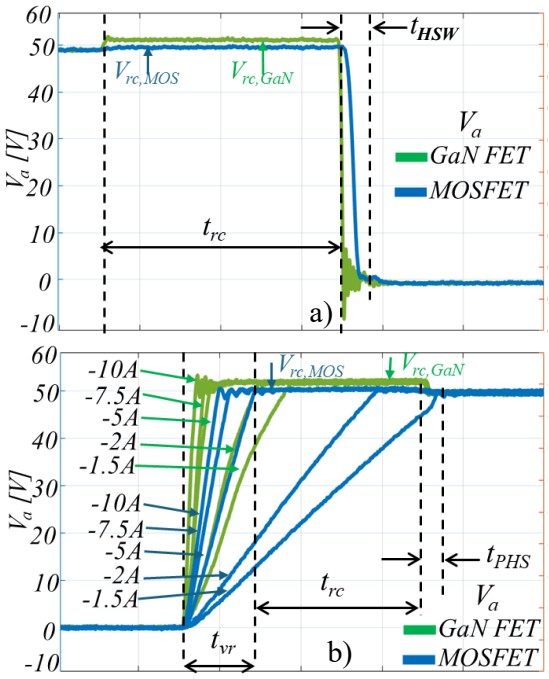

Fig. 6. a) Phase voltages V_a measured on GaN FET and Si MOSFET during the HS switch turn-off and LS device turn-on commutation with $I_a<0$ and $dV_a/dt<0$. b) Phase voltages V_a during the LS device turn-off and HS switch turn-on with $I_a<0$, $dV_a/dt>0$ and $t_{dt} = 150$ ns. ($V_a = 10$ V/div, time = 50 ns/div)

III. GaN FET Versus Si MOSFET Commutation Switching Energy Comparison

The tested evaluation board does not include current sensing to avoid influencing the switching board's performance. However, measuring transistor current is essential for analyzing energy loss behavior during commutations from an experimental point of view [23]. Therefore, SPICE simulations are utilized to investigate the energy behaviour involved in the

commutation. The GaN FET model used for the analysis has been validated in [24], while the manufacturer's official websites provide the Si MOSFET model.

The circuit in Fig. 1a is replicated in LTSpice. The simulated circuit replicates the experimental setup, while being operated under the same conditions: V_{DC} = 48 V, f_{sw} = 20 kHz, and a duty cycle of d=0.1. The model of the switching leg is validated by comparing the simulated waveforms with those resulting from the experimental tests shown in Fig. 3b and Fig. 5b. The simulation is performed for the following switching node currents (positive currents I_a are considered): I_a = 0.5 A, 1 A, 1.5 A, 2 A, 5 A, 7.5 A, and 10 A, consistent with the experimental conditions. The simulations are conducted using t_{dt} = 20 ns and t_{dt} = 150 ns, which are the typical dead time values used for GaN FETs and Si MOSFETs, respectively. These values are representative of those commonly used in inverters for motor drive applications. The analysis focuses on the energy losses associated with the low-side (LS) device.

A. Energy losses investigation with $dV_a/dt < 0$

In Fig. 7, the simulation results for GaN FET related to I_a = 10 A and I_a =2 A regarding the current in the parasitic output capacitance of the HS ($I_{C,HS}$) device and LS ($I_{C,LS}$) in two operative conditions: RC conditions (Fig. 7a) and PHS event (Fig. 7b) are shown.

In Fig. 7a, the current of the parasitic capacitors is positive for HS device and negative for the LS one, meaning that the LS switch is delivering charge to the HS during the V_a fall. As V_a stabilizes to the reverse drop, the parasitic capacitance current is zero because of the completed energy exchange between HS and LS parasitic capacitors. Differently, in Fig. 7b, the LS turn on when V_a is not zero (PHS). This condition causes the parasitic capacitances to exchange the remaining stored energy, featuring an almost instantaneous current peak.

The commutation where HS turns off and LS turns on, characterised by $dV_a/dt < 0$, reveals that different I_a amplitudes can lead to ZVS, RC, or PHS conditions. The energy associated with LS switch during the voltage variation, E_{VV}, is defined as:

$$E_{VV} = \int_0^{t_{Vfall}} |V_a \cdot I_{LS}| \cdot dt \tag{4}$$

Where I_{LS} is the current through the LS switch, and t_{vfall} is the time duration of the V_a phase voltage transition. The time t_{vfall} depends on the slope trend of V_a. ZVS occurs if t_{vfall} equals t_{dt}, and V_a reaches 0 V at the end of t_{dt}. On the other hand, RC condition is established when V_a reaches 0 V before t_{dt} ends (see Fig. 4b). When t_{vfall} is followed by RC lasting t_{rc}, the energy losses during t_{dt} are referred to as E_{RC} and calculated as:

$$E_{RC} = \int_{t_{Vfall}}^{t_{Vfall}+t_{RC}} |V_{RC} \cdot I_{LS}| \cdot dt \tag{5}$$

Where t_{rc} is the duration of the RC interval when V_a is negative and equal to $-V_{rc}$ for the GaN FET or Si MOSFET, the time interval $t = t_{vfall} + t_{rc}$ is theoretically congruent to t_{dt} and accounts for the turn-on delays of LS switch and the driving circuit's propagation delay.

Differently, PHS happens if V_a theoretically reaches 0 V after t_{dt}, but the LS device turns on when V_a is still positive (see Fig. 7a). The energy losses due to PHS, called E_{PHS} are determined as:

$$E_{PHS} = \int_{t_{dt}}^{t_{dt}+t_{PHS}} |v_a \cdot I_{LS}| \cdot dt \tag{6}$$

Where t_{PHS} is the duration of the PHS event that goes from the end of t_{dt} until the condition of I_{LS} = 0 A is triggered.

ZVS condition is characterized by E_{RC} = 0 J and E_{PHS} = 0 J. In this case, E_{VV} is the only energy involved in the switching event.

The energy E_{VV} is related to the energy exchange in the output parasitic capacitances (C_{OSS}) of the two switching devices of the half-bridge during the time in which both devices are in the OFF state. Indeed, at commutation with $dV_a/dt < 0$, the initial conditions involve the output capacitance C_{OSS} of the LS, which is charged to V_{DC}. Moreover, the parasitic output capacitance of the HS device is discharged to 0 V (see Fig. 6a). In the condition of ZVS or RC, the output parasitic capacitance of the HS switch charges absorbing the energy moving out from the C_{OSS} of the LS device until V_a = 0 V. Finally, C_{OSS} of the LS device is completely discharged, and C_{OSS} of the HS switch is fully charged. In the case of ZVS, E_{VV} is equal to:

$$E_{VV,ZVS} = \frac{1}{2} \cdot C_{eq} \cdot V_{DC}^2 \tag{7}$$

The value of $E_{VV,ZVS}$ is the maximum value of energy exchanged; however, the switching event features no energy losses.

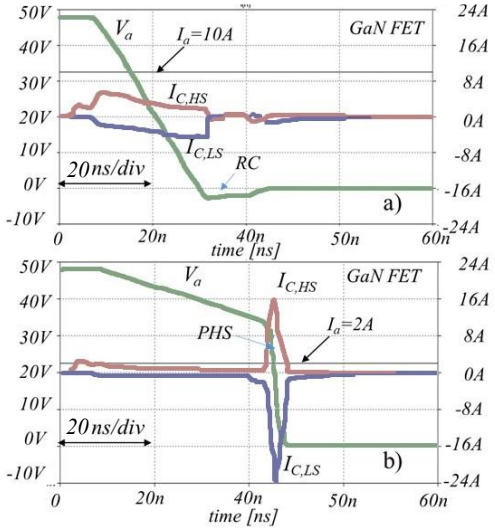

Fig. 7. Parasitic output current capacitances monitored on GaN FET during the LS switch turn-off and HS device turn-on commutation with I_a >0 and $dV_a/dt < 0$. a) Reverse conduction (RC) conditions. b) PHS event.

In conditions where the dead time is equal to or longer than the voltage fall duration, the energy exchange between the output parasitic capacitances of the switching leg transistors E_{VV} is maximum and equal to $E_{VV,ZVS}$. Vice versa, when the dead time elapses while the voltage variation is uncompleted, the energy exchange between the two parasitic capacitances E_{VV} is lower

than $E_{VV,ZVS}$. This is the case of the voltage waveforms obtained for a low current of 0.5 A when using the GaN FET in Fig. 3b. The GaN FETs, during the dead time set, at the growing of the current amplitude, work in the different operative conditions of PHS, ZVS, and RC. Fig. 8 shows the energy losses due to RC condition and PHS (E_{RC}+E_{PHS}) with t_{dt}= 20 ns (Fig. 8a) and t_{dt}= 150ns (Fig. 8a). In Fig. 8, the green dotted lines show the range of RC and PHS conditions, while the green dashed line highlights the ZVS event. Instead, the Si MOSFETs remain in PHS conditions for the current variation range (as highlighted by the dotted blue line of Fig. 8).

From Fig. 8 arises that PHS losses appear due to the LS turn-on with non-null V_{DS}. During this PHS, the LS device discharges all the remaining energy E_{PHS} almost instantaneously, causing a current peak. This is evident from the Fig. 8b current graph, which shows increasing PHS losses for currents lower than those of ZVS. The value of the PHS energies of the GaN are therefore due to the value of the non-exchanged energy:

$$E_{PHS} = E_{VV,ZVS} - E_{VV} \tag{8}$$

Comparing the energy losses during PHS of the GaN FET with the Si MOSFET shows that the GaN FET achieves lower energy losses in Fig. 8a as well as in Fig. 8b due to the shorter $t_{v\,fall}$ resulting from the GaN FET reduced C_{OSS} value.

Fig. 8a reveals that using t_{dt} = 20 ns, the GaN FET exhibits zero-voltage switching at a current of I_a = 6 A, whereas ZVS for the Si MOSFET occurs at currents higher than I_a = 10 A. Moreover, Fig. 8b shows that using t_{dt} = 150 ns, the GaN FET achieves ZVS with I_a = 0.8 A, while the Si MOSFET features ZVS at I_a = 1.5 A.

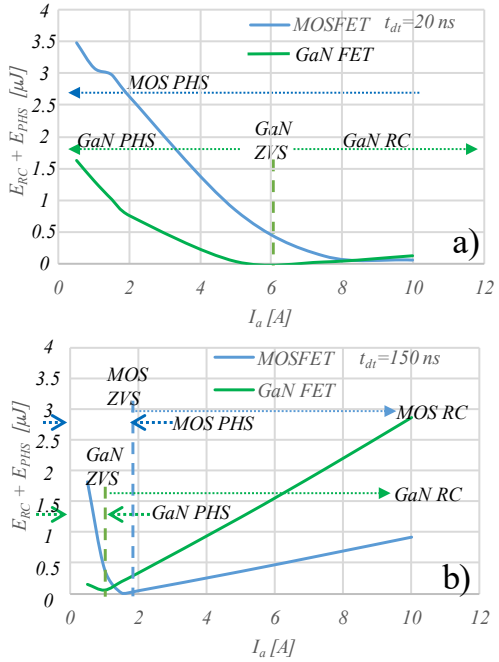

Fig. 8. Energies of LS device (Si MOSFET in blue and GaN FET in green) versus phase current I_a (with $I_a > 0$ A and $dV_a/dt < 0$). RC and PHS energies (E_{RC}+E_{PHS}) are considered. ZVS event is highlighted with a dashed line. PHS and RC zones are highlighted with dotted lines. a) t_{dt} = 20 ns. b) t_{dt} = 150 ns. (E = 0.5 μJ/div, I_a = 2 A/div)

When the current level exceeds the one required for ZVS, RC losses appear. On the contrary, losses due to the partial hard switching phenomenon occur when I_a is below the level causing ZVS.

As shown in Fig. 8a and Fig. 8b the ZVS is a switching event with zero energy losses and the E_{RC} obtained as:

$$E_{RC} = V_{rc} \cdot I_a \cdot t_{rc} \; with \; t_{rc} = t_{dt} - t_{vfall} \tag{9}$$

The RC conditions are slightly disadvantageous for the GaN FET in Fig. 8a, while showing a high disadvantage in Fig. 8b as the current increases due to the higher equivalent diode reverse voltage value of GaN technology than Si MOSFET [5], [10].

B. Energy losses investigation with $dV_a/dt>0$

The initial condition of the commutation with $dV_a/dt > 0$ is that the C_{OSS} of the LS switch is discharged while the HS switch is charged to V_{DC}. As the LS device turns off, the LS device immediately operates in reverse conduction until the HS switch turns on after t_{dt}. During t_{dt}, output parasitic capacitances (C_{OSS}) do not exchange energy. The hard switching condition follows t_{dt}, where the HS device switches with an applied drain-source voltage of $V_{DS,HS}$=V_{DC}+V_{rc} as achieved from Fig. 5b. The hard switching condition leads the energy stored in the C_{OSS} of the HS device to be dissipated. Additionally, the C_{OSS} of the LS switch is charged by the power supply. Therefore, the hard switching event results in an almost instantaneous current peak on LS and high switching losses. The hard switching energy loss E_{HSW} are calculated as:

$$E_{HSW} = \int_{t_{dt}}^{t_{dt}+t_{HSW}} |V_a \cdot I_{LS}| \cdot dt \tag{10}$$

where t_{HSW} is the time duration of the hard switching event.

This case study considers the energy losses E_{RC} during the RC condition contribution and the hard switching energy E_{HSW} during the HSW event. Fig. 9a and 9b show the energy losses E_{RC} at t_{dt}= 20ns and t_{dt}= 150n. The y-axis scale is the same in Fig. 9 to emphasize the differences in the reverse conduction losses for GaN FET and Si MOSFET at the different dead times considered.

The energy related to the RC zone (E_{RC}) increases proportionally with the I_a amplitude and the t_{dt} duration, according to (7). The comparison between the curves of GaN FET and Si MOSFET reveals that GaN FET E_{RC} curves are steeper and higher with increasing I_a than the Si MOSFET due to the higher V_{rc}. The results show that the increase of the t_{dt} is a drawback for GaN FET devices relative to E_{RC} losses.

The curves showing E_{HSW} as a function of I_a are depicted in Fig.10a and Fig.10b. The results in Fig. 10 show that the energy losses of the E_{HSW} of GaN FET are significantly lower than those of the Si MOSFET. The graphed curves follow different behaviours for the GaN FET and the Si MOSFET. In the GaN FET E_{HSW} is a constant value equal to $E_{HSW,min}$≈ 0.75 μJ. This loss value does not change with the I_a amplitude and the t_{dt} duration because it represents the energy stored in the discharging of the C_{OSS}, dissipating during the hard-switching event.

For higher I_a levels, Si MOSFET E_{HSW} increases with the I_a amplitude and the t_{dt} duration due to the higher reverse recovery charge Q_{rr} stored in the Si MOSFET P-N junction [5], [10], [25].

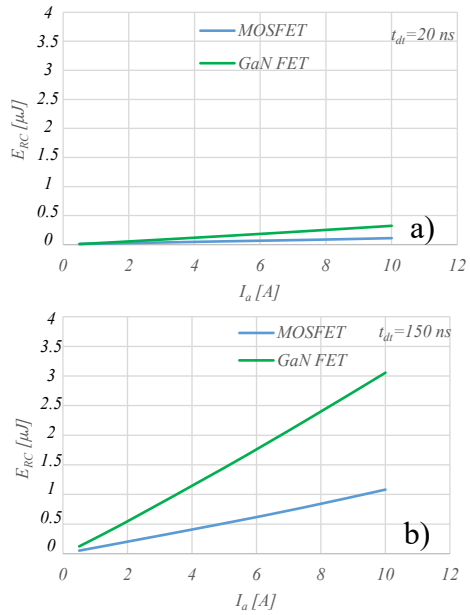

Fig. 9. Energies E_{RC} of LS device (SI MOSFET in blue and GaN FET in green) versus phase current I_a (with $I_a > 0$ A and $dV_a/dt > 0$). Reverse conduction energy E_{RC}. a) t_{dt} = 20 ns. b) t_{dt} = 150 ns. (E = 0.5 µJ/div. I_a = 2 A/div).

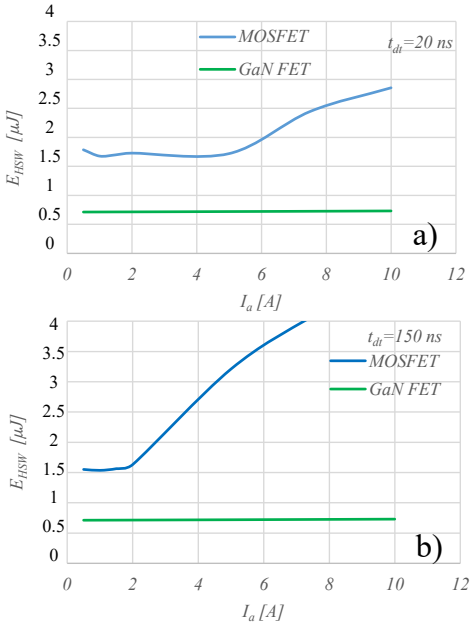

Fig. 10. Energies E_{HSW} of LS device (Si MOSFET in blue and GaN FET in green) versus phase current I_a (with $I_a > 0$ A and $dV_a/dt > 0$. a) t_{dt} = 20 ns, b) t_{dt} = 150 ns. (E = 0.5 µJ/div, I_a = 2 A/div)

IV. Dead Time Impact on the Devices Temperature

As shown in the previous paragraph, analyzing energy losses leads to some consideration of the correct dead time selection. This investigation can help reduce the switching losses and, consequently, lower the power components' operating temperature under the same operating conditions. This aspect can be verified experimentally by monitoring the temperature of the switching devices for various load currents and dead times. The functional schematic of the measurement setup is shown in Fig. 11. The two switching leg boards (i.e., half bridge GaN board and Si MOSFET board) shown in Fig. 1b are inserted alternatively in the measurement setup of Fig. 11 (i.e., board under test) to evaluate the different performance at different dead times with several current values. A programmable closed-loop current-controlled inverter operating at 10 kHz is used as an electronic load to regulate the GaN FET or Si MOSFET leg's output current. The converters are interfaced using an LCL filter, thus preventing interaction between their PWM current ripples. Both ferrite core filtering inductors are identical, with a nominal value of 300 µH, while the filter capacitor is 820 µF. The two converters shared a 48 V DC-link, meaning an external DC source only needed to supply system losses. In the proposed results, the board under test is operated in buck mode with positive output currents (i.e., exiting the switching node) and a constant 50% duty cycle. To ensure accurate current sharing between the two switches (HS and LS), the reference duty cycle is adjusted to account for the effect of dead time, so that both switches conduct for 50% of the switching period. In contrast, the load converter is closed-loop current-controlled, thus allowing to control the switching node current.

Due to the different switching losses of the two semiconductor technologies, the tests are performed using two distinct switching frequencies: 500 kHz for the GaN FETs and 200 kHz for the Si MOSFETs. The current ripple obtained at the output of the switching leg is sufficiently small to be neglected for both cases, allowing for the assumption of a constant output current. During the test at different dead times and load currents, the case temperature of the two transistors of the switching leg was monitored using an IR camera.

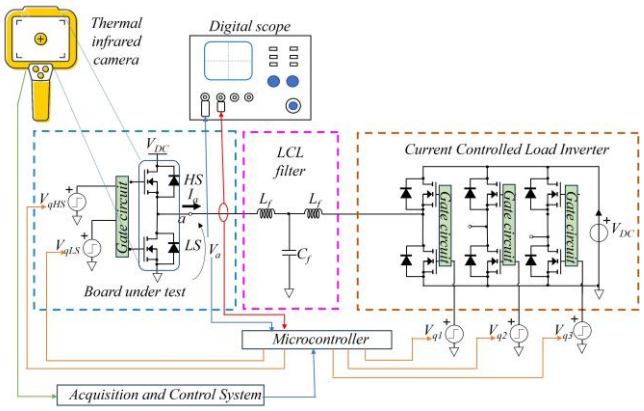

Fig. 11. The functional schematic of the measurement setup diagram of the experimental setup for the thermal measurements.

Each test condition, defined by a specific load current and dead time, was maintained for 10 minutes to allow thermal transients to settle, after which the maximum case temperature was recorded. Although the measurement procedure aimed to distinguish the temperatures of the high-side ($T_{C,HS}$) and low-side ($T_{C,LS}$) devices, the close physical proximity between the two led to significant thermal coupling. Therefore, the hotspot temperature was used in

the proposed analysis. An example of the IR camera results for the GaN FET switching leg is shown in Fig. 12.

The experimental results showing the maximum recorded temperature as a function of the dead time for different load currents are reported in Fig. 13a (GaN FETs) and Fig. 13b (Si MOSFETs). For each current level, the temperatures have been normalized with respect to the minimum recorded hotspot temperature at that current (e.g., the temperature at 2 A is normalized by the lowest value measured at 2 A). This normalization is essential because, at higher output currents, the absolute working temperature of the switching device naturally rises, which would otherwise obscure the relative impact of dead time on losses. For example, in the GaN FET tests, the normalization reference temperature was set at 57.5 °C for a load current of 2 A, while at 10 A the normalization temperature was 80.3 °C.

Notably, an optimal dead time was identified for each output current, defined as the value that minimizes the hottest switch's case temperature.

The optimal dead time for GaN FETS varies from tens of nanoseconds at low currents to less than 10 ns at high currents, reaching a minimum of 6 ns when the output current exceeds 10 A. This phenomenon is attributed to the differing slope of V_a with the current. The observed trend indicates that for conditions where current exits the switching node and dV_a/dt is positive, the optimal dead time converges to the zero-voltage switching point [26]. This is because it represents the optimal balance between hard switching losses and reverse conduction losses, thereby minimizing overall switching losses.

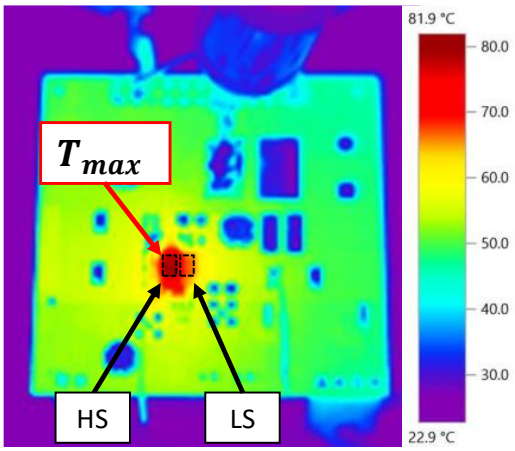

Fig. 12. High and Low side GaN FETs thermal image @I_a=10 A.

A comparison between the GaN FET and Si MOSFET curves in Fig. 13 yields the following observations:

1. For the same output current, GaN FETs achieve the minimum case temperature at a shorter dead time than Si MOSFETs, due to their lower output parasitic capacitance.
2. The temperature variation with respect to dead time is steeper for GaN FETs, which can be attributed to their inferior reverse conduction characteristics. Specifically, the effective diode losses in GaN devices are higher than those of the intrinsic body diode in Si MOSFETs.
3. Lowering the dead time below a certain threshold causes additional losses due to the cross-conduction between the devices.

In case of low I_a values, using a reasonably long t_{dt} causes PHS results in acceptable values of $T_{C,LS}$. For instance, using t_{dt} = 50 ns for $I_a \leq 1A$ leads to $T_{C,LS} < 60\,^{\circ}C$. These results suggest to limit t_{dt} at a maximum $t_{dt,max}$ in operating conditions (e.g. $t_{dt,max}$ = 50 ns). The graph showing the optimal dead time $t_{dt,opt}$ for LS turn on as a function of $I_a > 0A$ is obtained by interpolating the results described in Fig.13. Therefore, the experimental results presented in Fig. 13 are summarized in Fig. 14, which shows the optimal dead time as a function of output current for both GaN FETs and Si MOSFETs. As anticipated from both theoretical considerations and simulation, the Si MOSFET consistently requires a longer minimum dead time at a given a load current when compared to the GaN FET.

At low current levels, the optimal dead time for the Si MOSFET is noticeably higher, primarily due to its larger parasitic output capacitances. Even though the PCB layout of the two boards have minimal differences, the MOSFET itself contributes the majority of parasitics, outweighing board effects. Consequently, more time is needed to safely complete commutation and avoid cross-conduction losses. At higher currents, the minimum achievable dead time for the Si MOSFET remains greater than that for the GaN FET, but the primary reason shifts: the inherent lower switching speed of the Si technology mandates a longer dead time period. In contrast, the GaN FET, with its fast switching capability and lower parasitic capacitance, allows for substantially shorter and more efficient dead times throughout the full current range.

Looking at Fig.14 for GaN FETs arises that $t_{dt,opt}$ is shorter as I_a increases. Furthermore, $t_{dt,opt}$ stabilizes to a minimum value of $t_{dt,opt}$ = 7 ns for $I_a > 7A$.

From this comparison, it is evident that selecting a short dead time is particularly advantageous for GaN FETs. Doing so not only reduces switching losses but also contributes to improved output waveform quality [13].

V. Conclusion

This paper presents a comprehensive investigation of commutation transients in Si MOSFET and GaN FET devices within inverter switching legs, considering both hard- and soft-switching conditions. Experimental measurements on matched half-bridge boards, supported by SPICE simulations, reveal distinct differences in switching behavior, reverse conduction, and energy dissipation between the two technologies.

Despite a higher reverse-conduction voltage drop during dead time, GaN FETs achieve considerably lower overall losses at shorter dead times compared to Si MOSFETs, thanks to their reduced output parasitic capacitance and faster switching transitions. The analysis shows that even small deviations from the optimal dead time lead to pronounced increases in losses, as confirmed by the thermal results in Fig. 13a. Consequently, precise dead-time selection is especially critical in GaN-based designs: the optimal setting not only maximizes efficiency but also minimizes output-voltage distortion and improves waveform fidelity.

To facilitate this, a thermal analysis methodology has been proposed and experimentally validated to identify the optimal dead time that minimizes device temperature. These findings provide a practical, quantitative framework for dead-time optimization in low-voltage motor-drive inverters and underscore the importance of accurate, load-dependent tuning when employing GaN technology.

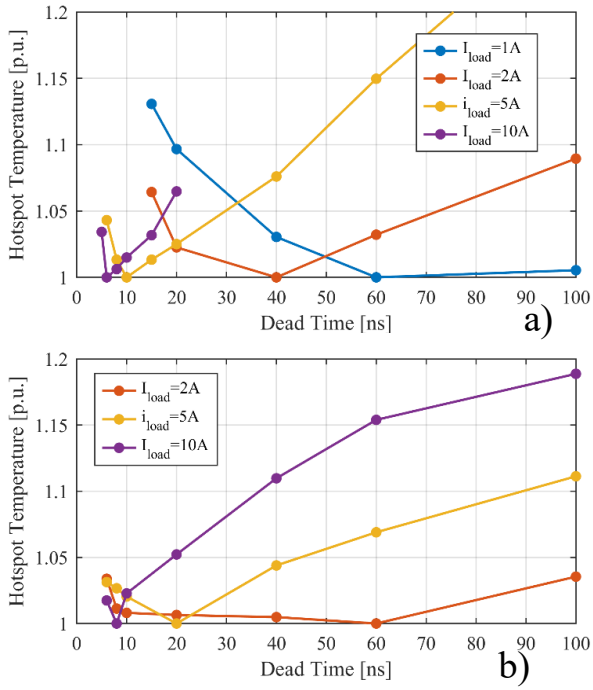

Fig. 13. Measured hotspot temperature as a function of the dead time for different load currents. Results are normalized to the minimum measured temperature for each I_a a) GaN FET. b) Si MOSFET

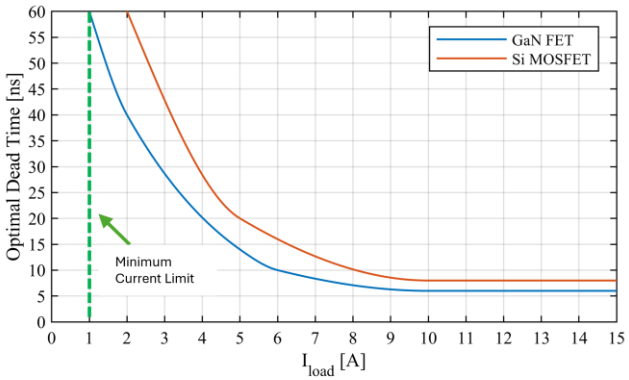

Fig. 14. Optimal dead time $t_{dt,opt}$ for LS turn on as a function of $I_a > 0$ A obtained via thermal analysis for GaN FET and Si MOSFET.

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S. MUSUMECI (M’18). He received his M.Sc. and Ph.D. degrees in electrical engineering from the University of Catania, Catania, Italy, in 1991 and 1995, respectively. From 1996 to 2001, he was with the R&D Department, ST Microelectronics Catania, Italy, as an Application Engineer on power device applications. From 2001 to 2017, he was involved in several research collaborations with the Department of Electrical Electronic and Systems Engineering, University of Catania, Catania, Italy. Since 2018 he has carried out research activity at the Energy Department "Galileo Ferraris" of Politecnico di Torino, Torino, Italy, in the field of Power Electronics, Electrical Machines, and Drives. Currently, he is an Associate Professor. Furthermore, he is involved in the Power Electronics Innovation Center (PEIC), a competence center of the Politecnico di Torino focused on power electronics. His research interests include advanced power devices, switching power converter applications, high-efficiency industrial motors, magnetic materials and their applications, battery management systems, and automotive power electronic applications.



F. STELLA (M’18) is a research fellow at Politecnico di Torino, Turin, Italy. He received the Bachelors and Masters degrees both in Electrical Engineering from the same university in 2012 and 2015, respectively. In 2017 he was a visiting PhD student at the University of Nottingham, UK and in 2019 he received his PhD degree from the Politecnico di Torino. He is currently an assistant professor at the Politecnico di Torino. His research interests include the design of power electronic converters, focusing on SiC semiconductors and reliability issues, and the control of converters via embedded systems.



V. BARBA (S’ 20) received the M.Sc. degree in electrical engineering from Politecnico di Torino, Italy, in 2021. He is currently a Ph.D. student at Politecnico di Torino. He is involved in the Power Electronics Innovation Center (PEIC) at the Politecnico di Torino. The topic of his research is the use of Gallium Nitrite FET in power converter, especially when they are used in motor drive applications.



F. MANDRILE (S’18, M’21) received the M.Sc. and Ph.D. degrees in electrical engineering from Politecnico di Torino, Italy, in 2017 and 2021, respectively. He is currently assistant professor at Dipartimento Energia ”G. Ferraris” at Politecnico di Torino. His main research interests are virtual synchronous machines and power electronics for grid-connected applications, on which he focused his Ph.D. and current research activity.



M. PALMA (M’23, SM’24) received his M.Sc. degree in Electronic Engineering from Politecnico di Torino and his Master of Business Administration (M.B.A.) from Bocconi Management School, Milano. He worked in International Rectifier and after in Infineon as an application Engineer in the field of integrated motor drive modules. He joined EPC in 2019, where is Director of motor drives systems and applications. He has over 20 years of experience in motor control power electronics ranging from switches to gate drivers, controllers, and algorithms. He is the author of several articles and patents in the field of power electronics applications and motor control.