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Transient current sharing in parallel GaN FETs: The role of parasitic capacitances

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ABSTRACT

This paper examines the impact of parasitic capacitances on the dynamic current sharing behaviour of Gallium Nitride (GaN) field-effect transistors (FETs) operating in parallel configurations. As GaN technology continues to gain prominence in high-performance power electronic systems, paralleling multiple devices has become a common strategy to increase current-handling capability. However, non-idealities such as parasitic elements introduce significant challenges in achieving balanced current distribution during switching transients. To examine these effects, a custom-designed experimental platform was developed, enabling independent gate control and current measurement for each GaN FET via dedicated source shunt resistors. The test setup facilitates the precise characterisation of transient behavior and allows for detailed analysis under controlled conditions. Complementary simulation studies were conducted to support the experimental results and to identify key parameters influencing transient current mismatch. The paper highlights the critical role of parasitic capacitances—both device-internal and layout-induced—in shaping the peak transient current distribution among parallel devices during turn-on events. A methodology is proposed to estimate the maximum allowable parasitic capacitance that ensures the peak pulse current remains within the safe operating limits specified by device manufacturers. This insight is essential for the robust design of multi-device GaN switching assemblies, where overcurrent during transients can compromise long-term reliability or lead to failure. The outcomes of this research provide practical design guidelines for optimising parallel GaN switch configurations, with particular attention to parasitic management, driver strategy, and layout considerations. These contributions support the development of reliable and high-efficiency GaN-based power modules for advanced power conversion applications.

1. Introduction

The adoption of high-electron-mobility transistors (HEMTs), particularly gallium nitride (GaN) field-effect transistors (FETs), is rapidly increasing in the field of power electronics. This trend is largely attributed to the superior electrical characteristics of GaN devices compared to conventional silicon (Si) transistors, especially in low-voltage applications below 100 V, as reported by Zhong (2022) and Moradpour (2019). GaN FETs offer several notable advantages, including higher switching frequencies, reduced conduction and switching losses, and improved thermal performance, making them highly suitable for advanced power conversion systems, as discussed by Avila (2018).

To meet the high current demands of modern applications—such as inverters for mild hybrid electric vehicles (MHEVs) or electrical drives for drones and humanoid robots, as well as DC-DC converters used in battery energy storage systems, parallel operation of GaN devices is commonly employed, as discussed in Scrimizzi (2022) and Moradpour (2019). Although this approach increases the overall current handling capability, it introduces challenges related to current imbalance among the paralleled devices. Such imbalances occur during both switching transients and steady-state conduction and are primarily caused by mismatches in intrinsic device parameters like threshold voltage (V_{th}), transconductance (g_m), junction temperature (T_J), intrinsic gate resistance, and parasitic capacitances, as demonstrated in Barba (2023).

In addition to device-level nonuniformities, extrinsic factors—such as variations in gate driver resistance and PCB-induced parasitic

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inductances—significantly contribute to dynamic current mismatch. These factors increase design complexity and necessitate comprehensive analysis to ensure functional reliability and optimal performance in parallel GaN FET configurations, as discussed by Zhang (2022).

This paper investigates the dynamic current-sharing behavior in paralleled low-voltage GaN FETs, with particular emphasis on the influence of parasitic elements—specifically, the combined effects of parasitic capacitances and inductances—during switching events. To support this investigation, a custom-designed evaluation board has been developed to replicate realistic operating conditions and enable controlled testing of device-to-device interactions. A dedicated testing methodology is proposed to isolate and independently evaluate the contributions of parasitic capacitances and stray inductances to transient current mismatches, with a specific focus on identifying the conditions that lead to peak transient drain currents at turn-on. Maintaining these transient peaks within the safe operating limits specified by device manufacturers is crucial to preventing long-term degradation or failure of individual devices.

Beyond this general analysis, the work provides two specific contributions that differentiate it from existing GaN parallel-device studies, as shown, for example, in Ramachandran (2016). First, this paper introduces a new multi-device experimental test board and measurement methodology specifically designed to isolate and quantify current-sharing mechanisms in parallel GaN FETs. The evaluation board (until 12 GaN FETs in parallel connection) includes independent gate drivers, per-device current sensing placed outside the gate loop. A PCB stack-up is intentionally designed such that the load inductance is significantly higher than the stray inductances of the GaN FET drain paths. This architecture enables controlled emulation of parametric mismatches and accurate measurement of individual transient and circulating currents, providing capabilities beyond those of conventional parallel test boards and improving the characterization of current-sharing mechanisms during transient operation. Second, this paper proposes a methodology that enables practical decoupling of inductive load-current dynamics from parasitic capacitive currents during turn-on. By enforcing a very low di/dt through the intentional design of the common inductance path, the measured turn-on current peak becomes dominated by the discharge of parasitic capacitances, thereby allowing the capacitive contribution to be experimentally isolated and characterized independently of the load current.

Furthermore, this paper evaluates the layout-dependent parasitic capacitances of the developed hardware platform. The resulting model enables more realistic LTspice simulations and support the prediction of maximum turn-on transient currents. The proposed methodology is applicable to other board architectures used in industrial applications, allowing estimation of layout-induced parasitic capacitances in parallel-device configurations. Overall, the insights obtained provide a deeper understanding of the mechanisms governing dynamic current distribution in parallel GaN implementations and offer practical guidance for mitigating current mismatch through informed gate-driver design, appropriate device parameter selection, and optimized PCB layout.

2. The impact of GaN FET parameters on parallel connection

Considering paralleled connected devices, the steady-state current distribution is governed by the on-state resistance R_{DSon}, which exhibits a positive temperature coefficient, as observed in MOSFETs and described in Lidow (2020). Another key electrical parameter influencing current sharing among devices is the transconductance g_m, which decreases with temperature, thereby improving the current sharing capability under static conditions. Additionally, differences in the junction temperature (T_J) influence the conduction current share. For good thermal balance, all GaN FET devices in parallel connection should feature similar thermal resistance and be installed on the same heatsink. The dynamic current variation, on the other hand, is primarily affected by mismatches in various device parameters. This can be exemplified by the drain current (I_D) variation in a single device, which can be described by the following equation:

$$\frac{dI_D}{dt} \approx \frac{g_m \cdot I_G}{C_{iss}} \approx \frac{g_m \cdot (V_{gg} - V_{Miller})}{C_{iss} \cdot R_G} \tag{1}$$

Where V_{gg} represents the gate-driver supply voltage, C_{iss} is the input capacitance of the GaN FET, R_G is the gate resistance, and V_{Miller} is the plateau voltage level of the gate, which is given by:

$$V_{Miller} = V_{GSth} - \frac{I_D}{g_m} \tag{2}$$

Equations (1) and (2) are used primarily for MOSFET devices switching modelling and are not accurate for precise transient simulation of GaN transistors, but, in this investigation, they are used as first-order small-signal approximations to illustrate the sensitivity of dynamic current imbalance to g_m, C_{iss}, and V_{th} device parameters. Although e-mode GaN HEMTs exhibit nonlinear charge behaviour and may not show a sharp Miller plateau, their effective small-signal parameters enable these relations to remain valid for comparative analysis and their impact in parallel connection analysis. Therefore, these equations are not intended to provide full GaN transient modelling, but to highlight parametric mismatch effects.

Additionally, the gate circuit parameters, such as the gate resistance (R_G) and V_{gg}, also play a significant role in determining the slope of the drain current, and consequently, the peak current attained during switching as published in Chou (2014). Furthermore, the parasitic inductances connected at the gate L_g, drain L_d and source L_s of the GaN FET inserted in a power converter circuit impact on the dynamics. In Table 1, the different effects of the main electrical parameters and parasitic spread involved in the current imbalance in the parallel connection of the GaN FET are reported and described. For both GaN FETs and MOSFETs, the threshold voltage (V_{th}) is a critical parameter that governs the behaviour of turn-on and turn-off transients, influencing both the current slope and peak in parallel configurations as considered in Lidow (2020). Notably, in GaN FETs, the threshold voltage remains relatively stable for junction temperature, as illustrated in Fig. 1.

3. Testing methodology

The methodology adopted for analysing the contribution of parasitic capacitances is grounded in a tailored gate control strategy, which employs a programmable gate delay signal for independent switching of each GaN device. To support this investigation, a dedicated experimental board was developed, capable of operating up to twelve low-voltage GaN FETs (specifically, EPC2302 devices - source Efficient Power Conversion – EPC), rated at $V_{DS,max} = 100$ V, $I_D = 101$ A at 25 °C,

Table 1
Effects of GaN FET parametric spread and parasitic differences between GaN FETs connected in parallel.

Parameter	Symbol	Effect
Conduction resistance	R_{DSon}	Current mismatch during conduction
Transconductance gain	g_m	Higher conduction current, Peaks at both switching events
Output parasitic capacitance	C_{OSS}	Distinct current peaks during switching
Gate charge	Q_G	Distinct current peaks during switching
Threshold voltage	V_{th}	Higher conduction current and current peaks during switching in one GaN FET
Source parasitic inductance	L_s	Slower commutation Current peaks Voltage oscillations
Drain parasitic inductance	L_d	Current and V_{DS} oscillations at turn-off
Gate parasitic inductance	L_g	Current peaks at turn-on Current and voltage oscillations at turn-off

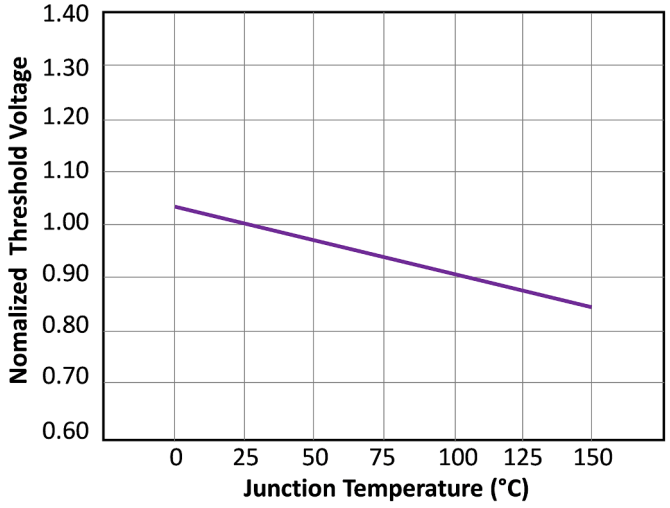


Fig. 1. GaN FET threshold voltage as a function of the junction temperature (for the device EPC 2302, @ I_D = 11 mA, V_{th}=2.5 V max).

with a pulse current rating of $I_{D,pulse}$ = 408 A for 300 μs at 25 °C) in parallel. Each transistor is driven by an individual gate driver circuit, allowing precise timing of switching events. The tests are carried out at room temperature.

The board enables current monitoring for each GaN FET through individual source-side shunt resistors, providing high-resolution data for transient analysis. Experimental testing was conducted under conditions representative of high-switching frequency (f_{sw} = 100 kHz), using an inductive load (L_{load} = 90 nH) and a super-fast freewheeling diode, as depicted in the schematic diagram of Fig. 2. The duty cycle in the test is fixed to 0.5. A high switching frequency is used with multiple pulse tests, and a duty cycle of 0.5 is required to stabilise the voltages after each transient. The multiple-pulse test described in Barba (2024) involves N pulses at various current points until the target current is reached. A short operating time is used for the test, thus maintaining a constant device temperature. The source current can be evaluated through a suitable resistive shunt for each device. The capacitors $C_{OSS} = C_{DS} + C_{GD}$ are the nonlinear output capacitances of every single GaN FET. In the schematic of Fig.2, the contribution of the Printed Circuit Board (PCB) layout parasitic capacitances is modelled by an equivalent capacitor called C_{PCB}.

Within the presented test methodology, L_{diode} represents the parasitic inductance of the diode (L_{diode} = 20 nH). L_d features the inductance of the interconnections between the GaN FETs, estimated at 2.7 nH. L_D is the inductance due to the board drain track in the PCB and is common to each device, designed to be 20 times greater than L_d. This design choice enables observation of the inductive load current's turn-on contribution and the discharge currents of global parasitic capacitances during the transient current peak. To comprehensively analyse this procedure, turn-on simulations were conducted in LTSpice using a developed GaN FET model validated in Palma (2023) and Barba (2024). These simulations considered an arrangement of eight parallel-connected devices (n = 8). A single GaN FET (GaN1) was activated while the remaining seven devices remained in the off-state, representing the worst-case scenario for current flow through the active device. The simulations were repeated across a range of $L_{diode} + L_D$ values (0.1 %, 1 %, 10 %, 50 %, and 100 %) relative to the actual PCB design's equivalent value. To isolate GaN FET transient performance and simplify the simulation, an ideal LTSpice diode was used in antiparallel with the load inductance, thereby avoiding oscillations caused by real diode parasitic components.

In Fig. 3a, the upper panel depicts the simulated waveforms for the board drain-source voltage (V_{DS}), load current (I_{load}), and board drain current (I_D). Concurrently, the lower panel of Fig. 3b provides the current waveforms for GaN FET1 (I_{SGaN1}) and GaN FETn (I_{SGaNn}). The prominent current peak in I_{SGaN1} (Fig. 3b) arises from the rapid fall in V_{DS} at GaN FET1 turn-on, interacting with the associated parallel parasitic capacitances, as detailed in Fig. 2.

A key observation is that the magnitude of the switching current peak is strongly influenced by the di/dt of the load current. Specifically, as the total series inductance, including the load inductance and the diode's intrinsic inductance (L_D + L_{diode}), increases, the slope of the current rise decreases. Under these conditions, the peak current

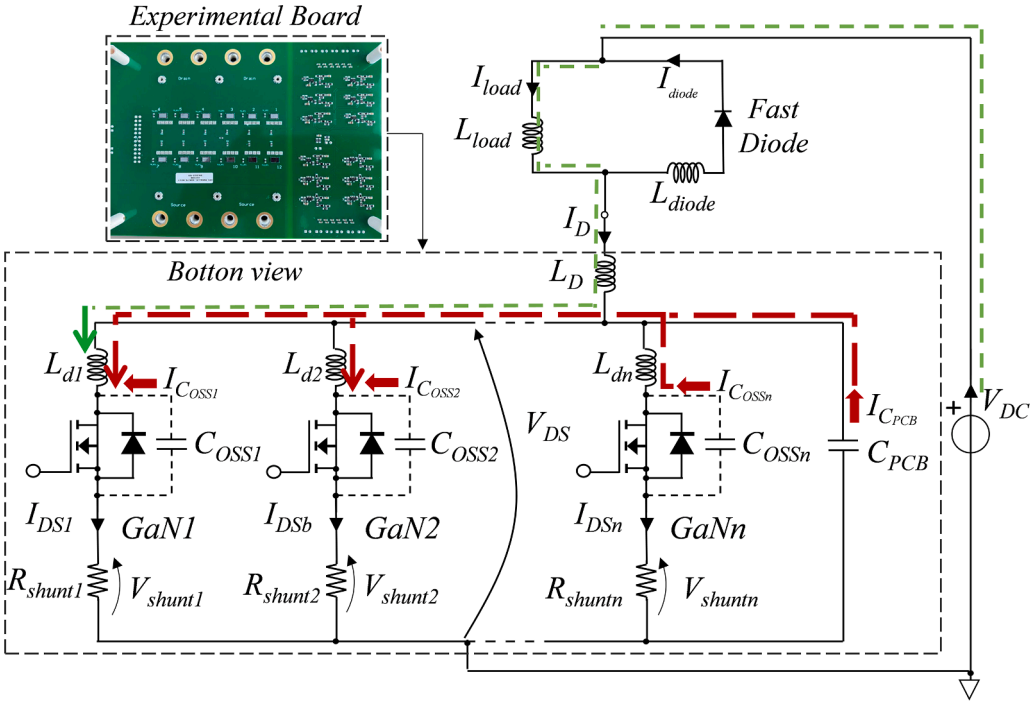


Fig. 2. Electrical schematic of the system used for the test with the equivalent electrical model of the board with GaN FETs connected in parallel.

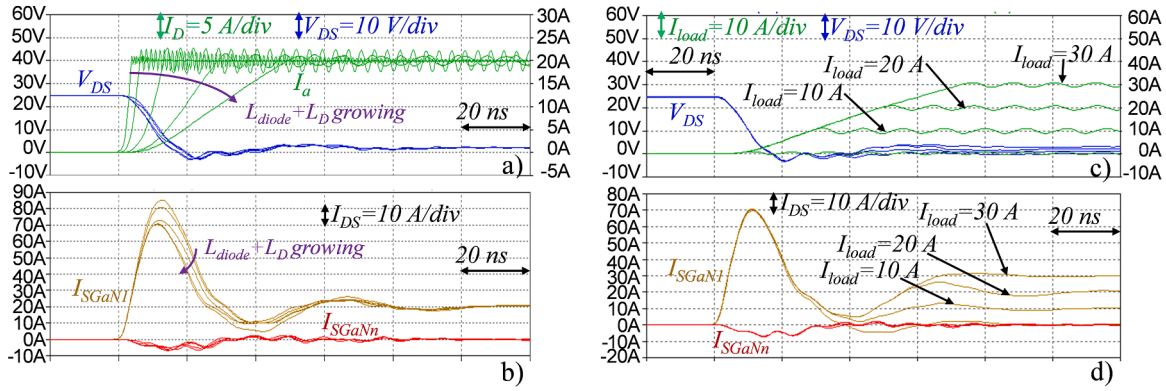


Fig. 3. Simulation results a) Turn-on transient at I_D = 20 A, for different L_D + L_{diode}: 0.1 %, 1 %, 10 %, 50 % and 100 % of the actual drain inductance (L_D +L_{diode} = 50 μH). Only GaN FET1 is turned on. Waveforms of V_{DS}, I_D, b) simulation results of I_{SGaN1}, and I_{SGaNn}. c) Turn on GaN FET1 at different I_{load} currents at low di/dt. d) Simulation results related to I_{SGaN1} and I_{SGaNn}. As shown the I_{SGaN1} peak is the same at different I_{load} values. Time = 20 ns/div.

observed at turn-on becomes increasingly dominated by the discharge of parasitic capacitances. To understand this switching mechanism, in Fig. 3c, the load current (I_{load} from Fig. 2) is varied from 10 to 30 A, maintaining the same lower slope (di/dt). The current peak phenomenon is illustrated in Fig. 3d, where the peak source current of a single device (I_{SGaN1}) remains constant across variations in load current amplitude, indicating that the observed peak is no longer determined by the inductive load but primarily by capacitive discharge.

This decoupling of effects between drain inductance and parasitic capacitance provides a critical insight: in the presence of sufficiently large drain inductances, the current peak attributable to capacitive discharge can be isolated and quantified independently from the load current amplitude. This result enables the estimation of the peak transient current induced by the parasitic capacitances of the paralleled GaN devices. Consequently, it becomes possible to investigate the mechanisms governing turn-on current sharing, particularly the role played by capacitive mismatches in transient imbalance.

The current peak ($I_{Ctot,peak}$) due to the parasitic capacitances of the N GaN used (see Fig. 2) can be estimated as

$$I_{Ctot\ peak} = C_{tot}.\frac{V_{DS}}{\Delta t} = (C_{PCB} + N_{GaN}.C_{OSS}).\frac{V_{DS}}{\Delta t} \quad (3)$$

With this fundamental achievement, it is possible to utilise the appropriate layout that permits investigation of the turn-on current sharing due to the effect of parasitic capacitances with several power devices in parallel connection at different gate drive conditions.

3.1. The experimental test board for the parallel connection operation

The developed parallel GaN FETs test board for a high-current switch is composed up to 12 parallel connected GaN FETs (GaN FET EPC2302) distributed in two rows used as a workbench for the experimental evaluation is shown in Fig. 4. The board features two driver options a common PWM gate driver for all devices and a single gate driver for each GaN FET. A shunt resistor R_{shunt} = 0.1 Ω is placed in the source path of each device, out of the gate loop, it is used for the device current measurement. The gate driver uP1966E drives GaN FET as a high-side device in order to reduce noise caused by the shunt resistors R_{shunt} of the gate power loop. The tests are carried out considering the paralleled devices, supplying an inductive load (L_{load} = 100 μH) and a voltage V_{DS}

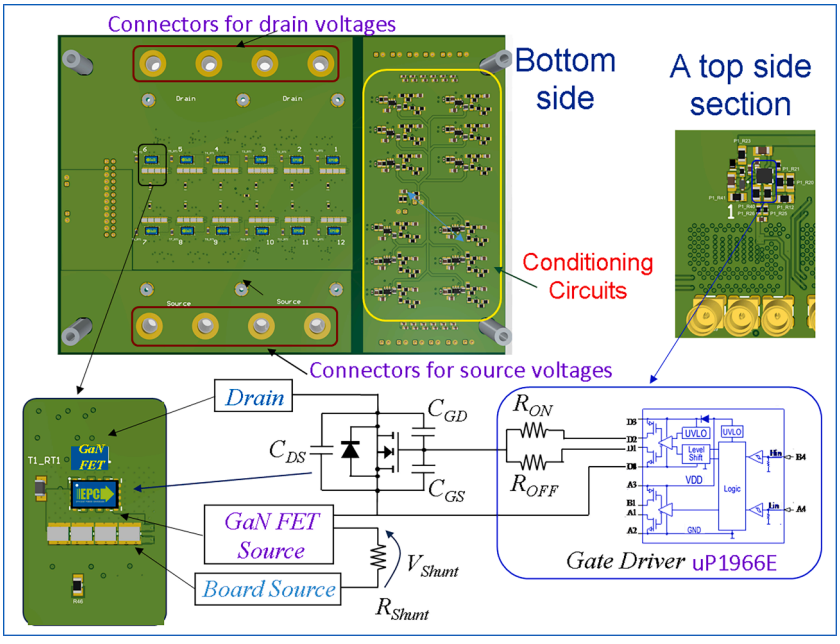


Fig. 4. Test board for GaN FETs in parallel connection.

= 24 V with a freewheeling super-fast diode (APT40DQ60BG).

The pictures with a description of the power and signal circuit of the experimental board are depicted in Fig. 5. In Fig. 5a, the top view is reported, while in Fig. 5b, the bottom view is shown.

3.2. The PCB equivalent capacitance evaluation procedure

The C_{PCB} is the equivalent capacitance related to the layout of the presented circuit board. The manufactured board considered consists of 14 internal layers with a thickness of 2 oz. Each layer is electrically connected to one net between the GaN FETs' drains, GaN FETs' sources or the board's sources, in an alternating sequence. In Fig. 6a, the parasitic capacitances model adopted for the actual experimental board schematic is described. The overall area of the board is $A = 135\ cm^2$. Consequently, the equivalent capacitance C_{xy} between two layers connected to different nets of the board, x and y can be calculated as

$$C_{xy} = \frac{A}{\epsilon_0 \cdot \epsilon_r \cdot D_{xy}} \tag{4}$$

From Fig. 6a, D_{xy} is the distance between the layers' x and y minus the thickness of the layer conductors as described in Lidow (2020). For the drain (D), device source (FS) and board source (BS) layers. Between the device source and the board source there is the shunt resistance (the gate driver circuit is referred to the device source as described in Fig. 4. The distance D_{xy} is different when considering the case with layer x immediately below layer y (consecutive), or the case where layer x and layer y present a third layer of a different net in the between (non-consecutive) as shown in Fig. 6a.

Furthermore, the copper layer thickness CL_{th} related to the proposed board is highlighted in Fig. 6a. In Fig. 6b the equivalent reduced board layer model (equivalent three layers' parasitic capacitances) is depicted. In the equivalent three layers, the parasitic capacitances are highlighted, in particular, the consecutive layers' capacitances are:

- C_{SS} (between BS and FS),
- $C_{FS,D}$ (between FS and D),

While $C_{BS,D}$ (between BS and D) is a parasitic capacitance between two non-consecutive layers. Finally, the equivalent schematic circuit of the GaN FET with the shunt resistor and parasitic capacitances linked to the different PCB layers is described in Fig. 6c.

From Fig. 6a and Fig. 6b, the consecutive capacitance layers $C_{BS,FS}$ are computed by 5, while the $C_{FS,D}$ is calculated by 6, and the parasitic capacitance between two non-consecutive layers $C_{BS,D}$ is featured by 7.

$$C_{BS,FS} = C_{6,8} + C_{8,9} + C_{9,11} + C_{11,12} + C_{4,5} + C_{5,6} \tag{5}$$

$$C_{FS,D} = C_{7,9} + C_{9,10} + C_{10,12} + C_{12,13} + C_{12,14} + C_{6,7} \tag{6}$$

$$C_{BS,D} = C_{8,10} + C_{10,11} + C_{11,13} + C_{11,14} + C_{5,7} + C_{7,8} \tag{7}$$

Considering consecutive layers, the distance is $D_{xy} = 0.13$ mm and results in $C_{xy} = 3.415$ nF, while $D_{yz} = 0.365$ mm and $C_{xy} = 1.216$ nF are obtained for non-consecutive layers (see Fig. 6a). The main parameters for the computation of the parasitic capacitances are reported in Table 2. Capacitances connected between the same two layers (drain-device source D,FS; drain-board source D,BS; device-source-board source FS, BS) are connected in parallel.

The equivalent capacitances between the different layers are: $C_{FS,BS} = 16.1$ nF; $C_{D,FS} = 13.9$ nF; $C_{D,BS} = 11.2$ nF.

For the paralleled GaN FETs, the fixed copper areas of each GaN transistor are equal. That is, the areas of each drain and each source, and the distance between the two layers, are equal, so the calculation of the parasitic capacitances is the same for each device and is not influenced by the slightly different power loops.

The validation of the equivalent parasitic capacitance calculation was performed by comparing the capacitance measured with a capacitance meter and the board unpowered (static condition). Considering all the capacitances shown in Fig. 6c and Fig. 6d, an error of around 15 % between measured and estimated values was found, which is quite satisfactory, considering the complexity of the layout system. The capacitance values carried out are used in the LTspice simulation results to validate the mechanism of the turn-on transient's current peak considering the effects of both the devices output capacitances and the layout equivalent capacitance.

From the layout rules, for a better layout arrangement to mitigate parasitic capacitance in PCB design, it is essential to avoid overlapping areas of differing voltage potentials across layers and to prevent vertical alignment of such regions. A layer partitioning strategy, where regions with the same potential are aligned vertically, is recommended to reduce equivalent PCB capacitances.

4. Parasitic capacitances impact at turn-on switching transients

In the experimental test carried out, eight GaN FETs were connected in parallel. The devices were deliberately chosen completely randomly.

The test circuit of Fig. 2 is considered to implement a switching commutation pole with a freewheeling super-fast diode in antiparallel to the load inductance. In the switching tests, the number of devices considered for the parallel connection influences the equivalent capacitance C_{oss} involved in the switching transients (as described in Fig.2).

To isolate the impact of equivalent capacitance, a test was conducted utilising two actively driven GaN FETs among eight total devices, with the remaining six switches in the turn-off state. These six inactive devices contribute to the current transient via their output capacitances' charge. The objective of this test was to demonstrate the influence of parallel parasitic capacitances, driven with a time mismatch, on the GaN

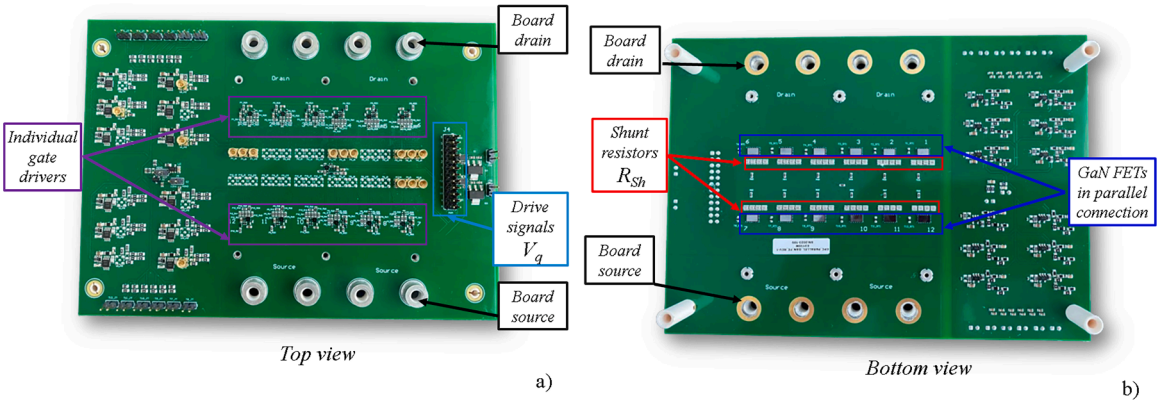


Fig. 5. Pictures of the test board for GaN FETs in parallel connection: a) top view. b) bottom view.

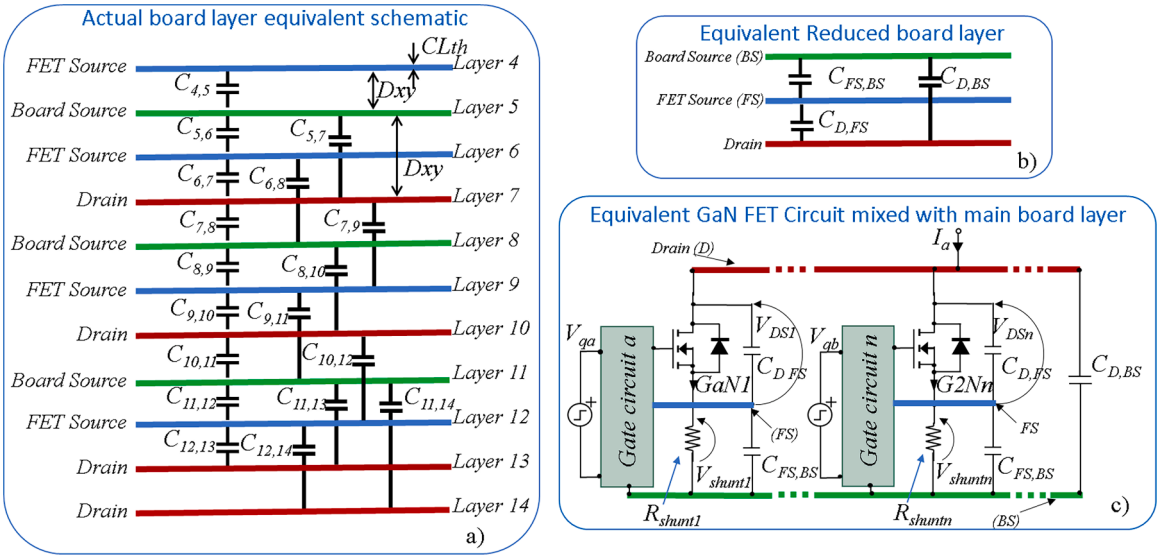


Fig. 6. Parasitic capacitances schematic model of the experimental test board. a) board layer arrangement. b) Equivalent reduced board layer. c) Equivalent GaN FET parallel circuit with the main board layer connections.

Table 2
Main layout parameters for calculation of parasitic capacitances.

Parameter	Symbol	Value	Unit
Vacuum permittivity	ε_0	$8.8542 \cdot 10^{-12}$	F/m
Relative dielectric permittivity	ε_r	3.7	
Copper thickness	CL_{th}	0.105	mm
Dielectric thickness (consecutive layer)	D_{xy}	0.13	mm
Total board surface	*Atot*	135,600	mm^2
Individual GaN FET source area	*AGaN*	11,300	mm^2

FET transient current. This time mismatch emulates the effects of varying gate loop inductance or the spread of dynamic parameters, such as threshold voltage, as discussed in Koch (2021), and the different parasitics of PCB tracks.

In the experimental setup, this delay was achieved by adjusting the driving signals, V_q. All switching tests were performed at an ambient temperature of 27 °C with a load voltage (V_{Load}) of 24 V. To better evaluate these effects, the drive signal delay was sought through the driver circuits such that the devices under test would turn on simultaneously. Once synchronisation was achieved (corresponding to compensating for parametric dispersion and layout effects), an additional delay was added between the turn-on of the first device and the second one to emulate the parametric dispersion and parasitic effects impact in the turn-on current peak.

Fig.7a shows the electrical schematic related to GaN1 and GaN2 in

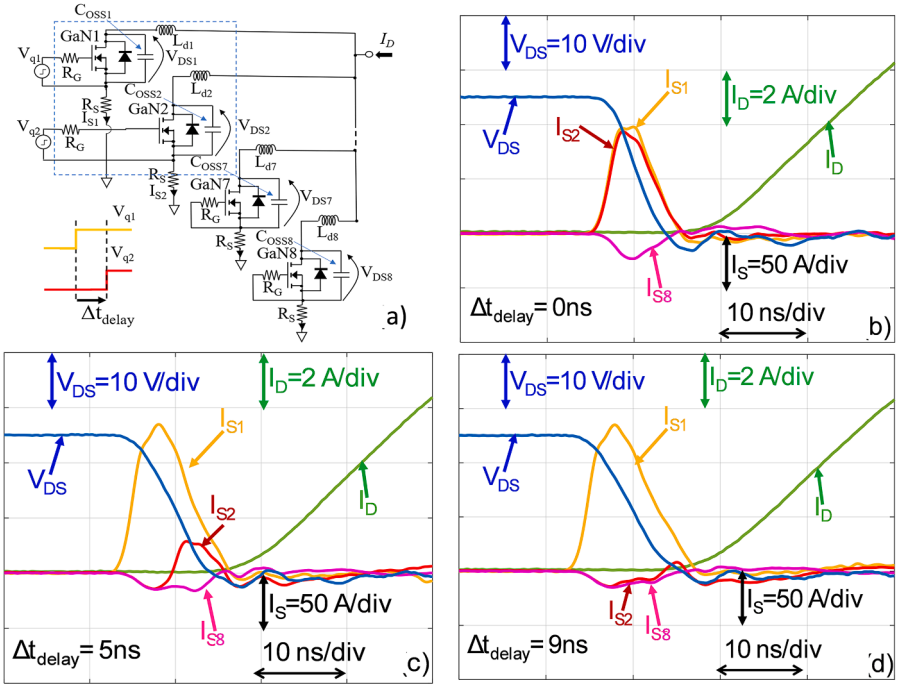


Fig. 7. Turn-on transient driving GaN2 with a delay in respect of GaN1. a) Electrical schematic of the two GaN FETs in the board driven with time-delayed V_q. b) delay = 0 ns. c) delay = 5 ns. d) delay = 9 ns. I_S= 50 A/div. I_D = 2 A/div. V_{DS} = 10 V/div. Time = 10 ns/div.

parallel connection driven with V_{q2} in a delay of Δt_{delay} with respect to V_{q1}. The resulting waveforms of the drain-source voltage V_{DS} and the board drain current I_D are depicted in blue and in green, respectively, in all experimental results. Additionally, Fig. 7 shows the measured currents of GaN1 I_{S1} (yellow), GaN2 I_{S2} (red), and that of a generic not driven GaN8 I_{S8} (magenta). The transient current is evenly distributed between the two devices. If a turn-on delay on GaN2 compared to GaN1 is introduced, the device that turns on first has a peak much higher than the second, relating to the length of the delay. Results obtained at current synchronisation are reported in Fig.7b This operative condition is considered with a $\Delta t_{delay} = 0$ ns, because is the starting point of the tests. While the waveforms achieved with $\Delta t_{delay} = 5$ ns and $\Delta t_{delay} = 9$ ns are depicted in Fig.7c and Fig.7d, respectively.

Examining the duration of the I_{DS} peak and the V_{DS} fall in Fig.7, it is evident that the case with $\Delta t_{delay} = 0$ ns in Fig.7b is the shortest, while the case with $\Delta t_{delay} = 9$ ns in Fig.7d lasts longer. This is due to a difference in V_{DS} between the GaN FETs as they are turned on with a larger delay. Moreover, Fig.7 shows that the device current peaks happen while the board drain current is still null ($I_D = 0$ A during the device turn-on current peak). The V_{DS} difference between GaN FETs causes a circulating current through the L_d inductance connecting GaN FETs in parallel as shown in Wang (2015). For example, in the case of GaN1 and GaN2, considering L_{d1}=L_{d2}, this current can be approximated as

$$I_{cir} = \int_{t_0}^{t'} \frac{V_{DS1} - V_{DS2}}{2 \cdot L_{d2}} \cdot dt \tag{8}$$

Where t_0 is the time of starting of the V_{DS} fall, and t' is a generic time between the interval where the V_{DS} voltage is falling.

Fig.8 shows the waveforms of V_{DS1} of GaN1, V_{DS2} of GaN2, and V_{DS8} of a non-driven GaN8 when GaN2 is turned on after Δt_{delay} with respect to GaN1 (From GaN3 to GaN8 the devices are in the off state).

Fig.8a shows the signal V_{q2} delayed by Δt_{delay} with respect to V_{q1} and the voltage across the devices evaluated.

Fig. 8b, Fig. 8c, and Fig. 8d show the results obtained with Δt_{delay} = 0 ns, 5 ns, and 9 ns, respectively. The measurements made in Fig.8 are in the same conditions as Fig.7. However, the two devices in parallel turned on with a fixed Δt_{delay} feature a drain inductance very high compared to the inductance connecting the two devices (L_D>>L_{dn} in Fig. 2). This means that the contribution of the load current is zero if only the switching transient is analyzed. The slow rise due to the load current only begins to have a real effect after the turn-on has passed (see I_D in Fig. 6, which is still zero after the transient of the I_{S1} peaks). Therefore, the test obtains the same results regardless of the load current value.

In Fig. 8b, when $\Delta t_{delay} = 0$ ns, V_{DS1} and V_{DS2} are congruent, while the devices from GaN3 to GaN8 remain in the off-state (in Fig. 8, the drain-source voltage of the off-state devices are called V_{DSn}) from which the voltage across drain source V_{DS3} to V_{DS8} falls later. As the GaN FETs are connected in parallel through inductances L_d, the higher value of V_{DS} of the off-state device (V_{DS8} in the Fig. 8) compared to V_{DS1} and V_{DS2} indicates current flowing from GaN8 to GaN1 and GaN2.

When GaN2 is turned on with a delay of $\Delta t_{delay} = 5$ ns, as shown in Fig. 8c, V_{DS2} falls later than V_{DS1} but earlier than V_{DS8}. The higher V_{DS2} compared to V_{DS1} indicates a current flow from GaN2 to GaN1. Simultaneously, V_{DS8} exhibits the highest values during the fall, indicating a current flowing from the non-driven GaN FETs (GaN8) to GaN1 and GaN2. This current flow has a higher amplitude as the voltage difference increases. The larger difference between V_{DS8} and V_{DS1} compared to V_{DS8} and V_{DS2} reveals a greater current flowing to GaN1 than to GaN2. Consequently, GaN1 conducts a minor current coming from GaN2 plus a higher current contribution from the non-driven GaN FETs. On the other hand, GaN2 conducts a minor current from the non-driven GaN FETs compared to the case with $\Delta t_{delay} = 0$ ns in Fig. 8b Additionally, a minor current flows from GaN2 to GaN1.

For $\Delta t_{delay} = 9$ ns, as shown in Fig. 8d, V_{DS2} is congruent with V_{DS8}, and both fall later compared to V_{DS1}. GaN2 behaves as a non-driven GaN FET (GaN8). The large difference between V_{DS1} and V_{DS2} indicates that the current flow through GaN1 is the maximum.

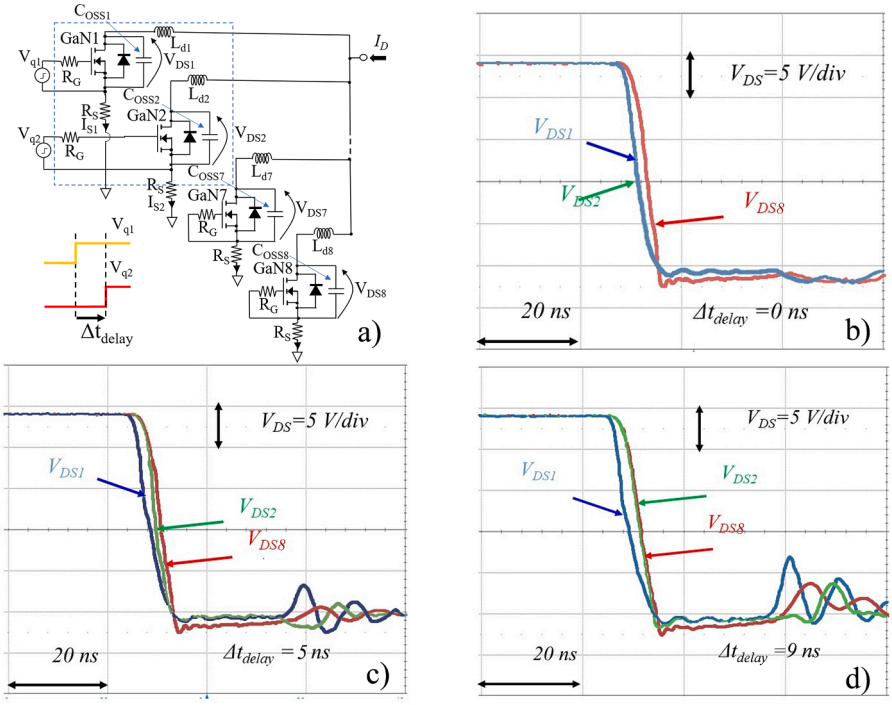


Fig. 8. Turn-on transient of the board prototype with *GaN2* in delay in respect of *GaN1*. Experimental waveforms for the voltage fall of: V_{DS1} for *GaN1*, V_{DS2} for *GaN2*, V_{DS8}, for *GaN8* (in off-state as GaN7 to GaN 3). a) Schematic of the parallel operation of *GaN1* and *GaN2* driven with V_{q2} in delay of Δt_{delay} in respect of V_{q1} while the other paralleled devices are in the off-state. b) Result with $\Delta t_{delay} = 0$ *ns*, c) Result with $\Delta t_{delay} = 3$ *ns*, d) Result with $\Delta t_{delay} = 9$ ns, $V_{DS} = 5$ V/div. Time = 20 ns/div.

5. Parasitic capacitances effect at turn-off switching transients

The experimental tests are extended at turn-off with the same methodology approach. Fig. 9a illustrates the electrical schematic of GaN1 and GaN2 connected in parallel, with V_{q2} delayed by Δt_{delay} relative to V_{q1}. The corresponding waveforms for the drain-source voltage V_{DS} and the board drain current I_D are shown in blue and green, respectively. Furthermore, Fig. 9 presents the measured currents of GaN1 I_{S1} (yellow), GaN2 I_{S2} (red), and a generic non-driven GaN FET current I_{Sn} (magenta).

The switching results without delay are depicted in Fig. 9b, whereas waveforms with $\Delta t_{delay} = 5$ ns and $\Delta t_{delay} = 9$ ns are shown in Fig. 9c and Fig. 9d, respectively. A comparative analysis of Fig. 9b, Fig. 9c, and Fig. 9d reveals that the I_D and V_{DS} waveforms remain unchanged across different delay cases. I_D falls slowly following the V_{DS} rising because of the high value of L_D. In the case without delay in Fig. 9b, the turn-off of GaN1 and GaN2 occurs simultaneously due to the immediate turn-off of both FETs. This results in an equal distribution of the load current between GaN1 and GaN2 and the absence of a current peak. Introducing a $\Delta t_{delay} = 5$ ns, as illustrated in Fig. 9c, results in a higher I_{S1} peak compared to I_{S2}, since GaN1 continues to conduct the entire load current alone immediately after the GaN2 turn-off. In the scenario of Δt_{delay}=5 ns depicted in Fig. 9d, the delay is long enough to leave GaN1 to conduct all the load current alone until it turns off. Consequently, at turn-off, the maximum I_S peak value corresponds to the load current, without contributions of parasitic capacitances as discussed in Koch (2021). As a result, the delay in the turn-off has to be kept short to control the maximum peak current. Nevertheless, the turn-off transient is less problematic than the turn-on.

6. Energy losses evaluation during switching transients

The characterization of the dynamic behavior of GaN FETs connected in parallel is crucial in high-power and high-frequency applications. Imbalanced current sharing results in increased losses and potential thermal runaway if not properly managed. By analysing the turn-on and turn-off delays, and their corresponding energy losses as described in Sørensen (2015) and Perera (2022), is essential to provide insights that can help in designing more efficient parallel GaN FET systems, ensuring better performance and longevity of the devices.

The GaN FET switching energy resulting from the experimental tests with different turn-on and turn-off delays is calculated as

$$E_{GaN} = \int_0^{\Delta t} I_S \cdot V_{DS}\, dt \tag{9}$$

where Δt is the time interval defined for the turn-on or the turn-off:

- turn-on: Δt it the time duration of the I_{s1} peak;
- turn-off: Δt goes from when I_{s2} starts falling and finishes when the peak of I_{s1} is reached.

The calculated energy indicates the contribution of the parasitic capacitances and the turn-on and turn-off delay between GaN FETs connected in parallel. The loss mechanism is similar in parallel connections of Silicon Carbide (SiC) MOSFETs as described in Lüdecke (2021).

The design of the PCB considered allows the contribution of losses due to load current to be excluded (the effects on currents caused by the discharge of parasitic capacitances and the rise of drain current are decoupled as discussed in the testing methodology section). Fig.10a depicts the GaN FET energies obtained with various driving delays between V_{q1} and V_{q2} at turn-on, while Fig.10b shows the results relative to the turn-off. The energy losses for GaN1 (E_{GaN1}) and those of GaN2 (E_{GaN2}) are represented in yellow and red, respectively; additionally, the sum of the two losses E_{tot} is depicted in black.

$$E_{tot} = E_{GaN1} + E_{GaN2} \tag{10}$$

Comparing Fig.10a and Fig.10b is notable that turn-on energy losses are significantly higher than turn-off losses.

Focusing on the turn-on in Fig.10a, it is evident that when GaN FETs turn on simultaneously (delay is null), losses are equal for both devices. Introducing a delay in GaN2 results in higher losses in GaN1, while E_{GaN2} is reduced. In particular, a delay of 5 ns is the condition in which GaN2 exhibits $E_{GaN2} = 0$ J. For delays longer than 5 ns, the negative E_{GaN2}

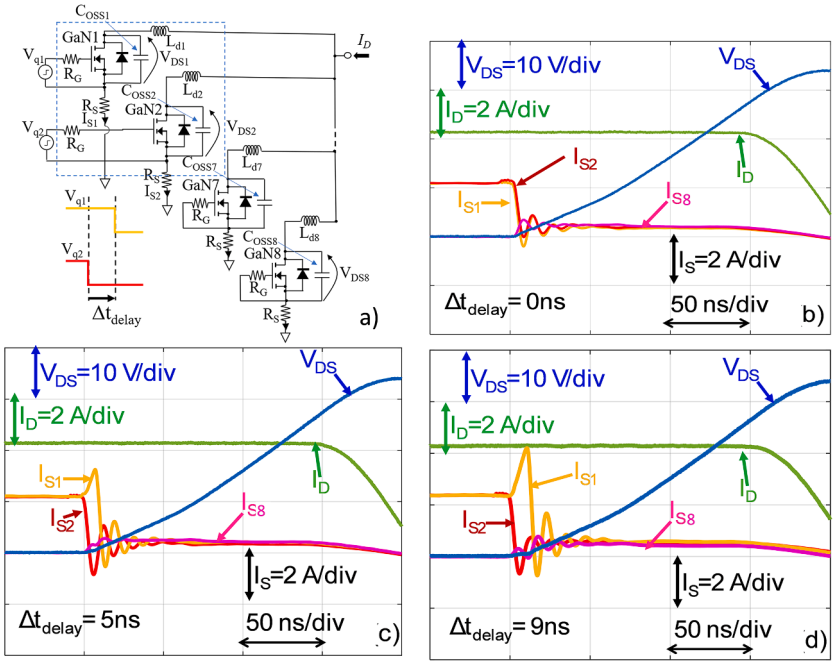


Fig. 9. Turn-off transient driving GaN2 with a delay in respect of GaN1. a) electrical schematic of the two GaN FETs in the board driven with time-delayed V_q. b) delay = 0 ns. c) delay = 5 ns. d) delay = 9 ns. I_S = 2 A/div. I_D = 2 A/div. V_{DS} = 10 V/div. Time =10 ns/div.

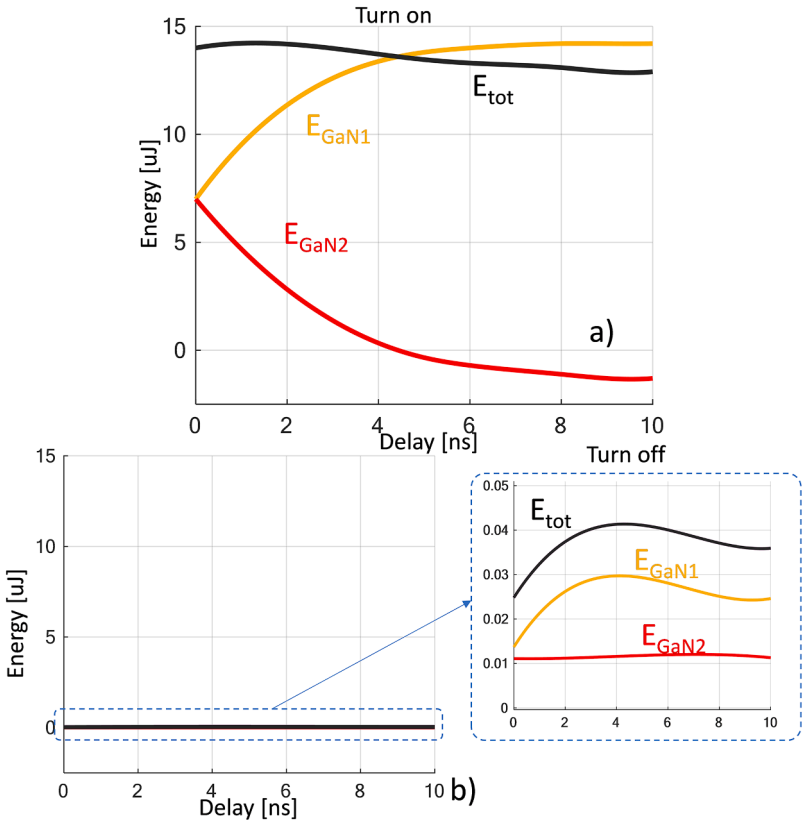


Fig. 10. Energy losses of GaN1(E_{GaN1}), GaN2(E_{GaN2}) and the sum of both (E_{tot}) obtained as a function of the driving delay. a) turn-on. b) turn-off.

indicates that the C_{OSS} charge of GaN2 is mostly conducted by GaN1. E_{GaN2} stabilizes to a minimum value for a delay higher than 9 ns because all the C_{OSS} charge of GaN2 is conducted by GaN1.

As a consequence, E_{GaN1} stabilizes to a maximum value for a delay higher than 9 ns. In this condition, GaN1 conducts the total parasitic current of the PCB and the parallel-connected devices. The total energy E_{tot} remains almost constant regardless of the delay since the total energy of the system is determined by the total charge and the applied voltage.

At turn-off, the enlarged view of Fig.10b shows that the turn-off losses of GaN1 (E_{GaN1}) and GaN2 (E_{GaN2}) remain constant along the entire Δt_{delay} range. It is equal to the energy losses at 0 ns of delay due to the simultaneous turn-off of devices. A non-zero delay causes an increase in E_{GaN1}, while E_{GaN2} remains unchanged. The energy losses of GaN transistors in parallel connection are described in Lu (2018). The total energy E_{tot} is at a minimum value when the delay is null and increases the longer the delay time, as shown in the enlarged y-axis diagrams of Fig. 10b

7. Conclusion

This paper presented a comprehensive investigation of the dynamic current-sharing behaviour in parallel low-voltage GaN FETs, with a particular focus on how parasitic capacitances, parasitic inductances, and device-to-device parameter variations influence transient current imbalance during switching events.

A custom evaluation board was developed to emulate realistic operating conditions and to enable controlled testing of individual device interactions. Featuring independent gate drivers, per-device current sensing placed outside the gate loop, and a PCB stack-up designed to ensure a dominant common-drain inductance, the board allowed accurate measurement of transient currents and the effects of parasitic capacitances that are difficult to characterise using conventional parallel test boards devoted to the industrial applications.

A central contribution of this work is the proposed methodology for experimentally decoupling the capacitive current spike from the load-current component during turn-on. By engineering the common inductance path to enforce very low current slew rates, the measured turn-on current peak is primarily determined by the discharge of parasitic capacitances. This enables the capacitive-only current contribution to be isolated and analysed independently, providing a clearer understanding of how device parameters and layout-induced parasitic shape of the peak transient current. The method also allowed the capacitive energy losses to be quantified and the conditions that produce non-simultaneous switching to be experimentally identified.

Although the parasitic-capacitance extraction performed in the paper is specific to the developed PCB, the resulting modelling approach enables more realistic circuit simulations and can be extended to other board architectures. From a layout perspective, the study highlights the importance of minimising parasitic capacitances by avoiding the vertical overlap of copper regions at different voltage potentials and aligning nodes of equal potential across layers. While this strategy reduces the charge contributing to turn-on current spikes, it may also increase dv/dt, underscoring the need for a careful trade-off with appropriate gate-drive optimisation.

Overall, the combined simulation–experimental framework developed in this paper offers comprehensive insights into the mechanisms governing current imbalance in paralleled GaN devices. The results carried out through the experimental characterization board provide practical design guidelines—spanning gate-driver requirements, PCB layout techniques, and mitigation of parasitic mismatches—that support the development of reliable, efficient, and high-performance GaN-based parallel connection in power stages for industrial applications.

CRediT authorship contribution statement

Salvatore Musumeci: Writing – review & editing, Writing – original draft, Validation, Supervision, Resources, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Vincenzo Barba:** Writing – review & editing, Validation, Methodology, Investigation, Formal analysis, Conceptualization. **Michele Pastorelli:** Writing – review & editing, Validation, Supervision, Project administration, Methodology, Investigation, Data curation, Conceptualization. **Marco Palma:** Writing – review & editing, Validation, Supervision, Resources, Project administration, Methodology, Investigation, Formal analysis, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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