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19 November 2026

Design and Characterization of a 6–7 GHz GaAs HBT Doherty Power Amplifier MMIC for Wi-Fi 6E

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***Abstract*—This contribution presents a 5-V 1.8-W GaAs HBT Doherty power amplifier MMIC conceived for Wi-Fi 6E applications in the 6-7 GHz band. The paper discusses the solutions adopted, at transistor and amplifier level, to deal with the challenges posed by the demanding design frequency, which is at the limit of the commercially available technologies. The proposed amplifier achieves more than 23 % efficiency in a 5-dB back-off range, as well as good linearity performance when tested with wideband Wi-Fi 6E modulated signals.**

***Index Terms*—Doherty power amplifier, Wi-Fi 6E, GaAs MMIC, HBT**

I. Introduction

The IEEE 802.11ax amendment, extended to the 6 GHz spectrum as Wi-Fi 6E, enables significantly increased network capacity and reduced interference by providing access to a large contiguous bandwidth (BW) in the 5.925–7.125 GHz range [1]. Operation in this band supports wide channel bandwidths up to 160 MHz and advanced transmission techniques such as orthogonal frequency-division multiple access (OFDMA), multi-user multiple-input multiple-output (MU-MIMO), and higher-order modulation schemes up to 1024-QAM. While these features substantially enhance spectral efficiency and multi-user throughput, they also generate signals with high peak-to-average power ratios (PAPR), imposing stringent requirements on the transmitter power amplifier, which must address the trade-off between efficiency and linearity under power back-off operation.

InGaP/GaAs heterojunction bipolar transistor (HBT) technology is well suited to address these challenges thanks to its high current density, favorable breakdown characteristics and good thermal stability, enabling efficient and linear operation at high output power levels. Furthermore, it benefits from mature, high-volume fabrication processes and proven cost effectiveness in mass-market applications. Such features, combined with the distinctive ability of Doherty power amplifiers (DPAs) to maintain high efficiency over a wide output power back-off (OBO), make HBT DPAs an attractive solution for high-power and high-linearity WLAN transmitters [2], [3]. However, at Wi-Fi 6E frequencies approaching 7 GHz, HBT devices are pushed close to their practical limits, as parasitics, gain roll-off and passive losses start affecting efficiency and linearity, hence requiring a careful design of the device biasing and matching networks and of the power combiner [4].

In this work, we present a 32.5 dBm Doherty power amplifier MMIC based on WIN Semiconductors' 4th generation HBT technology (H02U-C4), designed for operation in the 6-7 GHz range. The fabricated DPA shows remarkable CW performance, with a 5-dB OBO power added efficiency (PAE) in excess of 23 %, along with good linearity and efficiency performance under wideband 802.11ax signals, despite the close-to-limit operation of this technology, thereby demonstrating its suitability for Wi-Fi 6E applications.

II. Design

Due to the challenges posed by ultra-wideband design ($> 30\,\%$ of fractional BW) , the Wi-Fi 6E band is often covered by separate PA modules, each covering a 1 GHz band. More advanced integrated solutions include dual-band switched-PAs [5] and reconfigurable PAs [4]. The design of the 6-7 GHz Doherty PA presented here builds upon some previous successful designs in the 5-6 GHz range [3], [6] on the same technology, and it was conceived to complement them in order to cover the entire 5-7 GHz bandwidth with a dual-band module.

As detailed in [6], the biasing strategy adopted for all the MMICs is a constant-voltage approach, allowing to observe the intrinsic linearity of the technology and to boost peak efficiency. The same basic power cell of previous works was also initially adopted, but an improved version has ben then developed to counteract the gain penalty experienced at the higher operating frequency. To experimentally validate the effectiveness of the novel cell, both versions of the DPA, with the two different cells, were fabricated and characterized. Details are given in the following.

A. Power Cell Optimization

Targeting 32 dBm of output power requires the adoption of large, multi-finger transistors as basic building blocks. Although some large devices are included in the foundry portfolio, their layout and ballasting is optimized for sub-6 GHz 5G NR applications around 2 GHz. To ensure operation up to 7 GHz, a symmetric layout for a power cell combining 4 elementary transistor ($4\times3\times40\ \mu\text{m}^2$) has been developed. The final cell, shown in Fig. 1-left, includes DC and RF ballasting and stabilization elements to avoid both thermal and electrical instabilities as detailed in [3]. Starting form this

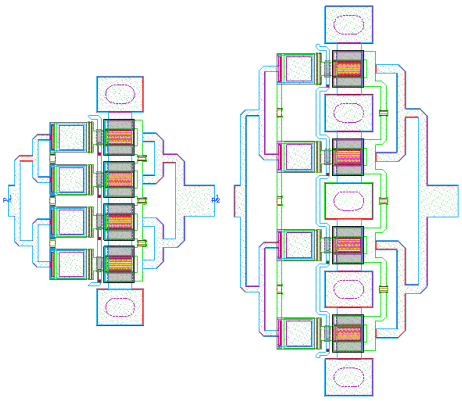


Fig. 1. Layout of the basic (left) and 5-VIA (right) power cells.

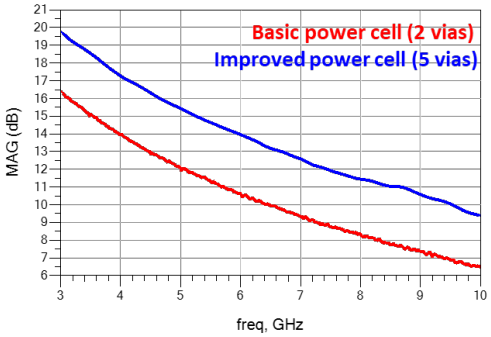


Fig. 2. Measured maximum available gain of the basic (red) and improved (blue) power cells.

layout, smaller cells, with only 2 and 1 elementary transistors, respectively, have been obtained as cut-outs, to ensure the same high-frequency capability and stability, while allowing for the optimization of the linearity-efficiency trade-off in the driver stages.

As experimentally observed in [7], the very good performance of the cell degrades when approaching 7 GHz, especially in terms of gain. In order to recover this penalty, a new layout has been developed for the 6-7 GHz DPA. As shown in Fig. 1-right, via holes have been added in between stages to minimize the emitter inductance while keeping reasonable area. Moreover, the larger occupied area of this 5-VIA solution comes indeed with the benefit of better thermal behavior, which is expected to boost also efficiency at high power levels.

Fig. 2 reports the comparison of the measured maximum available gain (MAG) of the 2 cells shown in Fig. 1. An improvement of roughly 3 dB is achieved at all frequencies, which becomes indeed crucial in the 6-7 GHz range, where the MAG of the original cell falls below 10 dB. The gain improvement of the 5-VIA cell is also confirmed in large-signal cell characterization [7], and by the results achieved within the complete DPA, as detailed in the Section IV.

III. Doherty Optimization

The schematic of the designed DPA is shown in Fig. 3: as in [3], it counts 3 stages adopting a 1:2:4 architecture. The developed 5-VIA power cell is exploited only in the final stage where its improved thermal characteristics can sensibly improve performance, while for the driver stage the basic 2-transistor cell (with 2 via holes rather than 3) is adopted. Although the load-pull analysis [6] indicates a load of $(8 + j4)\ \Omega$ as the optimum to achieve best compromise between power, efficiency and linearity, a purely real load has been lately considered in the design implementation. Indeed, the reactance-matching elements at the collector resulted in performance degradation due to less favorable harmonic terminations for the device and increased losses at 7 GHz. The Doherty combiner is designed following a semi-lumped strategy to optimize chip area consumption. Despite the relatively standard implementation of the quarter wavelength impedance inverter network (IIN) as a high-pass T network, and of the post-matching network (PMN) as a low-pass one, a careful electro-magnetic (EM) optimization was required to achieve good performance up to 7 GHz. Similarly, the inter-stage matching networks (ISMN) for the driving stages share the same capacitance–line–stub topology and are then EM-optimized based on the actual input impedance trajectory of the subsequent stage as a function of power, particularly within the Doherty region. In all stages, the RF-shorted stub acts also as DC biasing line, optimized to be insensitive to external impedance variations, exploiting the approach proposed in [8]. The DC collector voltage is 5 V for all devices, while the base voltage for all the cascaded cells in the main and auxiliary branches are 1.325 V (4.8 kA/cm^2) and 1.25 V (< 0.6 kA/cm^2), respectively. Nonetheless, each stage has an independent bias line to allow the maximum possible flexibility in measurement. The input power splitter (IPS) is a fully-lumped Wilkinson, while the input matching network (IMN) is a high-pass Π network for both main and auxiliary branches. To align current phases, a low-pass Π network (PCN, phase compensation network) is added in the main branch, counteracting the phase rotation introduced by the high-pass IIN at its output.

As anticipated, to validate the effectiveness of the improved cell, a second version of the PA, with same topology, but adopting the basic power cell in the final stage, has been also included in the foundry run, as well as selected passive networks for the assessment of the EM simulation accuracy with relatively large structures. Fig. 4 reports the microscope picture of the two DPAs: chip size is 4.7×2.9 mm^2 each.

IV. Measurement Results

This section illustrates the main results of the experimental characterization. The two DPAs have been characterized adopting ad-hoc designed test-jig, optimized for low-frequency stability and thermal management. Unless otherwise noted, the nominal quiescent bias adopted in simulations is enforced.

Small-signal characterization on DPAs and test structures is performed from 2 GHz up to 26 GHz. Fig. 5 reports the comparison between measured and EM simulated S-parameters for the output matching network, demonstrating

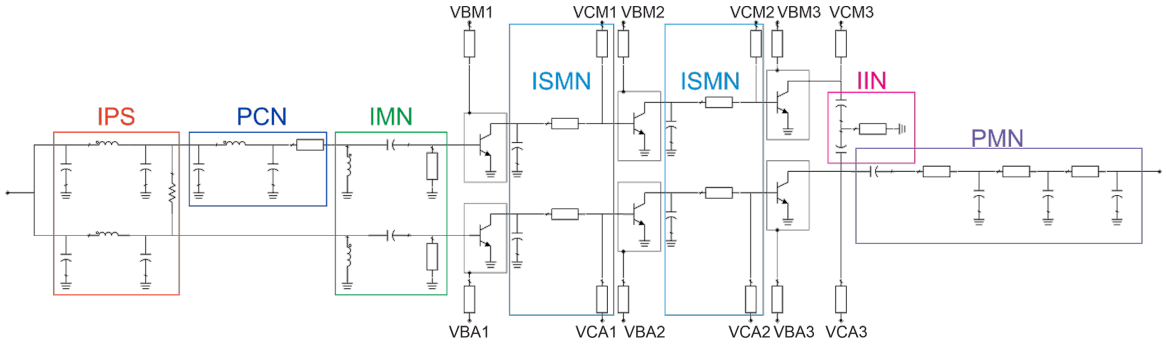


Fig. 3. Simplified schematic of the designed DPA. Device sizes for both the main (top branch) and auxiliary (bottom branch) are: $1\times3\times40$ μm^2 (stage 1), $2\times3\times40$ μm^2 (stage 2) and $4\times3\times40$ μm^2 (stage 3).

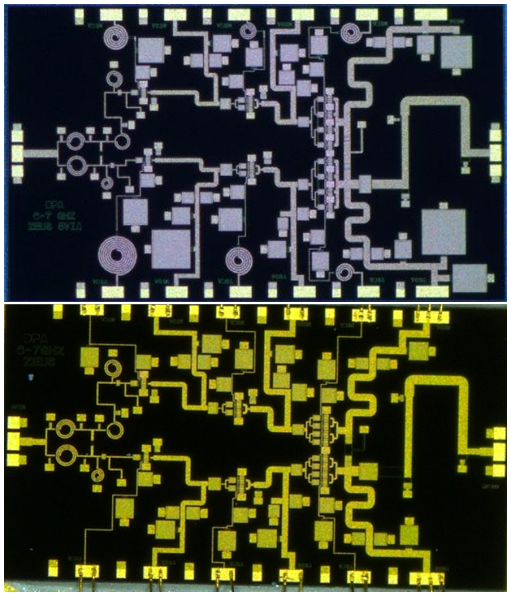


Fig. 4. Microscope picture of the two DPA versions with basic (bottom) and improved (top) power cell. Color differences are due to different set-ups adopted for taking the pictures.

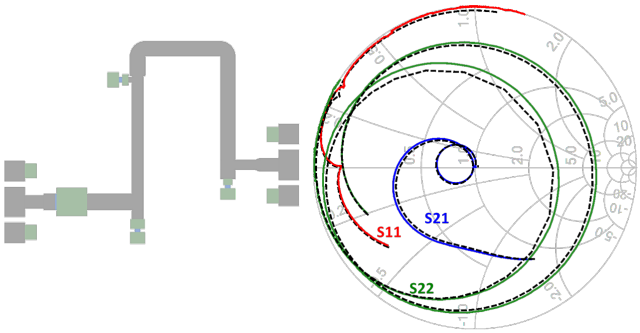


Fig. 5. Measured (solid, colored) vs simulated (dashed, black) S-parameters of the impedance inverting network cut-out shown on the left.

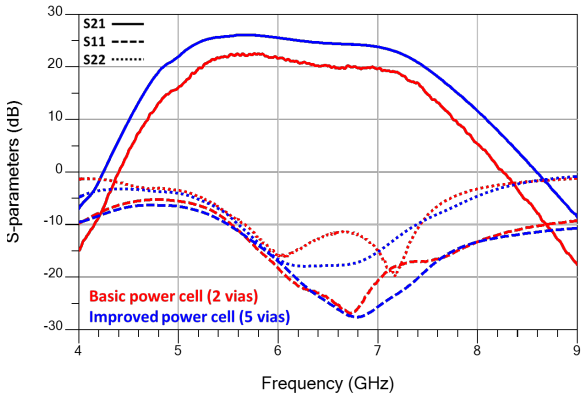


Fig. 6. Measured S-parameters: comparison between the two DPA versions with basic (red) and 5-VIA (blue) power cell.

excellent agreement and hence the accuracy of the adopted EM simulation set-up.

The S-parameters of the two DPA versions are compared in Fig. 6: as expected from simulations, the gain provided by the DPA based on the 5-VIA cell is sensibly better, and exceeds 24 dB in the whole band. The superiority of the improved cell is confirmed by large-signal CW characterization results as shown in Fig. 7.

Focusing on the improved version only, Fig. 8 and Fig. 9 report the measured performance compared to simulations, while Fig. 10 summarizes the measured in-band performance at saturation and at 5-dB OBO. The saturated output power is higher than 32.5 dBm in the entire range, with associated power-added efficiency and gain larger than 34 % and 20.5 dB, respectively. Although the simulated gain showed better flatness than the measured one, probably due to some inaccuracy in modeling the effect of the higher harmonics, the experimental gain obtained is remarkable, thanks to the improved cell. At 5-dB output back-off the PAE remains above 23 %, noticeably increasing towards the higher portion of the band.

Finally, Fig. 11 shows a preliminary linearity assessment of the DPA. The results obtained under modulated-signal characterization, with 40 MHz and 80 MHz 802.11ax MCS11 signals at 6.5 GHz, are compared to the predictions made according to the measured CW AM-AM and AM-PM data following the method described in [9]. The excellent agreement up to -30 dB of EVM indicates that this simpler approach is still effective in

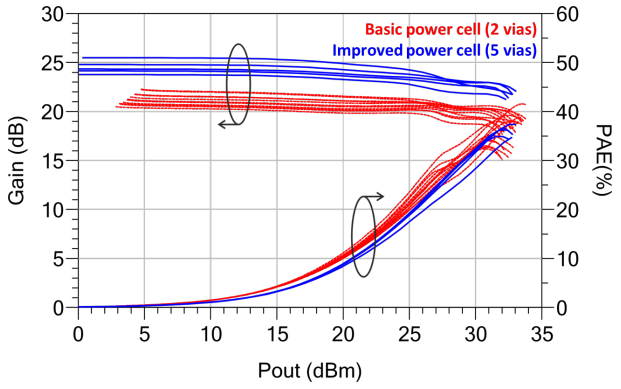


Fig. 7. Measured CW performance: comparison between the two DPA versions with basic (red) and 5-VIA (blue) power cell .

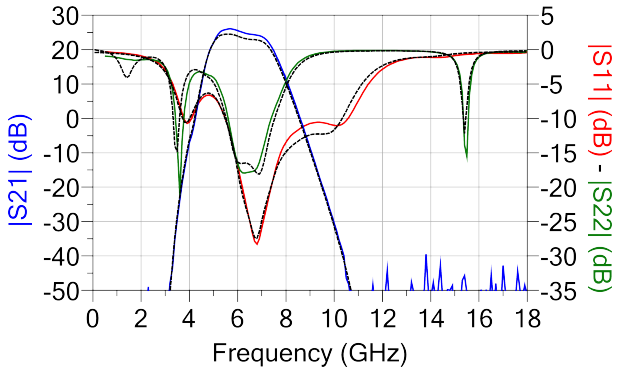


Fig. 8. Measured S-parameters (solid, colored) compared to simulations (dashed, black) of the proposed DPA based on improved power cell.

providing a fast, yet relatively accurate, linearity assessment method. Moreover, the small discrepancy between the CW-based estimation and actual modulated measurements with two different instantaneous bandwidths shows that slow-memory effects (e.g. due to thermal phenomena or biasing networks) play a minor role in determining the overall linearity. In these conditions, the proposed DPA shows 22.5 dBm output power and 12.5 % PAE at -22.5 dB EVM. Both the CW and the modulated results are in line with literature values [4], [5],

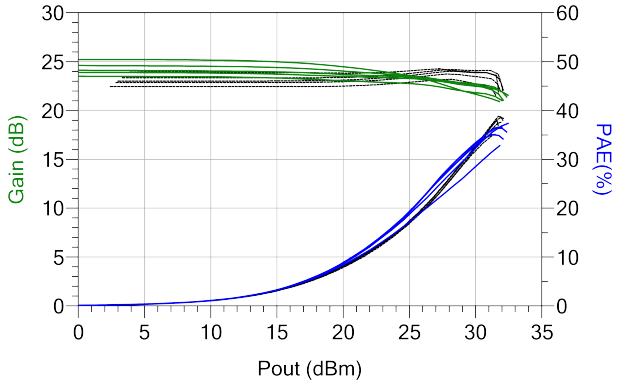


Fig. 9. Measured CW performance (solid, colored) compared to simulations (dashed, black) of the proposed DPA based on improved power cell.

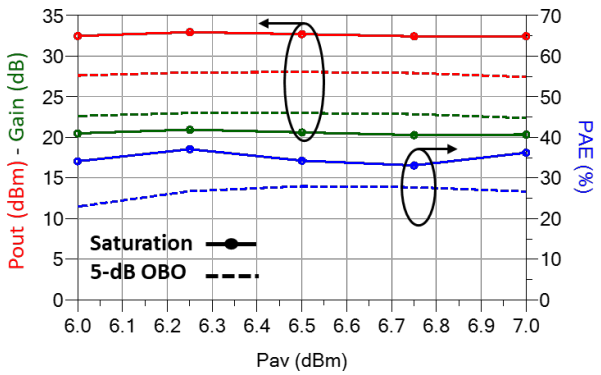


Fig. 10. Measured in-band performance at saturation (solid, symbols) and at 5 dB back-off (dashed) of the proposed DPA based on improved power cell.

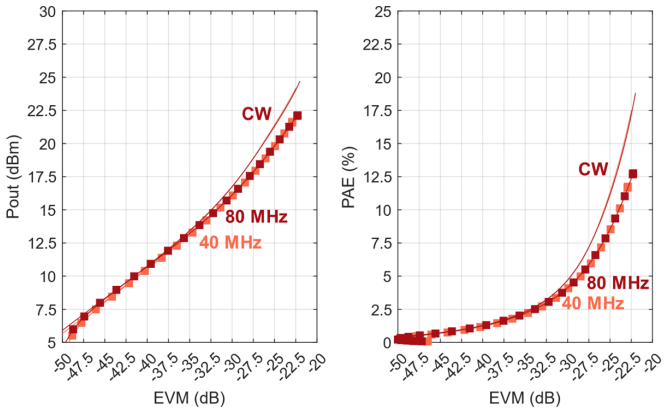


Fig. 11. Measured output power and PAE vs. EVM with 40 MHz and 80-MHZ MCS11 signal (symbols) compared to CW-based predictions (solid) at 6.5 GHz.

[10]–[15], demonstrating the effectiveness of the proposed DPA design for the intended application. It is also worth to note that according to simulations, linearity performance can be further tuned to different EVM threshold by simply changing the base bias voltage of some of the stages, allowing for further optimization according to the specific modulation of interest.

V. Conclusion

This paper has presented the design and experimental validation of a Doherty power amplifier MMIC in commercial-grade GaAs HBT technology targeting Wi-Fi 6E applications in the 6–7 GHz frequency band. The proposed solution addresses the technological limitations encountered at these frequencies through careful transistor-level combination, load modulation strategy, and broadband matching network design. Measured results demonstrate that the implemented Doherty architecture is effective in enhancing efficiency under back-off operation, achieving more than 23 % efficiency over a 5-dB OBO range. In addition, the amplifier exhibits satisfactory linearity when driven by wideband MCS11 modulated signals, confirming its suitability for high-data-rate wireless applications. Overall, the reported results validate the feasibility of

GaAs HBT Doherty MMICs operating at the upper edge of commercially available technologies and highlight their potential for next-generation Wi-Fi 6E transmitters, where efficiency and linearity at high frequencies are key performance drivers.

REFERENCES

[1] E. Mozaffariahrar, F. Theoleyre, and M. Menth, "A Survey of Wi-Fi 6: Technologies, Advances, and Challenges," *Future Internet*, vol. 14, no. 10, 2022.

[2] S. Wan, W. Chen, G. Lv, L. Chen, and Z. Feng, "A Fully Integrated High-Efficiency Three-stage Doherty Power Amplifier for Small-cell application," in *IEEE Int. Workshop Electromagn.: Appl. Student Innovation Competition, iWEM 2021*, vol. 1, 2021, pp. 1–3.

[3] F. Manni, R. Giofrè, C. Florian, A. M. Angelotti, G. P. Gibiino, M. Pirola, C. Ramella, and P. Colantonio, "An Integrated GaAs HBT Doherty Power Amplifier for Wi-Fi 6," in *Eu. Microw. Integrated Circ. Conf., EuMIC 2025*, 2025, pp. 1–4.

[4] S. Hwang, J. Jeon, S. Bae, B. Yoon, and J. Kim, "A Differential Amplifier with Enhanced Linearity of Average Power Region Using Dynamic Cross-coupled Capacitor for 5G NR-U," in *IEEE/MTT-S Int. Microw. Symp., IMS 2023*, 2023, pp. 207–210.

[5] pSemi, "PE565211 - 802.11ax (Wi-Fi 6) FEM from 5 to 7 GHz."

[6] C. Ramella, C. Florian, F. Manni, A. M. Angelotti, G. P. Gibiino, R. Giofrè, M. Pirola, and P. Colantonio, "MMIC Power Amplifier in GaAs HBT Technology for Wi-Fi 6 Applications," in *Int. Workshop Integrated Nonlinear Microw. Millimetre-Wave Circ., INMMIC 2025*, 2025, pp. 1–4.

[7] A. M. Angelotti, C. Florian, G. P. Gibiino, C. Ramella, M. Pirola, F. Manni, R. Giofrè, and P. Colantonio, "Load/Source-Pull Evaluation of Modulated Performance in GaAs HBT Power Cells for WiFi-6," in *Int. Workshop Integrated Nonlinear Microw. Millimetre-Wave Circ., INMMIC 2025*, 2025, pp. 1–4.

[8] C. Ramella, P. Colantonio, and M. Pirola, "A Simple Closed-Form CAD Approach for Sensitivity Analysis and Optimization of Passive Networks Against Load Variations," in *IEEE/MTT-S Int. Microw. Symp., IMS 2025*, 2025, pp. 610–613.

[9] A. M. Angelotti, G. P. Gibiino, T. S. Nielsen, A. Santarelli, and J. Verspecht, "Impact of Broadband Modulation in Active Load-Pull On-Wafer Measurements of GaN HEMTs," in *Microw. Meas. Conf., ARFTG 2022)*, 2022, pp. 1–4.

[10] Y. Kang, H. Lee, and I. Ju, "A 5/6 GHz Compact, Dual-Band, and Highly Linear Wi-Fi 6E SiGe HBT Power Amplifier Using Q-Modulated Switched Capacitor Interstage Matching Network and Optimized Output Stage," in *IEEE Radio Freq. Integrated Circ. Symp., RFIC 2025*, 2025, pp. 295–298.

[11] S. Lee, B. Yoon, J. Jeon, and J. Kim, "A Concurrent 2.45/5.8 GHz Power Amplifier with an Optimal Dual-band Matching Method," in *IEEE Top. Conf. RF/Microw. Power Amp. Radio Wireless Appl., PAWR 2024*, 2024, pp. 1–4.

[12] J. Li, Z. Zhang, and G. Zhang, "A 5.15–6.425 GHz Stagger-Tuning Neutralized Power Amplifier Using a Continuous-Mode Harmonically Tuned Network," *IEEE Microw. Wireless Technol. Lett.*, vol. 33, no. 2, pp. 173–176, 2023.

[13] X. Yang, Z. Leng, L. Chen, Z. Ge, J. Zhou, and F. Sun, "A fully integrated GaAs HBT power amplifier for WLAN 802.11ax applications," *Microw. Opt. Technol. Lett.*, vol. 66, no. 10, p. e70000, 2024.

[14] L. Huang, Z. Zhang, S. Li, and G. Zhang, "An InGaP/GaAs HBT power amplifier for 4.9–5.9 GHz Wireless-LAN applications," in *IEEE Int. Conf. Solid-State Integrated Circ. Technol., ICSICT 2014*, 2014, pp. 1–3.

[15] I. Ju, Y. Gong, and J. D. Cressler, "Highly linear high-power 802.11ac/ax wlan sige hbt power amplifiers with a compact 2nd-harmonic-shorted four-way transformer and a thermally compensating dynamic bias circuit," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2356–2370, 2020.