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Design Guidelines for Optimal Implementation of Doherty Power Amplifiers Based on Three-$\lambda/4$ Output Combiners

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***Abstract*—This work presents a design methodology for Doherty power amplifiers (DPAs) exploring two different topologies of output combiners composed of three $\lambda/4$ transmission lines. By imposing specific matching conditions in the theoretical analysis, design charts are derived to guide the selection of the optimal DPA configuration, starting from predefined target specifications. The theoretical findings are leveraged to design an integrated DPA in GaAs HBT technology for sub-6-GHz applications. The DPA achieves a peak output power of 33 dBm, with a power-added efficiency (PAE) and gain higher than 23% and 25 dB at 6 dB back-off, respectively, while maintaining a flat response with less than 0.5 dB ripple over 5–6 GHz. When measured with an 80-MHz-instantaneous bandwidth (BW) 1024-QAM 802.11ax signal, the DPA achieves an average output power of 22 dBm and a PAE of 12.5% at 3% error vector magnitude (EVM).**

***Index Terms*—Doherty power amplifier (DPA), GaAs, HBT, integrated circuit, sub-6 GHz, wireless communications.**

I. Introduction

THE evolution of wireless communication systems is now driven by the deployment of 5G networks and the continuous advancement of wireless local area networks (WLANs). 5G leverages FR1 frequency bands (sub-6 GHz) to ensure broad coverage while utilizing FR2 millimeter-wave (mmWave) bands to deliver high data rates and low latency services [1]. Looking toward the future, 6G systems are expected to enable emerging applications such as the Internet of everything (IoE), extended reality, vehicle-to-everything (V2X) communication, and integrated satellite networks. These systems are anticipated to exploit even higher frequency ranges to achieve extremely high data rates, ultralow latency, and massive connectivity [2], [3]. In parallel, WLANs enhance mobile networks by providing high-speed connectivity in densely populated environments operating in unlicensed sub-6-GHz frequency bands and, more recently, in the 6-GHz spectrum [4].

A common characteristic of these systems is the use of spectrally efficient modulation schemes, which produce time-domain signals with high peak-to-average power ratio (PAPR). This requires power amplifiers (PAs) capable of operating efficiently not only in saturation but also at large output back-off (OBO) [5]. In this context, the Doherty PA (DPA) remains one of the most widely adopted architectures for achieving high average efficiency in high-PAPR systems [6], [7].

A conventional DPA combines two active devices, typically referred to as carrier and peaking (or main and auxiliary), through a $\lambda/4$ transmission line ($\lambda/4$-TL) to achieve high average efficiency over a wide OBO range. However, the standard architecture inherently exhibits limited bandwidth (BW) [8], which is no longer compatible with the requirements of modern communication systems. Several techniques have been proposed to extend the DPA BW, including harmonic tuning and continuous-mode operation [9], [10], [11], device intrinsic output capacitance compensation [12], [13], and modified output combiner configurations [14], [15], [16], among others. Although these approaches have demonstrated impressive performance, particularly in hybrid implementations and high-power sub-6-GHz applications, their applicability to watt-level integrated DPAs remains largely unexplored. This aspect becomes even more critical considering that the optimal implementation of a DPA strongly depends on the adopted semiconductor technology. Indeed, given the wide range of applications across different frequency bands and design requirements, the choice of the underlying platform is typically driven by the target output power level. The latter, together with the characteristics of the chosen technology—particularly in terms of supply voltage and current density—determines the optimal output resistance (R_{opt}) of the active devices that must be synthesized by the DPA output combiner. This parameter plays a key role in the achievable DPA performance, especially in terms of BW, since it defines the required impedance transformation from the standard 50 Ω output termination. Moreover, R_{opt} can vary significantly across technologies and

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power levels, from hundreds of ohms in GaN implementations to tens or even a few ohms in GaAs and CMOS realizations [17], [18], [19], [20]. As a result, the optimal output combiner topology and matching strategy may differ depending on the application, and their identification at the early design stage remains a challenging task.

This work presents a detailed comparative analysis of two DPA output combiner schemes employing three $\lambda/4$-TL sections. Although both topologies are based on the same number of $\lambda/4$-TLs, their different placement within the output network results in different impedance transformation mechanisms and, consequently, different design tradeoffs. The first topology, originally introduced in [21] and widely adopted in wideband designs [22], [23], [24], employs one $\lambda/4$-TL in the carrier branch and two in the peaking branch. Unlike the constant-power contour approach proposed in [22], this work determines the characteristic impedances of the combiner to minimize the in-band reflection coefficient, thereby maximizing the achievable BW. In the second DPA topology, one $\lambda/4$-TL is placed between the carrier and peaking devices, while the remaining two form a postmatching network (PMN) that performs the final impedance transformation toward the output termination. Unlike [25], [26], where the PMN is designed only to transform the external load into R_{opt} at the combining node, this work treats the characteristic impedances of all three $\lambda/4$-TLs—subject to the constraints imposed by the DPA architecture—as design variables to optimize the frequency response.

By imposing appropriate matching conditions, analytical expressions for the characteristic impedances are derived and used to generate design charts that guide the selection of the combiner parameters according to DPA target specifications, including BW and OBO. Moreover, the comparative analysis highlights the design scenarios in which each topology provides the most favorable tradeoff between BW and the other DPA requirements for a given device R_{opt}, i.e., for a given technology.

To validate the methodology, an integrated DPA in GaAs HBT technology is designed for sub-6-GHz applications. The active devices are implemented by combining multiple transistor cells, resulting in a particularly low R_{opt}, a condition for which the proposed analysis is especially beneficial. Measurement results demonstrate a very flat frequency response with less than 0.5-dB power ripple across the 5–6-GHz BW, an output power and power-added efficiency (PAE) close to 2 W and 35%, respectively, together with an extremely low phase and amplitude distortion. The remainder of this article is organized as follows. Section II-A reviews the DPA operating principle and loading conditions. Section II-B derives the combiner's design equations. Section III presents the design charts and application examples. Finally, Sections IV and V discuss the MMIC design and related experimental results under small-, large-, and modulated-signal conditions.

II. Formulation of the Proposed Analysis

A. Review of the DPA Concept

The baseline architecture of a DPA is shown in Fig. 1. It consists of a carrier device, which is always on, and a peaking

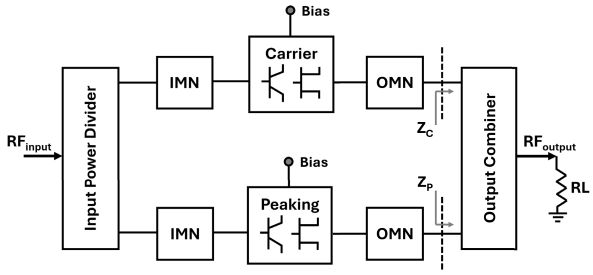


Fig. 1. Circuit diagram of a typical DPA architecture.

device that begins to conduct at a certain input power level. Once turned on, the peaking device actively modulates the load seen by the carrier toward lower impedance values. The proper loading conditions for both devices, Z_{C} and Z_{P}, as well as their modulation behavior along the input power range, must be ensured through the output combiner, starting from the output termination R_{L} (typically 50 Ω). At the same time, it is essential to compensate for the effects of the active-device intrinsic capacitances and parasitics, a task typically performed by the output matching networks (OMNs). On the other hand, the input matching networks (IMNs) and the input divider are designed to match the amplifier to the reference impedance while providing the required power splitting between the two branches. Depending on the combiner topology, bias conditions, and matching strategy, additional elements may be required to ensure the in-phase summation of the currents from the carrier and peaking branches at the output termination.

Before starting the detailed design of a DPA, a set of circuit requirements, including BW, saturated output power (P_{sat}), and OBO, is specified. The OBO, defined as the difference, in dB, between P_{sat} and the output power at which the peaking starts conducting, can also be related to the parameter α as follows:

$$\alpha = 10^{-\text{OBO}/20}. \tag{1}$$

The target P_{sat} typically drives the technology selection, which in turn determines the optimum loads for the carrier and peaking devices at both OBO and saturation conditions. These loads must then be synthesized by the output combiner within the specified BW.

The optimum resistance for the carrier device at saturation, hereinafter denoted as R_{opt}, can be written as

$$R_{\text{opt}} = \frac{\left(V_{\text{S}} - V_{\text{k,C}}\right)^2}{2 \cdot \alpha \cdot P_{\text{sat}}} \tag{2}$$

where V_{S} is the supply voltage and $V_{k,C}$ is the carrier device knee voltage. On the other hand, to maximize the efficiency at OBO, i.e., before the peaking device turns on, the carrier resistance should be equal to

$$R_{\text{opt}}@\text{OBO} = \frac{R_{\text{opt}}}{\alpha}. \tag{3}$$

Similarly, for the peaking device, the optimum resistance at saturation can be expressed as

$$R_{\text{opt}}@sat, P = \frac{\left(V_{\text{S}} - V_{\text{k,P}}\right)^2}{2 \cdot (1-\alpha) \cdot P_{\text{sat}}} = \frac{\alpha \cdot R_{\text{opt}}}{1-\alpha}. \tag{4}$$

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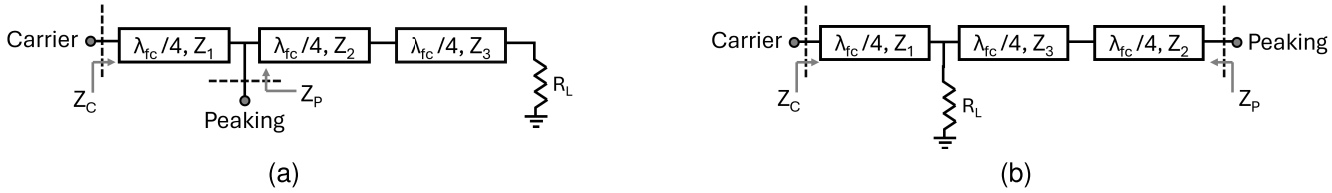


Fig. 2. Structure of the analyzed output combiners, hereafter referred as to (a) Type A and (b) Type B.

At OBO, instead, the load seen by the peaking device should be as close as possible to an open circuit.

The BW achievable by the DPA ultimately depends on how accurately the optimum loading conditions can be maintained across frequency. In this context, the output combiner plays a key role, and it will be shown that, depending on the target R_{opt}, different combiner implementations can achieve superior performance even if composed of the same number of elements.

B. Analyzed Combiner Configurations

Fig. 2 shows the configurations of the two output combiners analyzed in this work. Both are composed of three $\lambda/4$-TLs at the design center frequency (f_c), with characteristic impedances Z_1, Z_2, and Z_3. They differ, however, in the position where the output termination R_L and the peaking device are connected. As will be shown in the following, this structural difference can significantly affect the achievable BW, depending on the target P_{sat} and OBO levels, as well as on the selected device technology. Hereafter, the combiner in Fig. 2(a) is referred to as Type A, whereas the one in (b) is denoted as Type B.

The aim of this comparative analysis is to identify the most favorable topology capable of providing the optimal impedance for both carrier and peaking devices over frequency. To this purpose, matching conditions must initially be established, and the frequency-dependent behavior of the combiners evaluated accordingly. The matching condition for the carrier device at OBO and center frequency is written as

$$Z_{\text{C}}@\text{OBO}\,(f_c) := R_{\text{OBO}} = R_{\text{opt}}@OBO \cdot 10^{k/10}, \quad k \in \mathbb{R} \qquad (5)$$

where the parameter k allows the synthesized load at f_c to slightly differ from the theoretical optimal value ($R_{\text{opt}}@OBO$), providing a free parameter for the optimization of the characteristic impedances of the combiners in a wideband implementation. Indeed, achieving a perfect matching ($k = 0$) clearly provides the best performance for a narrowband amplifier, but selecting a different k may improve its average response over a given BW, depending on the properties of the combiners. This choice is motivated by the fact that k, as discussed in Section III-A, is selected to maximize the BW in back-off operation, which is of particular interest since the average power of modulated signals is expected to lie predominantly in this operating region.

Conversely, for the peaking device at saturation, the optimal loading condition is still maintained as

$$Z_{\text{P}}@sat\,(f_c) := R_{\text{P}} = R_{\text{opt}}@sat, P\,. \qquad (6)$$

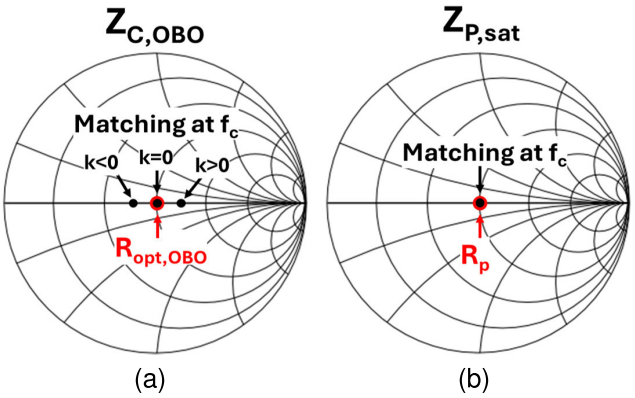


Fig. 3. Matching conditions imposed for (a) carrier and (b) peaking devices.

Indeed, the load presented to the peaking device as a function of frequency cannot be independently shaped. Consequently, the theoretical optimum load is imposed at center frequency, accepting that deviations from the optimum may occur away from it. This represents an acceptable tradeoff since, as discussed previously, a DPA operates predominantly in the OBO region, where the carrier device largely determines the overall amplifier performance.

The conditions expressed by (5) and (6) are graphically illustrated in the Smith charts of Fig. 3.

To derive the following analytical expression, it is also assumed that both devices attain their maximum voltage swing at saturation, defined as $V_{\text{sat}} = 2(V_{\text{S}} - V_{\text{k,C/P}})$, and that the peaking device behaves as an open circuit at OBO. On these bases, the characteristic impedances of the combiners can be extracted accordingly.

1) Type A Analysis: The equivalent circuit of this combiner at OBO and saturation is shown in Fig. 4(a) and (b), respectively.

Using the ABCD matrix formulation of a $\lambda/4$-TL at f_c, the following conditions on the characteristic impedances can be derived:

$$\begin{cases} Z_{1A} = \dfrac{R_P}{2} \cdot \left(\sqrt{1 + 4 \cdot \dfrac{R_{\text{OBO}}}{R_P}} - 1 \right) \\ Z_{2A} = \dfrac{Z_3 R_{\text{P}}}{2\sqrt{R_L R_{\text{OBO}}}} \cdot \left(\sqrt{1 + 4 \cdot \dfrac{R_{\text{OBO}}}{R_P}} - 1 \right). \end{cases} \qquad (7)$$

To accommodate different design requirements, the characteristic impedance Z_3 is left as a free parameter to optimize the matching provided by the combiner, as detailed in Section III-A.

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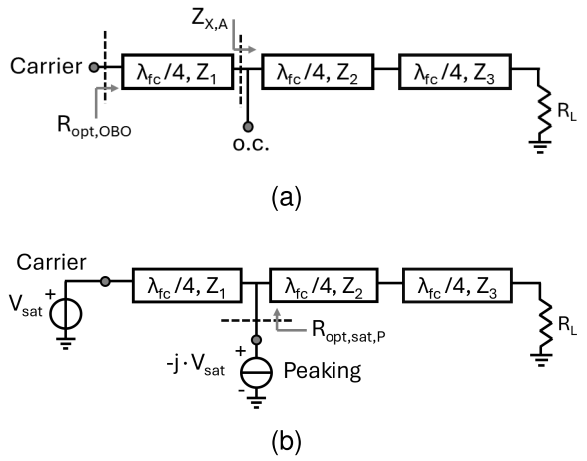


Fig. 4. Equivalent scheme of Type A combiner at (a) OBO and (b) saturation.

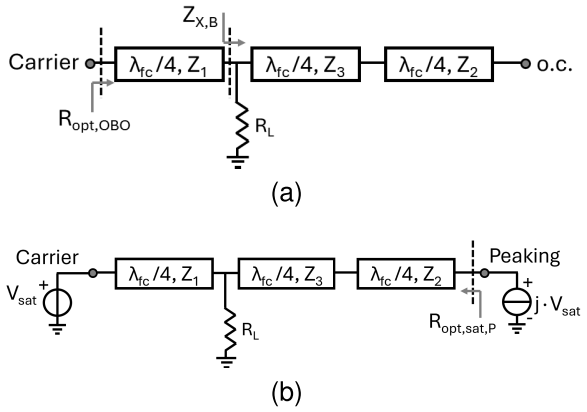


Fig. 5. Equivalent scheme of Type B combiner at (a) OBO and (b) saturation.

2) Type B Analysis: Fig. 5(a) and (b) shows the equivalent circuit of the Type B combiner at OBO and saturation, respectively.

In this case, the system of equations relating the lines' characteristic impedances is

$$\begin{cases} Z_{1B} = \sqrt{R_L R_{\mathrm{OBO}}} \\ Z_{2B} = \dfrac{Z_3 R_P}{2} \cdot \left(\sqrt{\dfrac{1}{Z_{1B}^2} + \dfrac{4}{R_P R_L}} - \dfrac{1}{Z_{1B}} \right). \end{cases} \tag{8}$$

As for the other configuration, the characteristic impedance Z_3 is left as a free parameter to allow flexibility in meeting various design requirements, as detailed in Section III-A.

Furthermore, by analyzing the circuit configurations at saturation, the following expression for the carrier impedance at saturation can be derived for both combiners:

$$Z_{\mathrm{C}}@sat\,(f_{\mathrm{c}}) = \frac{2R_{\mathrm{opt}} \cdot 10^{\frac{k}{10}}}{\alpha \cdot \left(1 + \sqrt{1 + 4 \cdot \frac{1-\alpha}{\alpha^2} \cdot 10^{\frac{k}{10}}}\right)}. \tag{9}$$

The variation of $Z_{\mathrm{C}}@sat$ relative to R_{opt} depending on the sign of k is illustrated in Fig. 6. This behavior directly follows from the loading condition imposed in the OBO region.

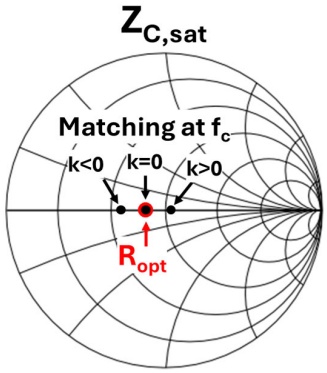


Fig. 6. Behavior of the carrier impedance at saturation at f_{c} based on k.

III. Design Charts and Use Cases

A. Design Charts

The goal is to identify, for each combiner topology, the set of Z_1, Z_2, and Z_3 that results in the optimal loading condition for the devices while satisfying the constraints given in (7) and (8). To this end, the magnitude of the reflection coefficient presented to the carrier device at OBO ($|\Gamma_{\mathrm{OBO}}|$) is evaluated. The latter is defined as

$$\Gamma_{\mathrm{OBO}} = \frac{Z_{\mathrm{C@OBO}}(f) - R_{\mathrm{opt@OBO}}}{Z_{\mathrm{C@OBO}}(f) + R_{\mathrm{opt@OBO}}} \tag{10}$$

where $Z_{\mathrm{C}}@OBO$ is the combiners' synthesized impedance over frequency while $R_{\mathrm{opt}}@OBO$ is the optimum condition. For both combiners, $Z_{\mathrm{C}}@OBO$ is defined by the following equation:

$$Z_{\mathrm{C}}@OBO = Z_1 \cdot \frac{Z_{\mathrm{X}} + jZ_1 \tan(\theta)}{Z_1 + jZ_{\mathrm{X}} \tan(\theta)} \tag{11}$$

where $\theta = \pi/2 \cdot f/f_c$ and Z_{X} is the residual impedance seen on the right side of the $\lambda/4$-TL in front of the carrier device [see Figs. 4(a) and 5(a)], which differs between Types A and B.

In both configurations, the reflection coefficient Γ_{OBO} is a function of the OBO value (α), the frequency (θ), the matching of the carrier at f_{c} (i.e., the k parameter), the optimum load of the carrier device [R_{opt} defined in (2)], the characteristic impedance Z_3, and the external load termination R_{L}. The objective of this analysis is to provide a practical design tool for selecting the most suitable combiner configuration under given design constraints. To this aim, graphical design charts, obtained by numerically evaluating Γ_{OBO} under the discussed boundary conditions of the matching problem, are much more effective than closed-form expressions. Moreover, to carry out a fair comparison between the two combiners and allow for a more effective interpretation of the available design space, the output termination in the following charts is fixed to $R_{\mathrm{L}} = 50\,\Omega$. For this reason, the use of an additional PMN at the combiner output, which is typically unfeasible in MMIC implementations due to its associated losses and occupied area, is not considered in this work.

Four different scenarios have been analyzed, i.e., OBO = 3, 6, 9, and 12 dB. For each case, the parameters k and Z_3 are determined through a systematic optimization that identifies the combination of values that minimizes the maximum of

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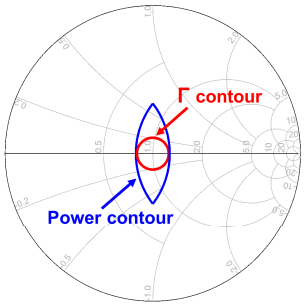


Fig. 7. Normalized 1-dB constant power contour and constant reflection coefficient contour.

$|\Gamma_{OBO}|$ for each target R_{opt} and BW, up to 200 Ω and 100%, respectively. The procedure aims at achieving the flattest possible in-band response of the reflection coefficient for target specifications.

A maximum value of −15 dB for dB($|\Gamma_{OBO}|$) is assumed, which, when (10) is evaluated at f_c, restricts the range of investigated k values to approximately $[-1.5, 1.5]$. According to the constant power contours theory [27], the parameter k can be related to the corresponding power decrease with respect to the optimum at f_c, which is therefore limited to 1.5 dB. The main reason for basing the analysis on constant-reflection-coefficient contours rather than constant-power contours is that the latter are derived under linear class A operating conditions and may therefore become inaccurate when applied to different operating regimes. On the contrary, the reflection coefficient provides a more general matching metric whose validity extends beyond these assumptions, making it more suitable for comparing the two combiner topologies. It is also worth noting that the condition on the reflection coefficient is more restrictive than the one imposed by the constant-power contours. As can be observed in Fig. 7, for example, considering $k = \pm 1$, the region of the Smith chart enclosed by the constant-reflection-coefficient contour is smaller than that enclosed by the constant-power contour.

Concerning the investigated Z_3 values, the range from 5 to 100 Ω is selected based on the impedance values that can be practically realized across different technologies. The corresponding Z_1 and Z_2 values are determined accordingly. Any solution that does not satisfy the specified design constraints, namely a maximum reflection coefficient exceeding −15 dB or impedance values outside the prescribed range in the evaluated BW, is discarded.

The resulting contours of dB($|\Gamma_{OBO}|$) for both combiners and different OBO values are plotted in Fig. 8. The regions between contours, represented by solid lines for Type A and by dashed lines for Type B, define the achievable matching quality in terms of reflection coefficient ranges bounded by adjacent levels (i.e., less than −15 dB, −15 to −20 dB, −20 to −30 dB, −30 to −40 dB, or better than −40 dB). The colored areas (light blue for Type A and yellow for Type B) indicate which combiner provides the more favorable matching, i.e., a lower reflection coefficient for the desired fractional BW and R_{opt}. The white areas indicate that a return loss better than 15 dB cannot be achieved by either of the two combiners. For instance, considering the case of 6-dB OBO in Fig. 8, a reflection coefficient better than −30 dB over a 20% BW with R_{opt} = 60 Ω can be achieved only with the Type B. Conversely, a return loss better than 30 dB over a 10% BW with R_{opt} = 20 Ω is obtained only with the Type A. On the other hand, a return loss better than 20 dB over a 30% BW with R_{opt} = 100 Ω can be achieved with both combiners according to $|\Gamma_{OBO}|$ contours, although the Type B combiner is the preferred option (Type B colored region).

The corresponding lines' characteristic impedances Z_1, Z_2, and Z_3 are shown in Fig. 9 for Type A and in Fig. 10 for Type B, with respect to different OBOs. The plots show the characteristic impedance values to be selected to cover the desired BW, with R_{opt} as the optimal carrier impedance, and the matching level indicated in Fig. 8.

B. Use Cases Examples

At first, the target values of OBO and BW must be selected. Then, the optimum load of the carrier device should be estimated using (2) or derived through load—pull analysis, depending on the required output power, technology, and typology of active device. Design charts guide the selection of the combiner topology and of the characteristic impedances of the three $\lambda/4$-TLs for the implementation of the DPA. Indeed, for a given set of BW, OBO, and R_{opt}, the corresponding point of interest can be identified through Fig. 8. Once located, the constant matching contours allow us to determine the achievable return loss with each combiner topology. Moreover, the colored regions indicate the preferred DPA combiner. If the point lies within a region that violates the return loss specification, the proposed combiners cannot, in principle, meet the required performance. As discussed previously, although only an estimate can be obtained, the expected in-band power reduction relative to the optimum OBO condition can be calculated as

$$\Delta P\ (dB) = 10 \cdot \log_{10}\left(\frac{1 + 10^{\frac{|\Gamma_{OBO,Max}|}{20}}}{1 - 10^{\frac{|\Gamma_{OBO,Max}|}{20}}}\right) \tag{12}$$

where $|\Gamma_{OBO,Max}|$ is the value in dB defined by the contours in Fig. 8. It is worth emphasizing that ΔP is defined with respect to the power that would be obtained by matching the load to $R_{opt,OBO}$, rather than to the in-band ripple, which may result in being lower than ΔP.

Some examples of design requirements and the obtained Z_1, Z_2, and Z_3 values are reported in Table I, for both combiners. The impedances are selected based on the contour plots of Figs. 9 and 10 and the target design point. The simulated frequency behavior of $|\Gamma_{OBO}|$, for the use cases reported in Table I, is shown in Fig. 11. As expected, such results are well in agreement with the values predicted by the contour plots of Fig. 8.

In addition to selecting the combiner exhibiting the more advantageous $|\Gamma_{OBO}|$, the choice between the two topologies can also be driven by the available technology for implementing the $\lambda/4$-TLs with characteristic impedances Z_1, Z_2, and Z_3. The Type A combiner typically requires lower characteristic impedances compared to the Type B configuration.

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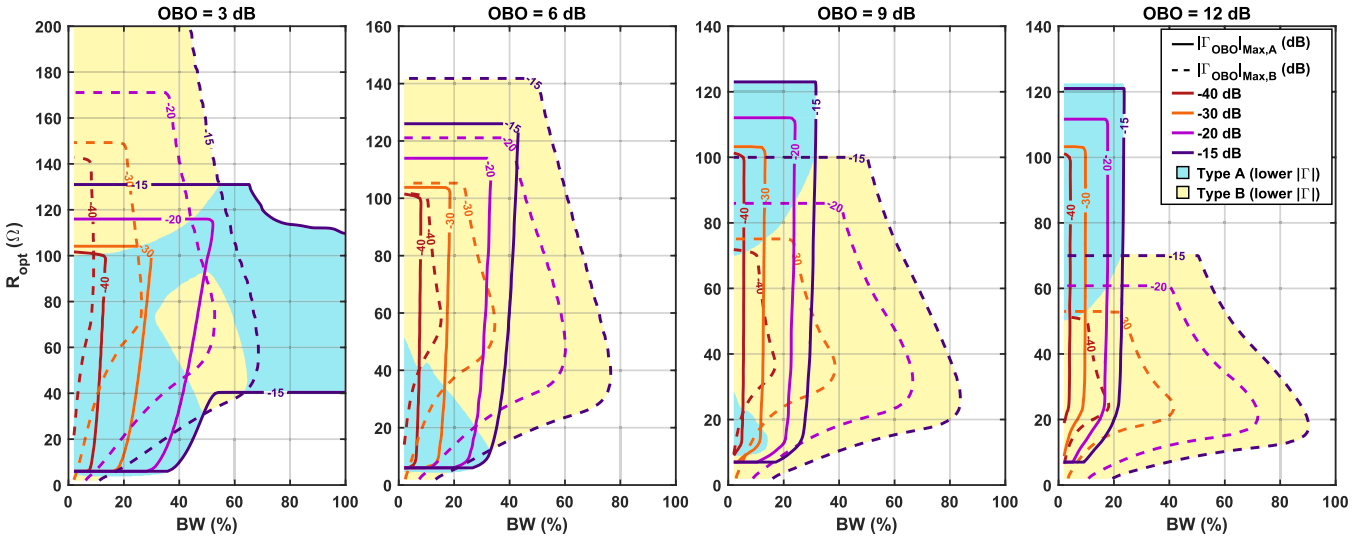


Fig. 8. Contour plots of the maximum value of $|\Gamma_{OBO}|$ in dB for the Type A (solid lines) and B (dashed lines) combiner, in the case of 3-, 6-, 9-, and 12-dB OBO. Colored regions indicate which combiner provides the lower maximum reflection coefficient relative to R_{opt} and BW.

TABLE I
CHARACTERISTIC IMPEDANCES $Z_{1/2/3}$ SELECTED FOR DIFFERENT DESIGN SPECIFICATIONS AND CORRESPONDING MAXIMUM $|\Gamma_{OBO}|$

OBO (dB)	$\mathbf{R_{opt}}$(Ω)	**BW** (%)	**Comb.**	$\|\Gamma_{OBO}\|$(dB)	$\mathbf{Z_3}$(Ω)	$\mathbf{Z_2}$(Ω)	$\mathbf{Z_1}$(Ω)
12	40	20	A	-17	15	6.5	34
			B	-36	60	27	88
9	100	15	A	-28.5	25	21	96
			B	-15.5	35	30	100
6	60	35	A	-18	29	22	50
			B	-29	95	73	75
3	80	60	A	-17	56	62	92
			B	-18.5	100	98	66

Therefore, power-handling capability, layout constraints, and transmission-line losses may also be taken into account, leading to a tradeoff among these factors.

C. Discussion on the Impact of Device Nonidealities

The active device output nonidealities have not been included in the analysis and in the derivation of the design charts, as the OMN is assumed to compensate for them. Nevertheless, these effects may limit the overall BW of the DPA.

Assuming that the outputs of the peaking and carrier devices can be modeled by an equivalent parallel RC circuit, and that an OMN is employed to compensate for capacitive effects [Fig. 12(a)], the resulting reflection coefficient can be indicated as Γ_{OMN}. By invoking the Bode–Fano criterion [28], a theoretical upper bound of the achievable BW of this network can be calculated as

$$BW_{OMN} \leq \frac{\pi}{\omega_0 RC \ln\left(\frac{1}{|\Gamma_{OMN}|}\right)} = \frac{\pi}{Q \ln\left(\frac{1}{|\Gamma_{OMN}|}\right)} \tag{13}$$

where Q is the quality factor of the device output section, which depends on frequency and technology. The reflection coefficient Γ_{OBO} obtained from the design charts reported above can be considered as the target matching specification for the OMN. Therefore, the effective BW of the DPA can be empirically approximated as

$$BW_{DPA} \approx \min\left(BW_{OMN}, BW_{COMB}\right) \tag{14}$$

where the overall BW is determined by the most limiting of the two contributions. Therefore, from a synthesis perspective, if the maximum fractional BW allowed by the OMN is significantly larger than the target operational BW of the combiner (BW_{COMB}), the physical constraints imposed by the Bode–Fano criterion at the device's output do not represent a critical limiting factor. In this case, the required matching BW (BW_{OMN}) can be achieved without resorting to high-order, highly complex OMN topologies.

An alternative approach is to absorb the active device output capacitances into the combiner, as shown for example in Fig. 12(b). Assuming identical output capacitances for the carrier and peaking devices, a condition that can be enforced by adding a shunt capacitor to the device exhibiting the smaller capacitance, the two capacitances can be absorbed into equivalent transmission lines having an electrical length θ_i^* and characteristic impedance Z_i^* according to the following relationships [8]:

$$\begin{cases} \theta_i^* = \arccos\left(\omega_c C Z_i\right) \\ Z_i^* = \dfrac{Z_i}{\sqrt{1-(\omega_c C Z_i)^2}} \end{cases} \tag{15}$$

where Z_i is the characteristic impedance of one of the $\lambda/4$-TLs derived from the proposed analysis and ω_c is the angular center frequency. The latter equations are limited by the condition $\omega_c C Z_i < 1$, and the resulting impedance Z_i^* is always higher than the initial Z_i, thereby limiting the applicability range of this approach. Moreover, these equations are valid at the design center frequency, and the response of the combiner becomes increasingly asymmetric as the capacitance increases.

Another aspect to be considered is that the presented analysis assumes an ideal open-circuit condition for the peaking in

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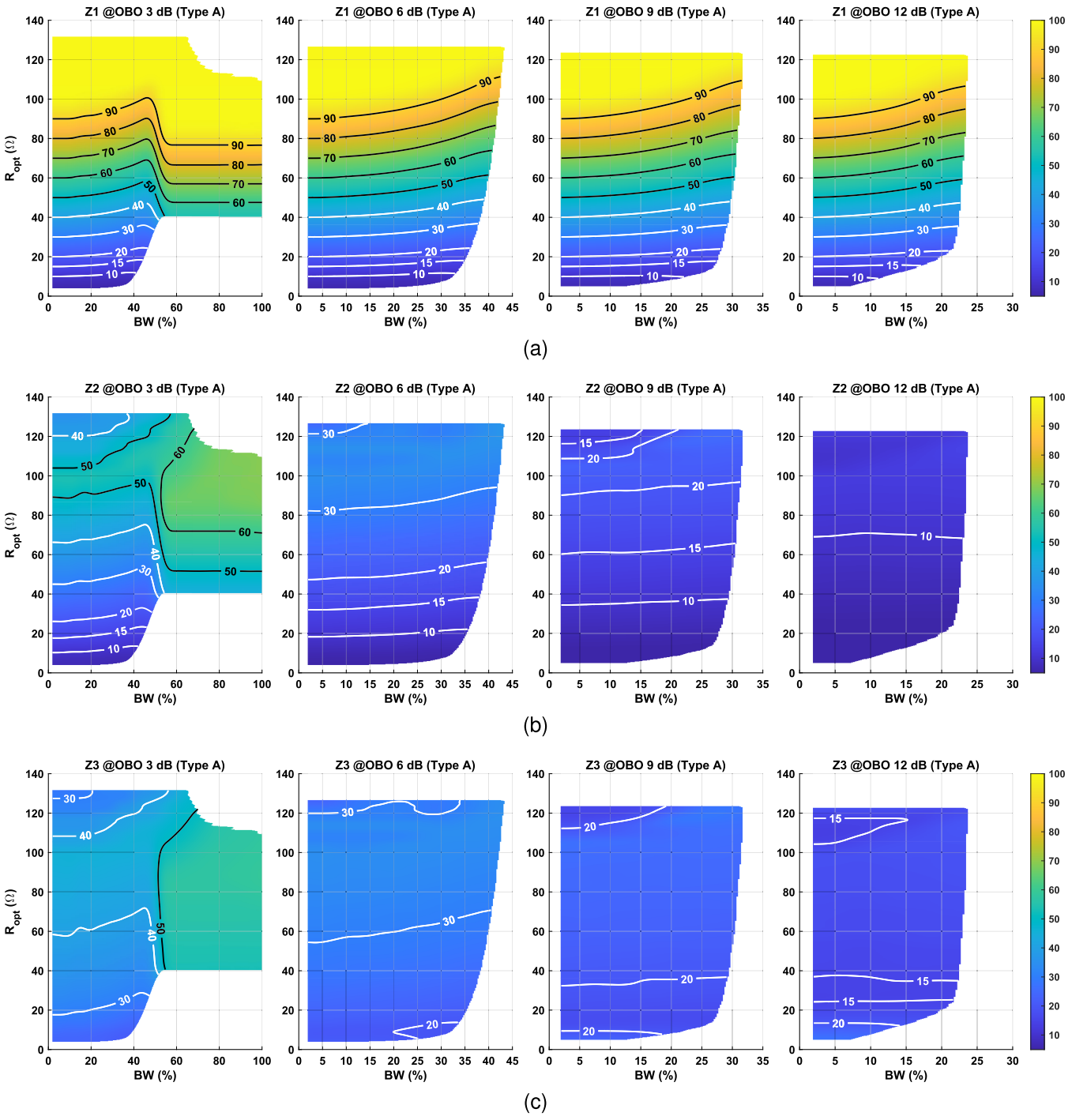


Fig. 9. Plots representing the value of (a) Z_1, (b) Z_2, and (c) Z_3 for Type A combiner at 3, 6, 9, 12 dB of OBO, as obtained from the optimization procedure.

back-off. In practical operation, the peaking device typically exhibits a high OFF-state impedance with a capacitive behavior, which can be approximated by a capacitance in parallel with a high-value resistance. The resistive effect can generally be neglected, while the capacitive behavior can be compensated for through the OMN or directly incorporated into the combiner design, as previously discussed. Furthermore, an offset line could be inserted along the peaking amplifier path, with its electrical length properly selected to transform its OFF-state impedance toward an open-circuit condition at the carrier combining point [29], [30]. These techniques can be used to mitigate the effects of the nonideal peaking OFF-state impedance, allowing the practical implementation to closely approach the ideal open-circuit condition assumed in the analytical model.

Despite these considerations, the most effective strategy for mitigating device nonidealities is application-dependent and extends beyond the scope of this work. Nevertheless, the comparative analysis presented herein remains generally applicable, regardless of the adopted compensation strategy,

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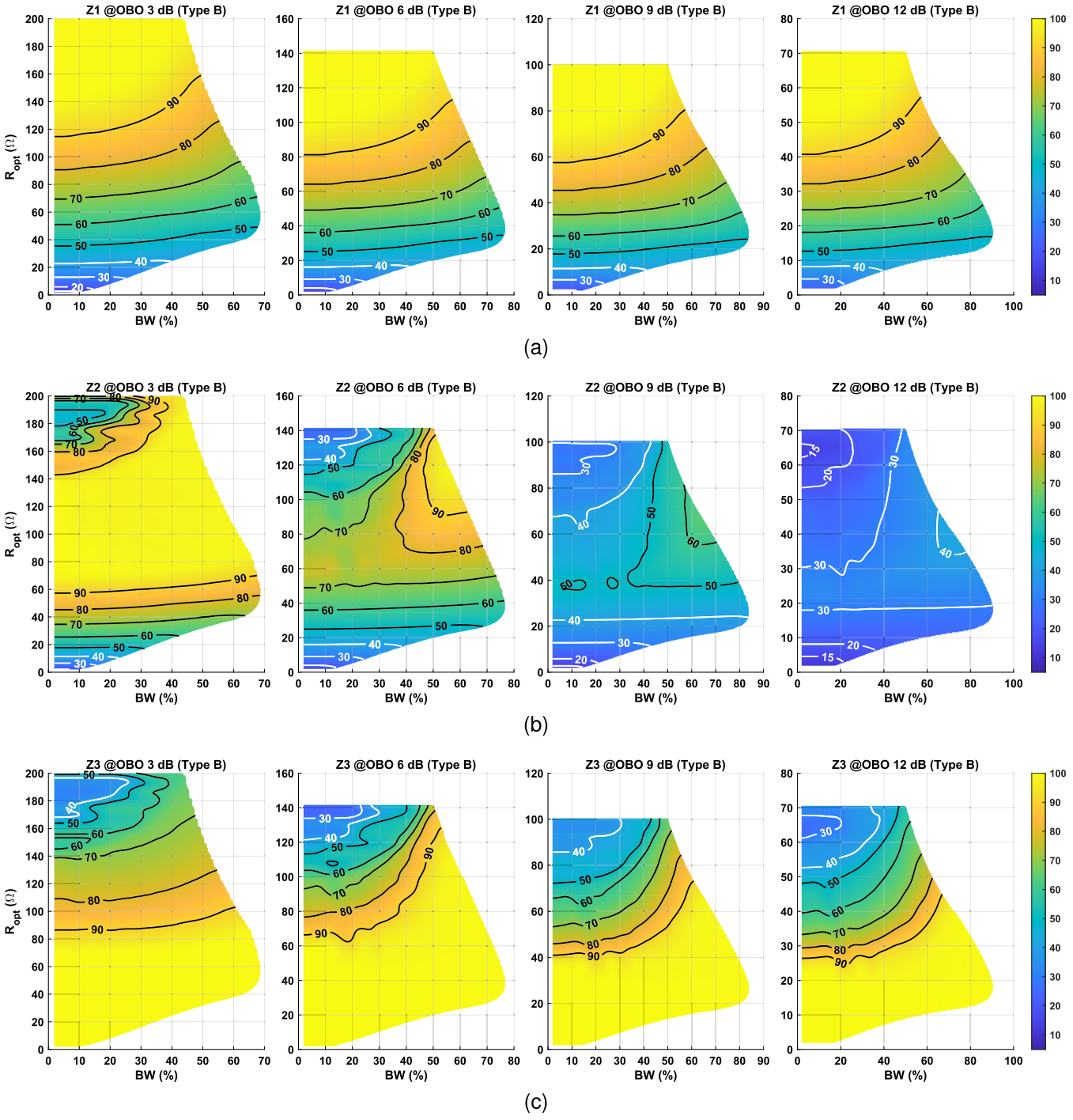


Fig. 10. Plots representing the value of (a) Z_1, (b) Z_2, and (c) Z_3 for Type B combiner at 3, 6, 9, 12 dB of OBO, as obtained from the optimization procedure.

and provides practical design guidelines for selecting the most appropriate combiner configuration based on the DPA requirements and the constraints imposed by the adopted technology.

IV. MMIC DPA Design

The design of a MMIC DPA, implemented in the 5 V H20U-C4 InGaP/GaAs HBT technology by WIN Semiconductors, is presented in this section. The output combiner of the DPA is designed according to the theoretical analysis presented above. The DPA is intended for high-linearity sub-6-GHz wireless communication systems employing modulated waveforms, particularly for Wi-Fi six systems. The design aims at achieving 32 dBm of P_{sat} with 6 dB of OBO within the frequency range 5–6 GHz. The advantages of HBTs lie in their high-linearity operation, but the low power density of the process necessitates combining multiple transistors to achieve sufficient power levels. Thus, a power cell (PC) combining four HBTs in parallel, each with four fingers of 3-μm width and 40-μm length, was designed for the final stage of the carrier and peaking branches [31]. The thermal and RF

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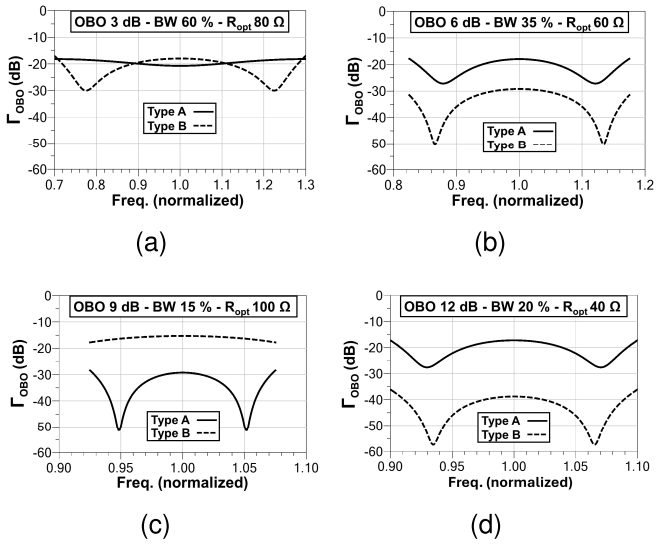


Fig. 11. Behavior of the reflection coefficient $|\Gamma_{OBO}|$ in dB, for the various design requirements in Table I: (a) OBO = 3 dB, (b) OBO = 6 dB, (c) OBO = 9 dB, (d) OBO = 12 dB.

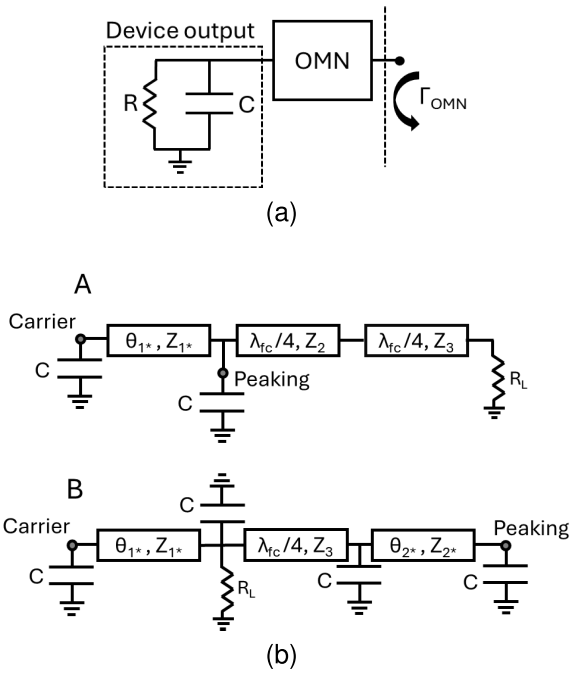


Fig. 12. Two possible approaches to compensate for device nonideal effects. (a) Using an OMN and (b) absorbing the output capacitances into the combiner.

stability of the amplifier was enhanced by acting at the PC level, leading to the final circuit implementation shown in Fig. 13. Each elementary transistor was equipped with an individual ballast resistor *RB* to prevent device failure caused by self-heating and current hogging phenomena [32]. In addition, the series network consisting of r_b = 2.1 Ω and C_b = 1.7 pF was introduced to ensure RF small-signal stability across the entire operating band according to Rollett's stability criterion [33]. Finally, *RP* = 65 Ω and *RC* = 14.9 Ω were included to suppress internal loop oscillations. The latter resistor values were determined according to Ohtomo's stability test under both small-signal and large-signal operating conditions [34].

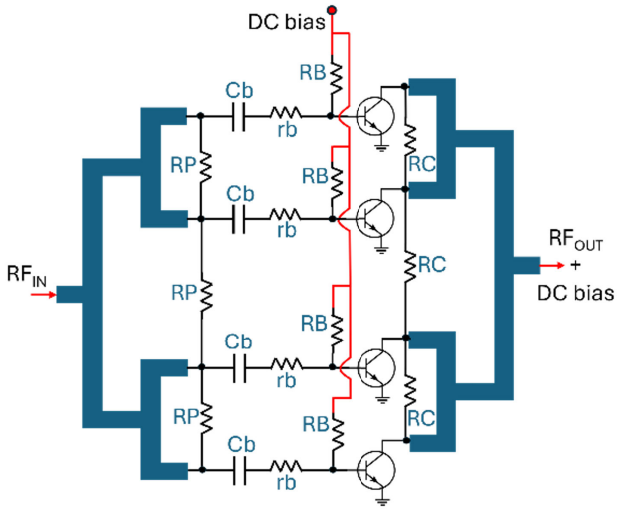


Fig. 13. Carrier and peaking final stage devices composed of four elementary HBTs.

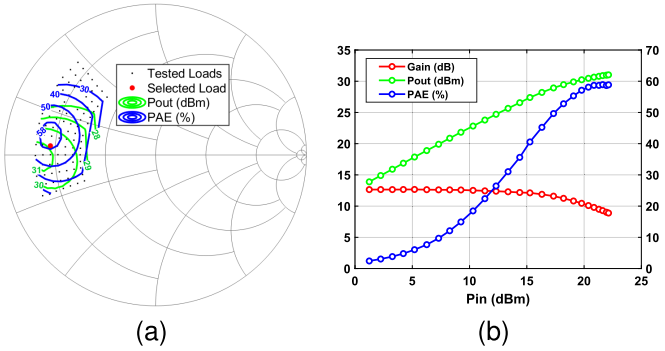


Fig. 14. (a) Investigated loads and selected one and (b) measured performance with the selected load.

The PC, with a total active periphery of 1920 μm^2, was manufactured and tested with a load—pull system at 5.5 GHz. The cell was biased with a collector voltage and quiescent current of V_C = 5 *V* and I_{CQ} = 192 mA, respectively. Fig. 14 shows a picture of the tested loads and the measured performance in terms of PAE, output power, and gain for the selected optimum one of $(8.8 + j \cdot 2)\,\Omega$. On this load, the PC is able to deliver more than 30 dBm of output power with almost 60% of PAE. After de-embedding the output intrinsic capacitance, this load is found to correspond to an optimal resistance of approximately R_{opt} = 8 Ω at the equivalent intrinsic plane of the PC.

Having selected the OBO, BW, and R_{opt}, it is possible to extract from Figs. 8–10 the minimum achievable matching at OBO ($|\Gamma_{OBO}|$) and the corresponding range of characteristic impedances (Z_1, Z_2, and Z_3), respectively, within the region of interest for both Types A and B combiners. It is important to remark that the reflection coefficient contours and corresponding values refer to the worst case matching condition within the selected BW. Table II summarizes the DPA design parameters and the corresponding ranges of characteristic impedances and $|\Gamma_{OBO}|$ for the two possible combiners, as obtained from the graphs. The Type A combiner was selected over the Type B configuration because of its superior return-

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TABLE II
DESIGN SPECIFICATIONS AND COMBINER CHARACTERISTICS

OBO	BW	R_{OPT}	Comb.	$\lvert\Gamma\rvert_{OBO}$ (dB)	Z_1 (Ω)	Z_2 (Ω)	Z_3 (Ω)
6 dB	18%	8 Ω	Type A	[-30,-20]	[5,10]	[5,10]	[20,30]
			Type B	[-20,-15]	[20,30]	[20,30]	[90,100]

loss performance and lower characteristic impedances. On the contrary, the Type B requires a significantly higher value of Z_3, making its MMIC implementation less attractive. The corresponding high-impedance transmission line requires very narrow conductor width, which may increase electric-field concentration, reduce power-handling capability, and increase sensitivity to fabrication tolerances.

The characteristic impedances of the selected Type A combiner were fine-tuned, resulting in the following values: $Z_1 = 7.5\,\Omega$, $Z_2 = 6.5\,\Omega$, and $Z_3 = 23\,\Omega$. To proceed with the DPA design process, the PC output nonidealities need to be accounted for. Accordingly, nonlinear simulations of the PC-biased in class AB were performed to extract an equivalent parallel RC model for its output section, yielding $R = R_{opt}$ and $C = 1$ pF. By calculating the quality factor at $f_c = 5.5$ GHz and imposing $|\Gamma_{OMN}| = 0.1$ (-20 dB is the theoretical worst matching provided by the combiner), using (13) and (14), it can be noticed that BW_{OMN} is much greater than $BW_{DPA} = 18\%$. Therefore, an OMN-based strategy was adopted to compensate for nonideal device effects. In particular, the collector bias line was exploited by optimizing its length and width. This also applies to the peaking, where a slightly higher capacitance value (1.6 pF) was used to emulate its behavior under off-bias conditions in the frequency range of interest.

Then, as a compromise between achievable performance and layout area, $\lambda/4$-TLs were implemented through a semidistributed approach. Z_3 and Z_2 were realized through a low-pass Π-network where the two adjacent capacitors are merged into a single one. Due to the nonnegligible sensitivity of large-signal performance to the second harmonic load, this low-pass topology was also leveraged to enforce a near-short-circuit condition. A semidistributed approach was applied for the implementation of Z_1 as well, where the $\lambda/4$-TL consists of a T-network in which two series capacitors are separated by a short-circuited stub. The Type A combiner as designed and including output device capacitances, prior to full EM and global optimization, is shown in Fig. 15(a). A comparison between the simulated performance of the theoretical combiner, composed of ideal $\lambda/4$-TLs, and the real combiner is shown in Fig. 15(b) at back-off and in (c) at saturation, where ideal voltage and current sources are used for the evaluation. Notably, the translation from ideal to real network does not introduce significant issues.

After designing the final stage, two additional driver stages were implemented to maximize gain while keeping the MMIC size compact. The tradeoff between efficiency and linearity was addressed by adopting a 2:1 active periphery ratio across the final, driver, and predriver stages, i.e., the driver device comprises a PC of two elementary HBTs, while the predriver uses a single transistor. A detailed circuit diagram of the final

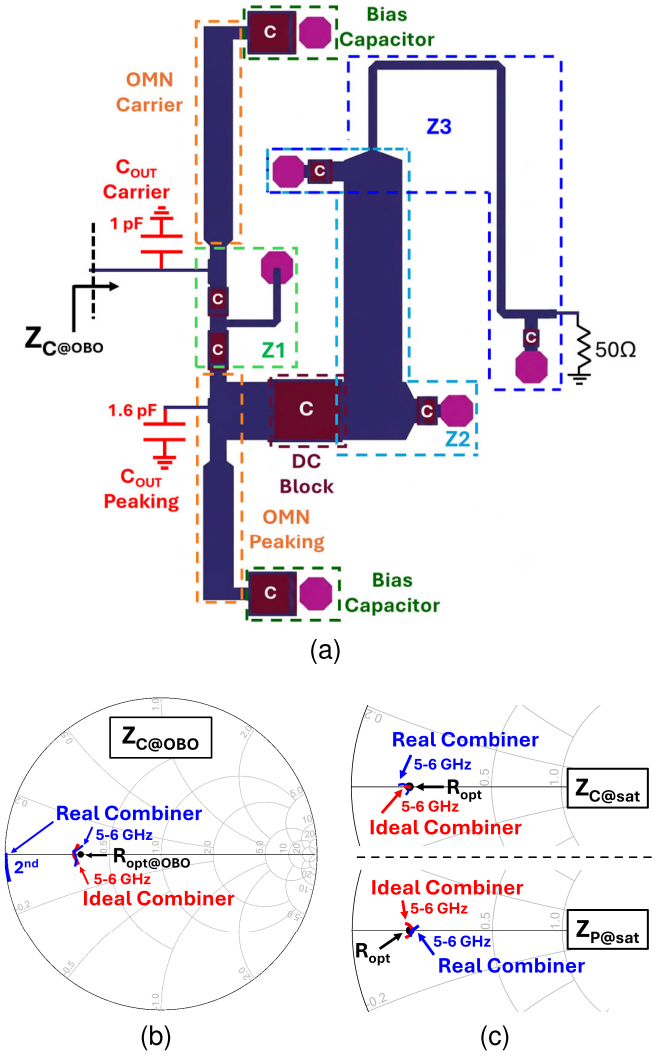


Fig. 15. (a) First version of the layout of the realized combiner, (b) comparison between the OBO carrier impedance of the ideal and real combiners, and (c) carrier and peaking loads at full power condition. The 2nd harmonic load is evaluated at the combiner plane.

version of the DPA, showing all components and their values, is presented in Fig. 16. Matching between stages was achieved through interstage matching networks (ISMNs) consisting of third-order high-pass filters and a collector bias line that serves to neutralize the residual capacitive effects at the device outputs. The active bias scheme used in each stage, which incorporates a linearizing capacitor [35], is also reported in Fig. 16. The resistance was adjusted for each stage to provide proper bias currents while maintaining a fixed base supply voltage of 2.8 V. The input of each branch was finally matched to 50 Ω via a lumped IMN, while the phase misalignment is corrected by a lumped phase compensation network (PCN) placed at the input of the carrier branch. The overall DPA architecture is then completed with a lumped 3 dB Wilkinson power divider. A full lumped-element implementation has been adopted at the input since the lower power levels allow the use of inductors for area reduction. The final layout was carefully optimized through EM simulations, and a microscope image of the fabricated MMIC is shown in Fig. 17.

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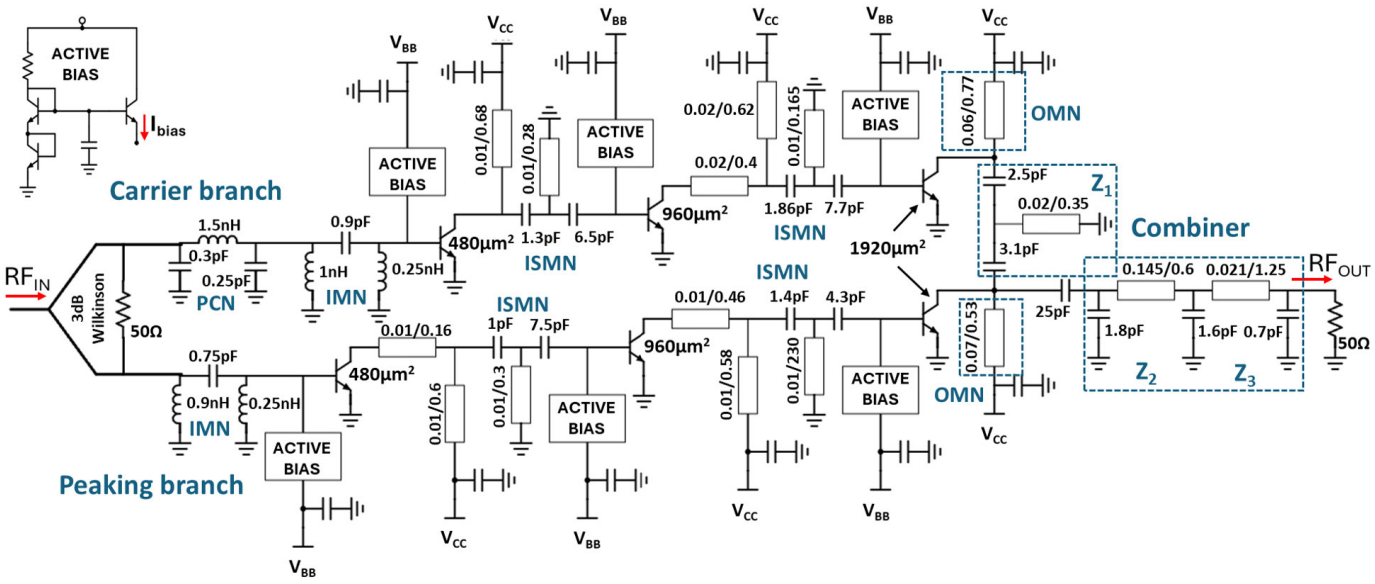


Fig. 16. Circuit diagram of the three-stage DPA, showing the values of lumped and distributed elements (length mm/width mm).

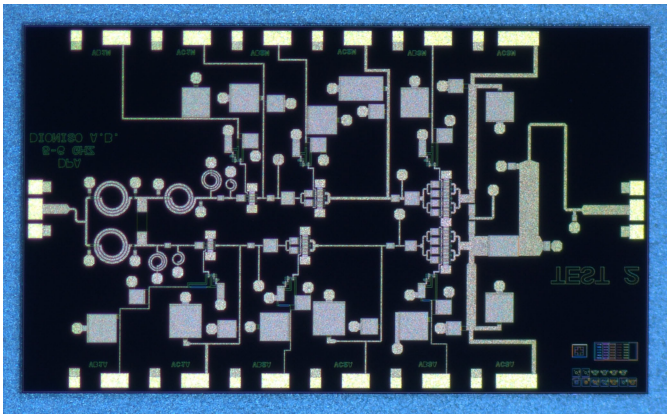


Fig. 17. Picture of the realized integrated DPA in HBT technology (size: 4.5 × 2.5 mm).

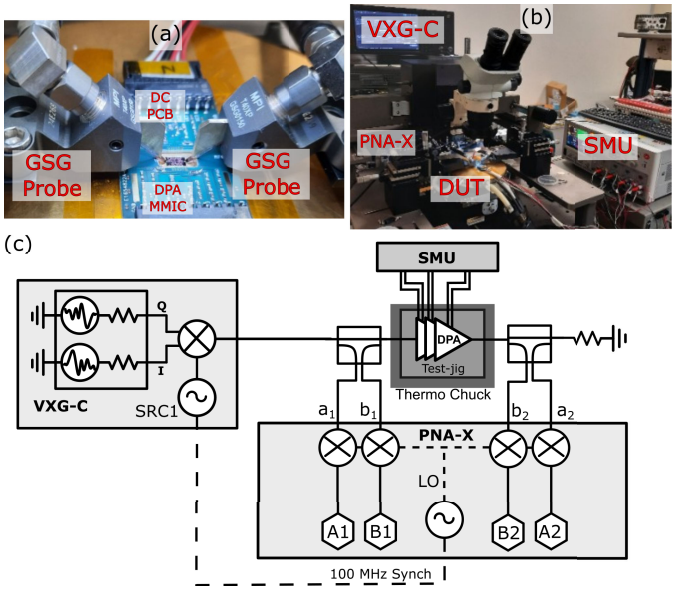


Fig. 18. (a) Test board for the DPA MMIC. Picture (b) and block diagram (c) of the measurement setup for the CW/modulated measurements.

V. Experimental Results

A. Measurement Setup

The MMIC was directly mounted onto a gilded copper carrier using a high thermal conductivity silver-loaded epoxy, which is then placed directly on a probe-station thermal chuck with a fixed baseplate temperature T_{bp} = 25 °C for all the measurements. The MMIC is DC-biased through a wire-bonded low-frequency FR4 PCB, mounted on the same metal carrier, providing additional levels of bypassing through SMD capacitors. Instead, the RF input and output are directly contacted through ground-signal-ground (GSG) probes (MPI T67LL-GSG0150-JC). The test board setup is shown in Fig. 18(a). The test bench for modulated and CW characterizations is instead shown in Fig. 18(b) and (c). The DPA is excited at the input by a vector signal generator (VSG, Keysight VXG-C M9484C), while incident and reflected waves at the device under test (DUT) reference planes are sampled through a direction coupler and acquired by a vector network analyzer (VNA, Keysight PNA-X N5247C) configured in spectrum analysis mode in order to reconstruct complex-modulated envelopes. All the measurements are short-open-load-thru (SOLT) and power calibrated up to the probe tips using the probe manufacturer's standard calibration substrate.

B. Small-Signal and CW Measurements

The DUT was initially characterized under small-signal and CW conditions. The base supply voltage was set to V_{BB} = 2.8 V, providing a class AB bias for the carrier branch and a class B bias with minimal current for the peaking branch. A class B bias was selected for the peaking branch as it allows for a smoother transition within the Doherty region, thus improving the linearity of the amplifier. The resulting collector quiescent currents of the carrier stages (predriver,

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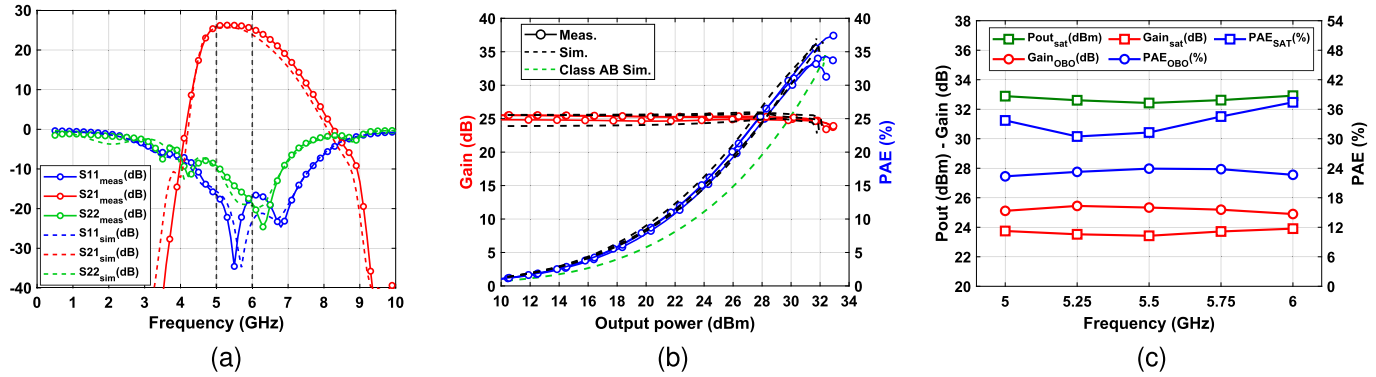


Fig. 19. (a) Comparison between measured (solid lines with circles) and simulated (dashed lines) small-signal parameters. Large-signal characterization: (b) gain and PAE versus output power and (c) performance at 6 dB OBO and saturation.

driver, and final) are 24, 46, and 92 mA, whereas those of the peaking are 3, 6, and 11 mA.

Fig. 19(a) shows the comparison between measured and simulated scattering parameters. In the frequency range from 5 to 6 GHz, a small-signal gain higher than 25 dB was registered, with an input and output return loss better than 16 and 10 dB, respectively.

Following small-signal characterization, the DPA was tested under large-signal CW operation to evaluate its power performance. Fig. 19(b) illustrates the measured gain and PAE as a function of output power at center frequency and at the band edges, compared with DPA simulations and class AB simulated PA. The DPA exhibits an efficiency profile similar to that of the class AB amplifier because of the selected bias condition for the peaking branch. Nevertheless, an efficiency improvement of more than 5% is still achieved. On the other hand, the gain remains highly linear from small-signal operation to saturation, owing to the adopted bias scheme and the proper synchronization of the carrier and peaking branches. In Fig. 19(c), the measured performance at 6-dB OBO and at saturation are also reported. The DPA achieves a peak output power of 32.9 dBm and a peak PAE of 37.5%, with the latter exceeding 23% at 6 dB OBO. It is also worth noting that the in-band power ripple is limited to less than 0.5 dB, demonstrating the effectiveness of the proposed analysis in achieving a very flat in-band response through the appropriate selection of the combiner and the characteristic impedances of the $\lambda/4$-TLs.

C. Linearity Characterization

The linearity of the DPA was evaluated using an 80-MHz-instantaneous BW 802.11ax (Wi-Fi 6) MCS11 modulated (1024-QAM) signal centered at 5.5 GHz across different OBO levels. The error vector magnitude (EVM) is taken as the key reference metric in this respect. The specific excitation used in this test is derived by closely approximating the complete standard-compliant waveforms (generated using MATLAB WLAN Toolbox) with a periodic compact test signal using the methodology in [36]. This allows reducing characterization time while, at the same time, complying with the requirements of a calibrated VNA-based platform and improving dynamic range through coherent averaging. In this framework, EVM is computed through a spectral-domain cross correlation between the input and output signals of the DUT, accounting for receiver equalization, with overlapping results with respect to classical vector-signal-analyzer-based methods [37].

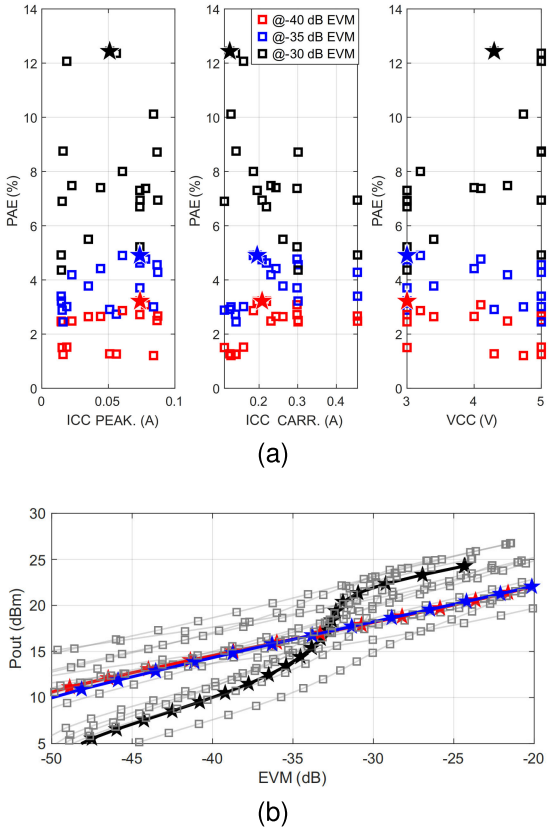


Fig. 20. (a) Results of the bias optimization process targeting the highest PAE at different EVM levels at 5.5 GHz and (b) corresponding output power. The star symbols identify the best performance for each EVM treshold: −40 dB (red), −35 dB (blue), and −30 dB (black).

The bias conditions of the carrier and peaking amplifiers strongly influence the DPA linearity, as they can affect both amplitude and phase distortions, either improving or degrading performance. Thus, to maximize EVM performance, a bias optimization strategy was carried out, targeting the highest measured PAE at EVM thresholds of −40 dB (1%), −35 dB (1.8%), and −30 dB (3%). The optimization, based on an

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TABLE III
COMPARISON WITH SOA INTEGRATED DPAS TARGETING COMPARABLE BW AND OPERATING AT SIMILAR FREQUENCIES

	Reference	[39]	[40]	[41]	[42]	[43]	T.W.
	Technology	GaAs HBT	GaN	GaAs pHEMT	GaN	GaAs pHEMT	**GaAs HBT**
	Freq. / BW (GHz)	3.3-4.2 / 1	4.5-6 / 1.5	4.6-5.6 / 1	5.1-5.9 / 0.8	7.2-8.7 / 1.5	**5-6 / 1**
CW	**SS Gain (dB)**	26.2-28.1	N.A.	12.5*	14.4	8*-12.8	**25**
	$P_{OUT\,@SAT}$ (dBm)	33.4-34.8	35-36	29.8-31	36-38.7	23.5-24.5	**32.5-32.9**
	$Gain_{@SAT}$ (dB)	N.A.	6-8.5*	12* @4.9 GHz	8* @5.9 GHz	5* @8 GHz	**23.5-23.9**
	$PAE_{@SAT}$ (%)	38-43	31.8-40.7	41-46	43.2-47.3	46-58.3 (DE)	**30.5-37.5**
	$Gain_{@6\,dB}$ (dB)	N.A.	7.5-11*	14* @4.9 GHz	13* @5.9 GHz	10.6 @8 GHz	**24.9-25.3**
	$PAE_{@6\,dB}$ (%)	22-24*	22.5-27.6	24-27	31.6-49.5	46-58.3 (DE)	**23-24**
	P_{OUT} in-band ripple (dB)	1.4	1	1.2	2.7	1	**0.4**
MOD.	**Signal**	5G NR	-	-	802.11ac	-	**802.11ax**
		256 QAM	64 QAM	-	256 QAM	-	**1024 QAM**
	BW (MHz)	100	100	-	80	-	**80**
	EVM (%)	1/1.8/3	3	-	2.5	-	**1/1.8/3**
	P_{OUT} (dBm)	17.5/24/25.5*	29.3	-	21.5	-	**14.5/16.5/22**
	PAE (%)	N.A.	25.7	-	N.A.	-	**3.5/5/12.5**

*value extrapolated from graphs

automatic Bayesian framework [38], explores various bias currents for the carrier and peaking branches, as well as collector bias voltages, to identify the optimal operating points. The results of the process are shown in Fig. 20(a), where the best PAE for each EVM level is highlighted by a star symbol. The corresponding behavior of output power as a function of the EVM is shown in Fig. 20(b). Without any predistortion technique, a maximum PAE of 12.5% with an average power of 22 dBm was achieved at −30 dB EVM, where the effectiveness of the Doherty architecture in improving performance is clearly visible. Conversely, for more stringent linearity requirements of −35 and −40 dB EVM, the maximum recorded PAE values were 4.9% and 3.2%, respectively. In these high-linearity regimes, the performance is primarily determined by the intrinsic characteristics of the PCs, thereby limiting the impact of the DPA operation.

A comparison with state-of-the-art DPAs operating in similar frequency ranges and targeting analogous BWs is provided in Table III.

VI. CONCLUSION

A design methodology for DPAs for wireless communication systems was derived based on two different combiner topologies, both using three λ/4-TLs. Design charts have shown the importance of selecting an appropriate combining strategy for different parameter sets, including device optimal load, BW, and OBO. Experimental characterization of the DPA prototype, realized in GaAs HBT technology for sub-6-GHz applications, demonstrated a remarkably flat response with power ripple below 0.5 dB across the 5–6-GHz target band. The DPA achieves a PAE higher than 23% and a gain higher than 25 dB at 6-dB OBO while providing a PAE and gain above 30% and 23.5 dB, respectively, with a minimum saturated output power of 32.5 dBm. Tests with modulated signals demonstrated the effectiveness of the DPA architecture also in terms of linearity, showing around 3% EVM while achieving 22 dBm of average output power and 12.5% PAE.

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