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Effects of Termination Impedance and Cell Topology on the Linearity of Gallium Nitride 180° High-Pass/Low-Pass Phase Shifters

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***Abstract*—Phase shifters (PSs) are fundamental components of phased-array antennas, but they can also be a major contributor to intermodulation distortion. This article investigates how the internal impedance and cell topology of gallium nitride (GaN) 180° PSs affect their linearity. A theoretical analysis, supported by a simplified, yet accurate electrical model of the series FET in the switch and by measured data, demonstrates that selecting an internal impedance other than 50 Ω can significantly improve the input-referred third-order intercept point. In addition, the influence of the PS cell topology (T versus Π) on linearity is examined. To validate the theoretical results, a comparative experimental analysis is carried out, considering both internal impedance and topology. To this aim, we designed and characterized three demonstrator PS cells. Two demonstrators employ the standard 50-Ω impedance but are implemented using a T topology and a Π topology, respectively. A third demonstrator uses instead a 120-Ω internal impedance, together with a matching network (MN), to prove the analyzed relationship between internal impedance and switch-induced distortion. All demonstrator cells were designed for operation at 10 GHz and manufactured in a 0.12-μm gate-length GaN HEMT MMIC process. As expected, the best linearity performance is exhibited by the 120-Ω PS, achieving an IIP3 of +47 dBm.**

***Index Terms*—Gallium nitride (GaN), linearity, MMICs, phase shifters (PSs), third-order intermodulation (IMD3), X-band.**

I. Introduction

MICROWAVE phase shifters (PSs) are key components in a wide range of electronic systems. In telecommunications and sensing applications, they are commonly employed to enable beam steering in multiple-input–multiple-output (MIMO) systems and active electronically scanned arrays (AESAs). These systems are typically designed to handle hundreds of watts of transmitted power while maintaining high linearity in receive mode. As a result, the microwave circuits in the front-end must satisfy stringent power-handling and linearity requirements. Design efforts are traditionally focused on the power amplifier (PA) and low-noise amplifier (LNA), which are generally assumed to be the dominant sources of nonlinearity in transmit/receive (T/R) modules. However, attention must also be given to the circuits directly interfaced with the PA and LNA, such as the PS. Regarding the T/R module's analysis, two distinct scenarios can be identified. In the first scenario, the overall input third-order intercept point (IIP3) of the RF chain is dominated by other blocks (e.g., the PA or frequency-conversion stages). In this case, improving the linearity of the PS does not immediately translate into a higher system-level IIP3, although it provides additional design margin and ensures that the PS does not become a limiting element as system requirements evolve. In the second scenario, the PS contributes to the overall distortion. Under these conditions, a 4–6-dB improvement in the PS's IIP3 can directly yield system-level benefits. For example, in an X-band phased-array transmitter, such an improvement may be exploited to increase the allowable equivalent isotropically radiated power (EIRP) or, alternatively, to enable array-size scaling (i.e., a larger number of active elements) while preserving the same linearity constraints. In this case, an MMIC-level PS linearity enhancement has a direct and measurable impact on the overall system performance.

PSs are often implemented in silicon technologies [1], [2], [3], especially when cost and volume production are key factors. However, when linearity is the main concern, other semiconductor technologies are exploited, such as gallium arsenide (GaAs) [4], or even better gallium nitride (GaN) [5]. Recently, an IIP3 exceeding +90 dBm has been demonstrated in a GaN p-i-n diode PS [6], confirming the interest of the microwave community in high-linearity PSs.

A common PS implementation, especially for large phase shifts, is the high-pass/low-pass (HP/LP) topology. In this architecture, the phase shift is obtained by switching the RF path from the HP (phase-anticipating cell) to the LP (phase-lagging cell). Focusing on GaN-based implementation, several demonstrations have been proposed, showing remarkable linearity figures of merit, such as IIP3 in excess of 50 dBm in the X-band [5] and higher than 40 dBm in the Ku-band [7].

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However, in most cases, the linearity improvement is obtained owing to the superior performance of the GaN switches, while the impact of the HP/LP cell topology and of the internal impedance on linearity is overlooked.

In this article, a harmonic-expansion-based approach is adopted to discuss how the input–output impedances of the HP/LP cell, that is, the terminations of the single-pole double-throw (SPDT) switches, affect the overall PS linearity. In addition, the impact of T- and Π-cell topologies on PS linearity is addressed, leveraging on their different behavior at fundamental and higher harmonics. Three 180° PS demonstrators are designed to verify the proposed analysis as follows.

1) 50-Ω 180° PS based on the T topology.
2) 50-Ω 180° PS based on the Π topology.
3) 120-Ω 180° PS based on the Π topology.

The latter includes matching networks (MNs) to 50 Ω (see Fig. 1). In this way, we can provide a comparative evaluation between the Π and T topology while maintaining the same impedance equal to the standard value of 50 Ω, but also evaluate the role of the internal impedance for a given cell topology. The demonstrator cells are designed to provide the required phase shift and matching at 10 GHz and are implemented in a commercial GaN-on-SiC technology.

The additional complexity associated with adopting a non-50-Ω internal impedance is most justified in scenarios, such as Earth observation, electronic defense, and satellite telecommunications, where high linearity and high power are critical requirements, and the PS's linearity directly impacts the system-level performance.

The novelty of this work with respect to the existing literature can be summarized as follows. First, a closed-form expression describing the dependence of the IIP3 on the internal switch impedance (Z_{int}) is derived. Second, a combined theoretical and experimental analysis of T and Π PS topologies is presented, explicitly accounting for internal impedance effects. Finally, the proposed analysis is experimentally validated through three MMIC demonstrators operating at 10 GHz.

The remainder of this article is organized as follows. Section II describes the industrial-grade GaN technology adopted for the demonstrator MMICs. Section III presents the theoretical analysis of the SPDT switch nonlinear behavior in a two-tone test and the comparison with a practical SPDT example. This section also outlines the design guidelines for the passive structures, namely the high-pass (HP) and low-pass (LP) networks of the PS, as well as the matching-network (MN) design, when applicable. Section IV discusses the linear and nonlinear characterization of the demonstrator circuits and compares the measured and simulated results. Finally, Section V provides a comparison with the state of the art and some concluding remarks.

II. Technology

The demonstrator circuits are fabricated using the WIN Semiconductors' NP12-01 GaN-on-SiC technology. This 0.12-μm gate GaN process is manufactured on 100-mm SiC substrates and exploits a source-coupled field plate to provide high breakdown voltage (>100 V), allowing for reliable operation at V_{ds} of 28 V. The reference transistor, with 4×50 μm geometry, exhibits a typical P_{sat} of 29 dBm, 13.5-dB linear gain, and drain efficiency over 50% at 29 GHz. The technology also offers switch mode transistors (cold-FETs) validated down to −40 V. The value of the switch-mode FET ON-state resistance, R_{on}, is 2.3 Ω·mm when $V_{\text{GS}} = 2$ V and 3.0 Ω·mm at $V_{\text{GS}} = 0$ V. The value of the switch-mode FET OFF-state capacitance, C_{off} is 250 fF/mm when $V_{\text{GS}} = -20$ V and 210 fF/mm when $V_{\text{GS}} = -40$ V, yielding 0.5-ps $R_{\text{on}}C_{\text{off}}$ time constant figure of merit for the technology when used in switching applications [8]. The NP12-01 platform supports multiple MMIC functions with different transistor layouts optimized for power, noise, or switching performance, two interconnect metal layers, high-reliability MIM capacitors, precision TaN resistors, and through-wafer vias for low-inductance grounding.

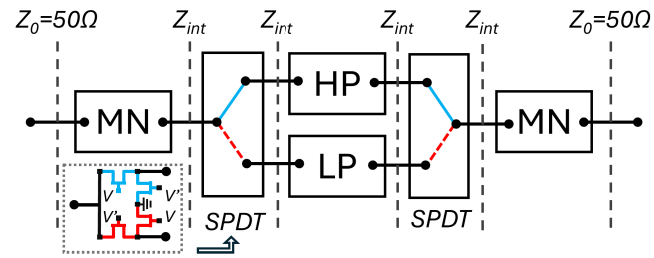

Fig. 1. Simplified schematic of an HP/LP PS. The impedances at external ports and internal sections are indicated. MNs are inserted when $Z_{\text{int}} \neq 50$ Ω. The series-shunt SPDT simplified circuit is given in the bottom-left inset.

III. Theoretical Study and MMIC Design

Let us consider the simplified block diagram of a single-bit HP/LP PS shown in Fig. 1, with generic internal impedance Z_{int}. In such a scheme, two main degrees of freedom are left to the designer: the choice to implement the cell in either a T or Π topology and to select Z_{int} different from 50 Ω. Evidently, since 50 Ω is the typical loading impedance of microwave systems, whenever the chosen Z_{int} is different, MNs should be inserted. Such MNs, designed not to limit the intrinsic PS bandwidth, can be exploited to properly shape the frequency response of the circuit.

A. SPDT Switch Design

The SPDT designed for this study is implemented in the typical series- and shunt-FET configuration, as seen in the dotted inset of Fig. 1, applying a tradeoff between linear and nonlinear requirements [9], [10]. In this study, the transistors' geometries are selected to provide IIP3 of approximately 45 dBm while ensuring 1.5-dB insertion loss and 20-dB isolation at 10 GHz in a 50-Ω environment. The selected IIP3 target is not state of the art, but represents a tradeoff between two contrasting goals. On the one hand, we aimed at maximizing the SPDT nonlinear performance in terms of IIP3, through careful balancing of the contrasting goals of SPDT insertion loss and isolation during the design phase. On the other hand, we deliberately avoided an excessively high IIP3 value to relax receiver's dynamic range requirements for the

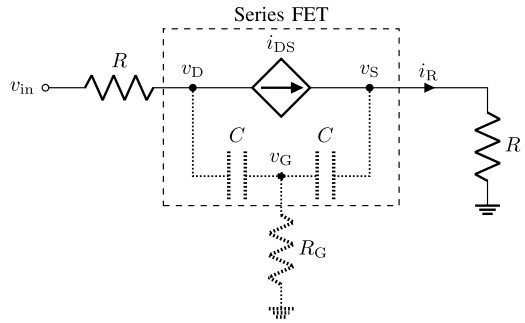

Fig. 2. Simplified model for the theoretical analysis of the SPDT nonlinearity. Dotted elements will be neglected in the final analytical formulation as detailed in the text.

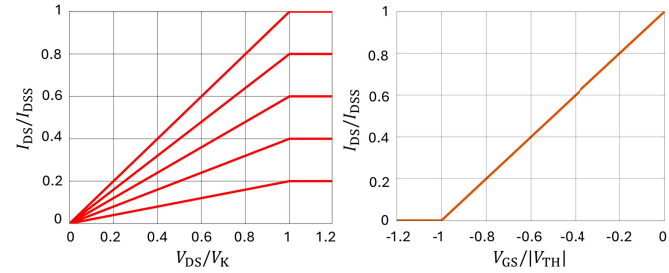

Fig. 3. Simplified model's DC characteristics.

subsequent characterization, taking into account the available setup described in Section IV.

The aim of this work is, in fact, a comparative evaluation between different topologies and the validation of the presented theoretical study on the internal impedance's impact on linearity, rather than presenting the *best-in-class* performance.

The series and shunt switches adopt a 3×60 μm and a 1×30 μm FET, respectively. Interestingly, WIN's FET switch configuration entails an odd number of fingers to maintain symmetrical behavior between the drain and source terminals. A description of the FET switch large signal model is provided in [11].

Admittedly, the periphery of the series FET is rather small, but, as stated above, this facilitates the nonlinear characterization of the PSs. A simplified linear model of the series FET switch is a 16-Ω resistor in the ON state and a 50-fF capacitor in the OFF state. The equivalent circuit values for the shunt FET-switch are instead 90 Ω and 10 fF. The ON and OFF states are implemented by imposing, respectively, 0 and −40 V at the gate terminal. The simulated linear insertion loss at 10 GHz of the SPDT is 1.4 dB. More detailed aspects of SPDT design can be found in [7] and [12]. The selected OFF-state voltage value is close to half the technology's breakdown voltage to maximize the nonlinear performance [13].

B. Impact of Internal Impedance (Z_{int}) on SPDT Linearity

The nonlinear distortion within the SPDT switch is mainly determined by the behavior of the series transistor in the ON state [14]. Consequently, we can pursue a closed-form formulation of the linearity dependence on Z_{int} by (1) analyzing only the series FET element instead of the full SPDT switch and (2) replace the FET itself with a simplified model. The obtained simplified circuit adopted for the study is shown in Fig. 2: it is composed by a single-series transistor with source and load impedances equal to $Z_{int} = R$ and the gate biased at $V_{ON} = 0$ V through a gate resistance R_G. The active device is modeled as a controlled current source i_{DS} plus the gate intrinsic capacitances $C_{gs} = C_{gd}$. The latter are considered identical, since a 1-finger FET switch is expected to be symmetric with respect to the gate, that is, the role of the source and the drain is interchangeable, as verified also in the foundry model. Furthermore, they are linearized adopting a constant capacitance value of 0.167 pF, extracted from the PDK model at the actual operating condition through an LS–SS approach.

The controlled source should accurately represent the FET behavior in the ohmic region. However, to account for the nonlinearity, the drain current is assumed to be a function of both v_{GS} and v_{DS} rather than being approximated with a simple v_{GS}-controlled resistance. As shown in Fig. 3, our model considers a piecewise linear trans-characteristic, with constant transconductance (above threshold) $g_m = I_{DSS}/|V_{TH}|$, a knee voltage V_K independent of v_{DS} and linear output resistance, yielding

$$i_{DS} = \frac{I_{DSS} + g_m v_{GS}}{V_K} v_{DS} = \frac{1}{R_{ON}} \left(1 + \frac{v_{GS}}{|V_{TH}|}\right) v_{DS} \tag{1}$$

where we defined the (minimum) ON resistance of the controlled source as

$$R_{ON} = V_K / I_{DSS}. \tag{2}$$

Despite the apparent simplicity of the circuit in Fig. 2, its analytical solution is not as simple. To proceed, two further circuit simplifications are made, which will then be verified against CAD simulation of the original scheme. First, R_G in Fig. 2 (dotted) can be neglected, implying that the gate terminal can be considered floating. This approximation holds since the gate control resistance is in the kilohm range (~3.3 kΩ) while other elements' impedances, R and $(\omega C)^{-1}$, are not exceeding few hundreds of ohm.

Eliminating R_G yields a straightforward relationship (capacitive voltage division) between the drain–source and gate–source voltages

$$v_{GS} = \frac{v_{DS}}{2} \tag{3}$$

that allows to rewrite (1) as

$$\frac{2\rho}{|V_{TH}|} v_{GS}^2 + (2\rho + 1)\, v_{GS} + RC \frac{\partial v_{GS}}{\partial t} - \frac{1}{2} v_{in} = 0 \tag{4}$$

where

$$\rho = R / R_{ON}. \tag{5}$$

Once the relationship between the input voltage and v_{GS} is obtained, the nonlinear characteristics of the SPDT, that is, the output voltage v_S, are simply

$$v_S = \frac{1}{2} v_{in} - v_{GS}. \tag{6}$$

The second simplification is based on the assumption that the current flowing through the capacitances is negligible with respect to that delivered to the load, which allows neglecting

the differential term in (4). This assumption, which will be further discussed later on, is valid up to frequencies at which the capacitances' impedance, $(\omega C)^{-1}$, is sufficiently larger than the equivalent resistance of the current generator, R_{ON}, and finally yields

$$\frac{4\rho}{|V_{\mathrm{TH}}|} v_{\mathrm{GS}}^2 + 2\,(2\rho+1)\, v_{\mathrm{GS}} - v_{\mathrm{in}} = 0. \tag{7}$$

It is important to remark that this simplification, crucial to the proposed closed-form analysis as it makes the model frequency-independent, can be done only provided that the validity of the capacitive division in (3) is maintained. Indeed, the presence of the capacitances plays a fundamental role in the linearization of the circuit acting as a negative feedback network. Thanks to it, any variation of the output voltage, V_{S}, is counteracted by an opposite variation of the input voltages and thus of i_{DS}. Such a mechanism implies keeping the error signal, represented in the equivalent feedback system by v_{DS}, working close to zero (ideal ON state), which in turn implies operating the FET in the most linear region, far from the knee voltage limit.

To quantify the circuit's linearity, the next step is to solve (7) and (6) considering a 2-tone input, that is, v_{in} composed by one tone at ω_0 and another one at $\omega_0 + \Delta\omega$, with the same amplitude $V_{\mathrm{in}} = A/2$. Introducing the harmonic balance (HB) formalism, (7) becomes

$$K_2 \mathbf{V}_{\mathbf{GS}}^{\mathbf{SQ}} + K_1 \mathbf{V}_{\mathbf{GS}} - \mathbf{V}_{\mathbf{in}} = 0 \tag{8}$$

where $K_2 = 4\rho/|V_{\mathrm{TH}}|$ and $K_1 = 2(2\rho + 1)$. The simplest possible Fourier expansion yielding third-order intermodulation product (IP) of the $\mathbf{V}_{\mathbf{GS}}$ variable is

$$\mathbf{V}_{\mathbf{GS}} = [V_0, V_1, V_2, V_{\mathrm{IP2}}, V_{\mathrm{IP3}}] \tag{9}$$

where the elements are the complex coefficients of the DC, fundamental, second harmonic, second, and third order IP, respectively. The coefficients of the vector $\mathbf{V}_{\mathbf{GS}}^{\mathbf{SQ}}$ are directly computed as the Fourier expansion of v_{GS}^2

$$\begin{cases} V_0^{\mathrm{SQ}} = V_0^2 + 4\,|V_1|^2 + 4\,|V_2|^2 + 4\,|V_{\mathrm{IP2}}|^2 + 8\,|V_{\mathrm{IP3}}|^2 \\ V_1^{\mathrm{SQ}} = V_1^* V_2 + 2\Re\left\{V_1 V_{\mathrm{IP2}}^*\right\} + 2\Re\left\{V_{\mathrm{IP2}}\right\} V_{\mathrm{IP3}} + 2\Re\left\{V_2^* V_{\mathrm{IP3}}\right\} \\ V_2^{\mathrm{SQ}} = V_1^2 + 4\Re\left\{V_1\right\} V_{\mathrm{IP3}} + 2\,|V_{\mathrm{IP2}}|^2 + 2\,|V_{\mathrm{IP3}}|^2 \\ V_{\mathrm{IP2}}^{\mathrm{SQ}} = |V_1|^2 + 2\Re\left\{V_1 V_{\mathrm{IP3}}^*\right\} + 2\Re\left\{V_2 V_{\mathrm{IP2}}^*\right\} + |V_{\mathrm{IP3}}|^2 \\ V_{\mathrm{IP3}}^{\mathrm{SQ}} = V_1^* V_2 + V_1 V_{\mathrm{IP2}}^* + V_2^* V_{\mathrm{IP3}} + V_{\mathrm{IP2}} V_{\mathrm{IP3}}^*. \end{cases} \tag{10}$$

The final HB system reads

$$\begin{cases} K_2 V_0^{\mathrm{SQ}} + K_1 V_0 = 0 \\ 2K_2 V_1^{\mathrm{SQ}} + K_1 V_1 - 0.5A = 0 \\ K_2 V_2^{\mathrm{SQ}} + K_1 V_2 = 0 \\ 2K_2 V_{\mathrm{IP2}}^{\mathrm{SQ}} + K_1 V_{\mathrm{IP2}} = 0 \\ 2K_2 V_{\mathrm{IP3}}^{\mathrm{SQ}} + K_1 V_{\mathrm{IP3}} = 0. \end{cases} \tag{11}$$

Even in this form, the system is still too complex for an analytical solution, and further simplification is needed to gain more insights into the mechanism generating intermodulation. Since the amplitudes of the harmonic and intermodulation coefficients decrease with order, we can keep in (10) only the lower-order terms. Similarly, since the DC term arises only as the result of the mixing, we also expect V_0 to be rather small. Under these assumptions we can rewrite (11) as

$$\begin{cases} 4K_2\,|V_1|^2 + K_1 V_0 = 0 \\ K_1 V_1 - 0.5A = 0 \\ K_2 V_1^2 + K_1 V_2 = 0 \\ 2K_2\,|V_1|^2 + K_1 V_{\mathrm{IP2}} = 0 \\ 2K_2\left(V_1^* V_2 + V_1 V_{\mathrm{IP2}}^*\right) + K_1 V_{\mathrm{IP3}} = 0 \end{cases} \tag{12}$$

from which all the harmonic coefficients can be computed. Notice that, as expected from a simplified (low-order) formulation, $V_1 \propto A$, V_2, V_{IP2} and $V_0 \propto A^2$, $V_{\mathrm{IP3}} \propto A^3$. In particular, the expressions for the fundamental and IP3 terms are

$$V_1 = \frac{0.5A}{K_1} = \frac{A}{2\,(2\rho+1)}, \quad V_{\mathrm{IP3}} = \frac{3\rho^2 A^3}{|V_{\mathrm{TH}}|^2\,(2\rho+1)^5}. \tag{13}$$

According to (6), for the output voltage we thus have that the fundamental and IMD_3 coefficients are

$$V_{1,\mathrm{out}} = 0.25A - V_1, \quad V_{\mathrm{IP3,out}} = -V_{\mathrm{IP3}} \tag{14}$$

and then the output power levels at the two frequencies are

$$P_1 = \frac{\left|2V_{1,\mathrm{out}}\right|^2}{2R}, \quad P_3 = \frac{\left|2V_{\mathrm{IP3,out}}\right|^2}{2R} \tag{15}$$

where the factor two accounts for the two-sided spectrum, finding

$$P_1 = \frac{2\rho^2 A^2}{(2\rho+1)^2 R}, \quad P_3 = \frac{18\rho^4 A^6}{|V_{\mathrm{TH}}|^4\,(2\rho+1)^{10} R}. \tag{16}$$

Finally, from (16), it is straightforward to find OIP_3 and IIP_3 as

$$\mathrm{OIP}_3 = \sqrt{\frac{P_1^3}{P_3}} = \frac{2\,|V_{\mathrm{TH}}|^2}{3R}\rho\,(2\rho+1)^2 = \frac{8\,|V_{\mathrm{TH}}|^2\rho^3}{3RG_{\mathrm{T}}} \tag{17}$$

$$\mathrm{IIP}_3 = \frac{\mathrm{OIP}_3}{G_{\mathrm{T}}} = \frac{8\,|V_{\mathrm{TH}}|^2\rho^3}{3RG_{\mathrm{T}}^2} = \frac{|V_{\mathrm{TH}}|^2}{6R}\frac{(2\rho+1)^4}{\rho} \tag{18}$$

observing that the transducer gain G_{T} is

$$G_{\mathrm{T}} = P_1 \frac{8R}{|2A|^2} = \frac{4\rho^2}{(2\rho+1)^2}. \tag{19}$$

To verify the validity of all the simplifications made on the circuit of Fig. 2, namely as follows.

1) Elimination of R_{G} (floating-gate assumption).
2) Elimination of the differential term in (4) (low-frequency assumption).
3) Limited Fourier expansion (low-order HB system formulation).
4) Elimination of higher-order mixing terms in (11) (simplified HB system solution).

We compare the results of the analytic formulas against a reference numerical solution obtained by setting up a 2-tone HB simulation of the full circuit of Fig. 2 in Keysight ADS, as shown in Fig. 4. A symbolically defined device is used for the controlled generator (1) where to fit the characteristic of the WIN's FET switch, we used $V_{\mathrm{TH}} = -2$ V, $V_{\mathrm{K}} = 1.5$ V, $I_{\mathrm{DSS}} = 110$ mA (yielding $R_{\mathrm{ON}} \approx 2.5$ Ω·mm), while $C_{\mathrm{gs}} = C_{\mathrm{gd}} = 0.167$ pF.

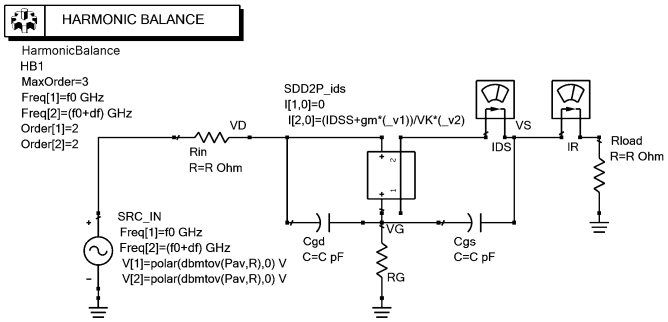

Fig. 4. ADS schematic for the numerical solution of the system in (10) and (11).

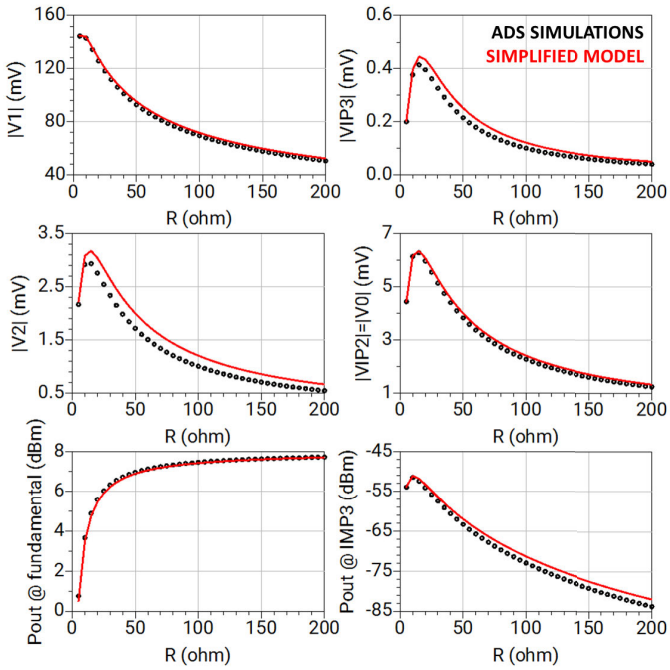

Fig. 5. Comparison between the simplified analytical solution and the numerical ADS solution of the HB system in (11): output power at fundamental and IP3 (bottom) and amplitudes of the harmonic coefficients of v_{GS} (top) as a function of R.

First, we observe in simulation that the difference between considering only low harmonic and mixing orders [2 and 3, respectively, as in simplification (3)] or including many more terms (up to 10 and 10) is negligible. Thus, we consider only the former case. Fig. 5 shows the harmonic coefficients and the output power found with the simplified analytic approach compared to the same results obtained in ADS (numerical solution of the full system), proving that the accuracy is maintained to a good level and hence the consistency of all other simplifying assumptions.

Fig. 6 remarks the excellent agreement between the full CAD numerical solution and our analytical approach in terms of OIP3. By increasing the value of R, the linearity performance improves, as R modifies the device voltage swing, that is, the feedback, hence reducing the impact of the device nonlinearity [15]. In the same figure, we also remark the fundamental role of the nearly open gate resistance and of the capacitive voltage divider. In fact, adopting a small R_G

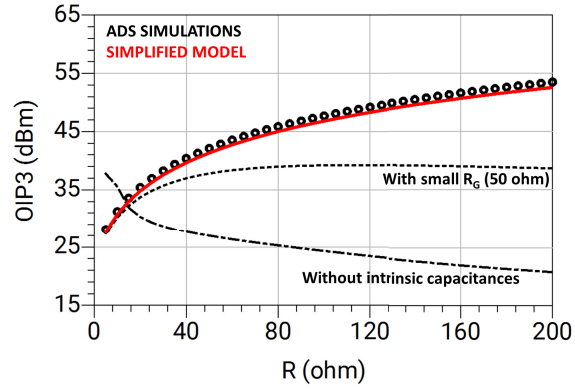

Fig. 6. OIP3 in (18) (red solid) compared to the numerical solutions computed in ADS (black). Symbols represent the correct ADS model, while dashed and dashed–dotted lines report the two deliberately wrong cases aimed at showing the importance of adopting a big gate resistance and the presence of the capacitive divider.

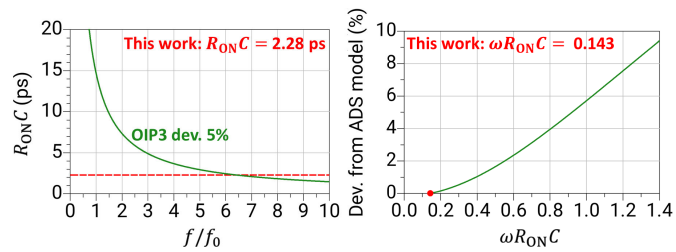

Fig. 7. Empirical assessment of model accuracy vs. frequency. On the left, the 5% contour plot of the relative deviation between the OIP3 behaviors computed with (18) and with ADS simulation in the frequency-$R_{ON}C$ plane shows that the $\omega R_{ON}C$ product is constant. On the right, the expected accuracy as a function of this product is reported. From both graphs, it is clear that in the present work, we are safely far from the frequency limit.

value, comparable with R and $(\omega C)^{-1}$ (dashed line) no more linearity improvement is obtained increasing R due to the current sinking effect of R_G that limits the negative feedback leverage. Instead, completely eliminating the capacitances (dotted–dashed line) dramatically worsens the linearity performance as negative feedback is no longer present.

As already pointed out, while the presence of the capacitances is key for the analysis, their contribution in (4) can indeed be assumed negligible, depending on operating frequency. Fig. 7 empirically demonstrates that the parameter that determines the accuracy of such an assumption is the constant $\omega R_{ON}C$ product. As long as this remains below unity, the discrepancy between the OIP3 predicted by (18) and that given by the full ADS model is below 6%.

Finally, Fig. 8 compares the OIP3 predicted by (18) with the actual OIP3 of the full SPDT switch, simulated with WIN's transistor library models, interconnections, and passive elements, the latter both simulated electromagnetically. The agreement is remarkable, demonstrating the effectiveness of the proposed analysis. The simulation data of the full SPDT indicate that it features 42 dBm OIP3 at 10 GHz when loaded on 50 Ω and up to 49 dBm when loaded instead with a higher resistance value. As the relative improvement decreases with larger R, and considering that the relative bandwidth achievable for MN decreases with the transformation ratio, an

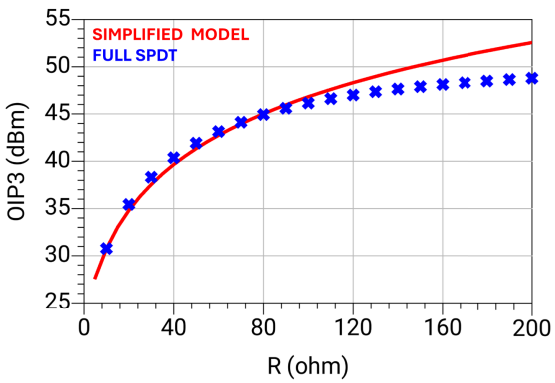

Fig. 8. OIP3 in (18) compared to the full SPDT simulation.

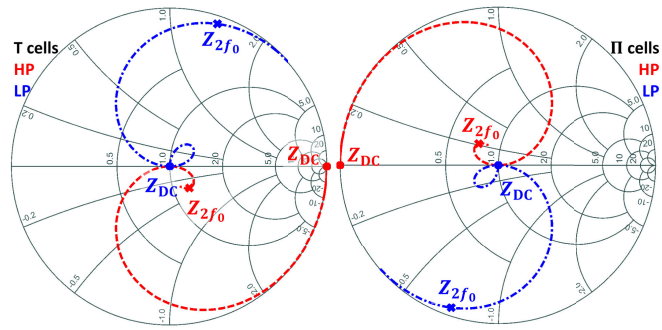

Fig. 9. Impedance presented by the different HP/LP cells to the SDPT from DC to the third harmonic.

intermediate value of 120 Ω is selected for the demonstrator, which is expected to provide 47-dBm OIP3.

C. Cell Topology Analysis

In nonlinear design, especially in the case of PA design, the source and load terminations seen at fundamental frequency, as well as those seen at baseband and at higher harmonic components, play a fundamental role in determining linearity, efficiency, and output power [16]. In HP/LP PSs, implementing either a T- or Π-cell topology can provide different trajectories of the internal impedance versus frequency. In fact, while HP and LP cells are ideally designed to show the same I/O impedance and insertion phase at the fundamental design frequency f_0, their behavior greatly diverges both toward DC and toward infinite frequency depending on the selected topology.

Assuming an ideal SPDT model consisting of a short circuit for the ON-path and an open-circuit for the OFF-path, the inductance and capacitance values of HP and LP cells are synthesized to implement the desired phase shift $\Delta\varphi$ and impedance (Z_{int}) at $\omega_0 = 2\pi f_0$. The design equations, available in [17] and [18], are here reprised for the reader's convenience

$$L_{HP}^{T} = \frac{Z_{\text{int}}}{\omega \sin\Delta\phi}; \quad C_{HP}^{T} = \frac{\sin\Delta\phi}{\omega Z_{\text{int}}\,(1-\cos\Delta\phi)} \tag{20}$$

$$L_{LP}^{T} = Z_{\text{int}}\frac{1-\cos\Delta\phi}{\omega \sin\Delta\phi}; \quad C_{LP}^{T} = \frac{\sin\Delta\phi}{\omega Z_{\text{int}}} \tag{21}$$

$$L_{HP}^{\Pi} = Z_{\text{int}}\frac{\sin\Delta\phi}{\omega\,(1-\cos\Delta\phi)}; \quad C_{HP}^{\Pi} = \frac{1}{\omega Z_{\text{int}}\sin\Delta\phi} \tag{22}$$

$$L_{LP}^{\Pi} = Z_{\text{int}}\frac{\sin\Delta\phi}{\omega}; \quad C_{LP}^{\Pi} = \frac{1-\cos\Delta\phi}{\omega Z_{\text{int}}\sin\Delta\phi}. \tag{23}$$

Note that these equations are valid for symmetric PSs, where, by construction, each network contributes half of the total phase shift, thus $\Delta\varphi = 2\Delta\phi$. In case of a 180° PS ($\Delta\varphi = 90°$) we have for all architectures

$$L = \frac{Z_{\text{int}}}{\omega}; \quad C = \frac{1}{\omega Z_{\text{int}}}. \tag{24}$$

As indicated by (24), the component values scale with both operating frequency and internal impedance as shown in Fig. 8, and their practical realizability ultimately depends on typical MMIC design tradeoffs. Data in Fig. 8 show that increasing the internal impedance beyond approximately 150 Ω does not yield a significant additional improvement in IIP3, considering the investigated switch model. Therefore, in practice, the maximum usable impedance is determined by the minimum between the impedances that can be synthesized with feasible component values and by the impedance above which no meaningful IIP3 benefit is obtained.

Fig. 9 shows the impedance seen by the SPDT switches of Fig. 1 up to the third harmonic for the different cell topologies with ideal elements: all circuits provide by design Z_{int} at f_0, but the impedances observed at DC and nf_0 ($n > 1$) change noticeably. In particular, for both LP topologies, the DC value is Z_{int} while from the second harmonic onward, the reflection coefficient approaches, with clockwise phase rotation, a unitary magnitude. However, for the T-cell, the phase rotates between $\gtrsim 90°$ and 0°, thus the impedance seen by the SPDT is an increasingly large inductance, while for the Π-cell, the phase goes from $\lesssim 270°$ to 180°, yielding smaller capacitive impedance with frequency. On the contrary, the impedance provided by both the T and Π topologies at nf_0 ($n \geq 2$) is very close (better than 15 dB of mismatch) to Z_{int}, showing just a mild capacitive or inductive behavior, respectively. The main difference in the HP topology is instead the DC impedance: an open circuit for the HP-T-cell and a short circuit for the HP-Π one.

The previous analysis is presented for the 180° PS. In DC and at f_0, all cells sharing the same topology exhibit identical impedance regardless of the phase shift value. In fact, all cells will provide Z_{int} at f_0 while the impedance at DC depends solely on the topology and not on the applied phase shift. In contrast, the magnitude and phase of the higher-order harmonics vary with the phase shift, as a consequence of component values scaling with the phase shift as indicated in (20)–(23). It can be rather easily demonstrated that only at a phase shift of 180° all higher-order harmonics exhibit near-unity magnitude. In contrast, the unitary magnitude condition of the higher-order harmonics is obtained for $n > 2$ when the phase shift is 90° and is practically never met in the 45° and 22.5° PS, when considering the 50-Ω case. Moreover, for a given phase shift value, the 120-Ω case results in higher harmonic magnitudes than the 50-Ω counterpart. Finally, HP networks implemented with ideal components exhibit an impedance close to Z_{int} at all higher-order harmonics. It is therefore reasonable to presume that different IIP3 values will be obtained as the phase shift

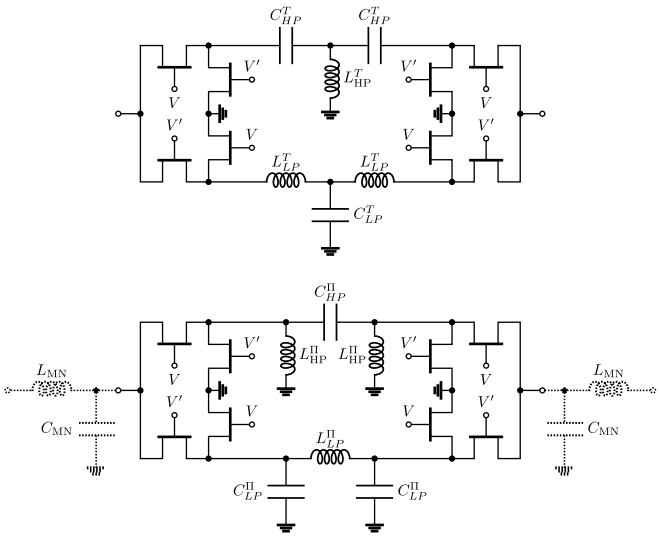

Fig. 10. Simplified schematics of the designed HP/LP PS cells: T-type (top) and Π-type (bottom) including the MNs (dotted) used for the 120-Ω case.

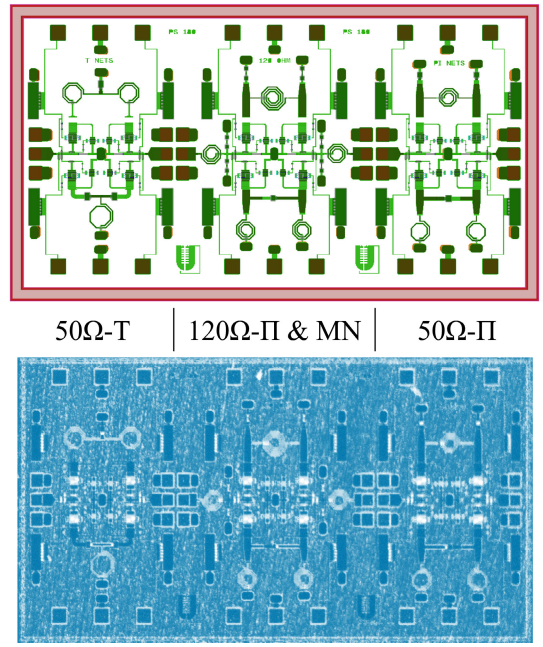

Fig. 11. GaN 180° PS demonstrators: MMIC implementation (bottom) and CAD layout (top). From left to right: 50-Ω-T, 120-Ω-Π, and 50-Ω-Π cells.

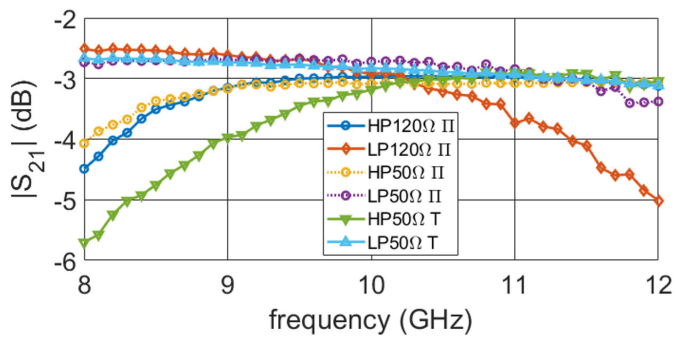

Fig. 12. Measured insertion loss of the three PSs in the HP and LP states.

varies for a given Z_{int}, f_0, and cell topology. However, it is fair to say the analysis here presented considers HP and LP networks implemented using ideal components, for which ideal ground or open-circuit conditions can be achieved at higher-order harmonics. In practical MMIC implementations, meeting such conditions is indeed significantly more challenging unless the complexity of the HP or LP networks is increased to explicitly control harmonic terminations.

D. MMIC Demonstrators Design

As discussed in Section I, three demonstrator PSs are designed in MMIC technology to verify the claim that different Z_{int} values can modify the PS's IIP3. The three demonstrator circuits are implemented applying the topologies appearing in Fig. 10. The three implementations are: two 50-Ω PS based on the T and Π topology, and one 120-Ω PS based on the Π topology. This configuration enables a comparative evaluation of the effects of varying either the internal impedance or the cell topology. When moving from an ideal circuit to an actual implementation, the choice of the topology also affects the load synthesized at the fundamental, as components' parasitic elements, interconnection lines, and layout construction enter the equation in different ways. Since it is not possible to conceive a generalized analytical study of the impedance trajectory that takes into account parasitic elements, which in turn differ depending on technology and layout choices, we will experimentally assess the different linearity performance of the two topologies by implementing two PS versions, both targeting 180° phase shift and Z_{int} = 50 Ω, based on the T and Π topology, respectively.

According to (24), the equivalent component values targeted in the electromagnetic (EM) optimization are C = 0.32 pF and L = 0.8 nH for both the 50-Ω cells, and C = 0.13 pF and L = 1.9 nH for the Π-type 120-Ω cell. An MN, with series inductance and shunt capacitance, has also been designed and EM-optimized for the 120-Ω cell. Notice that the additional chip area required by the MNs can be minimized in multibit shifters, where they are needed only at the MMIC I/O ports, while all internal sections can be matched to Z_{int}.

The fabricated MMIC containing the three demonstrator circuits is shown in Fig. 11: the chip size is 3.7 × 2.8 mm^2.

IV. Experimental Results

A. Linear Tests

Linear characterization is performed using an HP 8510C vector network analyzer (VNA). Figs. 12 and 13 show the insertion and return loss of the three PSs in the HP and LP states, respectively (six measured traces), while Fig. 14 shows the measured phase shift of the three cell topologies.

The typical PS insertion loss at 10 GHz is 3 dB, with minor deviations between the various cells/states. These data are consistent with the simulated loss of a single SPDT of 1.4 dB. Fig. 12 shows that the LP-50-Ω-Π PS has the best insertion loss, at 10 GHz, among all configurations. The states with higher losses are those having series inductors that can be rather lossy. In fact, the state with the highest losses is HP-50 Ω-T, which is the only state with two series-connected

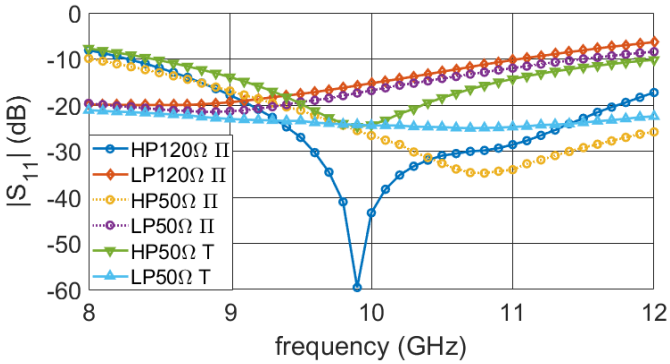

Fig. 13. Measured return loss of the three PSs in the HP and LP states.

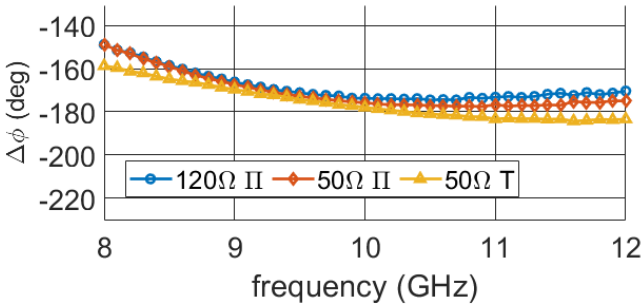

Fig. 14. Measured PS phase shift of the three PSs.

inductors. The measured return loss is better than 15 dB at 10 GHz in all cases. This, despite being an adequate value, indicates that a perfect matching to 50 Ω has not always been obtained, and therefore the internal impedance values (Z_{int}) are slightly different from expectations. In particular, the 120-Ω HP state shows a return loss of 40 dB at 10 GHz, whereas the LP state of the same cell shows a return loss of only 16 dB. In fact, the S_{11} of the 120-Ω LP cell indicates an internal impedance closer to 90 Ω. The other cell, having a return loss less than 20 dB, is the 50-Ω Π-cell in the LP state. In this case, the poorer return loss is due to a slightly capacitive behavior since the real part of its S_{11} lies on the 50-Ω circle. All other return losses are better than 25 dB, so we can assume that the internal impedances coincide with the design values. The 120-Ω-Π-cell appears to exhibit an internal impedance of about 90 Ω in the experiment. This unwanted effect is due to the simulation technique that was applied. During the design phase, EM simulations were performed at the single-branch level, meaning that the layouts of the three branches of each T- and Π-cell were simulated separately. In this configuration, the impedance was found to be closer to 120 Ω. However, a higher-level simulation, a full EM simulation of the complete cell layout, revealed that the internal impedance is closer to 90 Ω. Ultimately, the root cause was the use of EM simulations on a partial layout, followed by circuit-based simulation of the entire cell.

Finally, the measured phase shift, that is, the insertion phase difference between the HP and LP states, is shown in Fig. 14 and is well aligned with the expected value, −180° at 10 GHz. The observed phase and amplitude imbalance versus frequency is typical of narrowband circuit designs, where no subsequent tuning or optimization pursuing a uniform response over the targeted bandwidth is performed.

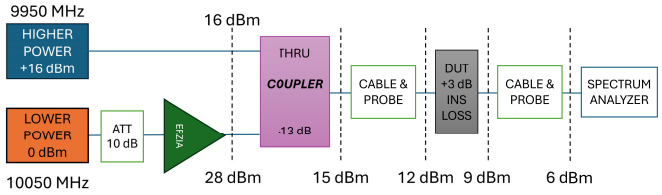

Fig. 15. Simplified block diagram of the two-tone test bench. The indicated power levels are referred to the single tone.

B. Nonlinear Tests

The two-tone test, around 10 GHz with 100-MHz tone spacing, is performed by combining two synthesized generators using a KRYTAR's 102040013K Directional Coupler, which provides a nominal coupling of 13 dB from 2 to 40 GHz. The through-path insertion loss is 1 dB below 20 GHz. The receiver is a Rohde & Schwarz FSV40-NS spectrum analyzer working up to 40 GHz. The synthesized signals connected to the coupled branch are preamplified to compensate for the coupling losses, achieving 12 dBm per-tone power at the devices under test (DUT) port. The ON- and OFF-state voltages are 0 and −40 V, as per design. A simplified block diagram of the test bench is provided in Fig. 15. As shown in the figure, the DUT is excited with two equal amplitude tones spaced by 100 MHz, each set to +12 dBm at the DUT input after calibration of cables, attenuators, and probe insertion losses. At the DUT output, the measured fundamental level is approximately +9 dBm per tone, in agreement with the DUT insertion loss and output losses indicated in the setup diagram. The analyzer reference level is set to 20 dBm, which automatically enables 20 dB of internal RF attenuation, resulting in an effective signal level at the analyzer front end of approximately −14 dBm per tone. Under these conditions, the analyzer operates with a two-tone intermodulation dynamic range exceeding 70 dB, ensuring that analyzer-generated IM3 products are well below those generated by the DUT. The directional coupler used in the two-tone generation chain provides sufficient isolation between the RF sources and the ERZIA driver amplifier, preventing mutual loading and excluding intermodulation generation upstream of the DUT. The spectrum analyzer resolution and video bandwidths are chosen to ensure stable amplitude estimation while avoiding any influence on the measured intermodulation levels. No variation of the extracted IIP3 values was observed when changing the analyzer reference level or internal attenuation, confirming that the measurement is limited by the DUT and not by the instrumentation.

Fig. 16 reports the measured *vs* theoretical PS IIP3 at 10 GHz for the three designed 180° PS cells in the HP and LP states, respectively. The theoretical value is obtained in simulation using the real SPDT and ideal HP/LP cells.

As expected, the version designed for Z_{int} = 120 Ω shows 46-dBm IIP3, 6 dB higher than that designed for Z_{int} = 50 Ω. As anticipated, the 120-Ω LP cell has a worse IIP3 due

TABLE I
SOA TABLE OF GAN PS CIRCUITS

REF	Tech.	# of bits	BW (GHz)	IL (dB)	IP1dB (dBm)	IIP3 (dBm)
[4]	GaN-SiC 150 nm	analogue PS	6–12	7	25	N/R
[19]	GaN-Si 800 nm	1	8–12	2	38	46
[20]	GaN-Si 250 nm	5	8–12	14	1	N/R
[21]	GaN-Si 100 nm	3PS+3AT	30–40	N/R	28	N/R
[22]	GaN-SiC 250 nm	5	8–12	13	29	N/R
[23]	GaN-SiC 150 nm	6	36–39	8	28	N/R
[24]	GaN-SiC 250 nm	6	4.5–5.5	7	38	50
T.W.	GaN-SiC 150 nm	1	8–12*	2.6	32	45

(*) *nonlinear measurements only at 10 GHz, nonlinear simulations from 8 to 12 GHz.*

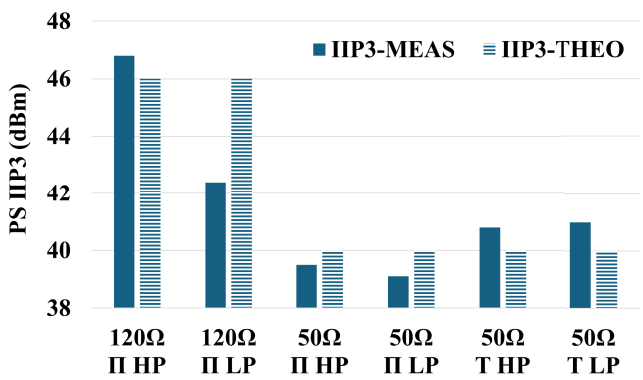

Fig. 16. Measured and theoretical PS IIP3 at 10 GHz of the three PS topologies in the HP and LP states.

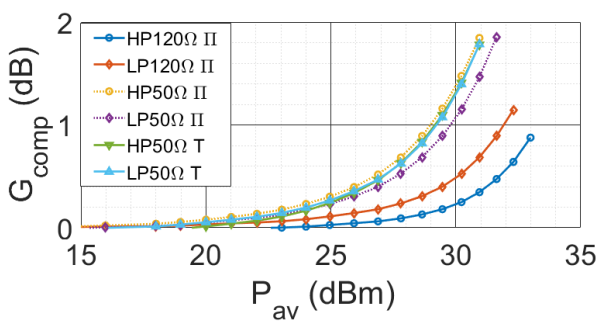

Fig. 17. Measured PS gain compression versus available input power at 10 GHz of the three PS topologies in the HP and LP states.

to the suboptimum impedance value found in the actual implementation. The characterization data are well consistent with the simulation reported in Fig. 8.

The deviation between the measured and theoretical results is mainly attributed to the limited bandwidth of the test bench, which cannot guarantee a 50-Ω termination at all higher-order harmonics. In greater detail, the ERZIA amplifier used to increase the power level of the lower power source (see Fig. 15) has an operating bandwidth from 6 to 18 GHz. Moreover, as discussed in Section III, the MMIC implementation provides reduced control over the termination behavior at higher-order harmonics, due to the unavoidable parasitics of the physical elements, compared with the idealized theoretical case. However, the nonlinear characterization clearly indicates that better GaN PS linearity can be obtained by tuning the internal impedance of the PS cell. Similar considerations were shown for GaAs SPDTs [14] and p-i-n-diode PSs [6], [25].

Finally, Fig. 17 reports the measured gain compression (G_{comp}) as a function of the available input power. The effect of different Z_{int} is also visible on the 1-dB compression point level (IP1dB). The IIP3 measurements were conducted at approximately 20-dB back-off from IP1dB, ensuring linear operation. Under these conditions, no self-heating effects are expected. Additionally, the 1-dB compression level is low enough to avoid the uprise of thermal effects during this test.

V. BENCHMARK AND DISCUSSION

A state-of-the-art survey comparing high linearity GaN PS circuits is provided in Table I. The circuit presented here compares well with the literature. However, the objective of this demonstrator is not to prove *best-in-class* performance but to highlight that nonlinear behavior can improve when selecting a different internal impedance value.

Within this investigation, the only observed practical difference was associated with variations in the internal impedance (Z_{int}). As a result, the choice between T and Π topologies becomes primarily a design decision left to the designer's expertise, taking into account practical considerations such as layout and technology constraints. In principle, the HP/LP cell topology can produce an effect on IIP3 provided the designer can precisely control the magnitude of the harmonic terminations while implementing a feasible circuit design and a feasible layout. Moreover, the investigated PS topology is inherently bidirectional, so the analysis is valid in both TX and RX modes. In principle, the designer or system engineer can freely choose which nonlinear figure of merit is more useful to adopt, possibly IP1dB in TX and IIP3 in RX.

Finally, the proposed 120-Ω solution is directly applicable to multibit PS architectures. While MNs are typically implemented only at the chip input and output in multibit designs, the internal impedance optimization discussed in this work applies at the unit-cell level and therefore remains valid regardless of the overall matching strategy. Regarding extension to other frequency bands, the proposed approach is inherently scalable with frequency, as the analysis is based on normalized relationships. Thus, the same internal impedance optimization principle applies, provided that the electrical lengths, component values, and parasitics are appropriately reoptimized for the target band.

VI. Conclusion

The effect of internal impedance and cell topology in GaN-HEMT-based HP/LP 180° PSs is analyzed. Theoretical analysis and measured data show that selecting an internal impedance different (higher) than 50 Ω improves the linearity of the PS by about 4–6 dB. The effect of cell topology (T and Π) for the same internal impedance is also investigated. In the present case, it appears to be negligible, consistent with the fact that the different DC and harmonic behavior of the cells shows no impact on simplified SPDT linearity analysis. Clearly, layouts and parasitic effects can favor one or the other topology, but this should be evaluated on a case-by-case basis.

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