POLITECNICO DI TORINO
Repository ISTITUZIONALE

Development of a 7-nm SET-Hardened Reconfigurable Logic Array

Original
Development of a 7-nm SET-Hardened Reconfigurable Logic Array / Cui, A., Girondi, G., Azimi, S., Sterpone, L.. - ELETTRONICO. - (In corso di stampa), pp. 1-7. (2026 IEEE Nordic Circuits and Systems Conference Tampere (FIN) 20-21 October 2026).

Availability:
This version is available at: 11583/3016331 since: 2026-10-05T12:35:05Z

Publisher:
IEEE

Published
DOI:

Terms of use:

This article is made available under terms and conditions as specified in the corresponding bibliographic description in the repository

Publisher copyright
IEEE postprint/Author's Accepted Manuscript

©9999 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collecting works, for resale or lists, or reuse of any copyrighted component of this work in other works.

(Article begins on next page)

23 October 2026

Development of a 7-nm SET-Hardened Reconfigurable Logic Array

Aobo Cui
Dipartimento di Automatica ed Informatica
Politecnico di Torino
Italy
aobo.cui@polito.it

Germano Girondi
Dumarey Softronix
Dumarey Group
Italy
germano.berto_girondi@dumarey.com

Sarah Azimi
Dipartimento di Automatica ed Informatica
Politecnico di Torino
Italy
sarah.azimi@polito.it

Luca Sterpone
Dipartimento di Automatica ed Informatica
Politecnico di Torino
Italy
luca.sterpone@polito.it

***Abstract*—This paper presents a 7-nm SET-hardened reconfigurable logic array implemented using the ASAP7 FinFET technology. The work aims to establish a practical foundation for the development of radiation-hardened FPGAs at advanced technology nodes. The proposed array comprises 200 single-event transient (SET)-hardened basic logic elements (BLEs), each integrating a 6-input look-up-table (LUT), a D flip-flop (DFF), and an output-selection multiplexer (MUX). Each component is analyzed through fault injection and selectively hardened against SET-induced failures. The resulting BLE achieves a substantial reduction in estimated SET cross section while introducing only moderate area, timing, and power overheads. The complete array is physically implemented using the OpenROAD flow, and a dedicated RTL-to-array mapping tool is developed to translate Verilog descriptions into BLE assignments, LUT configurations, and transistor-level interconnections. A comprehensive case study further demonstrates that the proposed logic array can implement practical circuits with improved SET resilience and limited additional overhead.**

***Index Terms*—7nm FinFET, Reconfigurable Logic, SET, FPGA**

I. Introduction

Reconfigurable devices are increasingly important for mission-critical computing because they allow hardware functionality to be modified after deployment, a capability that is particularly valuable in long-duration space missions where operational requirements may evolve after launch. Field-programmable gate arrays (FPGAs), the most widely used class of reconfigurable devices, provide programmable logic, storage, and interconnection resources for a broad range of applications. As these applications demand higher logic density and computational performance, FPGA technologies have advanced toward scaled FinFET nodes. However, this scaling also increases radiation-related concerns, as reduced supply voltages and node capacitances lower the critical charge required to disturb circuit nodes, thereby increasing susceptibility to single-event transients (SETs) and radiation-induced state errors.

The single-event response of advanced-node FPGAs has therefore received growing attention. The behavior of 16-nm Xilinx UltraScale+ FPGA, MPSoC, and RFSoC devices has been characterized for space and other high-reliability applications [1], [2]. Similar studies have investigated the configuration and embedded-memory resources of the 14-nm Intel Stratix 10 FPGA [3], while more recent work has evaluated single-event effects in the programmable logic, configuration memory, and processing resources of 7-nm Xilinx/AMD Versal devices [4], [5]. These studies demonstrate the susceptibility of advanced FPGA resources, but mainly characterize existing commercial devices rather than redesigning their underlying programmable logic.

At circuit level, radiation-hardening research in advanced FinFET technologies has primarily addressed isolated function-specific cells or circuits, including inverters, logic gates, and flip-flops [6], [7]. However, a hardened cell alone does not provide a programmable architecture on which arbitrary applications can be implemented. The fundamental computational block of a look-up-table-based FPGA is the basic logic element (BLE), which combines a look-up-table (LUT), a D flip-flop (DFF), and output-selection multiplexer (MUX). Since interconnected BLEs implement the combinational and sequential functions of a mapped circuit, an SET generated in any BLE component may propagate to an output or be captured as an incorrect state. Developing an SET-tolerant BLE and integrating it into a usable reconfigurable architecture are therefore necessary steps toward intrinsically hardened advanced-node FPGAs.

To address this need, this work develops an SET-hardened (SH) reconfigurable logic array using the predictive ASAP7 7-nm FinFET process design kit [8]. LET-based fault injection is first applied to the LUT and DFF to identify sensitive internal nodes and operating conditions. The results guide the selective application of radiation-hardening-by-design (RHBD) techniques to the LUT, DFF, and MUX. These components are integrated into a hardened BLE, which is then used as a basic module to construct a 200-BLE reconfigurable logic array. Its physical implementation is generated using an RTL-to-layout flow and evaluated in terms of area and implementation overhead.

A dedicated RTL-to-array mapping tool is also developed

to make the proposed hardware usable with conventional circuit descriptions. The tool accepts Verilog RTL, extracts combinational and sequential functions, assigns them to the available BLEs, and generates the required LUT configuration data and transistor-level interconnections. The tool therefore provides the required link between standard RTL design and the proposed SET-hardened architecture.

The functional correctness of the proposed logic array is evaluated using circuits from the ISCAS'85, ISCAS'89, and ITC'99 benchmark suites [9]–[11], while its SET resilience is evaluated using the C17 benchmark from ISCAS85. The benchmarks are mapped onto the proposed array and functionally verified against golden models. Monte Carlo LET-based fault injection is then performed on mapped implementations and compared with equivalent circuits constructed from unhardened ASAP7 components. The results show that the proposed architecture reduces SET-induced error rates while introducing limited area, timing, and power overheads.

The main contributions of this work are:

1) An SET-hardened 7-nm BLE integrating a hardened LUT, DFF, and output-selection multiplexer.
2) The construction and physical implementation of a 200-BLE reconfigurable logic array based on the proposed hardened element.
3) An RTL-to-array mapping tool that translates Verilog designs into BLE assignments, LUT configuration data, and transistor-level interconnections.
4) A benchmark-level evaluation demonstrating reduced SET susceptibility with limited implementation overhead.

These contributions provide a circuit-level, architectural, and design-flow foundation for future radiation-hardened FPGAs in advanced FinFET technologies.

The remainder of this paper is organized as follows. Section II reviews related works. Section III presents the proposed hardened BLE and the 200-BLE logic array. Section IV describes the RTL-to-array mapping tool. Section V reports the simulation results, and Section VI concludes the paper.

II. State of the Art

Radiation hardening for reconfigurable systems has been explored at several largely separate levels of the design hierarchy. At the physical-implementation level, [12] notes that the complexity of commercial radiation-hardened FPGA architectures limits the development of custom placement and routing methods and addresses this issue with GPU-accelerated routing for a fixed vendor architecture. A comparable gap exists earlier in the design flow, at RTL mapping, which is the stage this work targets. At the logic-element level, [13] shows that transient pulses can broaden as they propagate through the internal multiplexer chain of a commercial LUT before reaching a sampling flip-flop. This result highlights the LUT structure itself as a significant source of SET sensitivity, motivating the direct hardening of that structure rather than its characterization alone.

Not all approaches target the logic element itself. [14], for example, improves system-level fault tolerance by combining TMR in a dedicated health-monitoring core with scrubbing of the configuration and partial reconfiguration on commercial FPGA boards, while leaving the underlying device unchanged. Fault-injection and radiation tests demonstrate high detection coverage under sustained faults. Such system-level approaches also depend on the choice of fabrication technology. In this context, [15] compares 28-nm bulk CMOS and 16-nm FinFET commercial FPGAs under proton irradiation, reporting roughly an order-of-magnitude lower SEU sensitivity for FinFET devices but greater latch-up susceptibility. These results show that technology scaling redistributes, rather than eliminates, radiation risks and therefore does not remove the need for deliberate hardening of the logic elements at the selected technology node.

However, hardening the logic element itself has so far largely treated its combinational and sequential components separately. [16] evaluates a family of DICE and DMR-based flip-flops, including area-optimized variants with modified redundant-node spacing, fabricated and radiation-tested in a 22-nm FinFET process. [17] instead reuses the otherwise unused master latch of a standard D flip-flop as redundant storage, augmented by a Muller C-element, achieving comparable cross-section improvement with lower area than an equally resilient TMR flip-flop. Together with [13] and [18], these studies establish independent hardening precedents for the LUT and flip-flop portions of the BLE, but do not address them as jointly hardened and physically implemented logic elements.

Although radiation-hardened FPGAs are commercially available in multiple fabrication technologies, and dedicated solutions exist at several of the design levels discussed above, a fully integrated path for researchers to design a radiation-hardened reconfigurable device with the desiring fabrication technologies remains relatively underexplored. Commercial radiation-hardened FPGAs generally rely on fixed architectures and mature technology nodes, limiting designers' ability to examine or modify their underlying hardening strategies. Meanwhile, previous studies typically focus on individual stages of the design hierarchy, rather than integrating circuit-level hardening, physical implementation, and RTL mapping within a unified flow. This work aims to bridge these areas by establishing a verified path from RTL description to a physically implementable, radiation-hardened, specifically SET-hardened reconfigurable architecture, providing a foundation for the development of radiation-hardened FPGAs at advanced technology nodes.

III. Proposed 7-nm SET-Hardened Reconfigurable Array

The development of the proposed 7 nm SH reconfigurable array begins with the radiation-sensitivity analysis and hardening of the BLE. During this stage, LET-based fault-injection simulations are performed on the principal BLE components to identify sensitive internal nodes and guide the selective

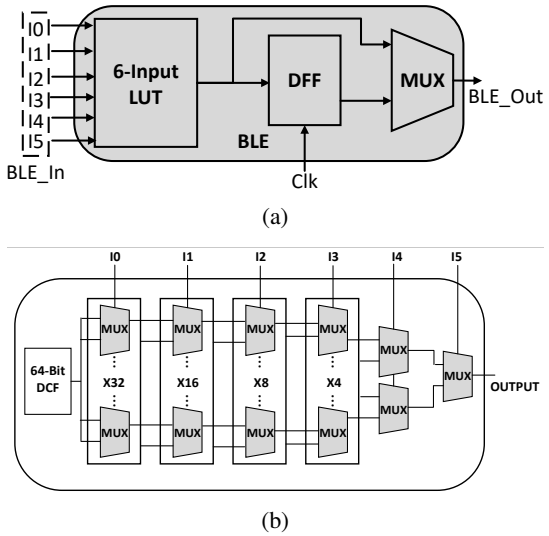

Fig. 1: The architecture of the BLE (a) and the 6-input LUT (b).

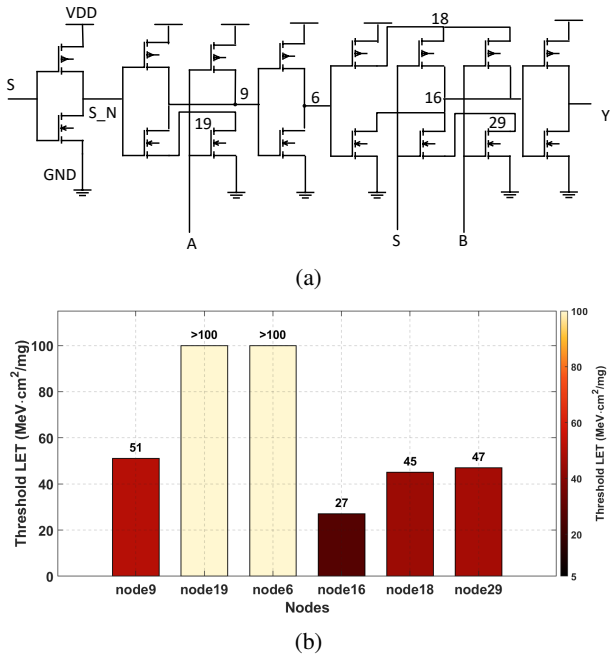

Fig. 2: Baseline 2:1 MUX: (a) transistor-level schematic and (b) threshold-LET values of its internal nodes.

application of RHBD techniques. The resulting SH-BLE is then evaluated in terms of SET susceptibility, propagation delay, power consumption, and area overhead with respect to a baseline BLE implemented using conventional ASAP7 circuit structures.

After the circuit-level design and characterization of the hardened BLE, the architecture is scaled to a reconfigurable logic array composed of 200 SH-BLEs. Physical implementation is generated using the OpenROAD flow [19], which performs logic synthesis, floor planning, placement, clock-tree synthesis, routing, and layout generation based on the ASAP7 technology platform. In addition to the BLE array, the implemented array includes the supporting logic and interconnection resources required to configure the operating mode and connectivity of the reconfigurable architecture. This physical-design stage enables a device-level evaluation of silicon area, cell utilization, routing demand, timing characteristics, and implementation overhead, thereby complementing the transistor-level radiation analysis of the individual BLE.

A. Construction of Basic Components

The BLE structure used in the proposed logic array is shown in Fig. 1(a). It consists of a 6-input LUT as the main logic-computation component, a DFF for sequential operation, and a 2:1 MUX that selects between the direct LUT output and the registered output. Six-input LUTs are widely used in modern high-performance FPGAs because they provide an effective balance among logic density, mapping efficiency, and implementation cost. To improve the radiation resilience of the complete BLE, all three components are hardened. As shown in Fig. 1(b), the 6-input LUT is constructed using a network of identical 2:1 MUX cells and a 64-bit data configuration (DCF). Therefore, radiation analysis and hardening are first performed on a single MUX cell.

The hardening process begins with LET-based fault injection. In HSPICE, SETs are modeled as current pulses using the Messenger equation in (1) and injected into each circuit node. In this model, Q_{coll} is the collected charge, $\tau_\alpha = 1.64 \times 10^{-10}\,\text{s}$ is the charge-collection time constant, $\tau_\beta = 5 \times 10^{-11}\,\text{s}$ is the ion-track establishment time constant, and $L = 21\,\text{nm}$ is the assumed charge-collection depth for the 7-nm technology [20]. The LET is swept from 5 to 100 MeV·cm^2/mg in 2 MeV·cm^2/mg increments, and all MUX input combinations are evaluated. For each node, the minimum LET producing an erroneous output is recorded as the threshold LET, LET_{th}. A lower LET_{th} then indicates greater radiation sensitivity and is used to identify the primary RHBD targets.

$$I(t) = \frac{Q_{\text{coll}}}{\tau_\alpha - \tau_\beta}\left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right)$$
$$Q_{\text{coll}} = 10.8 \times L \times LET \tag{1}$$

Fig. 2 (a) shows the structure of the 2:1 MUX, which contains six internal nodes. The corresponding LET_{th} values are presented in Fig. 2 (b), where a value larger than 100 indicates that no erroneous output was observed within the investigated LET range. The results show that node16 has a substantially lower LET_{th} than the other nodes and is therefore identified as the primary target for RHBD. Errors at node16 were observed for the input combinations $[S, A, B] = [1, 1, 0]$ and $[0, 0, 1]$, under which its nominal voltage should remain at logic '0'. This behavior indicates that node16 is particularly susceptible to radiation-induced voltage disturbances when held at a low logic level, motivating a hardening strategy specifically designed for this condition.

Accordingly, three 3-fin nFETs are inserted between node16 and ground to act as conditional voltage keepers. These

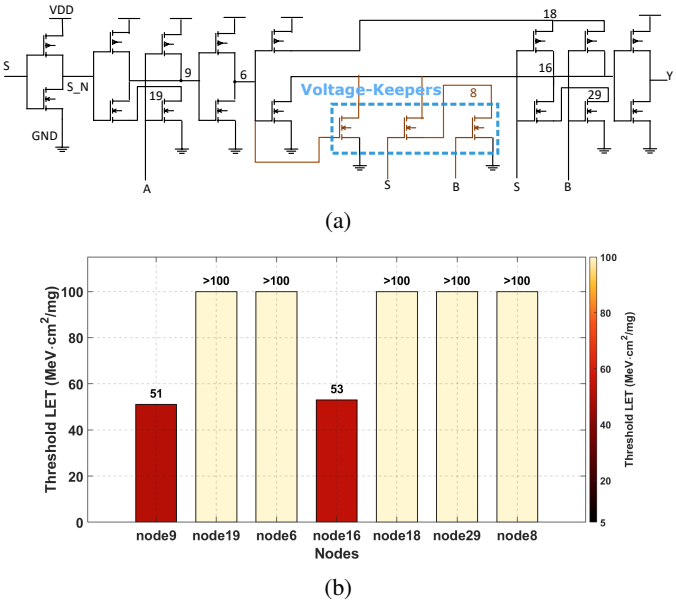

Fig. 3: Proposed SH 2:1 MUX: (a) transistor-level schematic with conditional voltage keepers and (b) threshold-LET values of its internal nodes.

transistors are controlled by S, B, and node6, respectively, and reinforce the low-voltage state of node16 whenever it is expected to remain at logic '0'.

Fig. 3(a) shows the structure of the proposed SH-MUX, in which three 3-fin nFETs are inserted as conditional voltage keepers. The complete fault injection campaign was then repeated for the hardened design, and the resulting LET_{th} values are reported in Fig. 3(b). The proposed RHBD technique increases the LET_{th} of the target node16 from 27 to 53 MeV·cm^2/mg. It also improves the robustness of node18 and node29, whose behavior is affected by node16, increasing their LET_{th} values from 45 and 47 MeV·cm^2/mg, respectively, to larger than 100 MeV·cm^2/mg. Although the hardened structure introduces an additional internal node, node8, no output error was observed for fault injections at this node.

The SH-DFF adopts the design that proposed in our previous research in [21], which is scheduled to appear in the conference proceedings. Because the present work focuses on the integrated BLE and logic array, the previously validated SH-DFF is reused without further structural modification. The structure of the SH-DFF is shown in Fig. 4. By selectively adopting RHBD techniques like transistor resizing and duplication, it is capable of increasing the targeted nodes' LET_{th} from around 35 MeV·cm^2/mg to above 60 MeV·cm^2/mg, demonstrating strong radiation robustness toward SET.

B. SET-Hardened BLE Characterization

The proposed SH-BLE is constructed by integrating the hardened LUT, DFF, and MUX, and its layout is shown in Fig. 5. Its SET resilience is evaluated through a Monte Carlo fault-injection campaign and compared with that of a BLE constructed by the unhardened cells in ASAP7. For each LET value, 5000 simulations are performed, with the input

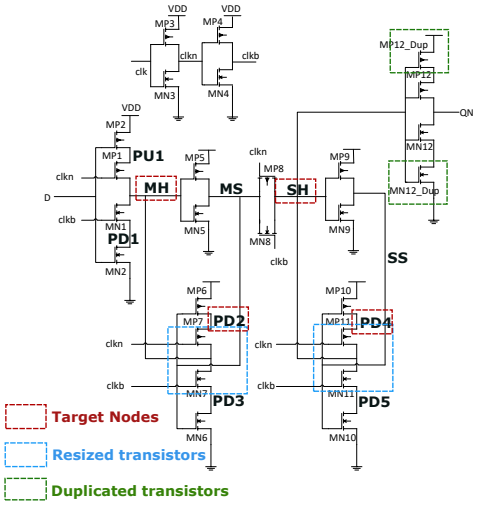

Fig. 4: Transistor-level schematic of the SET hardened DFF proposed in [21].

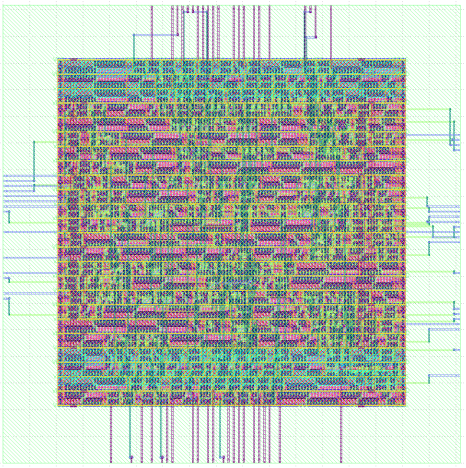

Fig. 5: The physical layout of the proposed SH-BLE.

stimulus and injection node randomly selected in each run to sample different operating and strike conditions. The SET cross section is calculated using (2), where N_{error} is the number of injections producing an observable output error, N_{strike} is the total number of simulations, and A is the estimated effective sensitive area, approximated in this work as the total area occupied by the logic blocks comprising the BLE.

$$\sigma_{\mathrm{SET}} = \frac{N_{\mathrm{error}}}{N_{\mathrm{strike}}} \cdot A \tag{2}$$

Fig. 6 compares the estimated SET cross sections of the baseline and proposed SH-BLEs. The uncertainty of each estimate is quantified using two-sided 95% Clopper–Pearson exact confidence intervals for the underlying binomial error probability. The proposed SH-BLE reduces the SET cross section by nearly one order of magnitude for LET values below 50 MeV·cm^2/mg and to less than half of the baseline value at higher LETs.

TABLE I: Performance comparison between the baseline and SH-BLEs.

Item	Sensitive area (μm^2)	Die area (μm^2)	Read time (ps)	Read energy (J)	Static power (W)
Baseline					
BLE	19.318	70.092	33.77	$1.273E^{-14}$	$2.228E^{-5}$
SH-BLE	24.098	73.685	39.94	$1.348E^{-14}$	$2.236E^{-5}$

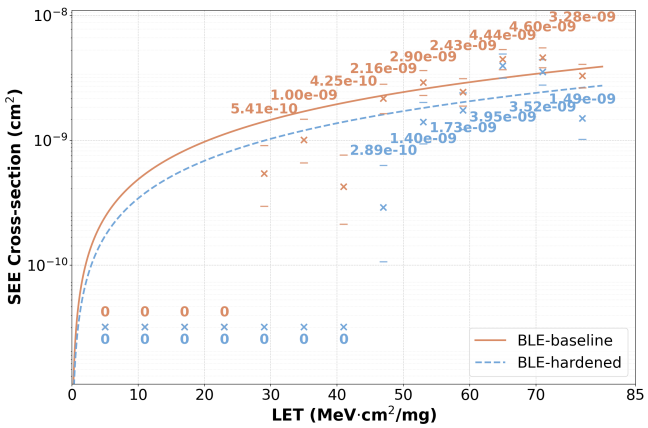

Fig. 6: Estimated SET cross sections of the baseline and proposed SH-BLEs with 95% Clopper–Pearson confidence intervals.

Table I compares the implementation overheads of the baseline and proposed SH-BLEs in terms of sensitive area, die area, read time, read energy, and static power. The sensitive area is defined as the total area occupied by the functional logic blocks, whereas the die area corresponds to the complete BLE layout. The read time and read energy are obtained by individually activating each of the six BLE input ports and averaging the corresponding measurements. Overall, the proposed SH-BLE achieves a substantial improvement in SET resilience over the unhardened design while introducing only moderate area, timing, and power overheads.

C. Physical Implementation of the SH Logic Array

The proposed SH logic array was physically implemented using the OpenROAD flow with the ASAP7 technology platform. The design starts from an RTL top-level module that instantiates 200 SH-BLEs together with the configuration and interconnection logic required to control their operation. Each BLE preserves a hierarchical structure composed of the SH 6-input LUT, DFF, and MUX. The RTL is elaborated and technology-mapped into an ASAP7 gate-level netlist using the open-source Yosys tool [22], after which OpenROAD performs floorplanning, placement, clock-tree synthesis, global and detailed routing, and final layout generation.

The implementation results are summarized in Table II. The synthesized design contains 95,838 mapped cells and occupies 11,983.19 μm^2. Of the 13,000 DFFs, 12,800 store the 64-bit LUT configurations of the 200 BLEs, while 200 serve as BLE output registers, showing that configuration storage dominates the sequential resources. The final layout occupies 22,381.96 μm^2, corresponding to an effective utilization of 53.54% and leaving sufficient space for placement, clock-tree insertion, and routing.

TABLE II: Implementation results of the 200-BLE SH logic array.

Metric	Value
Number of SH-BLEs	200
Total mapped cells	95,838
Total DFF cells	13,000
LUT configuration DFFs	12,800
Synthesized cell area	11,983.19 μm^2
Final die area	22,381.96 μm^2
Effective area utilization	53.54%

Following the physical implementation of the SH logic array, an RTL-to-array synthesis and mapping tool was developed to support its practical use. The tool accepts standard RTL descriptions and translates them into logic functions, BLE assignments, configuration data, and interconnections compatible with the proposed array.

IV. RTL-to-Array Mapping Tool

The review in Section II highlights a recurring limitation in non-standard radiation-hardened reconfigurable architectures: commercial design flows provide limited support when the fabric departs from established vendor architectures. [12] addresses this issue at a later design stage by developing dedicated routing for a fixed radiation-hardened architecture. A similar limitation arises at the RTL-to-array stage, since existing synthesis flows generally target fixed cell libraries rather than reconfigurable architectures with custom logic elements. To address this gap, a dedicated mapping tool was developed to generate the connectivity and configuration data required by the proposed array.

The physical implementations of the BLE primitives are not hardcoded. Instead, the tool treats them as pluggable components and associates them with its internal representation according to port positions rather than naming conventions. Consequently, alternative transistor-level implementations can be substituted without modifying the mapping logic.

The Verilog front end generates a unified parsed representation containing the circuit's primary inputs and outputs, combinational gate instances, and sequential elements. Supported combinational operations include bitwise AND, OR, NOT, XOR, and conditional operators. Sequential logic may be described either through explicitly instantiated reusable flip-flop modules or through register declarations with clocked process blocks. Each sequential instance is reduced to a clock net, optional asynchronous set and reset nets, a data-input net, and an output net. The tool supports positive and negative-edge-triggered flip-flops, asynchronous reset and set signals with either priority ordering, and multiple clock domains under the simplifying assumption of a common clock period.

The tool was evaluated by mapping combinational and sequential benchmarks of different sizes onto the proposed SH logic array. Table III reports the corresponding resource usage for benchmarks from the ISCAS'85, ISCAS'89, and ITC'99 suites. The functional correctness of the generated

TABLE III: Resource usage of the mapped benchmark circuits.

Benchmark	Trans.	Gates	FFs	Nets
C17 (ISCAS'85 [9])	7182	6	0	3412
S27 (ISCAS'89 [10])	12048	10	3	5682
B06 (ITC'99 [11])	39456	39	9	22123
B08 (ITC'99 [11])	150528	149	21	84518
B09 (ITC'99 [11])	168308	140	28	79414

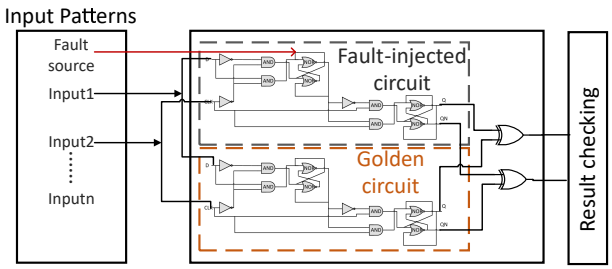

Fig. 7: The developed test setup circuit.

netlists was verified against golden models using HSPICE. For the combinational C17 benchmark, all 32 exhaustive input vectors produced the expected outputs. For the sequential S27 benchmark, the predicted outputs matched transistor-level simulation results over all 16 clock cycles using the BLE implementations. The same result was observed for the B06 benchmark, where all outputs and internal flip-flops states matched transistor-level simulation results over all 4 exhaustive clock cycles using the radiation-hardened BLE implementations. Verification is exhaustive for circuits with up to 20 primary inputs and larger circuits are validated using a fixed reproducibly seeded set of 1024 pseudorandom test vectors, although none of the benchmarks presented here required this fallback, as all remain well below the 20-input exhaustive threshold.

V. Experimental Results

The radiation resilience and deployment overhead of the proposed SH logic array were evaluated using the C17 benchmark. The mapping tool implemented C17 using six BLEs, each configured to realize a 2-input NAND function. To assess SET resilience, the test structure shown in Fig. 7 was constructed. The benchmark was duplicated and driven by identical inputs, with one copy serving as the golden reference and the other as the fault-injected circuit. Monte Carlo fault injection was performed over an LET range of 10–100 MeV·cm^2/mg in 10 MeV·cm^2/mg steps. For each LET value, 10,000 injections were applied to randomly selected internal nodes under randomly generated input stimuli. XOR gates compared the outputs of the two circuits, and any mismatch was classified as a soft error. For comparison, the same experiment was repeated on a C17 implementation constructed from baseline ASAP7 LUT components. Because the effective sensitive area of the mapped circuits could not be determined accurately, SET error rate rather than SET cross section is reported in Fig. 8. The results show that mapping C17 onto the proposed SH logic array substantially reduces the SET error rate relative to the baseline 7-nm LUT

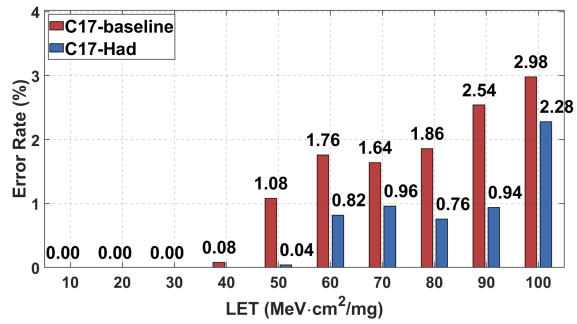

Fig. 8: SET error-rate comparison between the baseline and SH implementations of the C17 benchmark.

TABLE IV: Performance comparison between the different implementations of C17.

Item	Delay (ps)	Dynamic energy consumption (J)	Static power (W)
C17 (Baseline LUT)	156.39	$9.32E^{-14}$	$2.07E^{-4}$
C17 (SH logic array)	156.90	$1.01E^{-13}$	$2.25E^{-4}$

implementation. Specifically, for the injection with LET below 90 MeV·cm^2/mg, the error rate was decreased by more than 50%.

The deployment overhead was also evaluated. Table IV compares the C17 implementations based on the baseline 7-nm LUT and the proposed SH logic array. Delay and energy were measured over a 1-ns simulation window by toggling one input and observing the corresponding output transition, while recording the propagation delay and energy consumed during the event. The results indicate that the proposed SH logic array improves SET resilience while introducing only limited timing and energy overheads.

VI. Conclusions

This work developed and evaluated a 200-BLE SET-hardened reconfigurable logic array in predictive 7-nm FinFET technology. Fault-injection-guided RHBD was applied to the LUT, DFF, and MUX, producing a BLE with substantially lower SET susceptibility than the baseline design and only moderate implementation overhead. The complete array was physically implemented with a die area of 22,381.96 μm^2, and an RTL-to-array mapping tool was developed to generate BLE assignments, LUT configurations, and transistor-level interconnections from Verilog descriptions. Benchmark validation confirmed functional correctness, while C17 fault-injection experiments demonstrated more than 50% reduction in SET error rate below 90 MeV·cm^2/mg with limited timing, energy, and static-power penalties. These results establish a practical circuit-level and design-flow foundation for future radiation-hardened FPGA architectures in advanced FinFET technologies.

REFERENCES

[1] D. S. Lee, M. King, W. Evans, M. Cannon, A. Pérez-Celis, J. Anderson, M. Wirthlin, and W. Rice, "Single-event characterization of 16 nm finfet xilinx ultrascale+ devices with heavy ion and neutron irradiation," in *2018 IEEE Radiation Effects Data Workshop (REDW)*, pp. 1–8, 2018.

[2] P. Davis, D. S. Lee, M. Learn, and D. Thorpe, "Single-event characterization of the 16 nm finfet xilinx ultrascale+tm rfsoc field-programmable gate array under proton irradiation," in *2019 IEEE Radiation Effects Data Workshop*, pp. 1–5, 2019.

[3] A. Keller and M. Wirthlin, "Single-event characterization of a stratix ® 10 fpga using neutron irradiation," pp. 1–6, 2019.

[4] P. Maillard, Y. P. Chen, J. Barton, and M. L. Voogel, "Single event latchup (sel) and single event upset (seu) evaluation of xilinx 7nm versal™ acap programmable logic (pl)," in *2021 IEEE Radiation Effects Data Workshop (REDW)*, pp. 1–6, 2021.

[5] A. Dufour, F. Manni, F. Pierron, D. Dangla, F. Bezerra, J. Mekki, and P. Maillard, "Heavy-ion and proton single event effect (see) characterization of 7nm finfet amd versaltm," in *2023 23rd European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, pp. 1–8, 2023.

[6] S. Azimi, C. De Sio, and L. Sterpone, "Analysis of radiation-induced transient errors on 7 nm finfet technology," *Microelectronics Reliability*, vol. 126, p. 114319, 2021.

[7] S. Lin, Y.-B. Kim, and F. Lombardi, "Design and performance evaluation of radiation hardened latches for nanoscale cmos," *IEEE transactions on very large scale integration (VLSI) systems*, vol. 19, no. 7, pp. 1315–1319, 2010.

[8] V. Vashishtha, M. Vangala, and L. T. Clark, "Asap7 predictive design kit development and cell design technology co-optimization: Invited paper," in *2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 992–998, 2017.

[9] F. Brglez and H. Fujiwara, "A neutral netlist of 10 combinatorial benchmark circuits," *Proc. 1985 ISCAS*, 1985.

[10] F. Brglez, D. Bryan, and K. Koiminski, "Combinational profiles of sequential benchmark circuits," *IEEE International Symposium on Circuits and Systems,*, pp. 1929–1934 vol.3, 1989.

[11] F. Corno, M. Sonza Reorda, and G. Squillero, "Rt-level itc'99 benchmarks and first atpg results," *IEEE Design Test of Computers*, vol. 17, pp. 44–53, 2000.

[12] A. Portaluri, S. Azimi, A. Saracino, L. Sterpone, A. Kilic, and D. Dupuis, "Nxrouting: A gpu-enhanced cad tool for european radiation-hardened fpgas," *Electronics*, vol. 13, no. 14, 2024.

[13] C. De Sio, S. Azimi, L. Sterpone, and B. Du, "Analyzing radiation-induced transient errors on sram-based fpgas by propagation of broadening effect," *IEEE Access*, vol. 7, pp. 140182–140189, 2019.

[14] G. Cora, D. Rizzieri, C. De Sio, S. Azimi, and L. Sterpone, "In-hardware fault-tolerance controller for multi-fpga clustered architectures," *IEEE Transactions on Computers*, pp. 1–14, 2026.

[15] S. Azimi, C. De Sio, A. Portaluri, D. Rizzieri, and L. Sterpone, "A comparative radiation analysis of reconfigurable memory technologies: Finfet versus bulk cmos," *Microelectronics Reliability*, vol. 138, p. 114733, 2022. 33rd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis.

[16] P. Mohan, S. Das, O. Atli, J. Joffrion, and K. Mai, "Design and evaluation of flip-flops for efpga configuration hardening," *2024 24th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, pp. 1–4, 2024.

[17] P. Mohan, S. Das, O. Atli, J. Joffrion, and K. Mai, "A soft error tolerant flip-flop for efpga configuration hardening in 22nm finfet process," in *2025 Design, Automation Test in Europe Conference (DATE)*, pp. 1–6, 2025.

[18] S. Azimi, C. De Sio, B. Du, and L. Sterpone, "On the mitigation of single event transient in 3d lut by in-cell layout resizing," in *2020 20th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, pp. 1–4, 2020.

[19] T. Ajayi, D. Blaauw, T.-B. Chan, C.-K. Cheng, V. A. Chhabria, D. K. Choo, M. Coltella, R. G. Dreslinski, M. Fogac¸a, S. M. Hashemi, A. A. Ibrahim, A. B. Kahng, M. Kim, J. Li, Z. Liang, U. Mallappa, P. I. Pénzes, G. Pradipta, S. Reda, A. Rovinski, K. Samadi, S. S. Sapatnekar, L. K. Saul, C. Sechen, V. Srinivas, W. Swartz, D. Sylvester, D. Urquhart, L. Wang, M. Woo, and B. Xu, "Openroad: Toward a self-driving, open-source digital layout implementation tool chain," 2019.

[20] L. H. Brendler, A. L. Zimpeck, C. Meinhardt, and R. Reis, "Multi-level design influences on robustness evaluation of 7nm finfet technology," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 2, pp. 553–564, 2020.

[21] A. Cui, E. Vacca, L. Sterpone, and S. Azimi, "A novel node- and layout-aware radiation-hardened 7 nm d flip-flop," in *2026 24th IEEE Interregional NEWCAS Conference (NEWCAS)*, 2026.

[22] C. Wolf, J. Glaser, and J. Kepler, "Yosys-a free verilog synthesis suite," 2013.