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Original
Integrated electronics for the readout of neutrino detectors: The case of DENEB for DUNE / Pagliarino, V.. - In: EPJ WEB OF CONFERENCES. - ISSN 2100-014X. - 388:(2026). (Nuclear Energy and its Challenging New Technologies Varenna (Ita) 23-28 June 2025) [10.1051/epjconf/202638800009].

Availability:
This version is available at: 11583/3016179 since: 2026-09-30T20:12:58Z

Publisher:
EDP Sciences

Published
DOI:10.1051/epjconf/202638800009

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02 November 2026

EPJ Web of Conferences **388**, 00009 (2026) https://doi.org/10.1051/epjconf/202638800009
LNES 2025

Integrated electronics for the readout of neutrino detectors: the case of DENEB for DUNE

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Summary. — This work presents the ongoing design of the custom integrated electronics for the GRAIN detector within the DUNE (Deep Underground Neutrino Experiment). GRAIN is an active target consisting of a 1 ton liquid-argon cryostat monitored by single-photon cameras for scintillation track imaging. The DENEB chip, implemented in a 110 nm CMOS technology, integrates 1024 SiPM readout channels optimized for single-photon sensitivity, sub-100 ps timing resolution, and low-power operation under liquid-argon temperature conditions (77 K). The architecture combines analog front-end amplification, time and charge digitization, and digital buffering in a modular design suitable for large-scale integration in high-density cryogenic environments.

1. – Detecting neutrinos at DUNE

The Deep Underground Neutrino Experiment (DUNE) [1] is a flagship international project designed to explore the fundamental properties of neutrinos with unprecedented precision. Its primary scientific objectives include determining the neutrino mass ordering [1], studying CP violation in the leptonic sector of the Standard Model (SM) [3], and observing neutrinos from astrophysical sources such as supernovae [4]. DUNE comprises

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two main facilities: the Near Detector complex at Fermilab in Illinois, which characterizes the unoscillated neutrino beam, and the Far Detector at the Sanford Underground Research Facility in South Dakota, 1.5 km underground and 1285 km away, where oscillated neutrino interactions are recorded. The experiment utilizes a high-intensity, wide-band neutrino beam produced by the Long Baseline Neutrino Facility (LBNF) through pion and kaon decays. This dual-detector configuration enables precise measurements of oscillation parameters, minimizing systematic uncertainties through correlated near-far measurements. Collectively, these systems position DUNE to address some of the most fundamental open questions in particle physics and cosmology.

Within the Near Detector complex, the SAND (System for on-Axis Neutrino Detection) [5] plays a central role in beam monitoring and neutrino interaction studies. At its core the GRAIN (GRanular Argon for Interaction of Neutrinos) detector is installed. GRAIN is a one-ton liquid-argon (LAr) active target designed to image neutrino-induced interactions via scintillation light in the vacuum ultraviolet (VUV) range. The detector integrates an innovative optical readout system composed of SiPM-based cameras capable of reconstructing charged-particle tracks up to the primary interaction vertex. Two optical configurations are under development: a lens-based system using nitrogen-filled fused silica optics with high light transport efficiency developed by INFN-Genova, and a coded-mask system proposed by INFN-Bologna, which enhances spatial coverage and reduces signal pile-up. Approximately 60 SiPM cameras, each consisting of 1024 pixels, are distributed across the cryostat surfaces, providing both high spatial granularity and single-photon sensitivity [6].

2. – Signal processing requirements and challenges

The readout of the GRAIN detector imposes stringent requirements on signal processing due to the need to accurately reconstruct the time of arrival and number of detected photons for each scintillation event. Each SiPM camera, composed of 1024 channels, must timestamp photon bunches with sub-100 ps precision while preserving single-photon sensitivity and handling high photon pile-up rates resulting from dense ionization tracks. The result is a complex waveform requiring advanced optimization of the signal processing chain, like the one shown in fig. 1.

This dual requirement of precise timing on the first photon of each bunch and accurate charge integration (less than 2% of lost photons per pulse) mandates a dedicated front-end architecture capable of both fast pulse discrimination and linear charge measurement over a wide dynamic range (up to several hundreds of photons per pulse, with a maximum of 50 photons perfectly piled up). Because of the cryogenic environment of GRAIN (77 K inside the liquid-argon cryostat), the required performance level and the very high channel density, the use of conventional discrete electronics is unsuitable, thus requiring the development of custom cryogenic integrated electronics placed in close proximity to the sensors to minimize parasitic effects and signal degradation.

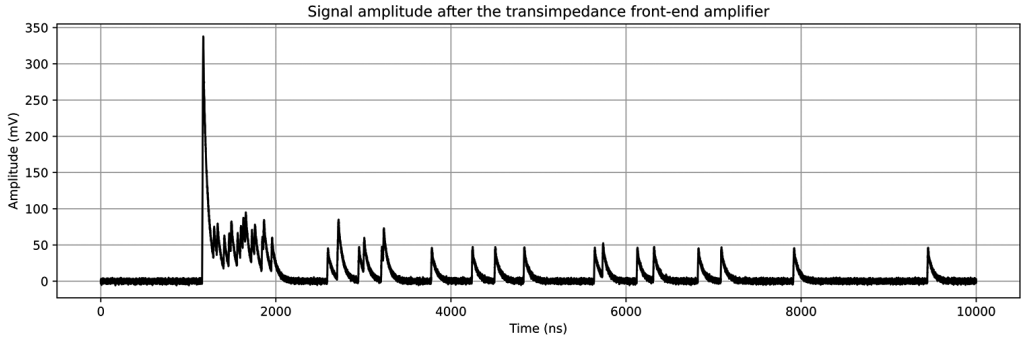


Fig. 1. – Typical signal waveform after the front-end amplifier of a single channel during a beam spill. Source: DENEB behavioural simulation environment, $3 \times 3\,\mathrm{cm}^2$ SiPM with $500\,\mathrm{M}\Omega$ quenching resistor.

Designing integrated circuits for cryogenic operation introduces a set of unique challenges that distinguish them from standard room-temperature implementations [7]. The electrical parameters of CMOS devices, such as threshold voltage, mobility, and transconductance, undergo significant shifts at cryogenic temperatures, affecting both biasing conditions and analog performance. Furthermore, the reduction of thermal noise is counterbalanced by the appearance of non-ideal effects such as carrier freeze-out, increased mismatch, and bias-dependent gain variations. Reliability and mechanical stability also become critical, as thermal cycling can induce stress and parasitic leakage paths. Additionally, the strict power dissipation limit ($< 5\,\mathrm{mW/channel}$, averaged) imposed by the cryogenic environment to prevent local boiling of liquid-argon constrains the analog front-end design, requiring low-power architectures and optimized ADC and TDC converters. The readout electronics, developed at INFN-Torino, include a cryogenic ASIC optimized for timing resolutions below 100 ps and low power dissipation to preserve LAr stability. The neutrino beam has a pulsed structure, consisting of $10\,\mu$s to $20\,\mu$s spill duration with a repetition rate of approximately 1 Hz. Additional data-taking windows are introduced in the inter-spill for searching for astrophysical neutrinos and for calibration purposes.

3. – Architecture of the DENEB ASIC

The DENEB (DUNE integrated Electronics for NEutrino Beams) ASIC, currently under design at INFN Torino, is a full-reticle cryogenic readout chip fabricated in a 110 nm CMOS technology node. The ASIC is mounted in a $500\,\mu$m-pitch BGA package optimized for thermal dissipation in cryogenic environments. The chip integrates 1024 channels organized in 32 columns, each composed of 32 pixels. Every pixel includes a dedicated input pad directly bonded to the package interposer and communicates with neighbouring pixels through a 64-bit high-speed digital bus for data transfer, together with clock, reset, and trigger lines. These signals are locally buffered and resynchronized within each

pixel in the digital domain, ensuring signal integrity regardless of the physical column length. At the end of each column, a dual-port high-density SRAM capable of storing up to 2048 × 64-bit words manages event buffering and decouples the high-throughput triggerless data push from the readout link. The stored data are serialized and transmitted via LVDS/SLVS-compatible transceivers, fully compliant with the CERN lpGBT e-link standard [8], enabling high-speed data communication at 320 MHz in both SDR and DDR modes (up to 640 Mbps). To reduce cabling complexity in low-bandwidth applications, the chip also supports transceiver sharing among multiple columns.

The DENEB architecture has been optimized for modularity, simplifying top-level integration and control. Each end-of-column block and each pixel incorporate redundant SPI configuration registers, allowing both global and fine-grained configuration of individual channels or user-defined subranges to minimize programming latency. The slow-control network provides full configurability of biasing, threshold, and timing parameters, supporting in-field calibration and adaptive operation in cryogenic conditions. For design-for-testability (DfT) and debugging, DENEB integrates multiple diagnostic features: a programmable digital test pulse generator for functional verification, and two dedicated analog pads that respectively allow signal injection into a chosen pixel and waveform probing of its analog front-end. Digital interfaces for probing digital signals of the logic are also placed in the end-of-column area.

The DENEB ASIC has been specifically conceived to ensure reliable operation in cryogenic conditions, addressing the changes in semiconductor behavior that occur at liquid-argon temperatures (77 K). At such low temperatures, the threshold voltage V_{TH} of MOS transistors increases significantly, leading to reduced headroom and altered bias points for analog circuits designed under nominal room-temperature conditions. Moreover, variations in carrier mobility, transconductance, and subthreshold slope affect both the gain and dynamic range of the analog front-end [9]. To mitigate these effects, the analog domain of DENEB integrates a baseline holder circuit with a narrow-band feedback loop that compensates for DC operating point drifts. This circuit stabilizes the input baseline against temperature-induced bias shifts, ensuring consistent charge and timing measurements.

In parallel, the digital and mixed-signal domains were optimized to maintain timing closure under cryogenic conditions: DENEB has been synthesized using High-Speed (HS) MOS devices and standard cells characterized by a lower threshold voltage, providing enhanced switching performance mitigating the effect of the threshold shift. Additionally, timing derate constraints were explicitly applied during the synthesis and place-and-route phases to reduce the probability of setup and hold-time violations arising from mobility enhancement and threshold shift in cryogenic operation. Since the foundry PDK is not natively optimized for cryogenic environments, the design benefited from the direct characterization of the ALCOR ASIC [10], previously developed and tested at INFN Torino, with the same technology.

The floorplan and packaging of the ASIC is represented in fig. 2, as well as the block diagram of the pixel architecture that is described below.

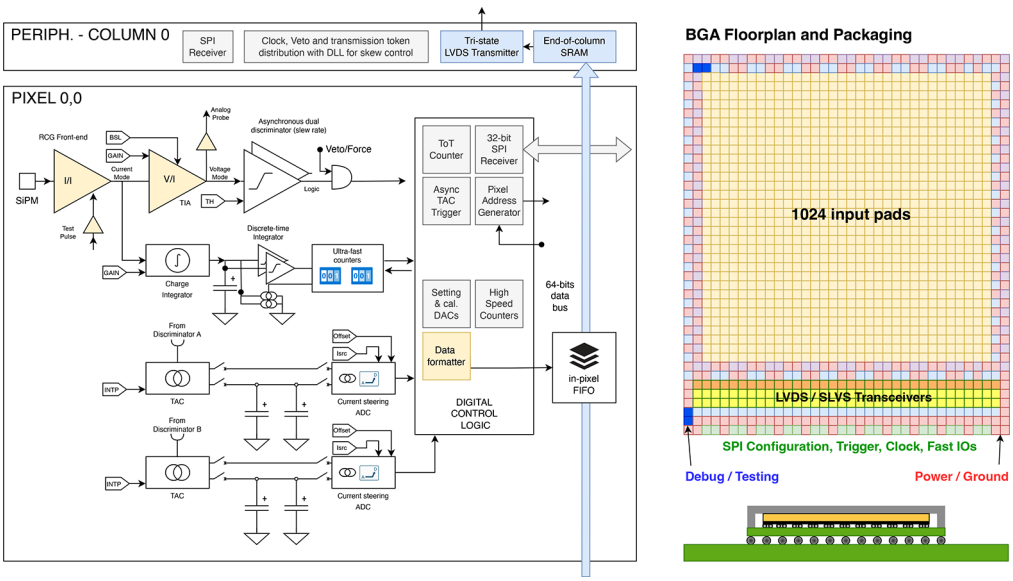


Fig. 2. – Schematic block diagram of the DENEB ASIC architecture (left), together with its floorplan and packaging layout (right).

4. – Architecture of a pixel

The DENEB pixel integrates the complete front-end chain required for analog signal amplification, discrimination, timing extraction, and charge digitization. Each pixel incorporates a custom input pad located in the north-west corner, the analog circuitry is laid out along the western side and the digital logic along the eastern side. To enhance mixed-signal isolation and minimize substrate coupling, columns are implemented in mirrored east-west pairs, reducing the total perimeter of analog-digital interfaces. Additional isolation is achieved through the systematic use of triple-well devices and dedicated guard rings, effectively suppressing digital switching noise propagation into sensitive analog nodes.

The input signal from the SiPM is processed by a dual-polarity regulated common-gate preamplifier with programmable gain, providing two outputs: a current-mode output routed to the digital charge integrator and a voltage-mode output generated by a transimpedance amplifier (TIA) for pulse discrimination. Two high-speed asynchronous discriminators with configurable thresholds are used for either time-over-threshold (ToT) operation, detecting the leading and trailing edges of the pulse, or time-walk correction, by measuring two points on the rising edge to extract the slew rate. The timing digitization is performed by two pairs of time-to-analog converters (TACs) followed by dual-mode analog-to-digital converters (ADCs) capable of operating in either Wilkinson or successive approximation (SAR) mode. These pairs operate under a round-robin scheme, improving derandomization and minimizing dead time under high event rates.

In its highest-resolution configuration, the TDC achieves a bin size of 17 ps RMS with 8-bit ADC resolution, while lower resolutions can be selected to optimize throughput.

To ensure accurate photon counting across a wide dynamic range, the digital charge integrator adopts a sigma–delta architecture in which a programmable 2-bit ADC generates a feedback signal for a 2-bit current-steering DAC that continuously discharges the integration capacitor. The resulting controlled current flow is monitored by synchronous high-speed counters, providing a digital representation of the accumulated charge. The analog and mixed-signal subsystems are managed by a local digital control logic that includes a bus arbitration finite-state machine (FSM) managing data transfers on the 64-bit high-speed inter-pixel bus, as well as a redundant SPI-based configuration register for robust and fine-grained control of pixel parameters.

5. – Conclusions

The DENEB ASIC is currently in the design phase and is planned for submission in 2026. Preliminary system-level and transistor-level simulations confirm that the proposed architectural choices successfully meet the demanding signal processing requirements for reconstructing tracks generated by scintillation light from neutrino interactions in the GRAIN detector of DUNE.

The implemented design solutions demonstrate the capability to achieve the targeted timing resolution, charge accuracy, and low-power operation even under cryogenic conditions, during simulations. Although the employed PDK is not characterized by the foundry for cryogenic operation, the experience gained with the ALCOR ASIC, developed by INFN Torino using the same technology and tested at liquid-argon temperatures, provides strong confidence in the reliability of the adopted simulation models and the overall design approach.

These results indicate that DENEB is on track to provide a robust and scalable readout solution for next-generation liquid-argon neutrino detectors and similar low-temperature photon detection systems that require a flexible and high-channel-density readout solution.

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