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Original
Robust Load Disturbance Rejection in PWM DC - DC Buck Converters / Pirrera, S., Gabriele, F., Lena, D., Pareschi, F., Regruto, D., Setti, G.. - In: IEEE TRANSACTIONS ON CONTROL SYSTEMS TECHNOLOGY. - ISSN 1063-6536. - 34:5(2026), pp. 2464-2479. [10.1109/TCST.2026.3701112]

Availability:
This version is available at: 11583/3015784 since: 2026-09-22T10:00:44Z

Publisher:
Institute of Electrical and Electronics Engineers

Published
DOI:10.1109/TCST.2026.3701112

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14 November 2026

Robust Load Disturbance Rejection in PWM DC-DC Buck Converters

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arXiv:2509.02102v1 [eess.SY] 2 Sep 2025

Abstract

This paper presents a novel approach to robust load disturbance rejection in DC-DC Buck converters. We propose a novel control scheme based on the design of two nested feedback loops. First, we design the controller in the outer loop using H_∞ optimal control theory, and we show, by means of $\mu-$analysis, that such a controller provides robust stability in the presence of uncertainty affecting the physical parameters of the circuit. Then, we introduce an inner feedback loop to improve the system's response to output load disturbances. As far as the inner loop is considered, we propose a novel load estimation-compensation (LEC) scheme, and we discuss under what conditions the insertion of such an inner loop preserves the robust stability of the entire control system. The LEC scheme is compared with the other two linear structures based on well-established disturbance rejection methods. The advantages of LEC in terms of both complexity of implementation and obtained performances are discussed and demonstrated by means of numerical simulation. Finally, we present experimental results obtained through the implementation of the proposed control scheme on a prototype board to demonstrate that the proposed approach significantly enhances disturbance rejection performances with respect to the approach commonly used in DC-DC buck converters.

1 Introduction

The Pulse-Width Modulated (PWM) Buck converter is a DC-DC converter that steps down an unregulated input voltage, delivering a constant output voltage. The output voltage supplies external units that require accurate regulation to operate correctly. Applications of Buck converters include photovoltaic systems [1], electric vehicles [2], and medical electronics [3], among many others.

Owing to its simplicity, Voltage-Mode Control (VMC) is one of the most popular control approaches for DC-DC converters. It is traditionally implemented in practice via a third-order (type-III) compensation network [4], whose design is based on an averaged Linear-Time Invariant (LTI) small-signal model of the converter [5]. From the converter perspective, the supplied system is a time-varying load current that may unpredictably change in time, causing output voltage fluctuations. Additionally, input supply (line) voltage may change, further degrading the output voltage tracking accuracy. Therefore, load and line variations are disturbances, and attenuating their effect on the output is a crucial aspect of the DC-DC converter design. In traditional VMC design, the Disturbance Rejection (DR) requirement contrasts with minimizing the propagation of switching noise caused by PWM [5]. Therefore, the controller must provide a trade-off that may result in an unsatisfactory response to disturbances.

Several techniques are available to improve DR performance. A popular technique in this context is the Feed-Forwarding (FF) [6–9], which is based on feedforward cancellation of the disturbance, which is assumed to be physically measured. Since the input voltage can be easily sensed, line-disturbance FF is feasible and implemented in commercial products; see, e.g., [10, 11]. In contrast, implementing load-disturbance FF is impossible because the output current cannot be directly measured.

Within digital control, effective DR methods are based on adaptive schemes; see, e.g. [12–15]. Moreover, hybrid and time-varying model predictive control have been proven effective for DR in [16] and [17], respectively. However, these approaches incur significant additional costs and require increased circuit area due to the inclusion of digital components such as analog-to-digital converters and sample-and-hold circuits [5]. For this reason, analog solutions are preferable in several application scenarios. Among them, we mention [18–21], which proposes alternative transistor-level architectures of Operational AMPlifiers (OpAMPs) and operational transimpedance amplifiers used to implement the traditional controller [4]. Other analog-based DR methods include [22–25], which introduce additional components to modify either the feedback signal or the PWM pulse depth in response to load variations. However, the effects of the proposed modifications on the feedback system's theoretical properties are not analyzed. Their validity is solely confirmed through empirical simulations and experimental measurements. Furthermore, these approaches are architecture-specific, thus limiting their generalizability.

From a broader perspective, not limited to Buck converters, most DR techniques supported by rigorous theoretical analysis involve estimating the disturbance to

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apply a proper correcting action; see [26] for a comprehensive review. Works [27–29] estimate the disturbance utilizing an Extended State Observer (ESO) [30]. To enhance performance, a generalization of the ESO called Generalized Proportional-Integral Observer (GPIO) is considered in [31–33]. The main drawback of GPIO is that its analog implementation is expensive because it consists of a high-order filter for which a potentially large number of OpAMPs is required, thus increasing the overall system complexity and cost. DR schemes for which a simple implementation is possible are investigated in [34, 35], where reduced-order observer design is proposed, and in [36], which considers Kalman filter-based design.

Another crucial aspect to be considered in the design of Buck converters is the presence of uncertainty in the values of the electrical components, which may strongly affect the closed-loop system's stability. In fact, ensuring closed-loop stability for all allowed component values (i.e., robust stability) is crucial for the safe operation of the circuit. This problem has been considered for various DC-DC converters in, e.g., [37, 38]. However, the problem of ensuring the robust stability of Buck converters that include DR schemes has received little attention so far. The problem is marginally considered in [35, Sec. II-E], where the authors study the location of the poles by varying the capacitance value only. They disregard the presence of uncertainty on other Buck converter component values, such as inductance, winding resistance, and capacitor series resistance. Instead, [36, Sec. III-A] evaluates the closed-loop gain and phase stability margins. Yet, it is widely established that these indices are unreliable indicators of robustness [39]. In this work, we are interested in developing novel DR schemes with guaranteed robust stability against uncertainty in all the component values using established results on $\mathcal{H}_\infty$ and μ-analysis [40, 41].

The main contributions of this paper are summarized here.

- Starting from a suitable formalization of performance requirements, we design an $\mathcal{H}_\infty$ optimal controller. Unlike previous works on $\mathcal{H}_\infty$ Buck control [42–44], we show that the $\mathcal{H}_\infty$ controller transfer function resembles that of the traditional controller commonly used in commercial Buck converters [4]. Furthermore, we prove its robust stability through μ-analysis [40].

- We propose three different load DR architectures. First, we apply the Disturbance Observer (DOB) [45, 46] and Unknown Input Observer (UIO) [47, 48] designs. Next, we introduce a third, original approach named Load Estimator-Compensator (LEC), tailored for Buck converters. While our primary focus is on VMC, the proposed methodology is versatile and can be applied to other Buck control methods, such as peak/valley voltage or current mode control [5].

- We demonstrate that direct insertion of LEC into the system preserves nominal closed-loop stability. This crucial property is not guaranteed when DR is performed using DOB and UIO. Furthermore, we derive a sufficient condition for robust stability in the presence of the LEC, and we show that the LEC can be designed to fulfill such a condition.

- We present a low-complexity analog implementation of the proposed LEC, thus avoiding the overhead costs involved in DR schemes based on using digital solutions and GPIO.

- We compare the performance of the three considered DR schemes by means of numerical simulation.

- We show the effectiveness of the proposed control scheme compared to the traditional approach commonly used in commercial Buck converters by performing experimental laboratory tests on a prototype board implementing the proposed solution.

The paper is organized as follows. In Sec. 2, we present the Buck converter and its mathematical model. In Sec. 3, we review the traditional VMC design for Buck converters and basic notions of $\mathcal{H}_\infty$ optimal control. Next, we formulate the control objectives and discuss the $\mathcal{H}_\infty$ design for the Buck controller, showing that it is closely related to the traditional voltage-mode controller. In Sec. 4, we introduce and analyze the three proposed load DR solutions. Sec. 5 focuses on the proposed LEC, providing nominal and robust stability results. Sec. 6 presents results from simulations comparing the three proposed architectures, describes the analog circuit implementation of the system using the LEC, and provides results from experimental measurements conducted on a prototype board. Finally, Sec. 7 draws conclusions.

2 Buck Converter Model

2.1 Architectural Description

In this paper, we consider the Buck converter in Fig. 1. From a high-level perspective, it consists of a feedback loop comprising the sawtooth-based PWM, the Half-Bridge (HB), the Power Stage (PS), and the controller $\mathcal{K}$. At this stage, we neglect the presence of the inner loop implementing the load DR scheme, i.e., we neglect the presence of the two blocks $\mathcal{E}$ and $\mathcal{F}$. We focus here on the outer control loop where the controller $\mathcal{K}$ has to be designed to regulate the output voltage $v_o(t)$ to the target level V_o^{target}.

The PWM stage implements a trailing-edge modulation. It compares the control signal $v_{\text{c,tot}}(t)$ against $v_{\text{saw}}(t)$, which is a sawtooth signal with amplitude V_{pk} and a fixed switching frequency of $f_{\text{sw}} = \omega_{\text{sw}}/(2\pi) = 1/T_{\text{sw}}$. Accordingly, the PWM output is a logic signal $d(t) \in \{0, 1\}$ having the same frequency as $v_{\text{saw}}(t)$. The HB includes the High Side (HS) and Low Side (LS) power MOSFETs. The HS pulls the SW node to the input voltage V_{in}; conversely, the LS ties the SW node to the voltage reference. For our purposes, the HS and LS MOSFETs are modeled with the switches $\text{SW}^{\text{HS,LS}}$ in series with their ON resistances $R_{\text{ON}}^{\text{HS,LS}}$. The signal

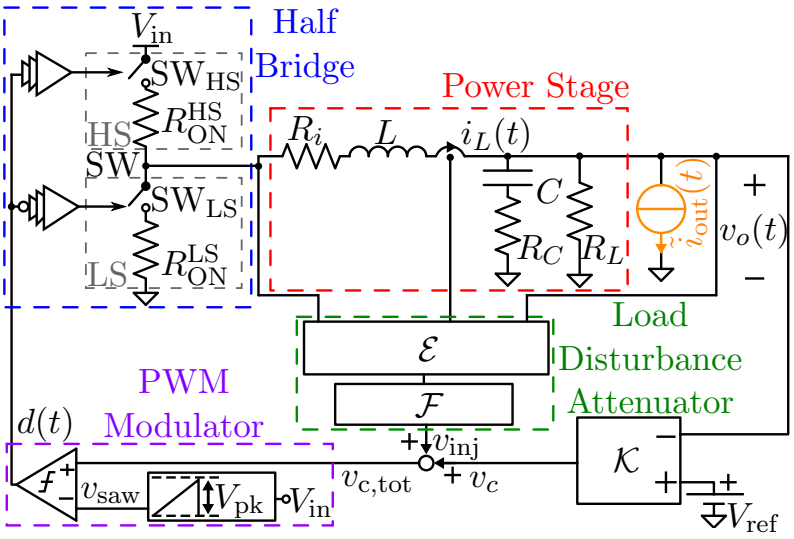


Figure 1: VMC Buck converter with load disturbance attenuator.

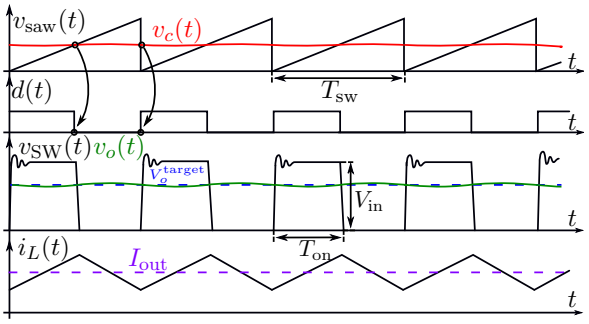


Figure 2: Steady-state operation of a Buck converter in CCM.

$d(t)$ drives the switches through gate drivers. The supply voltage, V_{in}, remains constant during the operation of the Buck, i.e., $V_{\text{in}}(t) = V_{\text{in}}$ for all $t \geq 0$, but its actual value is only known to lie in $[V_o^{\text{target}}, V_{\text{in,max}}]$. Concerning the input voltage, the PWM block implements FF compensation. The PS includes the output filter, composed of the inductor L and the output capacitor C, together with the respective parasitic resistances R_i and R_c. Furthermore, the load-resistance R_L fixes the DC output current I_{out}. Finally, the controller $\mathcal{K}$ compares the constant voltage reference V_{ref} with $v_o(t)$ to achieve the desired regulation by generating the command input $v_c(t)$. A detailed discussion about $\mathcal{K}$ is postponed to Sec. 3.

In this work, we will consider the Continuous Conduction Mode (CCM) operation of the Buck converter. In other words, we assume that during each period $[kT_{\text{sw}}, (k+1)T_{\text{sw}})$, $k \in \mathbb{N}$, the inductor current is always positive; see, e.g., [5]. The Buck operating principle in CCM is sketched in Fig. 2. At steady-state, the circuit time evolution is cyclostationary and the duty-cycle of $d(t)$ and $v_{\text{SW}}(t)$ is a constant value D_c. The value D_c is such that the mean of the output voltage $v_o(t)$ equals V_o^{target}. Conversely, when an exogenous disturbance is applied (e.g., a load current $i_o(t)$), $v_o(t)$ deviates from V_o^{target} and, consequently, $d(t)$ changes through the control action $v_c(t)$.

Throughout the paper, we will consider a case study to support the introduced arguments with numerical values. The considered parameter values and their uncertainties are listed in Table 1. The nominal load resistance and its uncertainty are defined respectively as $R_{L,\text{nom}} = (\underline{R_L} + \overline{R_L})/2$ and $\mathcal{I}_{R_L} \doteq [\underline{R_L}, \overline{R_L}]$, where

$$\underline{R_L} = \frac{V_o^{\text{target}}}{I_{\max}}, \quad \overline{R_L} = \frac{2L_{\min} f_{\text{sw}}}{1 - V_o^{\text{target}}/V_{\text{in,max}}}, \tag{1}$$

and $L_{\min}$ is the minimum inductor value considering its uncertainty. The interval $\mathcal{I}_{R_L}$ guarantees the converter operation in CCM [5].

2.2 Mathematical model

We model the Buck converter as the cascade connection of two blocks: the first one comprises the PWM and HB stages, while the second is the PS. This section presents the mathematical models of these blocks.

2.2.1 PWM stage and Half Bridge

The PWM stage is a nonlinear time-varying system implementing the function

$$d(t) = \text{PWM}(v_c(t)) = \begin{cases} 0 & v_c(t) < v_{\text{saw}}(t) \\ 1 & \text{otherwise.} \end{cases} \tag{2}$$

Motivated by the frequency-domain nature of the $\mathcal{H}_\infty$ design, we study the frequency behavior of the PWM block. Results in this matter are available in the literature. Our analysis is based on the following result from [49].

Result 1 (Trailing-edge modulation of a sinusoid)**.** *Let's define the signal* $v_1(t) = R_0 + R_1 \cos(\omega_1 t + \theta_1)$. *Suppose that* $\omega_1 < \omega_{\text{sw}}$ *and that* $R_0 + R_1 < V_{\text{pk}}$, $R_0 - R_1 > 0$. *The corresponding modulated signal* $d(t) = PWM(v_1(t))$ *is given by:*

Table 1: Main Buck converter parameter's nominal values (Nom. Val.) and their respective uncertainties (Unc.), when applicable.

Parameter	Nom. Val.	Unc.	Parameter	Nom. Val.	Unc.	Parameter	Nom. Val.	Unc.
C	$0.249\,\mathrm{mF}$	10%	R_C	$0.115\,\mathrm{m\Omega}$	15%	$R_{\mathrm{ON}}^{\mathrm{HS,LS}}$	$6.5\,\mathrm{m\Omega}$	$\pm 15\%$
L	$8.2\,\mu\mathrm{F}$	20%	R_i	$7\,\mathrm{m\Omega}$	$\pm 15\%$	$I_{\max}$	$10\,\mathrm{A}$	-
R_L	$R_{L,\mathrm{nom}}$	$\mathcal{I}_{R_L}$	f_{sw}	$500\,\mathrm{kHz}$	-	$V_{\mathrm{in,max}}$	$20\,\mathrm{V}$	-
k_{FF}	30	-	V_o^{target}	$5\,\mathrm{V}$	-			

$$d(t) = D_c + \frac{M}{2}\cos(\omega_1 t + \theta_1) + \tag{3a}$$

$$+ \sum_{m=1}^{+\infty} \frac{1}{m\pi}\{\sin[m(\omega_{sw}t + \theta_c)] + \tag{3b}$$

$$-J_0(m\pi M)\sin[m(\omega_{sw}t + \theta_c) - 2mD\pi]\} +$$

$$+ \sum_{m=1}^{+\infty}\sum_{n=\pm 1}^{\pm\infty} \frac{J_n(m\pi M)}{m\pi}\times \tag{3c}$$

$$\times \sin\left[\frac{n\pi}{2} - m(\omega_{sw}t + \theta_c) - n(\omega_1 t + \theta_1) + 2mD\pi\right]$$

where $J_n(z)$ are Bessel functions of the first kind, $D_c = R_0/V_{\mathrm{pk}}$ is the average duty ratio, and $M = 2R_1/V_{\mathrm{pk}}$ is the modulation index.

Let us now analyze each term of Eq. (3) separately.

1. $D_c + \frac{M}{2}\cos(\omega_1 t + \theta_1)$ in Eq. (3a) is equivalent to $(1/V_{\mathrm{pk}})v_1(t)$.
2. the terms in Eq. (3b) are frequency components at multiples of ω_{sw}. Since $J_0(z) < 1$ for all $z \in \mathbb{R}$ [50], each term of this series is bounded in magnitude by $D_{m,0} \doteq 2/(m\pi)$.
3. the terms in Eq. (3c) amount for the frequency components around $m\,\omega_{\mathrm{sw}}$. Their amplitudes depend on the modulation index M and, thus, on the amplitude R_1. However, using the property $|J_n(z)| \le z^n/(n!\,2^n)$ [50, Page 49] and given an upper bound $\overline{R}_1$ on R_1, we can bound the amplitudes of these terms as:

$$\frac{1}{m\pi n!}\left(\frac{m\pi M}{2}\right)^n \le \frac{(m\pi)^{n-1}}{n!}\left(\frac{\overline{R}}{V_{\mathrm{pk}}}\right)^n \doteq D_{m,n}. \tag{4}$$

Overall, an alternative representation of (3) is

$$d(t) = \frac{1}{V_{\mathrm{pk}}}v_1(t) + e_1(t) \tag{5a}$$

$$e_1(t) \doteq \sum_{m=1}^{+\infty}\sum_{n=-\infty}^{+\infty} A_{m,n}\cos[\omega_{m,n}t + \phi_{m,n}] \tag{5b}$$

with $\omega_{m,n} \doteq m\omega_{\mathrm{sw}} + n\omega_1$, $\phi_{m,n} \in [0, 2\pi)$, and $A_{m,n} \le D_{m,n}$. The bounds on $A_{m,n}$ are independent of v_1. Thus, as far as the controller design is concerned, we can consider each term of Eq. (5b) as a sinusoidal disturbance at frequency $\omega_{m,n}$ that needs to be rejected.

Based on Eq. (5), the PWM block allows for a linear model when a sinusoid is applied as input. Since the command input $v_c(t)$ does not contain a single harmonic, we look for a more general description. Consider the following assumptions:

Assumption 1. *The control input voltage, $v_c(t)$, is described by:*

$$v_c(t) = R_0 + \sum_{k\in\mathcal{I}_c} R_k\cos(\omega_k t + \theta_k) \tag{6}$$

where $\mathcal{I}_c$ is a (possibly infinite) set of indices such that $\omega_k < \omega_{\mathrm{sw}}$ and $\theta_k \in [0, 2\pi)$.

Assumption 2. *The PWM operates in a small-signal regime, i.e., the variations around the operating point (R_0, D_c) are small. Therefore, there exists a constant $\overline{R}$ such that $R_k \le \overline{R}$ for all k.*

Remark 1. *Assumption 1 is reasonable as long as the closed-loop system's bandwidth is lower than f_{sw}. This, therefore, leads to an easy-to-check design constraint.*

According to Assumption 2 and the linear description (5), we can apply superposition of effects. We define e_k according to (5b) with ω_k in place of ω_1, and allowing $A_{m,n}$, $\theta_{m,n}$ to depend on k. Accordingly, we have

$$d(t) = \frac{1}{V_{\mathrm{pk}}}v_c(t) + \sum_{k\in\mathcal{I}_c} e_k. \tag{7}$$

Remark 2. *The model in Eq. (7) is coherent with the averaged small-signal model of the PWM stage. Indeed, the latter coincides with the first term in Eq. (7), i.e., $1/V_{\mathrm{pk}}$; see [5].*

Remark 3. *Assumption 2 is compatible with the design constraint imposing that $v_c(t)$ never exceeds the voltage saturation limits imposed by the PWM stage, i.e.,*

$$0 \le v_c(t) \le V_{pk}, \quad \forall t \ge 0. \tag{8}$$

In fact, to meet this requirement, the sum of all contributions in (6) for $k \in \mathcal{I}_c$ must remain bounded by $\min(R_0, V_{\mathrm{pk}} - R_0)$.

Next, the logic signal $d(t)$ drives the HB block, which generates $v_{\mathrm{SW}}(t) = V_{\mathrm{in}}d(t)$. Considering Eq. (7), we have

$$v_{\mathrm{SW}}(t) = V_{\mathrm{in}}\frac{1}{V_{\mathrm{pk}}}v_c(t) + d_a(t) \tag{9}$$

where $d_a(t) = \sum_{k\in\mathcal{I}_c} V_{\mathrm{in}}e_k(t)$ represents the total actuator disturbance to be rejected. The magnitude of each harmonic of $d_a(t)$, i.e., $V_{\mathrm{in}}A_{m,n,k}$ is bounded by $V_{\mathrm{in}}D_{m,n}$, for all m, n and k. Eq. (9) depends on the converter supply voltage V_{in}, which is highly uncertain

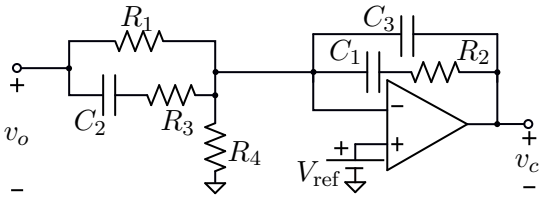


Figure 3: Type-III compensation network implementing $\mathcal{K}$.

in practice. Since the considered Buck implements input voltage FF, this dependency is actually eliminated. In practice, the PWM stage is designed such that V_{pk} is adjusted according to $V_{\text{pk}} = V_{\text{in}}/k_{\text{FF}}$, where k_{FF} is a constant called FF static gain. Therefore, Eq. (9) simplifies to

$$v_{\text{SW}}(t) = k_{\text{FF}} v_c(t) + d_a(t). \tag{10}$$

Eq. (10) is a linear model of the PWM and HB blocks.

2.2.2 Power stage

The PS is a multivariable LTI system described by:

$$\begin{bmatrix} v_o(s) \\ i_L(s) \end{bmatrix} = P(s) \begin{bmatrix} v_{\text{SW}}(s) \\ \tilde{i}_{\text{out}}(s) \end{bmatrix} = \begin{bmatrix} P_{11}(s) & P_{12}(s) \\ P_{21}(s) & P_{22}(s) \end{bmatrix} \begin{bmatrix} v_{\text{SW}}(s) \\ \tilde{i}_{\text{out}}(s) \end{bmatrix} \tag{11}$$

where $v_{\text{SW}}(t)$ is given in Eq. (10), $\tilde{i}_{\text{out}}(t)$ is the output current disturbance, and $i_L(t)$ and $v_o(t)$ are the measured inductor current and output voltage, respectively. Applying standard circuit theory, we obtain:

$$P_{11}(s) = \frac{R_L(1 + CR_c s)}{\alpha_0 s^2 + \alpha_1 s + \alpha_2} = P_{22}(s) \tag{12a}$$

$$P_{12}(s) = R_L \frac{-CLR_c s^2 - (L + CR_c R_i')s - R_i'}{\alpha_0 s^2 + \alpha_1 s + \alpha_2} \tag{12b}$$

$$P_{21}(s) = \frac{C(R_L + Rc)s + 1}{\alpha_0 s^2 + \alpha_1 s + \alpha_2} \tag{12c}$$

with

$$\begin{aligned} &R_i' = R_i + R_{\text{ON}}^{\text{HS,LS}}, \quad \alpha_0 = CL(R_L + R_c), \\ &\alpha_1 = L + CR_L(R_c + R_i') + CR_c R_i', \quad \alpha_2 = R_L + R_i' \end{aligned} \tag{13}$$

In the following, we denote as $\omega_{\text{ESR}} = 1/(CR_c)$ the frequency of the zero of P_{11} and as $\omega_{\text{PS}} = \sqrt{\alpha_2/\alpha_0}, \zeta_{\text{PS}} = \alpha_1/(2\sqrt{\alpha_0\alpha_2})$ the frequency and damping of the plant poles, respectively.

3 Design of the Voltage-Mode Controller $\mathcal{K}$

In this section we review the traditional design of $\mathcal{K}$ (3.1) and basic notions of $\mathcal{H}_\infty$ optimal control (3.2). Next, we formalize the control design objectives and present an $\mathcal{H}_\infty$ design of $\mathcal{K}$ (3.3), demonstrating its close connection with the VMC traditional design approach.

3.1 Traditional Design Approach

The traditional design of $\mathcal{K}$ is based on the availability of an averaged small-signal model of the Buck converter, i.e., an LTI model of the non-linear circuit derived under small-signal assumption. The small-signal averaging technique is a well-consolidated approach to derive LTI models of the PWM and the HB blocks, which constitute the only non-linear part of a Buck converter; see, e.g., [5, 51]. Specifically, the overall small-signal model of the plant (i.e., HB, PWM, and PS) is the transfer function:

$$G_{v_c}^{v_o}(s) = \frac{v_o(s)}{v_c(s)} = k_{\text{FF}} P_{11}(s). \tag{14}$$

In the traditional VMC design approach, which is widely adopted in commercial Buck converter implementations, $\mathcal{K}$ is realized by the type-III compensation network shown in Fig. 3. We can easily derive the transfer function of the traditional type-III controller using circuit theory:

$$\mathcal{K}_{\text{trad}}(s) = \frac{G_{\text{c0}}\,(1 + s/\omega_{\text{z,0}})\,(1 + s/\omega_{\text{z,1}})}{s\,(1 + s/\omega_{\text{p,0}})\,(1 + s/\omega_{\text{p,1}})}, \tag{15}$$

where $G_{c0} = R_1^{-1}(C_2 + C_3)^{-1}$, $\omega_{p,0} = (R_3 C_2)^{-1}$, $\omega_{p,1} = R_2^{-1}\frac{C_1+C_3}{C_1 C_3}$, $\omega_{z,0} = (R_2 C_1)^{-1}$, and $\omega_{z,1} = C_2^{-1}(R_1 + R_3)^{-1}$. Several design methodologies have been established to achieve both stability and the desired performances in VMC Buck converters [9, 52–55]. Typically the zeros $\omega_{z,0}, \omega_{z,1}$ are placed close to the frequency ω_{PS}, while the poles $\omega_{p,0} = \omega_{\text{sw}}/2$ and $\omega_{p,1} = \min\{\omega_{\text{ESR}}, \omega_{\text{sw}}/2\}$ serve to both suppress the switching-frequency noise and cancel out the effect of the ω_{ESR} zero in (14). Finally, the pole in $s = 0$ ensures zero steady-state output voltage regulation error. Furthermore, $G_{c,0}$ is designed to set the closed-loop system bandwidth well-below ω_{sw} and above ω_{PS}.

3.2 Review of $\mathcal{H}_\infty$ optimal control and μ-analysis

This section reviews basic notions from $\mathcal{H}_\infty$ optimal control theory. We refer the reader to, e.g., [40], [41] for more details.

The $\mathcal{H}_\infty$ norm of a system $G(s)$ is defined as

$$\|G(s)\|_{\mathcal{H}_\infty} \doteq \sup_{\omega \in \mathbb{R}} \sigma_x\left(G(i\omega)\right) \tag{16}$$

where $\sigma_x(A)$ denotes the maximum singular value of the matrix transfer function $A(s)$. The $\mathcal{H}_\infty$ norm is the system gain induced by the ℓ_2 to ℓ_2 norm for signals, i.e., if $z = Gw$, then

$$\|z\|_2 \leq \|G\|_{\mathcal{H}_\infty} \|w\|_2 \tag{17}$$

where $\|x(t)\|_2 \doteq \sqrt{\int_0^\infty \|x(t)\|_2^2 \,\mathrm{d}t}$. Accordingly, the physical meaning of the $\mathcal{H}_\infty$ norm is the maximum energy amplification of the system.

Consider the feedback control system depicted in Fig. 4 with plant $G(s) = k_{\text{FF}} P_{11}$, controller $K(s)$, and feedback gain G_f. The S/T mixed-sensitivity $\mathcal{H}_\infty$ optimal control problem is given by [40, 41]:

$$\gamma^* = \min_K \left\| \begin{bmatrix} W_1 S \\ W_2 T \end{bmatrix} \right\|_{\mathcal{H}_\infty} \tag{18}$$

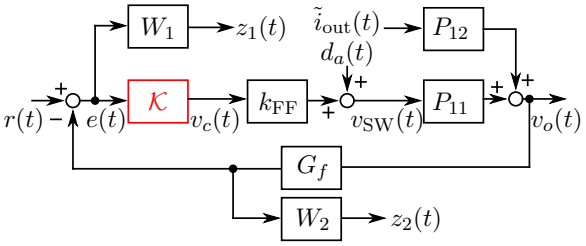


Figure 4: Generalized plant for $\mathcal{H}_\infty$ design.

where, $S(s) = (1 + \mathcal{K}(s)\,G(s)\,G_f)^{-1}, T(s) = 1 - S(s)$. The transfer functions $W_1(s), W_2(s)$ account for performance specifications by defining upper bounds on the desired magnitude of S and T, respectively. The model of the plant, when augmented with W_1, W_2 to generate fictitious outputs $z_1 = W_1 S r$ and $z_2 = W_2 T r$, is referred to as the generalized plant.

In this work, we devote special attention to robust stability, i.e., the property of the feedback system to be stable for all allowed perturbations of certain parameters. Uncertainty is usually described by means of the feedback interconnection of a known block M and an uncertain but bounded block Δ, called $M - \Delta$ structure (see, e.g., [40, 41] for details). If Δ is such that $\|\Delta\|_{\mathcal{H}_\infty} < 1$, we deal with unstructured uncertainty, and robust stability is ensured if

$$\sup_{\|\Delta\|_{\mathcal{H}_\infty}<1} \|M\Delta\|_{\mathcal{H}_\infty} = \|M\|_{\mathcal{H}_\infty} < 1. \tag{19}$$

When Δ is a matrix with a specific structure, e.g., when many independent sources of uncertainty are present, we deal with structured uncertainty. In this case, robust stability is ensured by looking at the structured singular value defined as

$$\mu(M) \doteq (\min\{k_m \mid \det(I - k_m M\Delta) = 0\})^{-1}. \tag{20}$$

If $\mu < 1$, robust stability is ensured. Methods to compute bounds on μ are available; see, e.g., [56].

3.3 Control objectives and $\mathcal{H}_\infty$ design

This section presents an $\mathcal{H}_\infty$ optimal controller design for the Buck converter. We consider the following performance objectives:

R1) zero steady-state regulation error;

R2) rejection of the disturbance $d_a(t)$ introduced by the PWM stage as defined in Sec. 2.2.1;

R3) minimization of overshoot/undershoot and settling time in the presence of output current disturbance;

R4) robust stability against the uncertainty of the Buck component values.

We formulate the problem in the $\mathcal{H}_\infty$ setting. Fig. 4 shows the generalized plant used for design. We design the weighting functions $W_1(s), W_2(s)$ in Eq. (18) to account for the performance requirements R1-R3. Instead, we account for R4 a-posteriori by proving robust stability of the designed controller through μ-analysis.

Remark 4. *In principle, we could account for R4 a-priori during the design phase in two ways. The first is computing a bound on the unstructured uncertainty Δ and including the constraint $\|M\|_\infty < 1$ in the $\mathcal{H}_\infty$ optimization. Such a bound on Δ can be computed using the polynomial method in [57]. However, this approach is conservative in presence of parametric uncertainty and leads to a closed-loop system with a very small bandwidth. The second approach is using μ-synthesis [56] to account for the structured uncertainty. This approach is non-conservative but involves an iterative procedure (D-K iterations) that may converge to suboptimal solutions. Therefore, we prefer to assess the robust stability of the designed control loop a-posteriori using $\mu-$ analysis.*

We account for R1-R3 by the following choices on W_1, W_2. To account for $R1$, we impose the presence of one pole at $s = 0$ in W_1. For $R2$, given

$$G_{d_a}^{v_c}(s) \doteq \frac{v_c(s)}{d_a(s)} = \frac{1}{k_{\text{FF}}} T(s), \tag{21}$$

to reject the generic component of $d_a(t)$ at frequency $\omega = \omega_{m,n,k} = m\omega_{\text{sw}} - n\omega_k$, we impose the constraint:

$$|A_{m,n,k}|\,\left|G_{d_a}^{v_c}(i\,\omega_k)\right| = \frac{D_{m,n} V_{\text{in}}}{k_{\text{FF}}}\,|T(i\,\omega)| \le \epsilon_{m,n} V_{\text{in}} \tag{22}$$

where $\epsilon_{m,n}$ is maximum error of $v_c(t)$ relative to V_{pk}, for all k. Using $V_{\text{pk}} = V_{\text{in}}/k_{\text{FF}}$, we get $|T(i\,\omega)| \le \epsilon_{m,n}/D_{m,n}$. The frequency components $\omega_{m,n,k}$ of $v_c(t)$ are mainly determined by the closed-loop crossover frequency ω_c. As discussed in Remark 1, we have that $\omega_k \le \omega_c < \omega_{\text{sw}}/2$. At the same time, $|T(i\,\omega)|$ is decreasing for $\omega \ge \omega_{\text{sw}}/2$. Consequently, $\omega_{\text{sw}}/2$ is the worst-case over k for constraint (22) and a sufficient condition for (22) is

$$|T\,(i\,(m - n/2)\omega_{\text{sw}})| \le \epsilon_{m,n}/D_{m,n}. \tag{23}$$

To ensure decaying error for increasing m, n, we select: $\epsilon_{1,0} = 10^{-2}$, $\epsilon_{2,0} = 10^{-3}$, $\epsilon_{m+1,0} = 0.5\epsilon_{m,0}$ for $m \ge 2$, $\epsilon_{m,1} = 10^{-3}$ for all m, and $\epsilon_{m,n+1} = 0.5\epsilon_{m,n}$ for all m and $n \ge 1$. Eq. (23) defines a set of constraints on the complementary sensitivity function T (see, red and orange horizontal lines in Fig. 5).

Finally, to account for R3, we consider

$$G_{\tilde{i}_{\text{out}}}^{v_o} \doteq \frac{v_o(s)}{\tilde{i}_{\text{out}}(s)} = P_{12}(s) S(s). \tag{24}$$

Thus, since $P_{12}(s)$ is fixed, R3 is naturally recast as constraints on $S(s)$ through W_1. Specifically, the pole at $s = 0$ in W_1 is sufficient to reject constant $\tilde{i}_{\text{out}}(t)$ at steady-state and a large bandwidth of W_1 is related to a fast response.

Overall, we select

$$W_1 = \frac{s^2 + 2\zeta_{\text{s}}\omega_{\text{s}} s + \omega_{\text{s}}^2}{S_{p0} s(s + 2\zeta_{\text{s}}\omega_{\text{s}})} \quad W_2 = \frac{s^2 + 2\zeta_t\omega_t s + \omega_t^2}{T_{p0}\omega_t^2} \tag{25}$$

where $S_{p0} \approx T_{p0} \approx 2.5$, $\zeta_{\text{s}} = \zeta_t = 0.3, \omega_{\text{s}} = 2\omega_{\text{sw}}$, and $\omega_t = \omega_{\text{sw}}/10$.

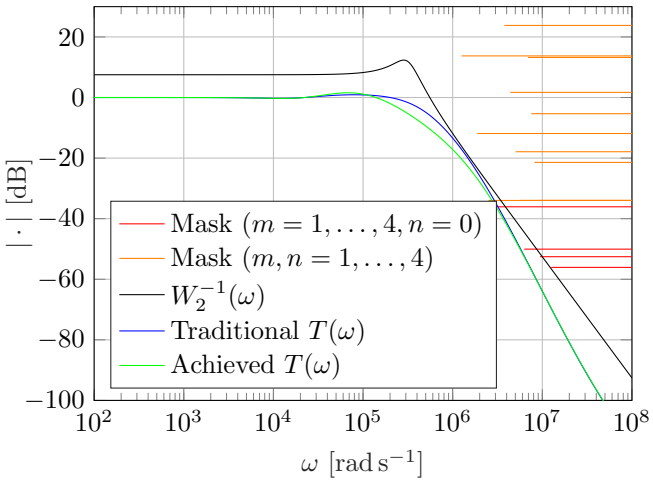


Figure 5: Magnitude Bode plot of W_2^{-1} and complementary sensitivity achieved with traditional and $\mathcal{H}_\infty$ controllers. Straight lines represent constraints (23).

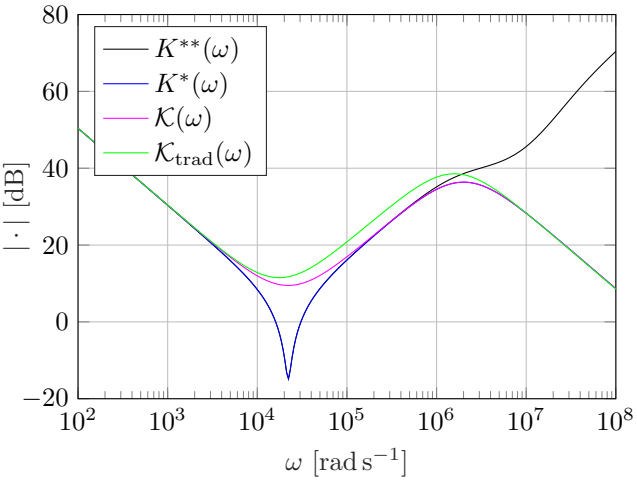


Figure 6: Controller magnitude Bode diagram

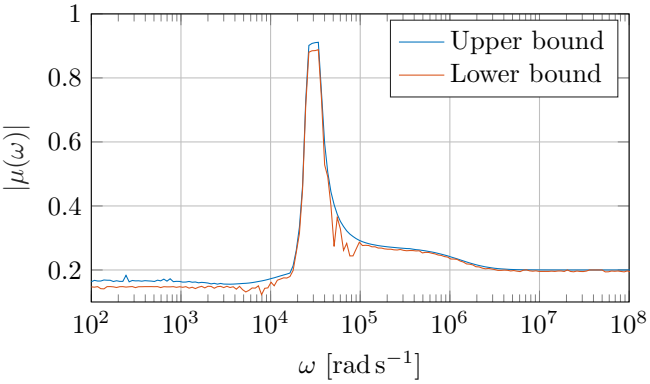


Figure 7: Bounds on μ for the final controller $\mathcal{K}$ in Eq. (27)

Remark 5. *W_1 is the inverse of the sensitivity associated with a prototype second-order transfer function with natural frequency ω_s, which is a high frequency for which $\tilde{i}_{out}(t)$ would be well-rejected.*

Remark 6. *W_2 is built such that its inverse satisfy constraints* (23)*. In other words, ω_t is such that, in Fig. 5, the magnitude bode plot of W_2^{-1} (——) is lower than the masks (——,——).*

The optimization problem (18) is solved using convex semidefinite programming optimization [58]. This way, we get a controller K^{**} with 5 poles $p_0, \ldots, p_4$ and 5 zeros $z_0, \ldots, z_4$. Specifically: the poles are such that $p_0 = 0$, $p_1 \approx -\omega_{\text{sw}}$, $p_2 \approx -0.5\omega_{\text{sw}}$, and $|p_3|, |p_4| > \omega_{\text{sw}}$, while the zeros are such that z_0, z_1 exactly cancel the plant poles at ω_{PS} and $|z_2|, |z_3|, |z_4| > \omega_{\text{sw}}$. The optimal objective value achieved by this controller is $\gamma^* > 1$, which means that the requirements imposed by W_1, W_2 cannot be simultaneously fulfilled. This is mainly due to the choice of a large ω_s. Indeed, R2 asks for a low bandwidth of the closed-loop system, and, at the same time, R3 requires a large bandwidth. This consideration strongly motivates inserting the disturbance rejection scheme discussed in Sec. 4.

The controller K^{**} is simplified by discarding high-frequency dynamics. This way, we obtain the third-order candidate controller

$$K^*(s) = \frac{G(s^2 + 2\zeta_{\text{PS}}\omega_{\text{PS}}s + \omega_{\text{PS}}^2)}{s(s + p_1)(s + p_2)}, \quad G \in \mathbb{R}. \tag{26}$$

We notice that the zeros of (26) are complex and conjugate; thus, their implementation using an analog circuit is critical. To overcome this issue, we replace them with real coincident zeros at ω_{PS}, obtaining the final controller

$$\mathcal{K}(s) = \frac{G(s + \omega_{\text{PS}})^2}{s(s + p_1)(s + p_2)}. \tag{27}$$

This is a valid approximation as long as the damping ζ_{PS} is not too small, which is true under in CCM.

Fig. 6 compares the magnitude Bode plot of the optimal order 5 controller, the simplified controller after the removal of high-frequency dynamics K^*, the final controller $\mathcal{K}$, and the traditional controller $\mathcal{K}_{\text{trad}}$.

Remark 7. *Eq.* (27) *and Fig. 6 show that the structure of the final controller obtained through $\mathcal{H}_\infty$ design coincides with that of the traditional VMC controller in* (15)*. Regarding the parameter values, the only difference is the frequency of the pole $\omega_{p,1}$, which is ω_{sw} for the $\mathcal{H}_\infty$ case and $\min\{\omega_{\text{ESR}}, \omega_{\text{sw}}/2\}$ for the traditional VMC controller.*

Finally, we account for the robust stability requirement R4 by performing a μ-analysis. We consider the controller (27) and the structured description of the uncertainty obtained from the component uncertainties. Fig. 7 shows the computed bounds on μ for the case study in Tab. 1. These results are obtained using MATLAB Robust Control Toolbox [59]. We observe that the most critical frequencies are around ω_{PS}, where the frequency response of the plant is very sensitive to parameter variations. Since $\mu < 1$ for all frequencies, we conclude that (27) achieves robust stability.

4 Disturbance Rejection Techniques

This section illustrates the design of three DR schemes. First, we present designs based on DOB and UIO methods. Next, we introduce an original approach called LEC, which combines the best features of the above two.

All three solutions in this section consist of the cascade of two blocks: an estimator $\mathcal{E}$ and a filter $\mathcal{F}$. The load disturbance is estimated via $\mathcal{E}$, while $\mathcal{F}$ compensates for its effects as if it were directly measured. The combination of $\mathcal{E}$ and $\mathcal{F}$ provides us with an additional feedback control action $v_{\text{inj}}(t)$, which adds to $v_c(t)$ produced by $\mathcal{K}$. Fig. 1 shows a diagram of the overall feedback control system.

4.1 Disturbance observer design

The design of the DOB (see, e.g., [45]) is based on the idea of describing the effect of disturbances and unmodeled dynamics as an unknown exogenous input disturbance $\delta(t)$ acting on the input in an additive way. Formally, we define an equivalent input signal $v_{\text{SW,eq}}(t)$ to account for the effect of the presence of the disturbance on the output, i.e., such that

$$v_o(s) = P_{11}(s)v_{\text{SW,eq}}(s), \quad v_{\text{SW,eq}}(t) \doteq v_{\text{SW}}(t) + \delta(t). \tag{28}$$

The signal $\delta(t)$ has no physical meaning and accounts for all the mismatches between the model output and the measured one, independently of their source.

Relying on measurements of the output $v_o(t)$ and the actual input $v_{\text{SW}}(t)$, the disturbance is computed as

$$\delta(s) = P_{11}^{-1}(s)v_o(s) - v_{\text{SW}}(s). \tag{29}$$

However, since the transfer function $P_{11}(s)$ is strictly proper, high-frequency poles must be included to define a physically realizable approximation of $P_{11}^{-1}(s)$. In the DOB literature, this is addressed by introducing a filter $Q(s)$ having as many poles as the plant relative degree to estimate the disturbance by

$$\hat{\delta}(s) = Q(s)[P_{11}^{-1}(s)v_o(s) - v_{\text{SW}}(s)]. \tag{30}$$

In our case, $P_{11}(s)$ has relative degree one and the most natural choice is $Q(s) = p_H/(s + p_H)$, where p_H is at high-frequency.

Furthermore, the implementation of $QP_{11}^{-1}(s)$ with a simple analog circuit is challenging due to the presence of complex conjugate zeros: this is the same issue arising during the design of the $\mathcal{H}_\infty$ optimal controller in Sec 3.3. Therefore, an analog implementation of the DOB estimator requires approximating the complex conjugate zeros with real ones. Overall, we obtain:

$$\hat{\delta}(s) = \mathcal{E}(s)\begin{bmatrix} v_o(s) \\ v_{\text{SW}}(s) \end{bmatrix} = \begin{bmatrix} G_{\text{DOB}}(s) & -Q(s) \end{bmatrix}\begin{bmatrix} v_o(s) \\ v_{\text{SW}}(s) \end{bmatrix}, \tag{31}$$

where

$$G_{\text{DOB}}(s) \doteq \frac{(1 + s/\omega_{\text{PS}})^2}{(1 + s/\omega_{\text{ESR}})(1 + s/p_H)}. \tag{32}$$

Next, we determine the compensating action $v_{\text{inj}}(t)$ that cancels the effect of $\delta(t)$ on the output, i.e., such that

$$k_{\text{FF}}P_{11}(s)v_{\text{inj}}(s) + P_{11}(s)\delta(s) = 0. \tag{33}$$

Therefore, we define $\mathcal{F}(s)$ as:

$$v_{\text{inj}}(s) = \mathcal{F}(s)\hat{\delta}(s) = -\frac{1}{k_{\text{FF}}}\hat{\delta}(s). \tag{34}$$

The DOB approach allows us to design the compensation mechanism using output voltage measurements only.

We also notice that DOB does not rely on models describing how the disturbance affects the system output. On the one hand, this makes the approach appealing when it is hard, or even infeasible, to obtain a good model for the disturbance. On the other hand, when an accurate model of how the disturbance influences the output is available (as in the considered case), neglecting this information leads to over-compensation. That is to say, not only is the effect of the disturbance compensated, but also other potentially harmless effects, e.g., the effect of component uncertainty. In general, over-compensation is not problematic, but, as it will be shown in Sec. 6.1, simulation examples demonstrate that in the presence of parameter uncertainty, the DOB compensation is associated with larger command input actions that potentially exceed the PWM stage saturation limits. The over-compensation effect is additionally emphasized by the need to approximate P_{11}^{-1} and to introduce Q. In fact, the estimate $\hat{d}$ will be non-zero even in the ideal case, i.e., when disturbances are absent and all components are perfectly known.

To complete our analysis of the DOB, we notice that with the considered DOB, the transfer function between $v_c(t)$ and $v_o(t)$ is not preserved. Accordingly, the theoretical properties ensured by $\mathcal{K}$ on the nominal plant, including robust stability, are lost. The robust stability of the feedback control systems incorporating DOB compensation is studied in [60]. Still, these results do not fully apply in our case due to the need to approximate $P_{11}^{-1}(s)$ to ease its analog implementation.

4.2 Unknown input observer design

The design of the UIO is based on the idea of using an observer to design the estimator $\mathcal{E}$. ESO and GPIO methods are based on the same idea but use different observers.

The main underlying assumption is that the disturbance can be modelled as the output of an exo-system:

$$\dot{\delta}(t) = A_d\delta(t), \qquad \tilde{i}_{\text{out}}(t) = C_d\delta(t) \tag{35}$$

For the case of interest, we take the following assumption

Assumption 3. *The output current disturbance, $\tilde{i}_{out}(t)$, is almost constant, i.e., $\frac{d}{dt}\tilde{i}_{out}(t) = 0$ for almost every time t.*

Accordingly, $\tilde{i}_{\text{out}}(t)$ is the constant output of an exo-system with a pole in origin, i.e., $A_d = 0$ and $C_d = 1$ in Eq. (35).

Consider the state-space representation of the plant

$$\begin{bmatrix} v_o(s) \\ i_L(s) \end{bmatrix} = \left[\begin{array}{c|cc} A_p & B_{p,1} & B_{p,2} \\ \hline C_p & D_{p,1} & 0_{2\times 1} \end{array}\right] \begin{bmatrix} \tilde{i}_{\text{out}}(s) \\ v_{\text{SW}}(s) \end{bmatrix}. \tag{36}$$

Combining (36) with (35), we define an augmented state-space description of the plant where the disturbance is regarded as an additional state:

$$\begin{bmatrix} v_o(s) \\ i_L(s) \end{bmatrix} = \left[\begin{array}{c|c} A_a & B_a \\ \hline C_a & 0_{2\times 1} \end{array}\right] \begin{bmatrix} v_{\text{SW}}(s) \end{bmatrix} \tag{37}$$

where

$$\begin{aligned} &A_a = \begin{bmatrix} A_p & B_{p,1} \\ 0_{1\times 2} & 0 \end{bmatrix} \in \mathbb{R}^{3\times 3}, \quad B_a = \begin{bmatrix} B_{p,2} \\ 0 \end{bmatrix} \in \mathbb{R}^{3\times 1}, \\ &C_a = \begin{bmatrix} C_p & D_{p,1} \end{bmatrix} \in \mathbb{R}^{2\times 3}. \end{aligned} \tag{38}$$

Using (37), we design a Luenbergher observer $\mathcal{E}(s)$ to estimate the states of (37). With this choice, $\mathcal{E}(s)$ is parametrized by a gain matrix $F \in \mathbb{R}^{3\times 2}$ and described by

$$\begin{aligned} \hat{i}_{\text{out}}(s) &= \mathcal{E}(s) \begin{bmatrix} v_{\text{SW}}(s) \\ v_o(s) \\ i_L(s) \end{bmatrix} = \\ &= \left[\begin{array}{c|cc} A_a - FC_a & B_a & F \\ \hline C_o & 0 & 0_{1\times 2} \end{array}\right] \begin{bmatrix} v_{\text{SW}}(s) \\ \begin{bmatrix} v_o(s) \\ i_L(s) \end{bmatrix} \end{bmatrix} \end{aligned} \tag{39}$$

where $C_o = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix}$ is used to select the estimate of the last state of (37) only, i.e., $\hat{i}_{\text{out}}(t)$. By design, F is such that

$$(A_a - FC_a)U = U\Lambda \tag{40}$$

for some invertible matrix $U \in \mathbb{R}^{3\times 3}$ and with $\Lambda = \text{diag}([\lambda_1, \lambda_2, \lambda_3])$. If $\lambda_i < 0$ for all $i = 1, 2, 3$, we have

$$\hat{i}_{\text{out}}(t) \to \tilde{i}_{\text{out}}(t), \quad \text{as } t \to \infty. \tag{41}$$

The convergence rate is determined by the choice of Λ. High frequency eigenvalues lead to a more accurate estimation of $\tilde{i}_{\text{out}}(t)$ and, consequently, better disturbance rejection performances. However, if the frequency is too high, the analog implementation of the filter is more challenging and eventually becomes infeasible.

According to the considerations in [61, Section 2.2], standard algorithms allow us to place at most m coincident eigenvalues, where m is the number of measured outputs. Therefore, in our case, thanks to the inductor current sensing, it is possible to choose $\lambda_2 = \lambda_3$.

Result 2 (Current estimator observability)**.** *The current estimator described by* (39) *has an unobservable mode. Consequently, $\mathcal{E}$ is exactly described by a row vector of* 3 *transfer functions of dynamical order* 2 *that share the same poles.*

Proof. We show that the rank of the observability matrix O associated with the system $\mathcal{E}$ is 2, i.e.,

$$\text{rank}\,(O) = \text{rank}\left(\begin{bmatrix} C_o \\ C_o(A_a - FC_a) \\ C_o(A_a - FC_a)^2 \end{bmatrix}\right) = 2. \tag{42}$$

Consider the eigendecomposition of $A_a - LC_a$:

$$A_a - FC_a = \sum_{i=1}^{3} \lambda_i u_i v_i^\top, \quad V = U^{-1}. \tag{43}$$

Let us now write the rows of the matrix O as:

$$\begin{aligned} C_oI = C_oUV &= \sum_{i=1}^{3} C_o u_i v_i^\top = \\ &= U_{1,3}v_1^\top + (U_{2,3}v_2^\top + U_{3,3}v_3^\top) \\ C_o(A_a - FC_a) &= \sum_{i=1}^{3} \lambda_i C_o u_i v_i^\top = \\ &= \lambda_1 U_{1,3}v_1^\top + \lambda_2(U_{2,3}v_2^\top + U_{3,3}v_3^\top) \\ C_o(A_a - FC_a)^2 &= \sum_{i=1}^{3} \lambda_i^2 C_o u_i v_i^\top = \\ &= \lambda_1^2 U_{1,3}v_1^\top + \lambda_2^2(U_{2,3}v_2^\top + U_{3,3}v_3^\top) \end{aligned} \tag{44}$$

Noting that the equations in (44) are linearly dependent, the result follows. □

According to the Result 2, it is possible to implement the estimator using second-order filters, which are cheaper to implement compared to third-order ones. Still, the UIO estimator requires three inputs, which makes it more expensive than the DOB.

Remark 8. *The estimator developed in this section is strongly related to the reduced-order enhanced state observer in [35]. Indeed, an observer with the same structure is developed and reduced to the second order. Differently from [35], our observer exploits the sensing of $i_L(t)$ to enhance the estimation speed and accuracy. Moreover, we estimate $\tilde{i}_{out}(t)$ rather than a term accounting for all unmodeled disturbances, thus avoiding overcompensation effects.*

Finally, the estimate $\hat{i}_{\text{out}}(t)$ is provided as input to a filter $\mathcal{F}(s)$, which must be designed such that the effects of $\tilde{i}_{\text{out}}(t)$ on the output are canceled. A detailed treatment on the design of $\mathcal{F}(s)$ is postponed to Sec. 4.4. Similarly to DOB, introducing the UIO does not preserve the transfer function between the control input and the output, thus losing the stability guarantee.

4.3 Load Estimator Compensator design

In this section, we present an alternative disturbance estimator, named LEC, intended to mitigate the abovementioned drawbacks of DOB and UIO. Specifically, unlike DOB, the LEC estimates the load current disturbance, thus avoiding overcompensation effects. Moreover, unlike UIO, the LEC allows for a cheap analog implementation (see Sec. 6.2). Finally, the LEC scheme allow us to derive robust stability conditions (see Sec. 5.2), which is a major advantage compared to both DOB and UIO.

The main idea is to estimate $\tilde{i}_{\text{out}}(t)$ through algebraic manipulations relying only on the knowledge of the measured outputs $v_o(t)$ and $i_L(t)$. In the following

equations, we omit, for brevity, the Laplace argument s. First, we obtain $v_{\rm SW}(s)$ as a function of $v_o(s)$ and $\tilde{i}_{\rm out}(s)$ as

$$v_{\rm SW} = \frac{1}{P_{11}} v_o - \frac{P_{12}}{P_{11}} \tilde{i}_{\rm out}. \tag{45}$$

Then, we replace into the Eq. (11) for $i_L(s)$:

$$\begin{aligned} i_L &= P_{21} v_{\rm SW} + P_{22} \tilde{i}_{\rm out} = \\ &= \frac{P_{21}}{P_{11}} v_o - \frac{P_{21} P_{12}}{P_{11}} \tilde{i}_{\rm out} + P_{22} \tilde{i}_{\rm out} = \\ &= \frac{P_{21}}{P_{11}} v_o + \frac{P_{22} P_{11} - P_{21} P_{12}}{P_{11}} \tilde{i}_{\rm out}. \end{aligned} \tag{46}$$

Let us denote $\Delta_P \doteq P_{22} P_{11} - P_{21} P_{12}$. From (46), we get

$$\tilde{i}_{\rm out} = \frac{P_{11}}{\Delta_P} \left(-\frac{P_{21}}{P_{11}} v_o + i_L \right). \tag{47}$$

Ideally, if the plant is exactly known, the right-hand side of Eq. (47) can be used to define the filter $\mathcal{E}$, and $\hat{i}_{\rm out} = \tilde{i}_{\rm out}$ by construction.

Remark 9. *Thanks to the algebraic design procedure, no assumptions on the nature of the current disturbance $\tilde{i}_{out}(t)$ are needed. This is particularly meaningful in comparison with observer-based solutions. Indeed, designs based on UIO and ESO are based on Assumption 3, while GPIO design requires a suitable assumption on the $\tilde{i}_{out}$ derivatives; see, e.g., [31].*

Remark 10. *Since the LEC design is based on algebraic cancellations, uncertainty on the plant parameters is critical, especially regarding the robust stability of the system. This point is extensively discussed in Sec. 5.2.*

In the remainder of this section, we prove that the resulting estimator is described by a first-order proper transfer function. Thus, it can be physically implemented through a cheap analog circuit. Let us compute each term of (47) as a function of the Buck components.

Result 3 (Characterization of Δ_P)**.** *For a Buck converter,*

$$\Delta_P = P_{11} \tag{48}$$

independently of the components' values.

Proof. We replace (12a)-(12c) into the definition of Δ_P. Let us now evaluate the products $P_{11}P_{22}$ and $P_{12}P_{21}$ as a preliminary calculation. For ease of notation, we denote $D = \alpha_0 s^2 + \alpha_1 s + \alpha_2$. Since

$$P_{12} = -R_L \frac{(1 + CR_c s)(sL + R_i')}{\alpha_0 s^2 + \alpha_1 s + \alpha_2}, \tag{49}$$

we have:

$$P_{11} P_{22} = P_{11}^2 = \frac{R_L^2}{D^2} (1 + CR_c s)^2 \tag{50}$$

and

$$\begin{aligned} -P_{12} P_{21} = \frac{R_L}{D^2} (1 + CR_c s)(sL + R_i') \\ ((CR_L + CRc)s + 1). \end{aligned} \tag{51}$$

Taking the sum of the above terms leads to

$$\begin{aligned} \Delta_P &= \frac{R_L}{D^2} (1 + CR_c s)(R_L + CR_L R_c s + \\ &\quad + (sL + R_i')(C(R_L + Rc)s + 1)) = \\ &= \frac{R_L}{D^2} (1 + CR_c s) D = P_{11} \end{aligned} \tag{52}$$

□

Result 4 (Characterization of P_{21}/P_{11})**.** *For a Buck converter,*

$$G_1 \doteq \frac{P_{21}}{P_{11}} = \frac{C(R_L + R_C)s + 1}{R_L(1 + CR_c s)}. \tag{53}$$

Proof. The result directly follows from Eqs. (12a) and (12c). □

Finally, replacing Eqs. (48) and (53) in the right-hand side of (47), we define the output current estimator $\mathcal{E}$ as

$$\hat{i}_{\rm out} = \mathcal{E} \begin{bmatrix} v_o \\ i_L \end{bmatrix} = \begin{bmatrix} -G_1 & 1 \end{bmatrix} \begin{bmatrix} v_o \\ i_L \end{bmatrix}. \tag{54}$$

Remark 11. *$\mathcal{E}$ is a proper transfer function and can be physically implemented using an analog circuit. See Sec. 6.2.*

4.4 Design of compensation filter for UIO and LEC

This section discusses how to design the compensation filter $\mathcal{F}$ assuming that the estimator stage $\mathcal{E}$ provides a correct estimate $\hat{i}_{\rm out}$ of the output current disturbance $\tilde{i}_{\rm out}(t)$. Ideally, the filter $\mathcal{F}$ should inject an additional control input $v_{\rm inj}(t)$ such that the effect of $\tilde{i}_{\rm out}(t)$ on $v_o(t)$ is null, i.e.,

$$k_{\rm FF} P_{11} v_{\rm inj} + P_{12} \tilde{i}_{\rm out} = 0. \tag{55}$$

From Eq. (55), a natural candidate for defining $\mathcal{F}$ would be $-P_{12} k_{\rm FF}^{-1} P_{11}^{-1}$.

Result 5 (Characterization of P_{12}/P_{11})**.** *For a Buck converter,*

$$G_2 \doteq \frac{P_{12}}{P_{11}} = -sL - R_i - R_{\rm ON}^{\rm HS,LS}. \tag{56}$$

Proof. The result follows by replacing P_{12} with (49) and P_{21} with (12c), and performing suitable simplifications. □

Result 5 allows us to conclude that $\mathcal{F}$ cannot be defined according to $-k_{\rm FF}^{-1} G_2$ because it is not a proper transfer function. To address this issue, we define $\mathcal{F}$ as

$$\mathcal{F} \doteq -\frac{G_2}{k_{\rm FF}} \frac{1}{1 + s/p_H} = \frac{sL + R_i + R_{\rm ON}^{\rm HS,LS}}{k_{\rm FF}(1 + s/p_H)}. \tag{57}$$

where $p_H > 0$ is a high-frequency pole. The rationale of this choice is that as $p_H \to \infty$, the original desired frequency behavior is recovered.

Remark 12. *As we will see in Sec. 5.2, the frequency of the pole p_H must be tuned to ensure a suitable trade-off between output current DR performance and robustness.*

5 LEC stability analysis

In this section, we analyze the stability and performance of the Buck converter featuring the LEC DR scheme defined by Eq. (54) and (57). We show that introducing LEC does not affect the command-to-output plant transfer function, thus preserving nominal stability. Next, we derive a sufficient condition for robust stability.

5.1 Nominal stability and performance

Consider the inner closed-loop system defined by the plant and the LEC:

$$\begin{bmatrix} v_o \\ i_L \end{bmatrix} = P \begin{bmatrix} v_{\text{SW}} \\ \tilde{i}_{\text{out}} \end{bmatrix}, \qquad v_{\text{SW}} = k_{\text{FF}}(v_c + v_{\text{inj}}) \tag{58a}$$

$$v_{\text{inj}} = \frac{-G_2}{k_{\text{FF}}(1 + s/p_H)}(-G_1 v_o + i_L). \tag{58b}$$

The following result holds.

Theorem 1 (Input-output behavior of the inner loop)**.** *The system* (58) *is nominally stable, and its input-output behavior is described by*

$$v_o = P_{11} k_{\text{FF}} v_c + P_{12} \frac{s}{s + p_H} \tilde{i}_{out}. \tag{59}$$

Proof. From (58), we get

$$v_o = P_{11} k_{\text{FF}} v_c + P_{11} \frac{G_2}{1 + s/p_H} (G_1 v_o - i_L) + P_{12} \tilde{i}_{\text{out}} \tag{60}$$

$$i_L = P_{21} k_{\text{FF}} v_c + P_{21} \frac{G_2}{1 + s/p_H} (G_1 v_o - i_L) + P_{22} \tilde{i}_{\text{out}} \tag{61}$$

Next, we get i_L from (61) as

$$\begin{aligned} i_L = &\frac{P_{21}^2 P_{12}}{P_{11}\left(P_{11}(1 + s/p_H) + P_{21}P_{12}\right)} v_o + \\ &+ \frac{P_{11}(1 + s/p_H)}{P_{11}(1 + s/p_H) + P_{21}P_{12}} \left(P_{21} k_{\text{FF}} v_c + P_{22} \tilde{i}_{\text{out}}\right). \end{aligned} \tag{62}$$

Replacing (62) into (60) and performing suitable simplications yields (59). The feedback loop is internally stable because (59) is BIBO stable, and no unstable cancellations occur when forming the loop function. □

Eq. (59) allows us to draw additional considerations on the LEC properties. First, we notice that the transfer function between $v_c(t)$ and $v_o(t)$ is preserved. Thus, any controller designed to achieve specific input-output performances on the original plant still performs the same when adopting the LEC. Importantly, this includes the nominal stability of the system, which is preserved. Secondly, the transfer function between $\tilde{i}_{\text{out}}(t)$ and $v_o(t)$ gets multiplied by $s/(s + p_H)$, which is a high-pass filter with gain 0 at low frequency and 1 at high frequency. Thus, independently of $\mathcal{K}$, the current disturbance will be rejected at steady state. Moreover, by letting $p_H \to \infty$, the effect of the output current is exactly canceled.

To summarize, the LEC is an additional stage that reduces the Buck output impedance (especially at low frequencies) while preserving the control-to-output behavior.

5.2 Robust stability

As presented in Sec. 3.3, we design the controller $\mathcal{K}$ to account for robust stability by verifying this property through μ-analysis. In the remainder of this section, we study under what conditions the introduction of the LEC (54), (57) preserves the robust stability property.

In the following, we denote by $\hat{\cdot}$ the quantities calculated using nominal component values, while the absence of the $\hat{\cdot}$ symbol indicates the value of the actual components. According to the this notation, the LEC is

$$v_{\text{inj}} = \frac{-\hat{G}_2}{\hat{k}_{\text{FF}}(1 + s/p_H)}(-\hat{G}_1 v_o + i_L). \tag{63}$$

To study the error due to the mismatch between G_1 and $\hat{G}_1$, we introduce the following additive uncertainty description

$$G_1(s) = \hat{G}_1(s) + \Lambda(s)\Delta_1(s), \tag{64}$$

where $\Lambda(s)$ is a suitable frequency weighting function and $\Delta_1(s)$ is such that $\|\Delta_1\|_{\mathcal{H}_\infty} < 1$.

Remark 13. *Computing a tight description of $|\Lambda(i\omega)|$ given bounds on each component value is possible. Specifically, for each fixed ω, $|\Lambda(i\omega)|$ is a polynomial function of the Buck's components. Therefore, computing the Bode envelope of Λ can be recast to polynomial optimization problems, which may be solved for a tight upper bound using semidefinite relaxation; see [57] for a detailed discussion.*

Using Eqs. (58a) and (63), we obtain:

$$v_o = P_{11} k_{\text{FF}} v_c + P_{11} \frac{\hat{G}_2}{1 + s/p_H} \frac{k_{\text{FF}}}{\hat{k}_{\text{FF}}} \left(\hat{G}_1 v_o - i_L\right) + P_{12} \tilde{i}_{\text{out}}. \tag{65}$$

Moreover, from (47)-(48), we have $i_L = G_1 v_o + \tilde{i}_{\text{out}}$. Using this to replace i_L into (65), we get

$$\begin{aligned} v_o = &P_{11} k_{\text{FF}} v_c + \\ &+ P_{11} \frac{\hat{G}_2}{1 + s/p_H} \frac{k_{\text{FF}}}{\hat{k}_{\text{FF}}} \left(\hat{G}_1 v_o - G_1 v_o - \tilde{i}_{\text{out}}\right) + P_{12} \tilde{i}_{\text{out}}. \end{aligned} \tag{66}$$

To study stability, we focus our attention on the input-output relationship $v_c(t)$ to $v_o(t)$. For this reason, we neglect the presence of the disturbance $\tilde{i}_{\text{out}}(t)$. From (66) and (64), we have

$$v_o = P_{11} k_{\text{FF}} v_c + P_{11} \frac{\hat{G}_2}{1 + s/p_H} \frac{k_{\text{FF}}}{\hat{k}_{\text{FF}}} \Lambda \Delta_1 v_o \tag{67}$$

which yields:

$$v_o = \frac{P_{11} k_{\text{FF}}}{1 - P_{11} k_{\text{FF}} W_r \Delta_1} v_c, \quad W_r \doteq \frac{\hat{G}_2}{\hat{k}_{\text{FF}}(1 + s/p_H)} \Lambda. \tag{68}$$

We highlight that W_r depends only on nominal parameter values and Λ, which can be computed as discussed in Remark 13. Therefore, $|W_r(i\omega)|$ is easily computed using available information. Conversely, P_{11} and k_{FF} in (68) are uncertain. Eq. (68) is the description of a plant with nominal value $P_{11} k_{\text{FF}}$ and affected by inverse

multiplicative uncertainty W_r. See, e.g., [40, Section 8.2] for details on this uncertainty description. This observation leads us to the following result.

Theorem 2. *Let $\mathcal{K}$ be a controller robustly stabilizing the uncertain plant $P_{11}k_{\mathrm{FF}}$. Let $S = (1+P_{11}k_{\mathrm{FF}}\mathcal{K}G_f)^{-1}$ denote the sensitivity function of the corresponding feedback control system. Robust stability is preserved after the introduction of the LEC defined according to Eq.* (54) *and* (57) *if*

$$\|SP_{11}k_{\mathrm{FF}}W_r\|_{\mathcal{H}_\infty} < 1. \tag{69}$$

Proof. The result follows from the application of the small-gain theorem on the $M-\Delta$ structure defined by the inverse additive uncertainty description (68). See [40, Section 8.6]. □

Remark 14. *The condition provided by Theorem 2 is only sufficient for robust stability and may be conservative. We could use μ-analisys [41] to get a tight result on robust stability considering the entire control architecture. Nonetheless, Theorem 2 is useful during the design phase to get additional information on the choice of p_H because it is involved in the definition of W_r in Eq.* (68).

Condition (69) involves the presence of P_{11}, k_{FF}, and S, which depend on the *actual* parameters, not the nominal ones. Consequently, we cannot check this condition directly. To proceed with our analysis, we introduce the function $N(\omega)$ with the property $N(\omega) \leq k_{\mathrm{FF}}^{-1}|P_{11}(i\omega)S(i\omega)|^{-1}$ for all $\omega \geq 0$. Similarly to what we discussed in Remark 13, the procedure presented in [57] applies to the problem of computing the function $N(\omega)$ given bounds on the component values. Using $N(\omega)$, a sufficient condition for (69) is

$$|W_r(i\omega)| < N(\omega), \quad \forall\omega. \tag{70}$$

Replacing W_r, we obtain an explicit condition on the choice of the frequency p_H as

$$\left|\frac{1}{1+\frac{i\omega}{p_H}}\right| < N(\omega)\left|\frac{\hat{k}_{\mathrm{FF}}}{\hat{G}_2(i\omega)}\right|\left|\frac{1}{\Lambda(i\omega)}\right|. \tag{71}$$

The left-hand side of (71) represents the magnitude frequency response of a first-order low-pass filter, which has a pole located at p_H and unitary DC-gain. In contrast, the right-hand side is influenced by the components' uncertainties. When p_H is at low frequencies, the left-hand side decreases, making it easier to satisfy (71). Conversely, if p_H approaches infinity, robust stability is guaranteed if the right-hand side does not exceed one at all frequencies.

To summarize, the pole at p_H renders the system physically realizable and enhances the system's robust stability at the cost of a performance decrease. Eq. (71) offers a quantitative way of tuning p_H to trade off nominal performances and stability robustness. We conclude this section with another useful observation on the nature of the uncertainty. Since G_1 only depends on components R_L, R_C, C, a huge uncertainty on their value potentially reduces the stability robustness, while uncertainty on $L, R_i, R_{\mathrm{ON}}^{\mathrm{HS,LS}}$ (which defines G_2) affects the stability robustness only *indirectly* through the factor $N(\omega)$. In other words, if R_L, R_C, C are precisely known, then $|\Lambda|(i\omega) \approx 0$ and condition (71) is fulfilled for any value of $L, R_i, R_{\mathrm{ON}}^{\mathrm{HS,LS}}$. This indicates that, during Buck design, the robust stability benefits from choosing a more expensive capacitor, while the precision of the inductor is almost irrelevant.

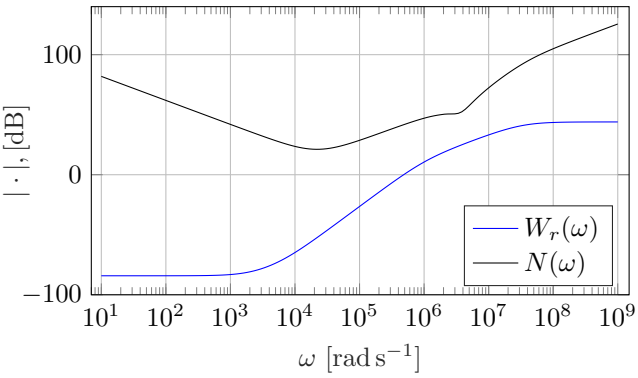


Figure 8: Magnitude Bode diagram of W_1 and N to check the robust stability condition (70)

6 Experimental results

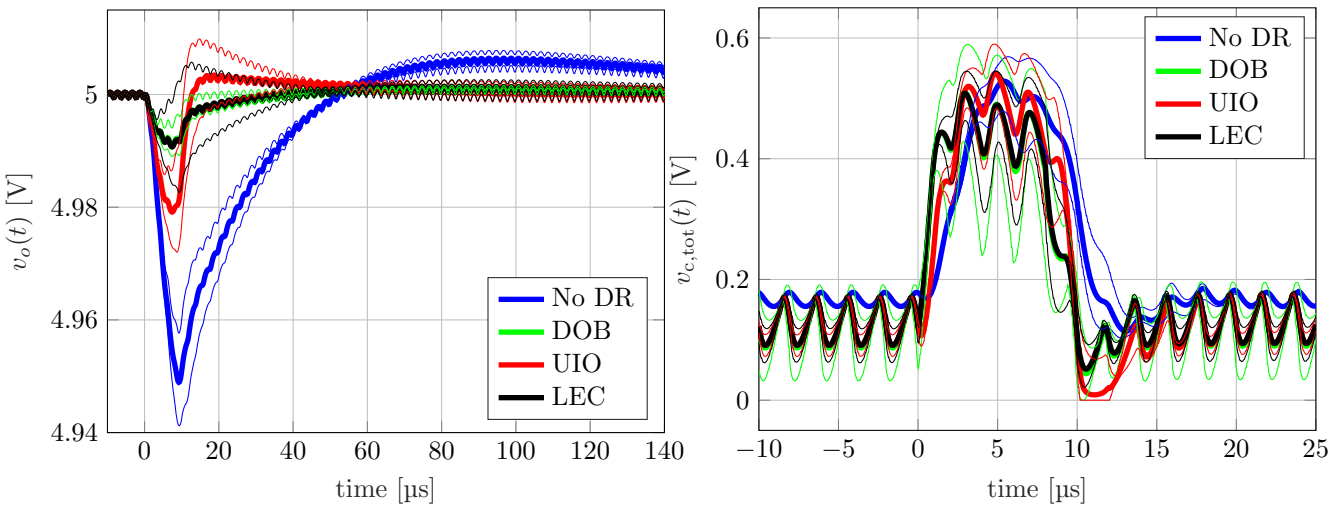
In this section, we compare the performance of LEC, DOB, and UIO through numerical simulations. Then, we discuss the analog circuit implementation of LEC and perform experimental measurements to validate the effectiveness of the proposed LEC-based approach on a real Buck converter. In the following, we will refer to the Buck converter parameter values in Table 1.

6.1 Simulation results

The LEC is designed as described in Sec. 4.3 and 4.4. The only free parameter to be selected, p_H, is set to $p_H = 10^6\,\mathrm{rad\,s^{-1}}$ to trade-off DR performance and robustness. In Fig. 8, we show the Bode diagram of $W_1(s)$ and $N(s)$, from which we conclude that condition (71) is fulfilled and, thus, robust stability is guaranteed. For a fair comparison, we set $p_H = 10^6\,\mathrm{rad\,s^{-1}}$ in (32) for the DOB design and $\lambda_1 = \lambda_2 = 10^6\,\mathrm{rad\,s^{-1}}$ and $\lambda_3 = 0.95\lambda_1$ in (40) for the UIO design.

We perform 50 simulations, selecting different values for each component. We set $V_{\mathrm{in}} = 20\,\mathrm{V}$ and the $R_L = 5\,\Omega$ to achieve a static 1 A load current value. All other component values are sampled randomly from the uniform distribution in the respective uncertainty interval. In each simulation, we apply a current disturbance step with an amplitude of 8 A and a slope of $1 \times 10^6\,\mathrm{A\,s^{-1}}$.

Fig. 9(a) and 9(b) show the responses of the output voltage $v_o(t)$ and the command input signal $v_{\mathrm{c,tot}}(t)$, respectively. Specifically, we compare the performance without the DR stage against the ones achieved using LEC, DOB, and UIO. Solid lines represent the average of all the simulation outcomes, while thin lines represent upper and lower bounds over all the realizations.



(a) Output voltages $v_o(t)$

(b) Command input voltages $v_{c,tot}(t)$

Figure 9: Comparison between uncompensated (blue), LEC (black), DOB (green), and UIO (red). The thick line is the average response among 50 runs, while the thin ones are bounds over all runs.

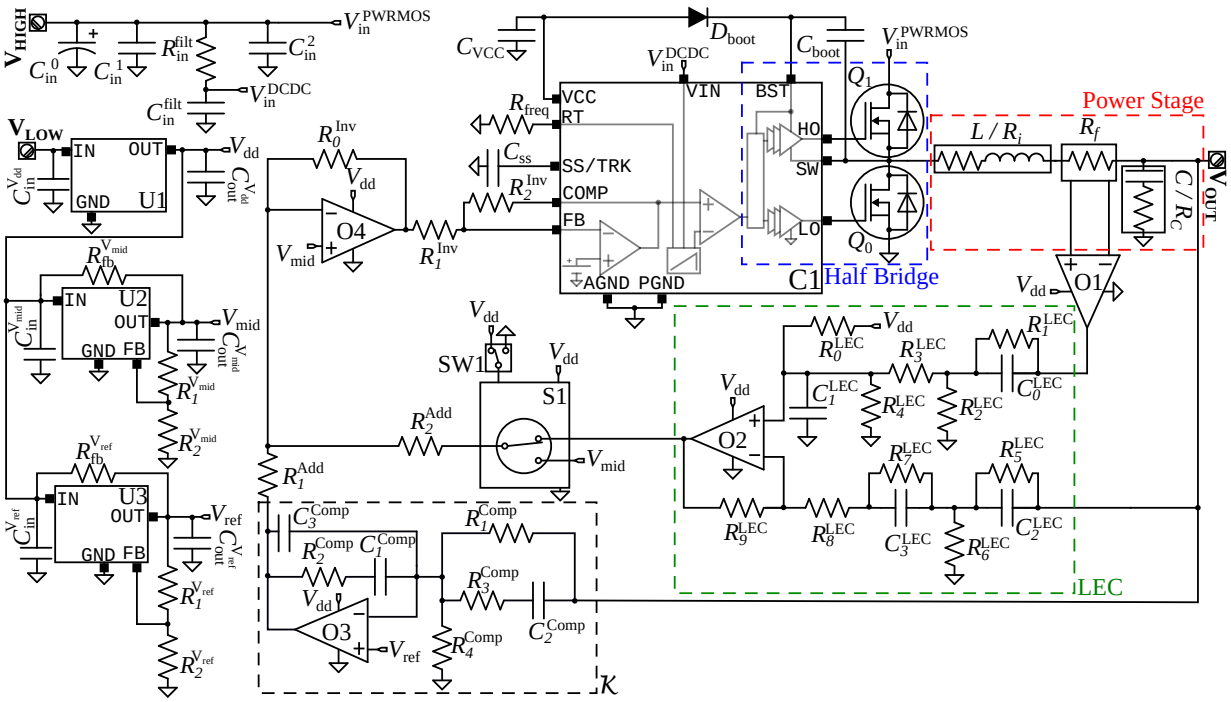


Figure 10: VMC Buck converter embedding the proposed LEC. The LEC is implemented as an analog circuit network.

Table 2: Values and part number of the circuit elements in Fig. 10.

Schematic Label	Part Number / Component Value	Schematic Label	Part Number / Component Value	Schematic Label	Part Number / Component Value
C_{in}^{0}	100 µF	C_{in}^{1}	2 x 10 µF	C_{in}^{2}	10 x 10 µF
$R_{\text{in}}^{\text{filt}}$	2.2 Ω	$C_{\text{in}}^{\text{filt}}$	0.1 µF		
$C_{\text{in}}^{V_{\text{dd}}}$	1 µF	$C_{\text{out}}^{V_{\text{dd}}}$	4.7 µF	$C_{\text{in}}^{V_{\text{mid}}}$	1 µF
$C_{\text{out}}^{V_{\text{mid}}}$	4.7 µF	$C_{\text{in}}^{V_{\text{ref}}}$	1 µF	$C_{\text{out}}^{V_{\text{ref}}}$	4.7 µF
$R_{\text{fb}}^{V_{\text{ref}}}$	200 µΩ	$R_{2}^{V_{\text{ref}}}$	10 kΩ	$R_{1}^{V_{\text{ref}}}$	3.4 kΩ
$R_{\text{fb}}^{V_{\text{mid}}}$	200 Ω	$R_{2}^{V_{\text{mid}}}$	12 kF	$R_{1}^{V_{\text{mid}}}$	38 kF
U1	LDL1117S50R	U2	CAT102TDI-GT3	U3	CAT102TDI-GT3
L/R_i	XAL1510-822MED / 8.2 µH	R_f	WSHM2818R0150FEA / 15 mΩ	C/R_{C_o}	GRM32EC72A106KE05 / 26 x 10 µF
Q_1	STL90N10F7	Q_0	STL110N10F7		
C1	L3751PUR	R_{freq}	20 kΩ	C_{ss}	47 nF
C_{VCC}	1 µF	D_{boot}	BAT46ZFILM	C_{boot}	100 nF
R_1^{Inv}	10 kΩ	R_2^{Inv}	10 kΩ		
O1	AD8410AWBRZ-RL	O2	ADA4891	R_0^{LEC}	68 kΩ
R_1^{LEC}	1 MΩ	R_2^{LEC}	4.12 kΩ	R_3^{LEC}	68 kΩ
R_4^{LEC}	680 kΩ	R_5^{LEC}	1 MΩ	R_6^{LEC}	35 kΩ
R_7^{LEC}	10 MΩ	R_8^{LEC}	316 Ω	R_9^{LEC}	350 kΩ
C_0^{LEC}	470 pF	C_1^{LEC}	1 nF	C_2^{LEC}	470 pF
C_3^{LEC}	100 pF				
O3	ADA4891	R_1^{Comp}	1 MΩ	R_2^{Comp}	4.12 kΩ
R_3^{Comp}	68 kΩ	R_4^{Comp}	680 kΩ	C_1^{Comp}	5.6 nF
C_2^{Comp}	1.8 nF	C_3^{Comp}	150 pF		
O4	ADA4891	S1	ADG819BRZ	SW1	204-121
R_0^{Add}	10 kΩ	R_1^{Add}	10 kΩ	R_2^{Add}	10 kΩ

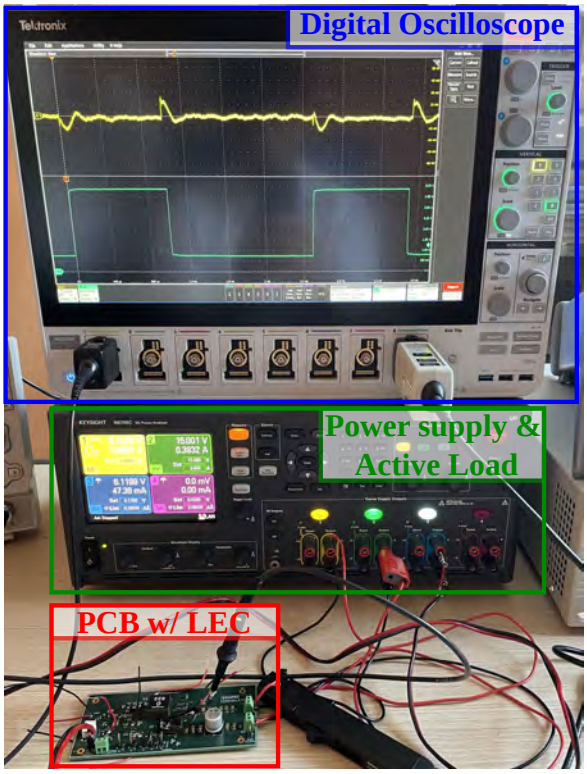


Figure 11: Experimental measurement setup.

All the examined techniques improve the DR performances compared to uncompensated VMC. Among the three analyzed schemes, UIO shows the worst performance concerning the response to the disturbance and the command activity, which saturates for several switching periods in several simulations. On average, DOB and LEC enjoy the same load DR performance regarding overshoot and settling time. Compared to LEC, the DOB scheme enjoys a lower variance in the output response. However, it also features a larger variance of the command input $v_{\text{c,tot}}(t)$, due to the overcompensation effect. Indeed, in some simulations, the DOB command activity saturates, while the LEC one does not.

6.2 Circuital implementation

To validate the effectiveness of the proposed LEC, we implemented a custom analog circuit through a Printed Circuit Board (PCB). The system implements a VMC Buck converter with LEC DR, as schematized in Fig. 1 from a high-level perspective. The circuit-level implementation of the complete system is shown in Fig. 10. The detailed list of the part numbers and the values of the components employed in the schematic is available in Table 2. In the design phase, we referred to the main Buck converter parameters listed in Table 1.

The HB is realized via the power MOSFETs $Q_{0,1}$, while the PS includes both the converter output filter, consisting of the L/R_i and C/R_C elements, and the inductor current sensing resistance R_f. The inductor current signal is conditioned via both R_f and the current-sense amplifier O1. The input voltage of the converter is supplied through the external pin V_{HIGH}, which is connected to a network of decoupling capacitors constituted by $C_{\text{in}}^{0,1,2}$. The converter output is available on the external pin V_{OUT}. The MOSFETs $Q_{0,1}$ are driven by the synchronous Buck controller C1, which is supplied

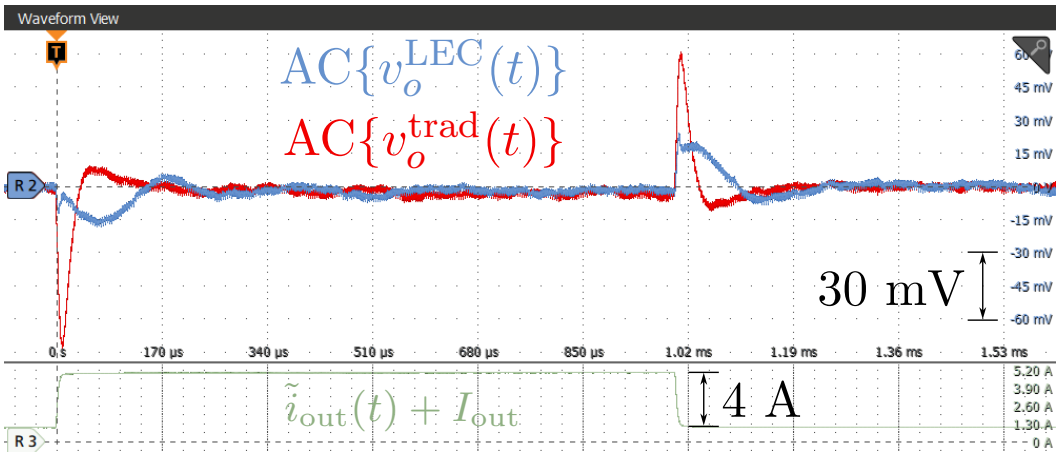


Figure 12: Oscilloscope measurements from prototype PCB.

from the external input voltage on $\mathrm{V_{HIGH}}$ additionally filtered by $R_{\mathrm{in}}^{\mathrm{filt}} - C_{\mathrm{in}}^{\mathrm{filt}}$.

The controller embeds the gate drivers, the sawtooth-based PWM stage, and additional circuit blocks implementing the VMC. The switching frequency is set via the resistor R_{freq}, while the soft-start time is programmable via the capacitor C_{ss}. An internal linear regulator generates a reference voltage on the `VCC` pin, which serves to implement the Dickson charge pump D_{boot}-C_{boot}. The outer loop controller $\mathcal{K}$ is implemented through a type-III compensation network highlighted in black in Fig. 10. The LEC circuit implementation design is conducted by considering the cascaded connection of the $\mathcal{E}$ and $\mathcal{F}$ blocks. It consists of one OpAMP and passive components and is highlighted in green in Fig. 10.

To either enable or disable the operation of the LEC, the circuit is equipped with a solid-state switch S1, which is in turn driven from a mechanical switch SW1. When the LEC is disabled, the feedback control action is uniquely provided by $\mathcal{K}$, implementing the traditional VMC technique. Otherwise, the LEC output is added to the $\mathcal{K}$ output, thus realizing the proposed load DR mechanism. The output signals of the LEC and $\mathcal{K}$ are added via the analog stage that comprises R_1^{Add}, R_2^{Add}, R_0^{Inv} and O4. Resistors R_1^{Inv} and R_2^{Inv} are required to configure the error amplifier inside C1 as an inverting stage with unitary gain. This inverting stage is required because the internal error amplifier is physically connected to the PWM stage. The stages U1, U2 and U3 together with their feedback resistors (i.e., $R_{1,2}^{V_{\mathrm{mid,ref}}}$ and $R_{\mathrm{fb}}^{V_{\mathrm{mid,ref}}}$) and decoupling capacitors (i.e., $C_{\mathrm{in,out}}^{V_{\mathrm{dd}}}$) are voltage regulators and references. These are required to generate the voltage levels that are employed to both supply the active analog stages in the system (i.e., the OpAmps and the current-sense amplifier) and set the voltage reference values (e.g., the reference on the + terminal of O3 for $\mathcal{K}$). These stages are supplied via the external voltage applied on the pin $\mathrm{V_{LOW}}$, which is in the range $[6, 7]$V.

6.3 Experimental measurements

Experimental measurements on the PCB prototype described in Sec. 6.2 have been conducted on the circuit shown in Fig. 10. These validate the effectiveness of the LEC in mitigating external load disturbances.

The experimental setup is shown in Fig. 11. The Buck converter is supplied via the DC power module Keysight N6752A, which is installed in the Keysight N6705C DC power analyzer. We apply a fixed resistive load R_L which fixes the static converter output current value to 1 A. We examined the load transient response of the converter when a sequence of step-load changes with amplitude 4 A is applied. The step-load is provided via the Keysight N6791A DC electronic load module installed in the Keysight N6705C. We use the Tektronix MSO58B oscilloscope to measure the load current and output voltage, both considering operation with disabled and enabled LEC. The comparative results are shown in Fig. 12, showing the AC-coupled $v_o(t)$ and the applied disturbance $\tilde{i}_{\mathrm{out}}(t)$. When the proposed LEC compensation is active, the output voltage undershoot/overshoot is significantly reduced. Specifically, the undershoot is $\hat{s}_{\mathrm{trad}} = e_{\max}^{\mathrm{trad}}/V_o^{\mathrm{target}} = {}^{70\,\mathrm{mV}}/_{5\,\mathrm{V}} = 1.4\%$ and $\hat{s}_{\mathrm{LEC}} = e_{\max}^{\mathrm{LEC}}/V_o^{\mathrm{target}} = {}^{18\,\mathrm{mV}}/_{5\,\mathrm{V}} = 0.36\%$ when LEC is respectively disabled and enabled.

7 Conclusion

This study presents three novel disturbance rejection mechanisms for load current disturbances in DC-DC Buck converters. Two of the proposed techniques build on well-established methods: the Disturbance Observer (DOB) and the Unknown Input Observer (UIO). The third one, named Load Estimator-Compensator (LEC), is an original approach tailored for Buck converters. These methods enhance disturbance rejection by augmenting the controller action and are designed for seamless integration into conventional control loops.

We conduct a rigorous stability analysis that ensures robust stability of the overall system when integrating the LEC. Simulations validate the effectiveness of the proposed approaches, showing that DOB and LEC achieve similar average performances. While DOB is less sensitive to parameter uncertainty, it requires more aggressive control, potentially leading to saturation effects. This motivates further investigations on this approach.

Experimental validation on a custom PCB implementing a voltage-mode Buck converter with LEC mechanism confirms the effectiveness of the proposed solution and corroborates its practical viability for high-performance applications.

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