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Additive Manufacturing for Power Electronics: New Challenges in Design, Manufacturing and Applications

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Abstract

Additive Manufacturing for Electronics (AME) techniques are currently becoming more widespread as they allow for the rapid production of electronic devices with confined costs. In this context, AME represents a relatively novel fabrication technique when used for power electronics applications. The research presented in this paper is focused on the investigation of the feasibility of inkjet-based AME for the fabrication of structures and components for power electronics applications. Seven circuit models for a power module were developed and printed with a multimaterial 3D printer. The models were then analyzed to optimize their design in terms of dimensional accuracy. Furthermore, the electrical conductivity and the magnetic field of one of the devices were examined with numerical simulation tools to verify its effectiveness and efficiency when compared to factory-built power modules. The resulting devices could be considered for coupling and improving the functionality of a module built using non-AME technology, showing that custom-built electronic devices of this kind can be a valid upgrade to the current state of the art. Thus, AME-fabricated devices might be considered as potential enablers for next-generation wide-bandgap (WBG) devices.

Keywords: additive manufacturing; power electronics; FEM simulations; technology investigation; passive components

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1. Introduction

1.1. Power Electronics Needs

A power module is a power electronics unit that integrates one or more power semiconductor devices together with the electrical, thermal, and mechanical interconnections required for their operation within a single housing [1]. It typically deals with large currents and high voltages while dissipating heat within a constrained footprint—a combination that places strict demands on both the electrical and thermal performance of the package [2,3]. On a power module board, different devices can be installed, such as diodes, IGBTs, MOSFETs, sensors, and drivers [1]. Their typical applications are related to current switching or power conversion (both voltage and frequency). Driven by market needs and the widespread presence of wide-bandgap (WBG) materials, the power density and switching frequency have continued to rise. Therefore, power module packaging has become

one of the main factors limiting converters' performance, since its parasitic elements and thermal path directly constrain how the devices inside packages can be operated [2].

As switching frequencies increase, the effects of parasitic inductances become more difficult to tolerate, which can be problematic for WBG devices, such as gallium nitride (GaN) high-electron-mobility transistors (HEMTs). Their fast switching frequency makes them particularly sensitive to parasitic inductance, which can lead to voltage overshoot, ringing, and higher switching losses compared to silicon devices. Printed circuit board (PCB) fabrication processes, which produce a planar structure, limit how fine the traces are and how many layers can be used. Moreover, wire bonding adds loop inductance and is a known weak point under thermal fatigue, while solder reflows limit how densely interconnects can be packed and how long the joints last. Package and PCB layouts therefore have to be designed carefully to keep the parasitic inductance to a minimum [3–5].

To adhere to the trend toward highly integrated and miniaturized devices, high-frequency electronic components need to feature a compact size and reduced footprint while enabling considerable cost savings in high-volume production. Achieving this level of miniaturization, however, requires manufacturing processes capable of producing truly three-dimensional structures—a capability that conventional planar fabrication techniques struggle to provide [6].

Packaging at higher voltages brings a related but separate problem. Distorted electric fields near internal material interfaces can weaken insulation and, in the worst case, cause breakdown [2].

Thermal management is another major challenge in power module design. One of the key parameters governing this aspect is the thermal resistance of the package, which describes how effectively heat generated at the semiconductor junction is transferred through the package toward the heat sink or the ambient. Since heat must flow through several material layers and interfaces, each contributing to its own thermal resistance, the overall thermal resistance increases with the number of layers [2,3]. Consequently, a trade-off arises with the breakdown voltage discussed above: increasing the insulator material thickness improves the dielectric strength but also increases the thermal resistance, thereby worsening the thermal performance of the module [5]. In addition, these modules are built as a stack of dies, solder layers, copper metallization, ceramic substrates, and baseplates, each with its own coefficient of thermal expansion. Every thermal cycle forces these mismatched materials to expand and contract against each other, and the stress built at their interfaces eventually manifests as warpage, solder fatigue, delamination, or a measurable increase in thermal resistance [3,7]. Indeed, an industrial survey found that a large share of converter failures could be traced back to the power semiconductor device itself, with temperature-related stress as the single largest contributor [7].

GaN HEMTs can worsen the problem since they concentrate more heat in a smaller area for a given substrate. FR4-based substrates have inherently low thermal conductivity and cannot carry away this heat quickly enough, so the junction temperatures rise, speeding up the fatigue process [2]. Ceramic substrates such as aluminum nitride (AlN) direct bond copper (DBC) can reduce the junction-to-ambient thermal resistance by up to 80% compared with PCBs, but their single copper layer and pattern resolution above 1 mm make it more challenging to keep the parasitic inductance low [7]. Therefore, a substrate that solves the thermal problem tends to exacerbate the electrical one, and none of the conventional fabrication methods can truly overcome both issues at the same time [3].

1.2. Additive Manufacturing for Electronics

Printed electronics represented the starting point for the progressive introduction of additive techniques in the electronics field. Additive manufacturing (AM) can be defined as a fabrication method consisting of the deposition of functional inks on various substrates or layers; its origins date back to the twentieth century, when printing techniques were already being used to create conductive patterns resembling PCBs [8]. Early examples of printed electronics mainly consist of the deposition of conductive inks to produce simple patterns, such as traces, electrodes, and thin-film structures, rather than fully three-dimensional devices.

In [9], Chen et al. showed a basic two-dimensional printed structure in which silver nanoparticles were deposited on flexible substrates, forming lines, dots, and other simple geometries, and then treated to become interconnections and electrodes. Another example can be found in [10], where Kamyshny et al. reported the fabrication of conductive patterns using inks based on metal nanoparticles and metal–organic compounds. These materials were used to fabricate radio-frequency identification (RFID) antennas, OLEDs, and thin-film transistors.

Overall, these early data show that printed electronics was first used to fabricate simple planar elements. Nonetheless, it paved the way for the evolution of more advanced forms of AM, where the same principles were progressively extended to three-dimensional structures. Indeed, moving to the third dimension was a natural response to the requirements of modern electronics, where devices and systems were expected to be increasingly miniaturized, customized, and highly integrated [11].

AM has recently attracted increased attention in the field of electronics as an alternative fabrication approach based on the layer-by-layer deposition of functional materials. In contrast with conventional subtractive processes, such as lithography, masking, and etching, AM allows fabrication through direct deposition [12].

Traditional electronic manufacturing techniques remain essential for high-resolution microelectronic fabrication; however, they are limited regarding the fabrication of complex geometries or embedded functionalities, leading to an increase in both capital costs and material waste. AM offers the possibility to overcome these challenges by depositing conductive, dielectric, magnetic, and polymeric materials in predefined geometries, allowing wider design freedom in the fabrication of electronic components, introducing shapes and architectures that are difficult or costly to obtain with conventional methods. Moreover, since each part is produced directly from a pre-processed digital model, AM allows for fewer manufacturing steps and reduced material waste [13].

According to the ISO/ASTM 52900:2021 classification [14], AM includes seven types of technologies that differ in the deposition and consolidation technique: vat photopolymerization (VPP), material extrusion (MEX), direct energy deposition (DED), binder jetting (BJ), sheet lamination (SHL), powder bed fusion (PBF), and material jetting (MJ). In the context of Additive Manufacturing for Electronics (AME), their relevance depends on whether they can be used to deposit functional materials such as conductive, dielectric, and semiconductive inks and pastes. Indeed, in the AME context, these technologies can be grouped into five categories: direct write and conformal, 3D printing, thermal conductivity 3D printing, planar 2D printing, and hybrid and structural electronics.

In particular, 3D-printed electronics is the most cutting-edge of these techniques. It can be implemented through different manufacturing strategies, ranging from hybrid approaches such as laser direct structuring, aerosol jetting, laser-induced forward transfer, and in-mold electronics to fully printed three-dimensional electronics. Hybrid approaches are mainly used to add conductive patterns onto 3D surfaces, whereas fully printed approaches are used to fabricate circuits directly within or onto 3D structures, using the same

equipment, thus reducing the dependence of the unit cost on the production volume and allowing customizability in low-volume production [15].

Recent studies have explored the use of AM for different classes of electronic components, such as PCBs, with an improved capacity for thermal dissipation due to the use of highly conductive silver inks, bulky magnetic devices, and planar inductors, which may require specific shaping abilities [16]. Furthermore, AM technologies have been used for the fabrication of antennas, where the possibility of producing complex geometries can be exploited to tailor their electromagnetic responses. Moreover, flexible and stimuli-responsive sensors can benefit from this technique, since conductive materials such as carbon nanotubes, silver nanoparticles, or PEDOT-PSS can be combined with polymeric substrates to obtain strain, temperature, humidity, or liquid sensors [17].

1.3. Additive Manufacturing for Power Electronics

As shown in Section 1.1, recent trends in power electronics show a constant increase in device power density and heat flux as the demand grows for energy-efficient power modules [18,19]. This growth has to satisfy the need for appropriate thermal management and packaging solutions to facilitate heat dissipation. However, the use of conventional fabrication techniques can represent a challenge in the implementation of efficient solutions as they are limited by geometric and material constraints. AME techniques provide advantages over traditional manufacturing methods as they can be used to create custom designs with complex geometries using both conductive and insulating materials. For instance, AME facilitates the creation of custom heat sink geometries using metals and ceramics [20,21], enabling the design of devices with a level of detail not achievable with conventional methods, as well as the use of challenging materials.

The increasing demand for efficient power conversion systems necessitates passive components, such as inductors and transformers, with improved power conversion efficiency and reduced volumes. In this context, AME technologies have emerged as promising fabrication methods for magnetic components, supporting the realization of complex three-dimensional geometries [22–24]. Several studies have demonstrated the feasibility of manufacturing inductors, transformers, and integrated magnetic components through the usage of conductive and magnetic inks or magnetically loaded composites [25]. Furthermore, the possibility of integrating multiple functionalities within a single structure can reduce assembly complexity, interconnection lengths, and parasitic effects, potentially improving both system efficiency and long-term reliability.

1.4. Aim of the Present Research Work

The aim of the presented research work is to investigate the feasibility of inkjet-based AME for fabricating structures and components specifically tailored to power electronics applications. Although this technology has already demonstrated significant potential in many fields [26], its applications in power electronics remain unexplored.

The starting point of the study is the printing of simple test models to compare real printed features with the 3D printing design rules, thus testing the dimensional accuracy of the printer, particularly near the lower printing limit and in the intermediate range.

Next, the focus of the current work shifts to demonstrating that AME can be useful for power electronics whenever unique shapes and alternating stacks of dielectric and conductive materials are required, such as pads enclosed in a cavity and passive components.

Concerning the latter, an inductor was designed and printed to demonstrate the potential of the process to print a working component while taking into consideration all factors studied during the preliminary tests.

After the analysis of the printed designs was completed, an examination of the electrical performance of the conductive traces was performed to highlight possible changes in the conductivity of the silver ink with respect to the ideal one due to the printing process.

To predict the electromagnetic and thermal behavior of the printed samples, finite element method (FEM) simulations were performed using COMSOL.

2. Materials and Methods

2.1. Technology Investigation

The innovative Dragonfly IV (Nano Dimension, Ltd., Ness Ziona, Israel) 3D printer was used to print the design realized for this investigation. This machine is a multimaterial 3D printer that relies on two types of ink: a conductive ink (CI) and a dielectric ink (DI). The conductive ink is AgCite 90072 (Nano Dimension, Ltd., Ness Ziona, Israel), which is based on a suspension of pure silver nanoparticles sintered using an infrared lamp, and it is used for printing conductive traces in circuits. The dielectric ink is INSU200 (Nano Dimension, Ltd., Ness Ziona, Israel), an acrylic-based ultraviolet photo-polymerizable polymer used for printing substrates, providing electrical insulation and structural support. These two materials are deposited simultaneously by employing two separate print heads, each consisting of 256 nozzles, to enable the production of AME and high-performance electronic devices.

The selected print head temperature for the CI was 40 °C, while that for the DI was 55 °C. The samples were printed on a Kapton substrate placed on the 200 mm × 200 mm printing plate, whose temperature was 160 °C. After deposition, the printed parts underwent the curing process.

The starting point of the study was an experimental assessment of the design rules provided by Nano Dimension. Indeed, the printing process is subject to specific constraints, which define the minimum and maximum dimensions and clearances that can be reliably achieved in the printed samples.

The maximum dimensions are not process-dependent but are physically limited by the size of the printing tray; in fact, the maximum recommended area in the XY plane is 160 mm × 160 mm. Along the Z direction, the maximum recommended height is 3 mm, since the accuracy tends to decrease with increasing thickness.

The minimum dimensions are instead process-dependent. As already mentioned, the printing process consists of the layer-by-layer deposition of two different inks through nozzles. The machine deposits a specific ink following the instructions provided by the associated slicing software through a pixel map. The pixel map is derived directly via the digital project created by the operator, but the slicing of the design is achieved using a nominal pitch of 18 μm as a unit of discretization, so all features in the pixel map associated with each layer are expressed through multiples of 18.

The value of the nominal pitch arises from physical constraints on the nozzles' disposition. The nozzles are separated by a distance of 70.5 μm, which is why the overlapping of the droplets during deposition is necessary to obtain continuous shapes. This overlapping is achieved by performing multiple depositions for each layer with a slight displacement; a simplified example is shown in Figure 1, where the distance between the centers of each droplet is exactly 18 μm.

Hence, the nozzles' distance of 70.5 μm defines a theoretical minimum reachable dimension. The AM design rules for a sample printed with the Dragonfly IV in ideal conditions are shown in Table 1.

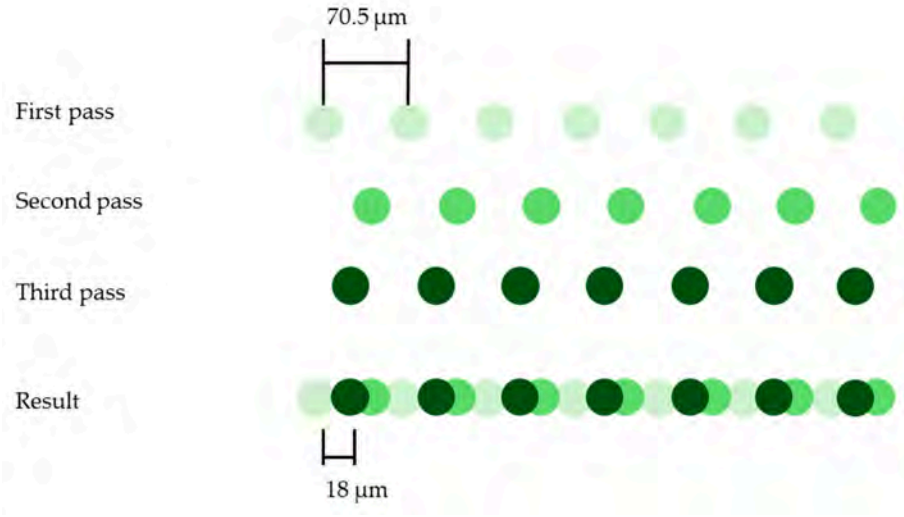


Figure 1. Schematic of the printing process for one layer.

Table 1. Minimum recommended XY sizes for samples printed with Dragonfly.

	Value (µm)	Trace Thickness (µm)
Minimum recommended trace width	70 ± 9	<100
Minimum recommended electrical clearance	100 ± 9	17–100

Vertical interconnections are often required in PCBs to connect different planes of a circuit. They can be divided into three main types: generic vias, which are vertical interconnections composed of a conductive material; through-holes (THs), which are empty cavities in the dielectric substrate; and plated through-holes (PTHs), which are empty interconnections with conductive walls. In metallic vias, two sections of the pad must be defined: the pad surrounding, which is a thin region surrounding the actual circular pad, found in both generic vias and PTHs, and the plated ring, which is the width of the metal walls in the PTH. Both are shown in Figure 2.

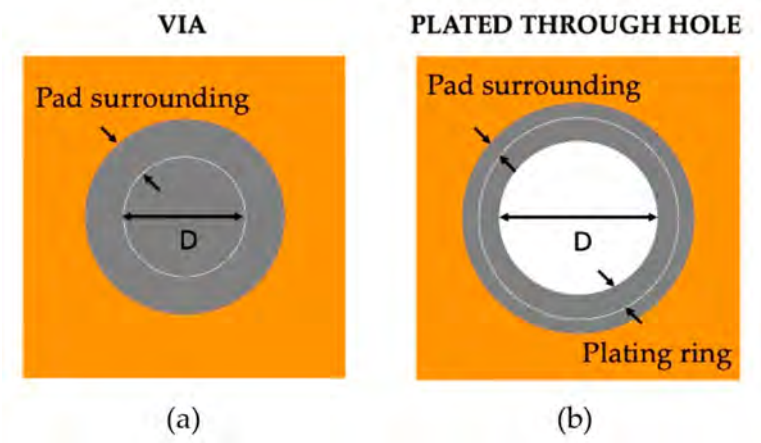


Figure 2. (**a**) Definition of pad surrounding for vias; (**b**) definition of plated ring for PTH.

Vertical interconnections are also subjected to specific design rules in the Dragonfly printing process, as reported in Table 2.

Table 2. Via and TH rules for samples printed with Dragonfly.

	Diameter (µm)	Pad Surrounding (µm)	Plated Ring (µm)
Via	$(150 \div 200) \pm 9$	100	-
TH	400 ± 18	-	-
PTH	400 ± 18	100	150

Assessing the dependency of the minimum feature size and confirming the given design rules was the first goal of the work. To achieve this aim, the first investigation involved the design and testing of simple geometries. The printing process consisted of three steps: object design, the preprocessing of the printing files, and printing. Regarding the design of the object to be printed, both the SolidWorks 2024 (Dassault Systèmes SE, Vélizy-Villacoublay, France) and KiCad 9.0 (KiCad Development Team, open-source software) design software programs were used and compared. The preprocessing of the designs was performed with Flight Control 1.3.0 (Nano Dimension, Ltd., Ness Ziona, Israel) and PCBJC Editor 1.0.0 (Nano Dimension, Ltd., Ness Ziona, Israel), as shown in Figure 3. Then, a statistical investigation was performed on the printed objects, measuring the obtained trace sizes with a digital microscope (DSX1000, Olympus Corporation, Tokyo, Japan) and calculating the offset and errors with MATLAB R2024B (Mathworks, Inc., Natick, MA, USA).

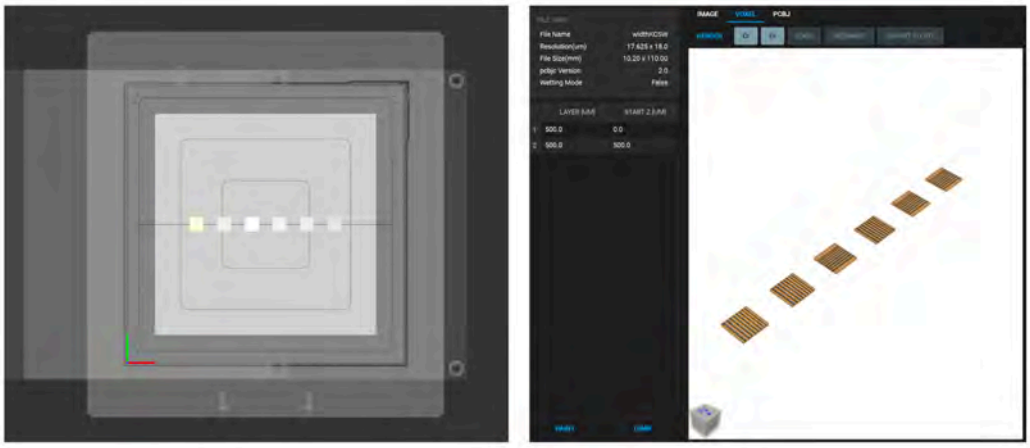


Figure 3. (**a**) View of the samples in Flight Control; (**b**) the same samples visualized in PCBJC Editor.

As a starting point for the analysis, two simple preliminary models were printed. Model 1 was characterized by parallel conductive traces, as shown in Figure 4, with simple geometries and different widths and thicknesses. It was fabricated to test the printing accuracy, exploiting a parallel and perpendicular orientation to the plate movement to test the directionality of the printing process.

In Model 2, vertical interconnections were investigated using the same design in both SolidWorks and KiCad. Specifically, in SolidWorks, the offsets found in the trace investigation of Model 1 were considered in order to correct the via design since the offset was only constant in SolidWorks.

The design was divided into three groups of vias. Group 1 consisted of generic vias, group 2 of THs, and group 3 of PTHs. The diameters and dimensions are shown in Figure 5.

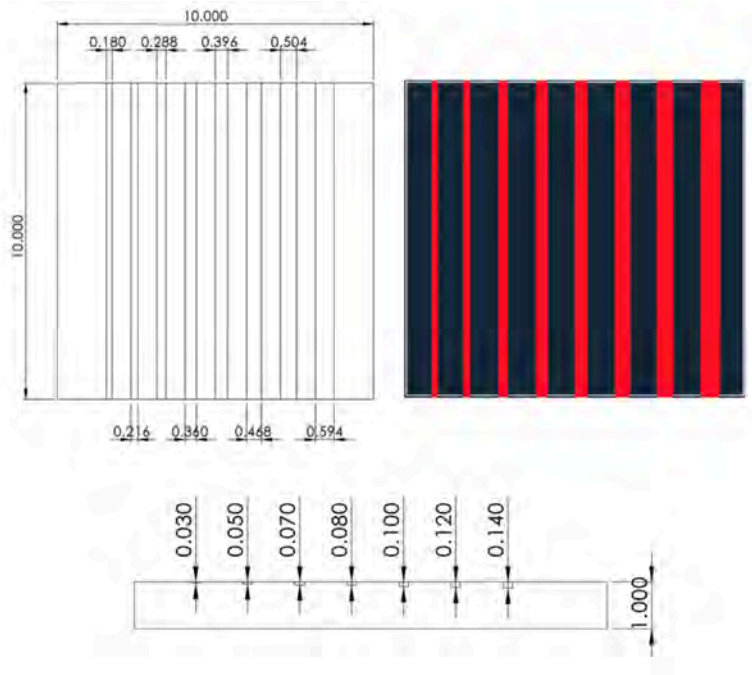


Figure 4. Model 1: (**a**) parallel trace design in SolidWorks and (**b**) KiCad, with dielectric material (dark blue) and conductive traces (red); (**c**) side view of the trace design in SolidWorks. All measurements are in mm.

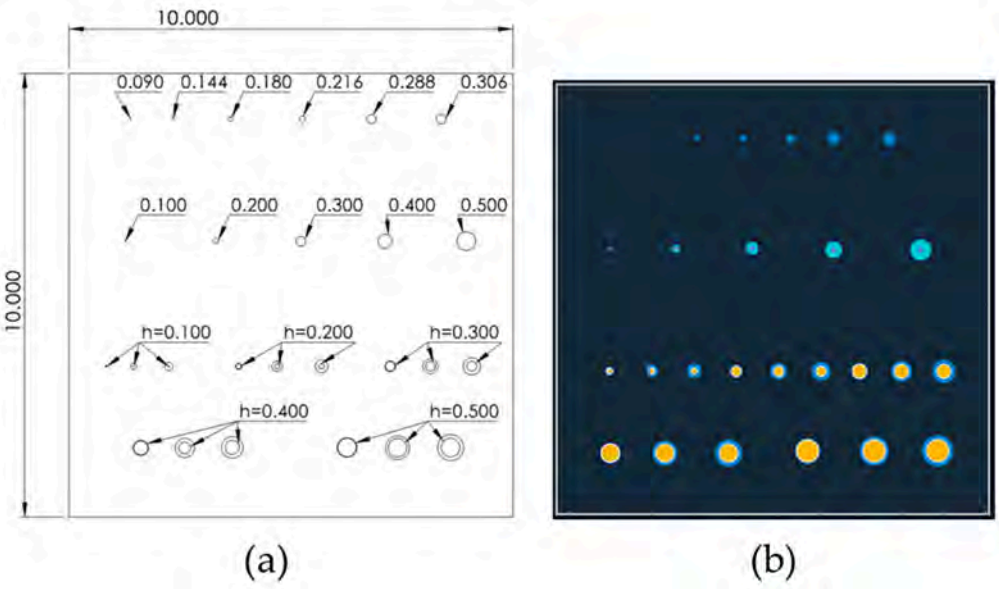


Figure 5. Model 2: (**a**) via design in SolidWorks; (**b**) via design in KiCad, in which the yellow and light blue crossed circles represent empty holes, while the dark blue ones are metal regions on the back of the sample. All measurements are in mm, and the plated regions are 100, 200, and 250 µm, respectively, for each diameter of the PTH.

2.2. Application Focus

Following these preliminary investigations, the study focused on the fabrication of five additional models with different geometrical complexities, each of them built taking into consideration the design of the previous ones.

In Model 3, a pad was designed inside a cavity intended to hold a capacitor (MCT 0603, Vishay Beyschlag, Heide, Germany); this was designed considering the cone-like shape of the cavity walls observed in the Model 2 structures. All designed dimensions were increased by a correction factor of 1 mm to ensure the correct placing of the component (Figure 6). An

LED (1.6 mm × 0.8 mm SMD CHIP LED LAMP, Kingbright Electronic Co., Ltd., New Taipei City, Taiwan) with the same footprint but with a greater height was then soldered with a silver paste (EPO-TEK H20E, Epoxy Technology, Billerica, MA, USA) to provide an immediate visual indication of the correct functionality of the structure, which was confirmed with a multimeter (MK1320, MiTek Electronics & Communications, Phoenix, AZ, USA).

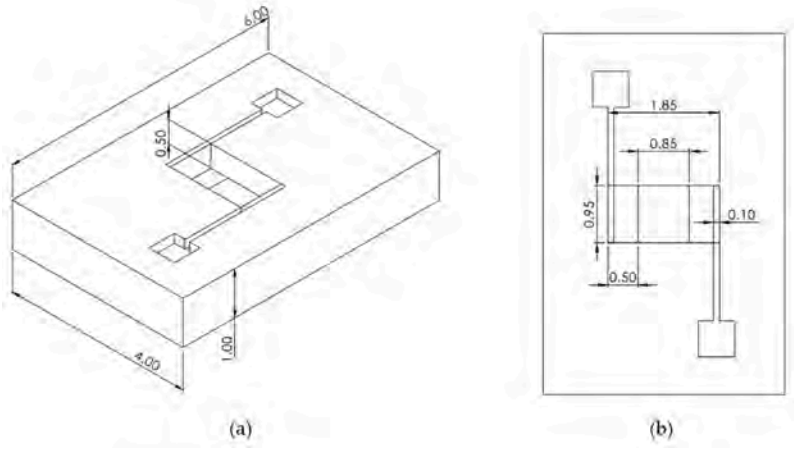


Figure 6. Model 3: (**a**) 3D view of the cavity design; (**b**) upper view of the cavity design. All measurements are in mm.

To evaluate the capability of the Dragonfly machine to print large and uniform conductive pads or busbars, Model 4 (Figure 7) was designed in SolidWorks. It consisted of a buried conductive channel connecting two pads. Horizontal dielectric pillars with a diameter of 108 µm and pitch of 50 µm were integrated within both the channel and the pads. These pillars were added to reduce possible internal stress due to the sintering process using large amounts of conductive ink [27]. This case study was used to verify the potential of manufacturing fine three-dimensional features embedded inside cavities and to investigate the interaction between conductive and dielectric inks during the printing process. Scanning electron microscopy (SEM, PHENOM XL G2, Thermo Fisher Scientific Inc., Waltham, MA, USA) was used to analyze the internal morphologies of the different structures inside the channel.

Additional trials were conducted to investigate the fabrication of multilayer devices. Model 5 was intended to evaluate the influence of the layer thickness on the dimensional accuracy of stacked structures. Furthermore, the sample was designed to understand how to manufacture large conductive pads suitable for high-current power electronics while minimizing the occurrence of defects such as cracking and dimensional distortion. Model 5, as shown in Figure 8a, had dimensions of 5.95 mm × 4.25 mm × 0.89 mm. It consisted of seven embedded conductive layers, each of them with a thickness of 100 µm and separated from the adjacent one by 30 µm of dielectric material. Electrical continuity between the conductive layers was achieved through an array of vertically conductive vias with a diameter of 108 µm, allowing the realization of a three-dimensional conductive structure. The geometry was intentionally divided into two functional regions to reproduce two applications of power electronics packaging. As shown in Figure 8b, in the region indicated in red, the conductive and dielectric layers alternated throughout the entire thickness of the device, forming an interconnection in which the uppermost and lowermost conductive layers could act as electrical terminals or busbars, designed with a cross-sectional area able to transfer high currents. The second region had only three layers but with a larger surface area, forming a large conductive pad, which was designed to enable current densities typical of power electronics applications.

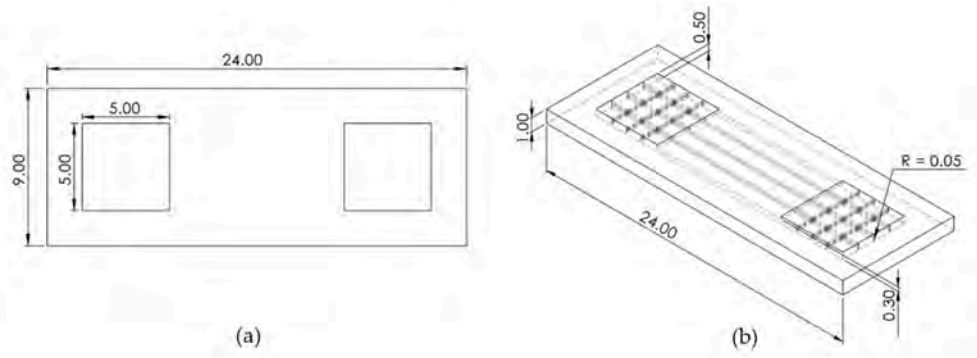


Figure 7. Model 4: (**a**) top view and (**b**) 3D view of the pads and a trace sample. Dashed lines represent pillars. All measurements are in mm.

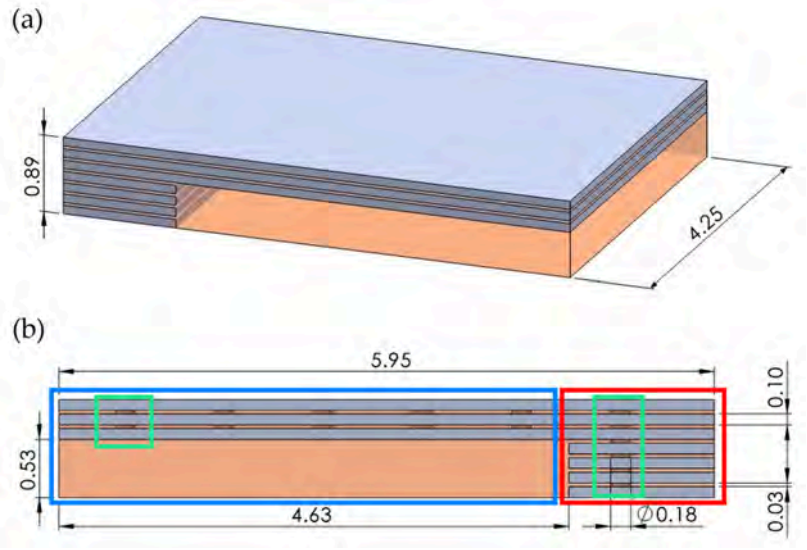


Figure 8. (**a**) Three-dimensional view and (**b**) side view of Model 5. In red, the portions of the device intended to act as terminals are indicated. In blue, the portion of the device intended to serve as a pad is indicated. In green, the vias that were used to connect the layers are indicated. All measurements are in mm.

As a proof of concept, the described AM technology was employed to fabricate custom passive components, with particular attention to integrated inductors, resulting in Model 6 (Figure 9). In this model, a cylindrical conductive solenoid with 10 coils was realized, featuring an inner diameter of 4.9 mm and an outer diameter of 5.1 mm. The coil had a squared section with 100 µm sides; the dielectric space between the turns was 150 µm, while the overall sample height was 2.8 mm. The electrical pads, located on the top and bottom surfaces of the sample, had dimensions of 3.0 mm × 3.0 mm, with a thickness of 100 µm. A precision LCR meter (LCR-8110G, Good Will Instrument Co., Ltd., New Taipei City, Taiwan) was used to measure the inductance, applying a frequency of 1 MHz and a voltage of 1.00 V.

Lastly, Model 7 (Figure 10) was printed to analyze how the conductivity was affected by flaws in the printing process. This model was characterized by four equal-sized parallel traces embedded in a dielectric substrate. The traces were wider than the ones in Model 1 to facilitate the positioning of the measuring tips.

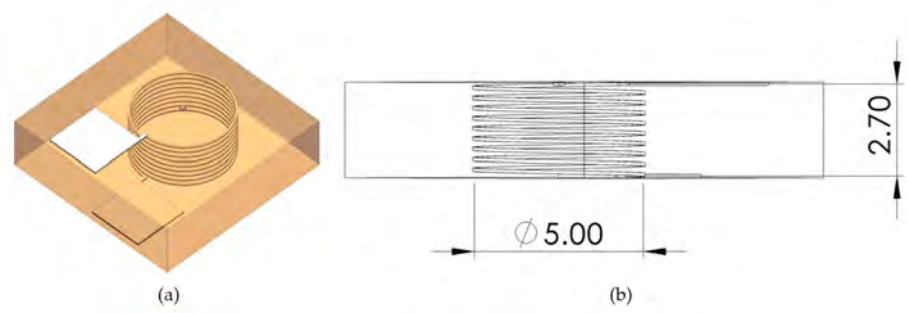


Figure 9. (**a**) Three-dimensional view and (**b**) side view of Model 6. All measurements are in mm.

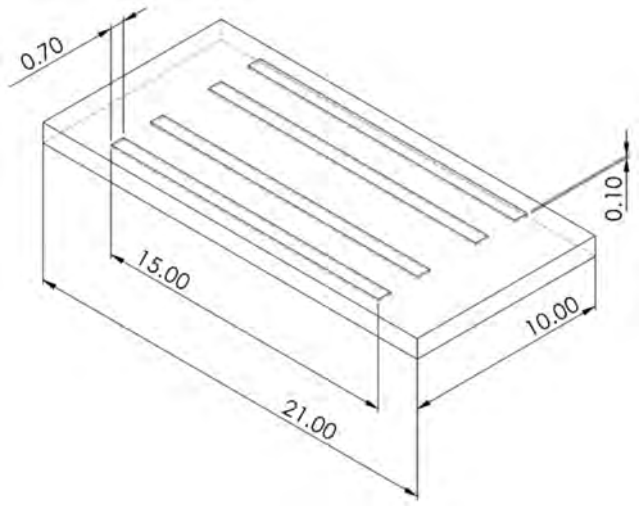


Figure 10. Model 7: conductive traces for electrical measurements. All measurements are in mm.

The electrical measurements were performed with a Keithley 6430 device (Keithley Instruments, Tektronix, Inc., Solon, OH, USA) with a four-terminal setup, whose smallest measurement range available was 20 Ω. The measurements were performed on the traces of three copies of Model 7, yielding a total of twelve measured traces. Since the resistance to be measured was expected to be low, Offset Compensation mode was enabled. This mode allows for better accuracy, since it offers an alternate measure between a null value for the current and the value fixed by the operator (1):

$$R = \frac{\Delta V}{\Delta I}[\Omega] \tag{1}$$

The current was set at 1 mA and the compliance at 2 V. From the resistance, the resistivity was calculated, as reported in (2):

$$\varrho = R \cdot \frac{A}{L} \quad [\Omega \cdot m] \tag{2}$$

Considering first the dimensions set in Model 7, a length L of 10 mm and a cross-section area of 0.7×0.1 mm^2 were considered. As a last step, the conductivity was derived from the resistivity as its inverse.

To obtain more robust results, a rigorous analysis was performed using the uncertainty propagation technique, adopting Equation (3):

$$u_x = \sqrt{\left(\frac{\partial x}{\partial R}u_x\right)^2 + \left(\frac{\partial x}{\partial w}u_w\right)^2 + \left(\frac{\partial x}{\partial t}u_t\right)^2 + \left(\frac{\partial x}{\partial L}u_L\right)^2} \tag{3}$$

Real measured values of the width, thickness, length, and resistance and their corresponding uncertainties were considered.

An additional calculation was performed using the same technique with a probe station connected to a source measure unit (SMU, Keysight B2912A, Keysight Technologies, Santa Rosa, CA, USA), whose smallest measurement range was instead 2 Ω. The current was set within the interval [0.1, 0.4] mA, with 1000 sampling points and compliance of 1 V.

2.3. Simulations

Two FEM simulations were performed using COMSOL Multiphysics 6.4 (COMSOL AB, Stockholm, Sweden) to investigate both the electromagnetic and thermal behavior of the AM-fabricated structures, particularly those of Model 6. The conductive coil and the connection pads shared the same geometric design in both numerical models, while the computational domain was defined according to the requirements of each analysis. The geometry and dimensions of the test structures, matching those used in the COMSOL models, are described in detail in the previous section.

The Magnetic Fields, Currents Only interface was employed to evaluate the magnetic flux density distribution around the inductor over a frequency range of 1 kHz to 1 GHz, while a separate electric–thermal simulation was performed using the Electric Currents and Heat Transfer in Solids interfaces to analyze the temperature rise caused by Joule heating under an electrical current. The simulations were carried out to predict the behavior of the designed structure prior to fabrication and experimental characterization. The numerical models can also serve as a reference for future experimental validation by enabling a direct comparison between the simulated and measured responses of the fabricated device.

For the magnetic field simulation, the conductive coil was enclosed within a surrounding air domain measuring 10 mm × 8 mm × 8 mm to represent the free-space region around the device. A silver-like material was assigned to the coil model. This custom material's properties are listed in Table 3.

Table 3. Silver-like material properties.

Property	Value	Unit	Notes
Electrical conductivity (silver nanoparticles)	9.2×10^6	S/m	Value taken from measurements on Model 7
Thermal conductivity	429	W/(m·K)	
Density	10,490	kg/m^3	[27]
Heat capacity at constant pressure	235	J/(kg·K)	
Relative permittivity	1	-	

The electrical conductivity of the conductive ink was assumed to be frequency-independent over the investigated simulation range (1 kHz–1 GHz). The magnetic flux density results reported in this work, however, are limited to frequencies up to 1 MHz. This assumption is consistent with the Drude model of electrical conduction in metals, according to which the conductivity remains approximately equal to its DC value as long as the excitation frequency is much lower than the electron scattering rate—a condition that is satisfied by good conductors such as silver over the frequency range considered in this study [28]. In the magnetic field model, air was assigned to the surrounding computational domain with electrical conductivity of 1×10^{-10} S/m to represent an electrically insulating medium, while the remaining air properties were taken from the COMSOL Material Library. No surrounding air domain was included in the electrothermal model.

For the magnetic field simulation, a terminal current of 10 mA was applied to the front side of one connection pad, while the front side of the opposite pad was set to ground, driving the current through the coil. To provide a spatially localized yet numerically stable measure of the magnetic flux density generated by the coil, a small circular boundary probe with a radius of 0.25 mm was defined, centered on the coil axis at the geometric center of the coil, using a dedicated work plane. The magnetic flux density norm was evaluated as the average value along the boundary of this circle at each simulated frequency.

For the electrothermal simulation, a boundary terminal with a current of 10 mA was applied to the front side of one connection pad, with the front side of the opposite pad set to ground. A fixed temperature of 293.15 K was imposed on the surfaces of one connection pad, while the remaining boundaries of the conductive structure were assigned to a thermal insulation condition.

A frequency-dependent study was performed over a range of 1 kHz to 1 GHz (values of 1, 10, 100, 1000, 10,000, 100,000, and 1,000,000 kHz were set) to evaluate the magnetic flux density response and the inductance of the conductive coil. The electrothermal simulation was likewise performed to determine the resulting temperature distribution due to Joule heating under the applied current. The reported magnetic flux density results are limited to frequencies up to 1 MHz, since, above this frequency, the assumptions underlying the present source model are no longer considered adequate for accurately capturing the current redistribution caused by the skin effect.

3. Results

3.1. Printing Accuracy Investigation

The actual dimensions of the printed traces were investigated using digital microscopy. From the measurements of the trace widths and vertical interconnection diameters (Model 1 and Model 2) obtained by analyzing multiple identical samples, statistical calculation was performed with MATLAB, through which the mean value and uncertainty of each value were obtained. The results of the statistical investigation for the widths of the printed traces in Model 1 are presented for both SolidWorks and KiCad in Tables 4 and 5, while results for the thickness are shown in Table 6.

The same investigation was also conducted for the different types of vias designed with both SolidWorks and KiCad in Model 2. It is important to consider that 80 µm was subtracted from each value assigned in SolidWorks to correct for the trend highlighted in the results of Model 1; meanwhile, in KiCad, the assigned dimensions were those explicitly reported in the tables.

Table 7 shows the results for generic vias and Table 8 shows those for THs, while Tables 9 and 10 show the results for the PTHs—first for the hole diameter and then for the plated region.

Table 4. Trace width errors and offsets (SolidWorks).

Assigned Width (µm)	Real Width (µm)	Offset (µm)
180	262.29 ± 1.23	82.29 ± 1.23
216	314.01 ± 6.16	98.01 ± 6.16
288	369.43 ± 9.85	81.43 ± 9.85
360	445.00 ± 3.14	85.00 ± 3.14
396	470.40 ± 2.46	74.40 ± 2.46
468	545.50 ± 3.28	77.50 ± 3.28
504	576.25 ± 1.89	72.25 ± 1.89
594	669.89 ± 9.85	75.89 ± 9.85

Table 5. Trace width errors and offsets (KiCad).

Assigned Width (µm)	Real Width (µm)	Offset (µm)
180	194.67 ± 5.81	13.67 ± 5.81
216	244.16 ± 2.08	28.00 ± 2.08
288	300.67 ± 2.33	12.67 ± 2.33
360	388.00 ± 2.89	18.00 ± 2.89
396	426.00 ± 8.66	30.00 ± 8.66
468	476.72 ± 8.72	16.00 ± 8.72
504	543.67 ± 15.98	39.67 ± 15.98
594	628.33 ± 15.03	34.33 ± 15.03

Table 6. Trace thickness errors and offsets (SolidWorks and KiCad).

Assigned Thickness (µm)	Real Thickness (µm)	Offset (µm)
30	31.62 ± 1.05	1.62 ± 1.05
50	53.80 ± 0.95	3.80 ± 0.95
70	71.90 ± 1.22	1.90 ± 1.22
80	87.36 ± 5.51	7.36 ± 5.51
100	108.35 ± 4.03	8.35 ± 4.03
120	130.26 ± 6.12	10.26 ± 6.12
140	160.67 ± 12.46	30.67 ± 12.46

Table 7. Generic via diameters.

Assigned Diameter (µm)	Real Diameter in SolidWorks (µm)	Real Diameter in KiCad (µm)
90	87.73 ± 2.37	109.02 ± 0.02
144	129.33 ± 0.33	165.12 ± 1.59
180	176.00 ± 6.24	211.61 ± 3.21
216	207.33 ± 9.87	245.26 ± 4.82
288	285.00 ± 3.06	311. 00 ± 3.17
306	318.33 ± 3.18	341.44 ± 4.81

Table 8. Through-hole diameters.

Assigned Diameter (µm)	Real Diameter in SolidWorks (µm)	Real Diameter in KiCad (µm)
100	-	-
200	-	254.00 ± 8.39
300	294.00 ± 2.52	401.33 ± 5.93
400	418.67 ± 5.46	522.00 ± 6.08
500	520.00 ± 5.86	623.67 ± 4.91

Table 9. Plated through-hole diameters.

Assigned Diameter (µm)	Real Diameter in SolidWorks (µm)	Real Diameter in KiCad (µm)
100	-	-
200	-	-
300	217.67 ± 6.66	-
400	328.50 ± 29.74	427.33 ± 3.27
500	405.17 ± 1.74	514.83 ± 3.83

Table 10. Plated through-hole plated widths.

Assigned Width (µm)	Real Width in SolidWorks (µm)	Real Width in KiCad (µm)
100	-	305.83 ± 6.36
200	185.08 ± 8.64	298.83 ± 4.45
250	230.67 ± 6.00	308.83 ± 10.61

Figure 11 shows a three-dimensional image of the profile of the PTH of Model 2, taken with the Display-3D setting in the Olympus DSX1000 digital microscope. Here, the cone-like nature of the walls of the vias can be seen.

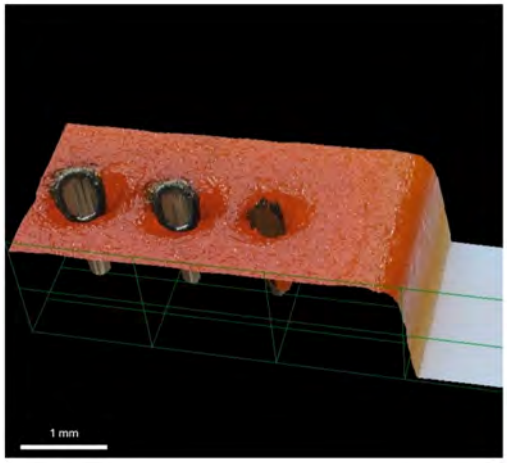


Figure 11. PTH profile. Via walls are sloped and cone-shaped.

Figure 12 shows the printed cavity of Model 3 with and without the soldered component. An LED was soldered using silver paste to provide an immediate visual indication of the correct functionality of the structure. Indeed, Figure 13 shows that the model operated properly, since the embedded LED was turned on when current was applied to its terminals.

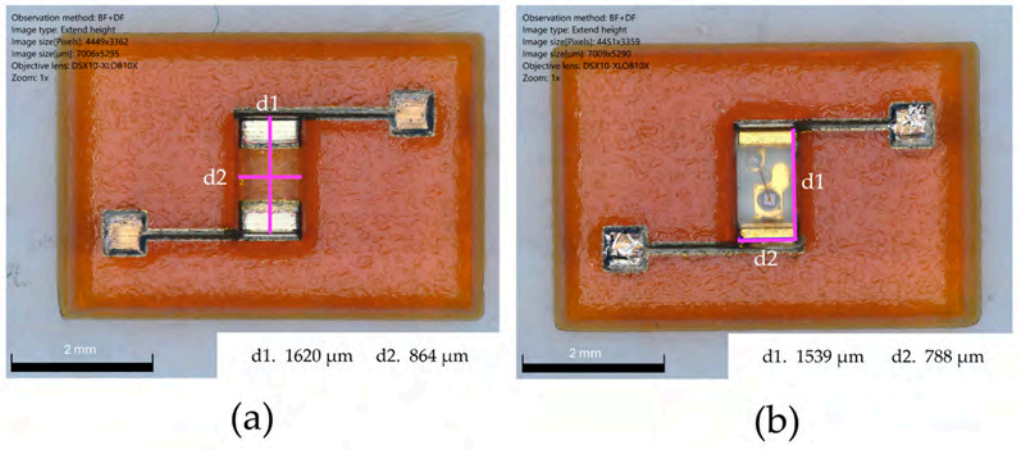


Figure 12. (**a**) Empty printed cavity; (**b**) cavity with the soldered component.

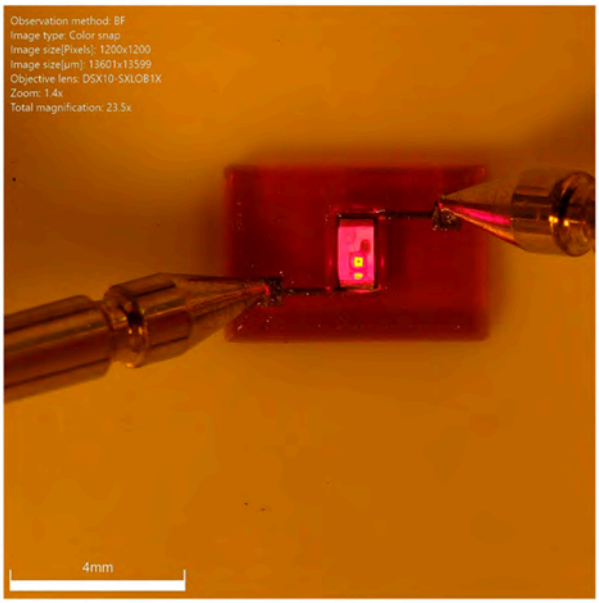


Figure 13. Soldered LED in ON state.

Figure 14 shows the print outcome of Model 4. It differed from the original CAD model in several ways. The most evident features were the checkerboard-like pattern (Figure 14a) visible on the surfaces of both pads and the localized grooves present on the left pad (Figure 14b). These grooves were placed where dielectric pillars were expected to be found, according to the CAD model. Although the traces appeared to be defective on the surface, electrical conductivity was achieved along its entire length. Moreover, the overall geometry was maintained, and the dimensions remained consistent with the dimensions defined in SolidWorks.

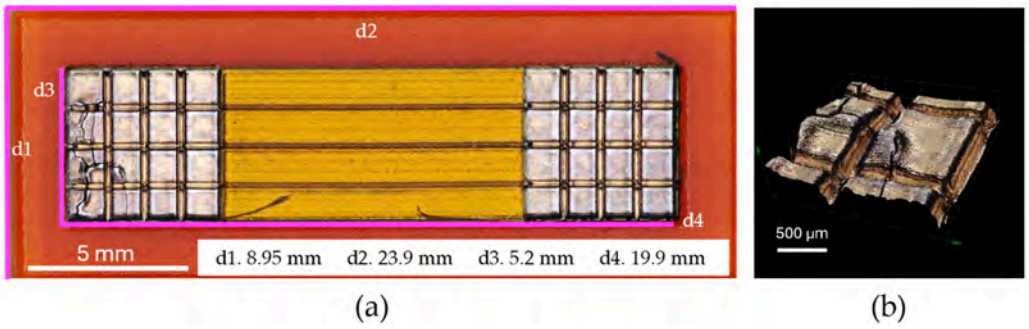


Figure 14. (**a**) Top view of Model 4; (**b**) 3D profile of the fractured surface of the pad at the bottom left.

The model was laser-cut through the center along its shorter dimension to investigate the internal features of the printed device via SEM analysis. Figure 15 shows the cross-section inside the trace. As can be seen, the circular pillars along the channel did not maintain their intended shape along their axes, as they appeared flattened and exhibited an elongated striped profile. The interface between the dielectric and conductive layers was characterized by a dent, showing incorrect material deposition.

Figure 16 shows the top and bottom surfaces of Model 5. The conductive pad showed extensive fractures covering the entire surface. The surface was not completely planar and presented local height variations that were visible over the entire pad.

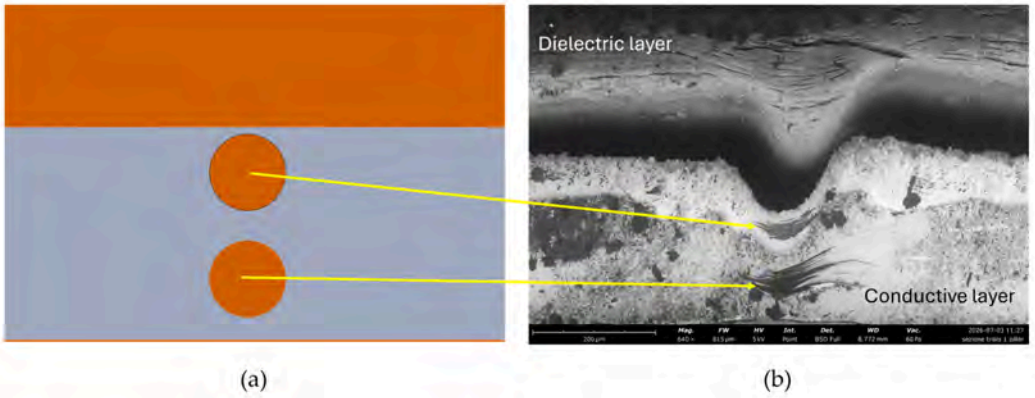


Figure 15. Comparison between (**a**) CAD model and (**b**) SEM cross-section of the channel, showing the dielectric pillars and the absence of a conductive layer after the second pillar.

A higher-magnification cross-sectional image of the structure is reported in Figure 17. The individual conductive and dielectric layers were clearly discernible. The measured thicknesses of the dielectric and conductive layers were 32 µm and 99 µm, respectively. The conductive via was also successfully printed, and its diameter was 198 µm.

Figure 18a shows that Model 6, characterized by an inductor embedded within a dielectric component, was successfully printed. The measured outer and inner diameters were 5.10 mm and 4.70 mm, respectively. The conductive trace of the coils had a width of 186 µm. The conductive trace connecting the pads had a width of 324 µm, while the pad had a side length of 3.07 mm. Cross-sectional images of the device, shown in Figure 18b,c, revealed that the coils were printed correctly. The measured thickness of the trace was 96 µm, while the steps between the coils measured 188 µm. As previously observed for the printed vias, the conductive material exhibited a non-uniform internal morphology.

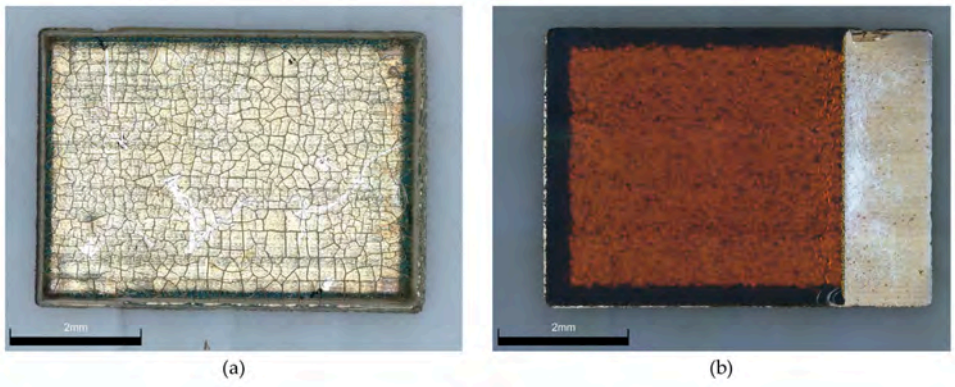


Figure 16. Printed Model 5. (**a**) Top view; (**b**) bottom-view of the multilayered device.

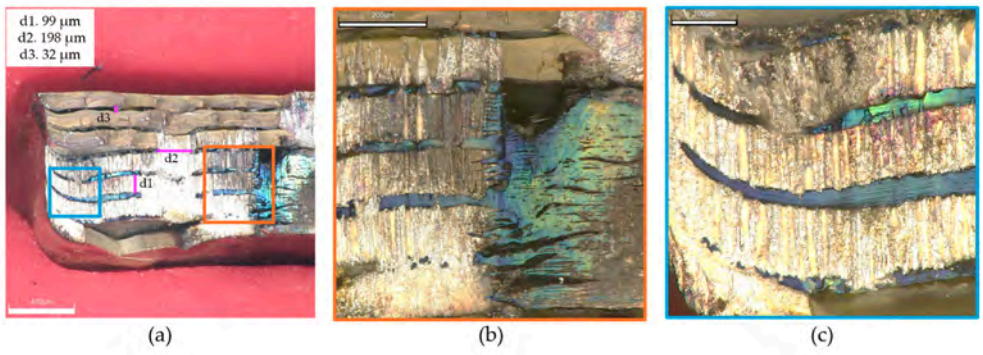


Figure 17. (**a**) Side view of the multilayered device; (**b**) detail of the interface between the layers and the dielectric substrate; (**c**) detail of the dielectric layers.

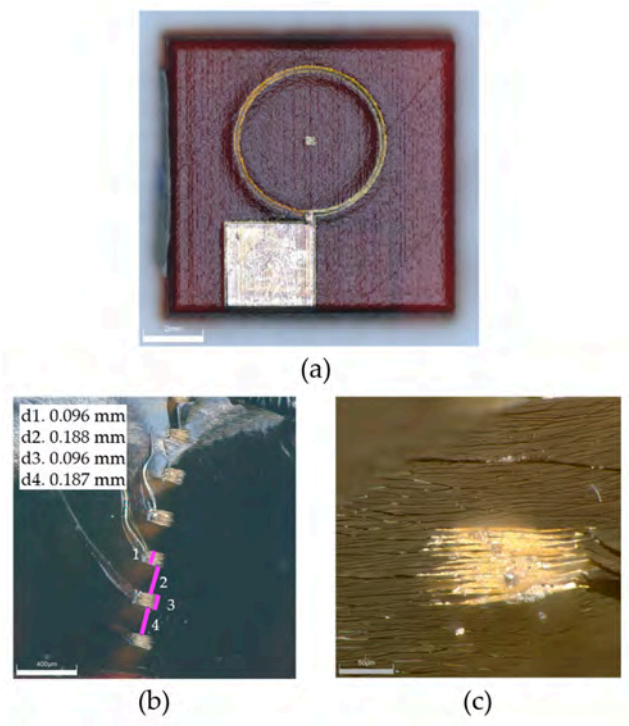


Figure 18. (**a**) Top view of Model 6; (**b**) side view of the internal structure of the device; (**c**) detail of one of the turns of the coil.

Three copies of the model were printed to measure the inductance and resistance. The results are reported in Table 11.

Table 11. Values of the inductance and resistance of three identical copies of Model 6 printed along the printing direction.

Inductor 1	Inductor 2	Inductor 3
(0.425 ± 0.005) µH (6.720 ± 0.538) Ω	(0.435 ± 0.005) µH (6.048 ± 0.538) Ω	(0.434 ± 0.005) µH (7.124 ± 0.538) Ω

Following the analysis of the printing quality of the inductor, conductivity measurements were carried out on twelve tracks printed from three copies of Model 7. The average of the measurements resulted in the following conductivity of the silver traces:

$$\sigma = (0.92 \pm 0.05) \cdot 10^7 \mathrm{S/m}.$$

For the following calculations, the considered features were L = (9699.00 ± 101.82) µm, w = (797.00 ± 5.71) µm, and t = (108.35 ± 4.03) µm. The conductivity derived from the propagation equation, with the average resistance R = (0.0014 ± 0.0001) Ω, corresponded to

$$\sigma = (8.02 \pm 0.31) \cdot 10^7 \mathrm{S/m}.$$

Lastly, the conductivity calculated with the same method using an SMU, with average resistance R = (0.008544 ± 0.000156) Ω, was

$$\sigma = (1.31 \pm 0.06) \cdot 10^7 \mathrm{S/m}.$$

To better understand the values reported above, images of the trace cross-sections were acquired using both digital microscopy and SEM, highlighting the hair effect (Figure 19).



Figure 19. Hair effect as observed with (**a**) digital microscope; (**b**) SEM. In both pictures, the growth direction is highlighted.

3.2. Simulations

The frequency-dependent FEM simulation predicted the magnetic flux density distribution around the proposed additively manufactured conductive coil. As illustrated in Figure 20a, the magnetic flux density was higher around the conductive coil and decreased with increasing distances from it. The corresponding magnetic flux density values obtained at each frequency are summarized in Tables 12 and 13. The volume-average magnetic flux density (Table 13) was calculated over the entire simulation domain, while the value in Table 12 was evaluated using a circular boundary probe (radius 0.25 mm) centered on the coil axis at the geometric center of the coil. The two metrics are reported together to provide both a domain-wide and a spatially localized measure of the generated field. The results are reported for frequencies up to 1 MHz, since, above this frequency, the reported values are not considered physically reliable.

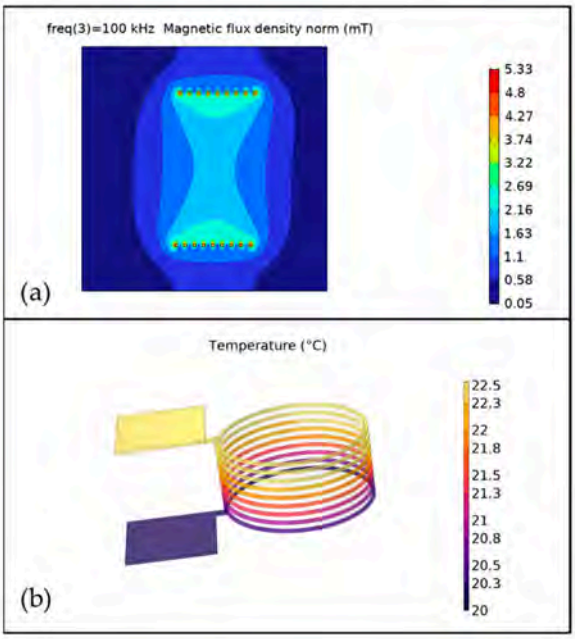


Figure 20. Results of the COMSOL simulations: (**a**) magnetic flux density norm of the device for f = 100 kHz; (**b**) graph of the temperatures reached on the solenoid.

Table 12. Magnetic flux density averaged over a circumference located in the middle of the coil.

Frequency (kHz)	Magnetic Flux Density (T)
10^0	1.72×10^{-3}
10^1	1.72×10^{-3}
10^2	1.75×10^{-3}
10^3	3.91×10^{-3}

Table 13. Average magnetic flux density norm.

Frequency (kHz)	Magnetic Flux Density (T)
10^0	6.22×10^{-4}
10^1	6.23×10^{-4}
10^2	6.80×10^{-4}
10^3	2.08×10^{-3}

The electrothermal simulation predicted the temperature distribution under the applied excitation current of 10 mA. As shown in Figure 20b, the lowest temperature was observed at the connection pad, which was maintained at the prescribed reference temperature of 20 °C, whereas the opposite connection pad exhibited the highest temperature, reaching approximately 22.5 °C, corresponding to a temperature increase of about 2.5 °C above the ambient reference temperature.

From the electromagnetic simulation, an inductance value of 0.380 µH at 1 MHz and 1 V was obtained.

4. Discussion

The results presented in this article are derived from analyses of the potential of AME in power electronics component fabrication. The preliminary tests on the traces' behavior enabled the identification of three main factors of variability: the positions of the features along a specific axis, the printing direction, and the software used to design the samples.

Regarding the latter, the dimensions in the XY plane were found to be the most affected by printing inaccuracies, as shown in Tables 4 and 5. In particular, differences were observed depending on whether the geometries were designed using SolidWorks or KiCad. For Model 1, SolidWorks showed higher but mostly constant offset values between the assigned and real ones, with an average difference of 80 µm, while KiCad showed lower errors but with a random distribution of the offset for each width value in the range of 10 µm to 40 µm. For this reason, despite the higher offset found in SolidWorks, this software appears to be the most reliable, since a constant correction factor could be used on future fabricated features.

The Z direction was rather unaffected by the chosen design software and generally showed higher accuracy (Table 6). Nevertheless, the error tended to increase together with the thickness. In addition, along the Z axis, all printed shapes tended to widen along the XY plane, progressively assuming a cone-like geometry and showing shrinkage at the bottom of about 1 mm with respect to the assigned dimensions.

Regarding the printing direction, printing the samples parallel to the direction of ink deposition helped to reduce both the printing time and the dispersion of the silver ink. These dispersions consisted of small drops of silver scattered into the dielectric part. Nevertheless, this phenomenon did not significantly affect the dimensional accuracy.

The same investigation was repeated in Model 2 for both SolidWorks and KiCad. In SolidWorks, the design was created considering the previous offset of 80 µm calculated for Model 1; for this reason, the diameters of the generic vias were closer to the assigned

ones. The use of the correction factor allowed us to highlight the differences in behavior between full and empty holes, since the further enlargement of the diameters with respect to the already calculated offset was found in the case of the TH for both software programs. Indeed, the dielectric ink tended to expand increasingly on the XY plane as the Z coordinate increased—to a greater extent than the conductive one. Moreover, in the KiCad model, where no correction was used since the offset was not constant, the via diameters showed the same behavior as the traces, with an offset of between 10 µm and 40 µm, while the TH, as already stated, tended to be enlarged further with an offset of around 120 µm for larger holes. Despite the design rules in Table 2, the realization of a hole smaller than 400 µm was achievable in both software programs, with a minimum reachable diameter of about 254 µm in KiCad.

The final consideration is related to vertical interconnection printing—more specifically, that of the PTH, which was dependent on both the direction and material. They all showed an oblique profile along Z instead of a straight one, as can be seen in Figure 11, which was due to the directional deposition and the different trends in dielectric and conductive growth along Z. The greater enlargement of the dielectric component caused the silver ink to slide down and accumulate laterally and at the bottom; this incorrect deposition of the silver caused the closing of some of the smaller holes and the incorrect deposition of the plated width.

The geometry of Model 3, shown in Figure 6, was designed considering the previously reported trend, i.e., the cone-like shapes of the features along Z. For this reason, each dimension was increased by exactly 1 mm with respect to the reference capacitor. To obtain immediate visual proof of the correct functionality of the structure, an LED was soldered and turned on with a multimeter, with a positive outcome.

Concerning the samples created specifically to test the printing performance for power electronics structures, the print quality was affected by the factors described above—especially the offsets and layer shrinkage.

In Model 4, the striped features of the dielectric pillars inside the conductive channel were caused by the different properties of the two inks. This effect, described in the design rules, is known as the hair effect. Consequently, since the Dragonfly could not print self-supporting structures, the conductive layers above the pillars tended to fill the gap created by the irregular shape beneath, resulting in the checkboard pattern visible in Figure 14.

Model 5 confirmed the ability of the machine to print thick conductive pads by stacking multiple conductive layers interconnected through vertical vias. However, increasing the dielectric thickness between adjacent conductive layers would have prevented the sliding of the conductive ink along the sidewalls, improving the quality of the structure. Although the multilayer structure was preserved, the conductive layers did not exhibit perfect planar interfaces, as shown in Figure 17, and they presented an irregular surface morphology. The cracks were due mainly to the sintering process of the conductive ink. In particular, the large amount of silver deposited to form the conductive layers was subjected to volumetric shrinkage during sintering, generating mechanical stress and thus causing the cracks visible on the surface. Therefore, optimizing the sintering process—especially considering how to manage the temperature profile during the curing process—would be helpful to minimize crack formation and improve the electrical and mechanical performance of the device. The conductive regions displayed the same characteristic striped morphology that was previously observed on the dielectric pillars of Model 4.

Besides the striped nature of the coils in Model 6, the solenoid geometries were successfully reproduced, and the spacing between adjacent coils was preserved, confirming the importance of ensuring an appropriate relationship between the thicknesses of the printed structures. The measured inductance values showed only limited variation, demonstrating

good repeatability under identical conditions. The average measured inductance, which was approximately 0.431 µH, differed by 13.5% from the simulated value. Hence, despite the defects caused by the process, it was able to produce samples with characteristics coherent with the ideal case.

Regarding the electromagnetic simulation, the field values reported in Tables 12 and 13 are limited to frequencies up to 1 MHz. This limitation follows from the modeling approach adopted, in which the current distribution used as the source for the frequency-domain magnetic field solution is obtained from the Magnetic Fields, Currents Only interface and is kept frequency-independent. At 1 MHz, the skin depth of the conductive ink, calculated as $\delta \approx 166$ µm using the measured conductivity ($\sigma = 0.92 \times 10^7$ S/m), remains larger than the 100 µm trace thickness, so the frequency-independent current distribution used in the present model remains a reasonable approximation at this frequency. Above this frequency, the skin depth decreases below the trace thickness ($\delta \approx 52$ µm at 10 MHz and $\delta \approx 5$ µm at 1 GHz), and the current is expected to progressively redistribute toward the conductor surface. Since the current distribution used as input to the frequency-domain solution does not change with the frequency, this redistribution was not captured, and the resulting magnetic flux density values above approximately 1 MHz were considered physically unreliable and are not reported. Both the volume-averaged (Table 13) and probe-averaged (Table 12) magnetic flux density values showed an increasing trend over the reported frequency range.

Regarding the thermal simulation, the results indicated that, under the applied operating conditions and the material properties considered in the model, Joule heating produced only a modest temperature increase within the conductive structure (Figure 20b). The electrical characterization performed on the traces printed from Model 7 showed a discrepancy between the various conductivity measurements. Considering the official value reported in the datasheet of $\sigma = 2.21 \cdot 10^7$ S/m, among the experimental results, the value obtained using the SMU, including the complete uncertainty propagation, was considered the most representative and reliable, since it lay within the uncertainty range provided by the manufacturer. The discrepancy between the measurements was most likely related to differences in the experimental setups and in the operating ranges of the two instruments.

Nevertheless, the conductivity was slightly lower than the ideal one, and the reason could be found in the previously mentioned hair effect. Indeed, the metallic features, which should have been continuous shapes, were instead characterized by a mixture of metallic and thin dielectric layers due to the droplet nature of the deposition. The traces did not have simple rectangular cross-sections, as expected from the design, but showed fringes on the edges with dielectric infiltration, resulting in a smaller effective conductive area and consequently lower conductivity.

5. Conclusions

The aim of the present research was to demonstrate that AME could be considered a promising approach in high-power electronics. The investigation started by determining the limits and perspectives of this technology, relying on simple geometries for testing the dependency of 3D printing on the feature design software, size, and position. It was observed that the mentioned factors affected the outcomes differently. Looking at the used software, despite the offset calculated from the dimensional analysis, due mostly to the characteristics of the printing technique, different conclusions can be drawn. For SolidWorks, the error was highly predictable for most of the features; thus, it could be easily compensated for; meanwhile, for KiCad, the error was randomly distributed. Indeed, considering the slope of the profile and performing the required corrections, it was possible to fabricate working pads enclosed in a cavity for a specific component, confirming the

ability of AME to reproduce unique designs. Models 4 and 5 demonstrated that the process was able to print thick conductive structures. Furthermore, Model 5 showed the feasibility of the process in printing well-defined vertical interconnections. Although the interfaces between the conductive and dielectric layers were not ideal due to their different properties, the process was able to yield the main features of the samples. However, future research is needed to optimize the outcomes of the process.

The embedded inductor of Model 7, whose design was realized considering all effects and the corrections discussed, demonstrated the feasibility of printing passive components directly within a substrate. In this context, the results obtained for the three printed inductors demonstrated that the process could yield samples with good repeatability under identical conditions.

The average measured inductance was approximately 0.431 μH, differing by 13.5% from the simulated value. Hence, despite the defects caused by the printing step, the process was able to produce samples with characteristics coherent with the ideal case. In addition, despite the tendency of the conductive features to be mixed with very thin dielectric layers due to the layer-by-layer technology, the calculation of the conductivity still showed a value with the same order of magnitude as the official one, proving that the features were highly conductive.

The FEM simulations predicted the magnetic flux density distribution around the proposed additively manufactured conductive coil for frequencies up to 1 MHz. As illustrated in Figure 20a, the magnetic flux density was mainly concentrated around the conductive coil. Results above 1 MHz were excluded, since, above this frequency, the skin depth of the conductive ink becomes smaller than the trace thickness, and the frequency-independent current distribution used as the source for the frequency-domain solution does not capture the resulting redistribution of the current toward the conductor surface. Within the reported range, both the volume-averaged and probe-averaged magnetic flux density values showed an increasing trend with the excitation frequency. A specific study of the skin effect at higher frequencies, including a frequency-dependent current distribution, is left for future work.

Author Contributions: Conceptualization, G.M. and G.G.; methodology, M.A. and G.G.; software, F.P., S.M., and S.T.; formal analysis, S.T.; investigation, S.T. and F.P.; resources, M.A., G.G., E.A., and D.G.; data curation, S.T., F.P., and E.A.; writing—original draft preparation, E.A., D.G., F.P., S.M., and S.T.; writing—review and editing, M.A., G.G., and V.B.; visualization, L.S., S.F., and G.M.; supervision, L.S.; project administration, V.B.; funding acquisition, S.F. All authors have read and agreed to the published version of the manuscript.

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References

1. Santi, E.; Tian, B.; Peng, K. Power Electronic Modules. In *Power Electronics Handbook*; Elsevier: Amsterdam, The Netherlands, 2024; pp. 151–170.
2. Zheng, L.; Ji, S.; Yao, X. A Review of High Voltage Challenges and Developments of Power Electronics Packaging. In Proceedings of the 2024 IEEE International Power Modulator and High Voltage Conference (IPMHVC), Indianapolis, IN, USA, 28 May–1 June 2024; pp. 1–4.
3. Shammas, N.Y.A. Present Problems of Power Module Packaging Technology. *Microelectron. Reliab.* **2003**, *43*, 519–527. [CrossRef]
4. Sun, Z.; Takahashi, M.; Guo, W.; Munk-Nielsen, S.; Jørgensen, A.B. Thermal Cycling Characterization of an Integrated Low-Inductance GaN EHEMT Power Module. *Microelectron. Reliab.* **2024**, *161*, 115482. [CrossRef]
5. Shen, H.; Zhang, J.; Sun, P.; Ma, X. Review on the Thermal Parameters Applications in the Reliability of Power Semiconductor Device. In Proceedings of the 2024 IEEE 7th International Electrical and Energy Conference (CIEEC), Harbin, China, 10–12 May 2024; pp. 4482–4487.
6. Piekarz, I.; Wincza, K.; Gruszczynski, S.; Sorocki, J. Low-Cost Fully Additively Manufactured Passive Microwave Components Exploiting Available 3D Flexibility. *Sci. Rep.* **2023**, *13*, 2886. [CrossRef] [PubMed]
7. Wang, M.; Gao, P.; Shi, F.; Hu, W.; Wang, X.; Yan, H.; Mei, Y. Advanced Packaging Technology of GaN HEMT Module for High-Power and High-Frequency Applications: A Review. *IEEE Trans. Compon. Packag. Manuf. Technol.* **2024**, *14*, 1537–1550. [CrossRef]
8. Beedasy, V.; Smith, P.J. Printed Electronics as Prepared by Inkjet Printing. *Materials* **2020**, *13*, 704. [CrossRef] [PubMed]
9. Chen, S.-P.; Chiu, H.-L.; Wang, P.-H.; Liao, Y.-C. Inkjet Printed Conductive Tracks for Printed Electronics. *ECS J. Solid State Sci. Technol.* **2015**, *4*, 3026–3033. [CrossRef]
10. Kamyshny, A. Metal-Based Inkjet Inks for Printed Electronics. *Open Appl. Phys. J.* **2011**, *4*, 19–36. [CrossRef]
11. Zikulnig, J.; Chang, S.; Bito, J.; Rauter, L.; Roshanghias, A.; Carrara, S.; Kosel, J. Printed Electronics Technologies for Additive Manufacturing of Hybrid Electronic Sensor Systems. *Adv. Sens. Res.* **2023**, *2*, 2200073. [CrossRef]
12. Tan, H.W.; Choong, Y.Y.C.; Kuo, C.N.; Low, H.Y.; Chua, C.K. 3D Printed Electronics: Processes, Materials and Future Trends. *Prog. Mater. Sci.* **2022**, *127*, 100945. [CrossRef]
13. Espera, A.H.; Dizon, J.R.C.; Chen, Q.; Advincula, R.C. 3D-Printing and Advanced Manufacturing for Electronics. *Prog. Addit. Manuf.* **2019**, *4*, 245–267. [CrossRef]
14. *ISO/ASTM 52900:2021*; Additive Manufacturing—General Principles—Fundamentals and Vocabulary. ISO: Geneva, Switzerland; ASTM International: West Conshohocken, PA, USA, 2021.
15. Wang, Z. *3D Electronics/Additive Electronics 2024–2034: Technologies, Players, and Markets*; IDTechEx Ltd.: Cambridge, UK, 2024.
16. Dhinesh, S.K.; Joshua Robert, J.; Tushar Nair, S.; Sharne Moni, D.H.; Sona Fowzeya, S.; Senthil Kumar, K.L.; Raghunath, M.; Nagarajan, P. Recent Trends in Additive Manufacturing of Electronics Devices. *Mater. Today Proc.* **2022**, *66*, 928–941. [CrossRef]
17. Aronne, M.; Polano, M.; Bertana, V.; Ferrero, S.; Frascella, F.; Scaltrito, L.; Marasso, S.L. Application of 3D and 4D Printing in Electronics. *J. Manuf. Mater. Process.* **2024**, *8*, 164. [CrossRef]
18. Lopera, L.; Rodriguez, R.; Yakout, M.; Elbestawi, M.; Emadi, A. Current and Potential Applications of Additive Manufacturing for Power Electronics. *IEEE Open J. Power Electron.* **2021**, *2*, 33–42. [CrossRef]
19. Saito, W. A Future Outlook of Power Devices From the Viewpoint of Power Electronics Trends. *IEEE Trans. Electron Devices* **2024**, *71*, 1356–1364. [CrossRef]
20. Wu, T.; Wang, Z.; Ozpineci, B.; Chinthavali, M.; Campbell, S. Automated Heatsink Optimization for Air-Cooled Power Semiconductor Modules. *IEEE Trans. Power Electron.* **2019**, *34*, 5027–5031. [CrossRef]
21. Galfré, G.; Girelli, D.; Aronne, M.; Mossotti, G.; Apiletti, E.; Melis, G.; Messere, M.; Ferrero, S.; Scaltrito, L.; Bertana, V. Additive Manufacturing for Electronics (AME): Prototyping High Surface Area Substrates to Improve Thermal Performance. *Electronics* **2026**, *15*, 1002. [CrossRef]
22. Bowen, D.; Basu, D. Exploration of the 3-D Printing of Transformer Structures With Embedded Ferrite Cores. *IEEE Trans. Magn.* **2019**, *55*, 8400705. [CrossRef]
23. Obeidat, A.S.; Enakerakpo, E.; Busse, E.; Umar, A.; Al-Haidari, R.; Alhendi, M.; Poliks, M.D.; Erdtmann, M.; Pyke, A. Additive Manufacturing of Passive Electronic Components Using Aerosol Jet Printing and Reliability Tests for Spaceborne Applications. In Proceedings of the 2025 IEEE 75th Electronic Components and Technology Conference (ECTC), Dallas, TX, USA, 27–30 May 2025; pp. 1765–1772.
24. Tsui, L.-K.; Hartmann, T.M.; Dye, J.; Lavin, J.M. Additive Manufacturing of Coreless Flyback Transformers Using Aerosol Jet Printing and Electrochemical Deposition. *IEEE Trans. Compon. Packag. Manuf. Technol.* **2023**, *13*, 1302–1309. [CrossRef]
25. Yan, Y.; Moss, J.; Ngo, K.D.T.; Mei, Y.; Lu, G.-Q. Additive Manufacturing of Toroid Inductor for Power Electronics Applications. *IEEE Trans. Ind. Appl.* **2017**, *53*, 5709–5714. [CrossRef]

26. Mariello, M.; Blad, T.W.A.; Mastronardi, V.M.; Madaro, F.; Guido, F.; Staufer, U.; Tolou, N.; De Vittorio, M. Flexible Piezoelectric AlN Transducers Buckled through Package-Induced Preloading for Mechanical Energy Harvesting. *Nano Energy* **2021**, *85*, 105986. [CrossRef]
27. McKerricher, G.; Gonzalez Perez, J.; Shamim, A. Fully Inkjet Printed RF Inductors and Capacitors Using Polymer Dielectric and Silver Conductive Ink With Through Vias. *IEEE Trans. Electron Devices* **2015**, *62*, 1002–1009. [CrossRef]
28. Ashcroft, N.W.; Mermin, N.D. *Solid State Physics*; Harcourt Brace: Fort Worth, TX, USA, 1976; ISBN 9780030839931.

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