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A Simple and Cost-Effective Method for Condition Monitoring of Inverter DC-Link Film Capacitors Based on Capacitance Variation

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ABSTRACT DC-link capacitors are among the most critical components in traction inverters, with a high likelihood of failure. Effective condition monitoring (CM) of these capacitors is crucial for improving converter reliability and preventing catastrophic failures. This article presents a cost-effective and reliable methodology for evaluating the health state of film capacitors used as dc-link in traction inverters. The proposed approach uses a controlled discharge test to track capacitance variations over time, which can be used as an indirect indicator of the capacitor's health state. Key advantages of this technique include the minimal additional component requirements for cost efficiency, strong noise immunity, and high precision. Furthermore, the proposed aging detection test can be fully automated without requiring the removal of the capacitor or modifications to the converter's power stage. Experimental results are provided to validate the effectiveness of the proposed solution.

INDEX TERMS Condition monitoring, dc-link capacitors, film capacitors, traction inverters.

I. INTRODUCTION

Nowadays power electronic converters have an important impact on electrical industries due to their ability to convert and control the flow of electric power. Modern converters used in safety-critical applications such as aerospace, automotive, and medical should guarantee high levels of safety and reliability. An unforeseen failure in such applications could result in catastrophic consequences and potentially endanger human life. Consequently, preventive maintenance and condition monitoring systems are vital to ensure the safe and reliable operation of power converters [1], [2], [3]. According to the literature, capacitors and semiconductors rank among the components with the highest failure rates [4]. Fig. 1 shows the distribution of failure for power electronic components, indicating that dc-link capacitors are among the most vulnerable parts of the system. For this reason, implementing a condition monitoring system capable of assessing the health state of dc-link capacitors can enable preventive maintenance, thereby preventing unexpected failures [4]. Various methods for condition monitoring of capacitors have been discussed in the literature [5], [6], using different parameters as indirect indicators of capacitor health. The main lifetime indicators can be categorized into two main groups: nonelectrical indicators and electrical indicators.

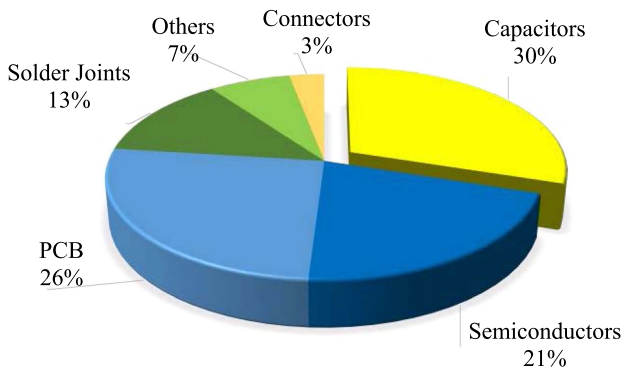

FIGURE 1. Distribution of failure modes in power electronic converters [4].

Nonelectrical indicators such as weight, structural changes, internal pressure, and internal temperature can be used as indirect indicators to determine the health state of the capacitor.

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For example, degradation in capacitors can be accompanied by a decrease in weight [7] (e.g., due to electrolyte losses).

Another nonelectrical indicator of degradation is the structure change of the capacitor, which can be monitored using X-ray images [8] or strain gauges. However, nonelectrical methods often demand costly equipment, and accurately defining end-of-life criteria based on these indicators can be particularly challenging.

Electrical indicators such as ESR, capacitance, dissipation factor, and voltage ripple are commonly preferred as lifetime indicators.

Most of these methods rely on ESR or capacitance variations to assess the health state of capacitors [9]. In film capacitors, the ESR is substantially lower than electrolytic capacitors. Therefore, it is hard to measure the ESR, and the capacitance variation is usually preferred as an indirect indicator of the health condition. It is well established in the literature that as the capacitor ages, the capacitance decreases over time [4], [5], [6], [7], [8], [9], [10], [11], [12]. The drop in the capacitance happens due to multiple reasons, however the aging mechanisms are not in the scope of this article. For example, for film capacitors, a 5% decrease in capacitance is generally considered indicative of the capacitor reaching its end-of-life [6].

In general, electrical parameters can be measured directly by tools such as *LCR* meters [13]. However, to use these tools, the capacitor must be detached from the converter and specialized laboratory equipment must be used. This limits their use in practical applications. Alternatively, *onboard estimation methods* offer a cost-effective solution for capacitor condition monitoring, as they can be implemented directly within the converter without the need to detach the capacitors. Onboard estimation methods can be divided into three main categories [6], as follows.

1) Periodic small-signal ripple [14], [15], [16], [17], [18], [19], [20].
2) Box models, which use data training algorithms [21], [22], [23].
3) Nonperiodic large-signal charging/discharging profile [24], [25], [26], [27].

A. PERIODIC SMALL-SIGNAL RIPPLE-BASED METHODS

In these methods, voltage and current ripples on dc input are used to indirectly estimate the ESR or the capacitance. In study [14], a condition monitoring system for electrolytic capacitors used as dc-link capacitors in front-end rectifier-fed three-phase inverters is proposed, in which both ESR and capacitance are monitored. Sensors directly measure the voltage and current ripples of the capacitors. Then, a Goertzel algorithm is used to extract the low-frequency components and estimate the capacitance. To avoid using current sensors, some condition monitoring systems based on current or voltage injection are proposed in studies [15], [16], [17], [18], [19], and [20]. In study [15], a controlled ac current is injected into the input terminals of an ac–dc PWM converter, causing a voltage ripple on the output. The ESR is calculated using the ac voltage and current components and filters. A simple temperature-sensing circuit is also designed to consider the temperature effect. In studies [16] and [17], the capacitor current is calculated by subtracting the traction inverter's input current from the semiconductor module's input current. They try to estimate the ESR and capacitance to detect the aging of electrolytic capacitors. In study [18], an ac voltage with a lower frequency than the line frequency is injected into the dc-link and the capacitance is calculated through the stored power in the capacitor. A set of training data is used to describe the relationship between the capacitor's power and its corresponding capacitance. In study [19], at no load condition a controlled ac voltage or ac current, with a lower frequency than the line frequency, is injected into the lower side of an ac–dc pulsewidth modulation (PWM) converter, resulting in an ac voltage ripple at the dc output. By extracting the ac voltage, current and power components, the capacitance can be extracted using the recursive least squares (RLS) method. In study [20], a condition monitoring for evaluating the health state of electrolytic capacitors is proposed, in which a regulated ac component is injected in the stator winding of a motor when it is operating in the regenerative mode, which causes a voltage ripple on the output. The capacitance could be estimated from voltage and current ripples using the RLS method. However, these approaches require high-precision, high-bandwidth sensors, which are typically unavailable in standard power converters. In addition, such sensors are costly, making these methods unsuitable for cost-sensitive applications like automotive systems.

B. BOX MODELS

In these methods, the dc-link is considered a box model. The current and voltage are considered as the inputs of the model, and the capacitor parameters can be estimated using data training algorithms [6]. Artificial neural network based methods are used in studies [21], [22], and [23] to estimate the capacitor parameters. The main issue in these methods is to find a suitable training dataset. In other words, various capacitance and load conditions should be studied during the training process to accurately establish the relationship between the inputs (voltage, current, etc.) and the outputs (capacitor parameters), which can influence the precision of the estimation.

C. NONPERIODIC LARGE-SIGNAL CHARGING/DISCHARGING PROFILE

In these methods, the charging/discharging profile of the capacitor during the start-up or shut-down process of the converter is measured to obtain the capacitor parameters. In studies [24] and [25], the capacitance is considered as the lifetime indicator of the capacitor. The dc-link capacitor is discharged through the three-phase stator windings of a motor. There is no need for complex algorithms. Furthermore, the proposed methodology does not interfere with normal converter operation, as it is performed exclusively during the

converter's start-up or shut-down phases. However, the sampling of the current and voltages is critical, thus requiring high precision and high bandwidth sensors. Furthermore, the resistance of the machine changes drastically with temperature. Since the current is calculated using the model of the motor, the changes in the resistor value could affect the results. In study [26], an *LC* resonant network comprising two-phase stator windings of an electrical machine is used to discharge the capacitor, which inevitably generates torque in the load motor. In study [27], an external network consisting of two resistors and two switches is used as a discharging path for the capacitor. This method does not require injecting signal or additional current sensor. However, it is proposed for electrolyte capacitors, which are not suitable for traction inverters due to their low RMS current capabilities.

This article introduces an innovative and cost-effective methodology for evaluating the health state of film capacitors in traction inverters, utilizing capacitance variation as an indirect indicator of their condition. The capacitance variation is determined from the voltage discharge profile obtained during a controlled discharge test performed during the converter's start-up phase.

The proposed solution requires only a minimal number of additional low-cost components, such as a discharge resistor and a low-current switch (e.g., MOSFET or IGBT). The capacitor's voltage discharge profile is measured using the existing dc-link voltage sensor already available in standard traction inverters, eliminating the need for additional sensors and further reducing system complexity and cost. By performing some mathematical manipulation, it is possible to precisely compute the capacitance variation without the need to use calibrated measurement systems or components (i.e., no calibrated discharging resistor is needed). PLECS simulations, along with experimental results, are provided to validate the proposed methodology.

Preliminary results of this work were presented in study [28] over a limited number of operating conditions. Moreover, the accuracy of the proposed method, which is central to its practical applicability, was not addressed. In this work, we expand on those initial findings by presenting additional experimental results that examine the technique under a broader range of operating conditions. Detailed design considerations for the key components are also discussed. Furthermore, this work investigates a critical reliability issue related to the aging of the discharging resistor and switch in the external component network, which was not previously considered.

The structure of this article is as follows. Section II details the proposed condition monitoring test, Section III presents the simulation results, and Section IV provides the experimental results validating the theoretical analysis. Finally, Section V concludes this article.

II. PROPOSED CONDITION MONITORING TEST

To evaluate the aging of a capacitor, the value of its capacitance should be monitored over time. In the proposed solution, the variation in capacitance is used as an indirect indicator of the capacitor's health state. The proposed condition monitoring test should be performed at the start of the converter's life to measure the initial capacitance value and repeated at regular intervals to track capacitance variations over time.

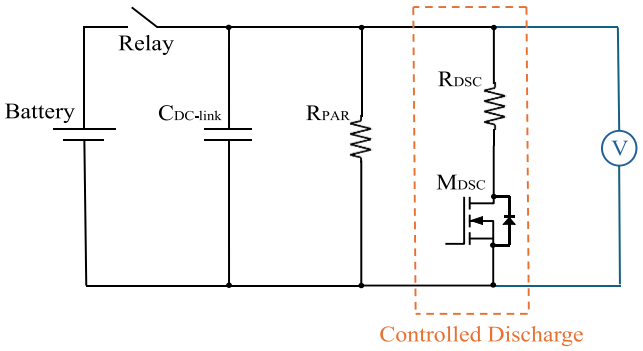

FIGURE 2. Functional electrical schematic of the proposed condition monitoring test circuit showing the inverter's dc-link capacitor connected to the battery using a safety high-voltage relay (or contactor) and the proposed discharge circuit.

A. SCHEMATIC FOR CONDITION MONITORING SYSTEM

The proposed solution monitors the discharge voltage profile of the dc-link capacitor to indirectly estimate its capacitance change over time. The functional schematic of the proposed condition monitoring test circuit is shown in Fig. 2, where $C_{DC\text{-}link}$ represents the main dc-link capacitor, while R_{PAR} accounts for the parallel discharge resistors connected across the capacitor for safety purposes, as well as the parasitic effects of other components (e.g., leakage current from inverter power MOSFETs). The components R_{DSC} and M_{DSC} denote the discharge resistor and the low-current MOSFET, respectively, which form part of the proposed condition monitoring circuit. In addition, the dc-link voltage sensor (already available in standard power converter) labeled "V," is used to measure the voltage profile. A power relay connects the vehicle's battery to the dc-link, allowing the inverter to be safely disconnected from the battery when necessary. It is important to mention that the resistance value of R_{PAR} is much higher than the R_{DSC} that it can be neglected in the discharging test. Moreover, the ESR in film capacitors has a very small value, which is in the range of a couple of mili-ohms. The value of ESR may change as the capacitor ages; however, this variation is in the range of micro-ohms. Therefore, with respect to the R_{DSC}, the value of ESR remains negligible. Thus, R in the (1) to (9) refers to R_{DSC}.

The condition monitoring test steps can be summarized in the flowchart of Fig. 3, which are explained as follows:

1) The dc-link capacitor initially charged at the battery voltage is disconnected from the power source (e.g., vehicle battery) by opening the power relay (usually present for safety reasons). During this phase, all the switches of the power converter are open.
2) $C_{DC\text{-}link}$ starts discharging slowly through R_{PAR}.

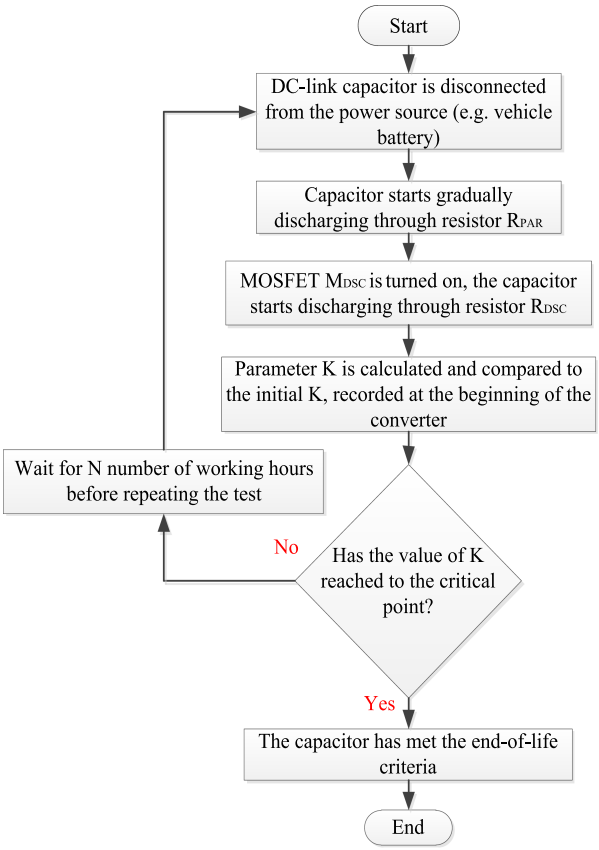

FIGURE 3. Flowchart of the proposed condition monitoring test.

3) The MOSFET M_{DSC} is switched ON, allowing the dc-link capacitor to discharge through R_{DSC}. The discharge voltage is monitored using a voltage sensor (e.g., the same sensor employed to measure the dc-link voltage during the converter's normal operation). The voltage discharging curve is given by the following equations:

$$V_{new}(t) = V_0 e^{\frac{-t}{RC_{new}}}; \qquad V_{aged}(t) = V_0 e^{\frac{-t}{RC_{aged}}} \tag{1}$$

where $V_{new}(t)$ and $V_{aged}(t)$ represent the voltage profile of the new capacitor and the aged one respectively and V_0 is the initial voltage of the capacitor when the discharging MOSFET is turned ON.

4) The measured discharge voltage curve can be integrated over time (by selecting appropriate t_{start} and t_{end}). The coefficient K can be calculated, as shown in the following:

$$K = \int_{t_{start}}^{t_{end}} V_0 e^{\frac{-t}{RC}} dt \tag{2}$$

t_{start} and t_{end} must be chosen in accordance with V_{start} and V_{end}. Fig. 4 shows the voltage profiles in the case of the new capacitor and the aged one, where the area of integration has been highlighted. V_{start} is the value of the capacitor voltage, chosen to start the integration. V_{end} is the value of the voltage at which the integration should be stopped.

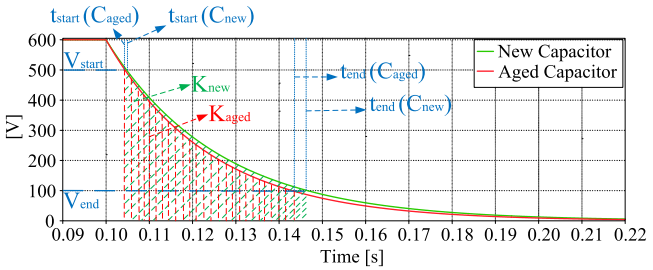

FIGURE 4. Voltage profiles of both new and aged capacitors.

By selecting the values of V_{start} and V_{end}, the values of t_{start} and t_{end} can be calculated accordingly

$$V(t_{start}) = V_{start}. \tag{3}$$

Using (1) and (2), t_{start} and t_{end} can be derived as follows:

$$t_{start} = -RC \ln\left(\frac{V_{start}}{V_0}\right); \quad t_{end} = -RC \ln\left(\frac{V_{end}}{V_0}\right). \tag{4}$$

Two conditions must be considered in these equations. V_{start} must be lower than V_0 and V_{end} must be lower than V_{start}, otherwise the value of t_{start} and t_{end} will be negative based on (3) and (4). Furthermore, the value of t_{end} should be greater than t_{start}. By substituting (4) in (2), K can be obtained as follows:

$$K = V_0 RC \left(e^{\frac{RC \ln\left(\frac{V_{start}}{V_0}\right)}{RC}} - e^{\frac{RC \ln\left(\frac{V_{end}}{V_0}\right)}{RC}} \right). \tag{5}$$

Solving (5) for both new and aged capacitors enable to derive (6) as follows:

$$\frac{K_{new}}{K_{aged}} = \frac{C_{new}}{C_{aged}} \tag{6}$$

where K_{new} is the initial value of the K, recorded at the beginning of the converter's life and K_{aged} is the value obtained from the most recent test. Remarkably, the ratio between the K_{aged} and K_{new} is the same as the ratio of C_{aged} over C_{new} regardless of the value of the capacitor or the discharging resistor.

5) By comparing the "K_{new}," with the value of "K_{aged}," the capacitance variation over time can be assessed.
6) The test will be repeated in regular time intervals until the aged capacitor reaches to the end-of-life criteria, which is assumed to be at 95% of the initial capacitance.

According to the electronic component reliability theory, the failure rate of film capacitors can be explained by a bathtub shaped curve [29], which indicates that at the early stages of working under stress, also called the "infant phase," the failure rate of the capacitor is higher [29], [30]. This is because initial operation exposes hidden weaknesses, such as tiny manufacturing defects, moisture/contamination, or marginal connections, that were not evident in basic tests. The first days of putting stress on the capacitors, the weak units will fail to continue to operate. The duration of this phase may be

different based on the type and model of the film capacitor. After this time period, the useful life of the film capacitor begins, in which the failure rate is at the minimum level, until the capacitor reaches to the end-of-life criteria. Based on this theory, it is beneficial to conduct the condition monitoring test in shorter time intervals during the infant phase. The time interval can be increased after the infant phase of the capacitor is finished. The selection of time intervals for repeating the condition monitoring test may vary according to the characteristics of the film capacitor used in the system, and should be chosen based on the requirements of the application. This article aims at estimating the capacitance variation in a reliable and precise way, and the test can be repeated in any time intervals that has been selected for the application.

The condition monitoring test should be conducted before the converter is started, ensuring that the capacitor's temperature is equal to the ambient temperature, which typically remains within a limited range. Film capacitors are known for their stable capacitance over varying temperatures [31]. However, if significant fluctuations in ambient temperature are expected, a thermal model of the capacitor can be utilized to account for capacitance variations with temperature. For instance, a temperature change of 40 °C may lead to an approximate 1% capacitance shift in the monitored capacitor, as highlighted in study [31]. In the case of thermal equilibrium (i.e., before the starting of the converter), the capacitor temperature matches that of the other converter components, therefore the existing heatsink temperature sensor can be repurposed to track the capacitor temperature as well.

B. SELECTION OF THE DISCHARGING RESISTOR

The following considerations can be made in the selection of the discharging resistor.

1) The resistor value should be high enough to ensure the discharge process lasting long enough to collect the necessary data during the integration period. Specifically, during the integration period a consistent number of samples should be collected to effectively filter out noise. In normal converter operation, the sampling rate is typically one sample per switching period, dictated by the control system. The proposed method does not require oversampling, as with a properly selected resistor, the required data can be easily obtained within the standard sampling frequency.
2) The resistor value also affects the selection of the MOSFET. A higher resistor value reduces the discharge current, allowing the use of a MOSFET with a lower current rating. In addition, the resistor should be sufficiently large so that the MOSFET'S ON-state resistance (which may vary significantly over time) remains negligible during operation.
3) On the other hand, the value of the resistor should be low enough to be able to neglect the current flowing in the parasitic resistor R_{PAR}. If the value of R_{DSC} is too high, the current flowing to R_{PAR} becomes significant, thus affecting the accuracy of the test. It must also be noted that the current flowing in R_{PAR} cannot be effectively compensated as this resistor may change significantly over time (e.g., due to the aging of the semiconductors).
4) The resistor must have a sufficiently high power rating to minimize temperature rise during the test, thus preventing excessive component aging and avoiding any significant change in its resistance value due to temperature increase.

All these considerations should be taken into account during the designing process. The value of the resistor should be selected in a way that all the requirements of the system are satisfied.

C. AGING OF THE CONTROLLED DISCHARGING SYSTEM

The discharge test is performed intermittently throughout the converter's lifetime and produces minimal heat in the resistor, so its impact on the resistor aging remains limited. However, gradual changes in resistance over time may still occur, potentially introducing errors in the proposed methodology. Equation (5) indicates that the value of K_{aged} is directly related to the value of the resistor. For instance, if the resistor value increases by 1% , K_{aged} would be overestimated by 1% , and (6) will become as follows:

$$\frac{K_{\mathrm{new}}}{1.01 \times K_{\mathrm{aged}}} = \frac{C_{\mathrm{new}}}{C_{\mathrm{aged}}}. \tag{7}$$

This will impact the evaluation of C_{aged} which would be overestimated by 1% . Therefore, selecting a resistor that can remain constant over time is crucial.

A similar analysis can also be done for the voltage sensor, since it may start having an offset that changes over time. A possible offset from the sensor would lead to a shift in the measured voltages V_{start} and V_{end} in (5). Equation (5) can be written as follows:

$$K = RC\left(V_{\mathrm{new}} - V_{\mathrm{aged}}\right). \tag{8}$$

For instance, if the measurement error is 1% , solving (8) gives the following error in K:

$$K = RC(1.01)\left(V_{\mathrm{new}} - V_{\mathrm{aged}}\right). \tag{9}$$

Equation (9) shows that 1% of measurement error would result in 1% error in calculation of K, and (7) can also be considered true in this situation. However, if there is an additive offset error (i.e., the same offset is added to both V_{start} and V_{aged}), it will cancel out in (8), and K will remain unchanged. Therefore, it is safe to assume that the proposed methodology is only affected when the offset changes over time.

On the other hand, the aging of the power switch is not critical, since its conduction resistance is negligible compared to the one of the discharge resistor. It is important to mention that the test will be conducted at the start-up process of the inverter, when its temperature is still the same as the ambient temperature. Furthermore, to monitor the health of the capacitor, it is not necessary to perform the test multiple times a day, since the aging of the capacitor takes years to happen.

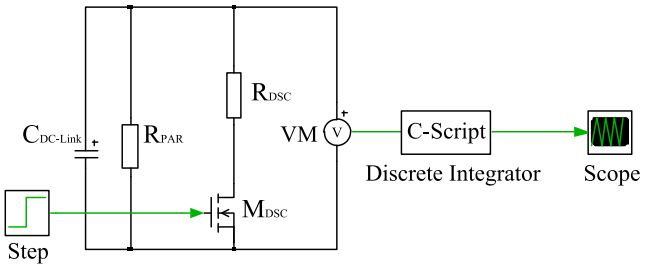

FIGURE 5. PLECS implementation of the controlled discharging test.

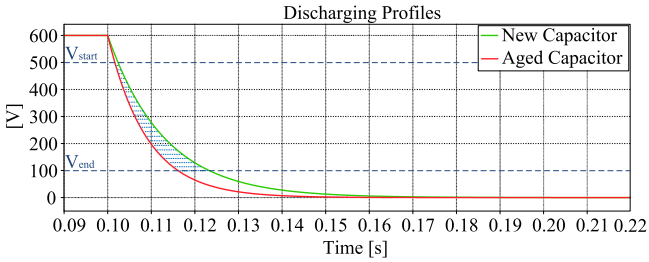

FIGURE 6. Difference between the voltage profiles of the new capacitor and the aged one.

TABLE 1. Simulation Results for Different Combinations of Capacitors and Discharging Resistors

C_{new} (μF)	C_{aged} (μF)	R_{DSC} (Ω)	K_{new}	K_{aged}	C_{aged}/C_{new}	K_{aged}/K_{new}	Error (%)
260	*240*	*100*	*10.406*	*9.602*	*0.923*	*0.9227*	*0.041*
260	240	200	20.802	19.214	0.923	0.9236	0.057
260	*240*	*300*	*31.198*	*28.796*	*0.923*	*0.9230*	*0.001*
130	120	100	5.175	4.783	0.923	0.9242	0.121
130	*120*	*200*	*10.366*	*9.557*	*0.923*	*0.9219*	*0.127*
130	120	300	15.591	14.389	0.923	0.9229	0.019
65	*60*	*100*	*2.602*	*2.406*	*0.923*	*0.9248*	*0.187*
65	60	200	5.195	4.803	0.923	0.9245	0.154
65	*60*	*300*	*7.787*	*7.199*	*0.923*	*0.9245*	*0.154*

TABLE 2. Simulation Results for Different Resistor Values at a Reduced Sampling Rate of 1 kHz

C_{new} (μF)	C_{aged} (μF)	R_{DSC} (Ω)	K_{new}	K_{aged}	C_{aged}/C_{new}	K_{aged}/K_{new}	Error (%)
130	*120*	*100*	*103.907*	*96.067*	*0.923*	*0.9245*	*0.154*
130	120	200	208.112	191.933	0.923	0.9222	0.095
130	*120*	*300*	*311.817*	*287.798*	*0.923*	*0.9229*	*0.019*

Therefore, the test can be done in regular time intervals (e.g., once a week or after a specified number of operating hours) with the discharging circuit only being used for a couple of milliseconds. Under these conditions, the aging of the resistor and other test components is minimal.

III. SIMULATION RESULTS

The proposed condition monitoring test has been preliminary validated in PLECS, where different combinations of discharging resistor and dc-link capacitor are tested in an ideal operating condition. The implemented test circuit is shown in Fig. 5, where $f_{sampling} = 20$ kHz, $R_{PAR} = \infty$. The initial voltage of the capacitor is set to 600 V. The capacitor voltage is measured and integrated using a discrete-time integrator implemented with a C-Script block.

The difference between the discharge voltage profiles of the new and aged capacitors should be maximized to ensure adequate measurement sensitivity. Fig. 6 shows the difference between voltage discharging profiles in the case of new (120 μF) and old (100 μF) capacitors using a 200 Ω resistor.

The greater the measurement sensitivity, the more accurate the results will be. Therefore, the integration is performed when the measurement sensitivity is at the highest, as shown in Fig. 6 in the highlighted area. In these simulation test, V_{start} is selected to be 500 V and V_{end} is 100 V, which can guarantee the required sensitivity. Although V_{start} and V_{end} are the same for both capacitors, it must be noted that t_{start} and t_{end} are different for the two capacitors.

Table 1 summarizes the results of the simulations for different tests. Three different capacitor values were tested with three discharge resistances of 100, 200, and 300 Ω, respectively. The results clearly show that the ratio $\frac{K_{aged}}{K_{new}}$ is always equal to $\frac{C_{aged}}{C_{new}}$. This confirms that variations in the capacitor or discharge resistor values do not influence the test outcome, and (6) remains valid under all conditions.

An estimation error arises in the simulation tests due to the discretization introduced by the discrete integrator that is operated at 20 kHz. Notably, the estimation error decreases as the capacitor value increases (i.e., longer time constant). Although increasing the sampling frequency can further reduce this error, it remains below 0.2% even at its maximum, underscoring the high accuracy of the proposed technique.

The simulations have been repeated at a lower sampling rate to make sure the methodology can be used in applications that operate in lower sampling frequencies. Table 2 shows the results of the same simulations, when $f_{sampling} = 1$ kHz.

Table 2 demonstrates that the results obtained at a lower sampling rate remain consistent with those recorded at 20 kHz, confirming the robustness of the proposed methodology. Consequently, the method can also be applied to systems operating with lower sampling frequencies, provided that the number of acquired samples is sufficient to accurately reconstruct the capacitor's discharge curve.

The simulations presented so far were carried out under ideal conditions, assuming noise-free voltage measurements. To evaluate the performance of the proposed solution under more realistic conditions, a white noise component with an amplitude of 5% was added to the capacitor voltage signal in PLECS, and the tests summarized in Table 2 were repeated with a sampling frequency of $f_{sampling} = 20$ kHz. The results,

TABLE 3. Simulation Results When There Is 5% Noise on the Measured Voltage

C_{new} (μF)	C_{aged} (μF)	R_{DSC} (Ω)	K_{new}	K_{aged}	C_{aged}/C_{new}	K_{aged}/K_{new}	Error (%)
130	*120*	*100*	*5.24*	*4.78*	*0.923*	*0.9122*	*1.178*
130	*120*	*200*	*10.414*	*9.587*	*0.923*	*0.9205*	*0.269*
130	*120*	*300*	*15.678*	*14.501*	*0.923*	*0.9249*	*0.197*

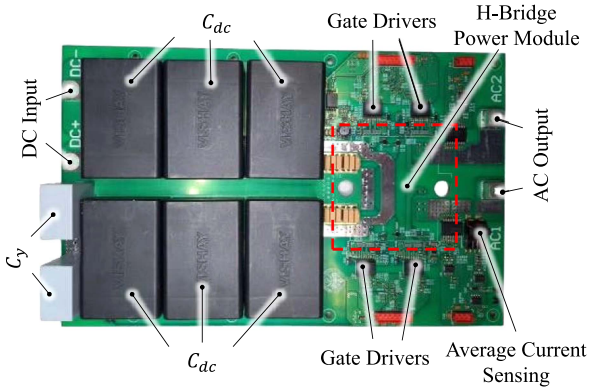

FIGURE 7. Experimental H-bridge converter.

reported in Table 3, indicate that although the estimation error slightly increases in the presence of noise (especially if a low discharging resistor is used, where a limited number of samples is collected), the proposed method maintains good accuracy when the discharge resistor is appropriately selected.

Tables 2 and 3 indicate that decreasing the value of the discharging resistor will result in a larger estimation error. With smaller value of the resistance, the capacitor will be discharged too fast, which leads to having a lower number of data samples in the discharging profile thus resulting in a higher estimation error.

IV. EXPERIMENTAL RESULTS

A. EXPERIMENTAL TEST RIG

The experimental test rig used to validate the proposed technique is shown in Fig. 7. The setup consists of an 800 V, 20 kVA, H-bridge SiC converter that was originally designed to work as a rotor exciter for automotive applications.

For convenience, one of the four switches in the H-bridge is employed as the discharging switch (M_{DSC}), to provide a path for discharging the dc-link capacitor through R_{DSC}.

The power schematic of the H-bridge converter is shown in Fig. 8, where R_{DSC} is connected between output 1 and the positive pole of the dc-link, while the MOSFET M_2 is used as the discharging switch. The resistor R_{PAR} is not included in this schematic, since R_{PAR} value is much higher than R_{DCS} that it is neglected.

In the proposed tests, R_{DSC} is set to 150 Ω, and then 200 Ω to compare the estimation errors in both situations. The capacitance value of the dc-link is 150 μF, then a 10 μF is removed in the first step, which is called C_1, and then another 10 μF

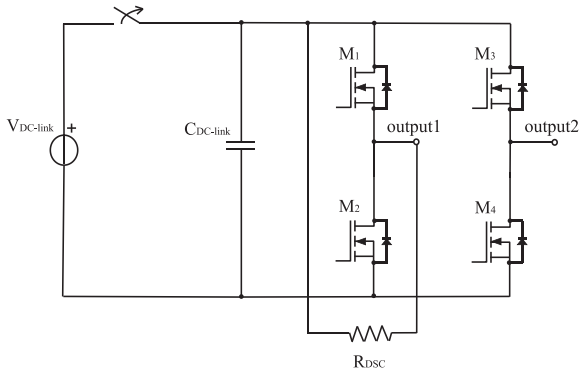

FIGURE 8. Schematic of the experimental test rig, where a MOSFET (M_2) is used as the discharging switch.

TABLE 4. Summary of Experimental Results

R=150 Ω	LCR Meter Capacitance Values (μF)	K V_{start}=500V V_{end}=100V	Estimation Error (%)	K V_{start}=400V V_{end}=200V	Estimation Error (%)
DC-link	*151.99*	*4.2397*	*-----*	*2.0895*	*-----*
DC-link-C_1	*141.94*	*3.9478*	*–0.297*	*1.9601*	*0.452*
DC-link-(C_1+C_2)	*131.91*	*3.686*	*+0.174*	*1.8217*	*0.451*
R=200 Ω	LCR Meter Capacitance Values (μF)	K V_{start}=500 V V_{end}=100 V	Estimation Error (%)	K V_{start}=400 V V_{end}=200 V	Estimation Error (%)
DC-link	*151.99*	*5.5840*	*-----*	*2.7868*	*-----*
DC-link-C_1	*141.94*	*5.2133*	*–0.029*	*2.5987*	*–0.147*
DC-link-(C_1+C_2)	*131.91*	*4.8459*	*–0.007*	*2.4085*	*–0.424*

capacitor, called C_2, is removed in the second step. In this way the capacitance value will be decreased from approximately 150 to 140 μF and then to 130 μF.

The discharging voltage profile is measured using the V_{bus} measurement system of the converter, which comprises a voltage divider connected to an isolated operational amplifier. The output of the operational amplifier is sampled by the 12-bit MCU's ADC at 20 kHz, which matches the switching frequency of the converter during normal PWM operation.

B. EXPERIMENTAL RESULTS

Table 4 shows a summary of the experimental results with two different values for the discharging resistor. For each value of the discharging resistor, two capacitors have been removed from the dc-link in two steps, to emulate the aging of the capacitor.

The exact capacitance values of the capacitors are measured with an *LCR* meter, then the capacitance values are estimated with the proposed methodology. The value of K is calculated in two conditions, in the first one $V_{start} = 500$ V and $V_{end} = 100$ V, while in the second one $V_{start} = 400$ V and $V_{end} = 200$ V.

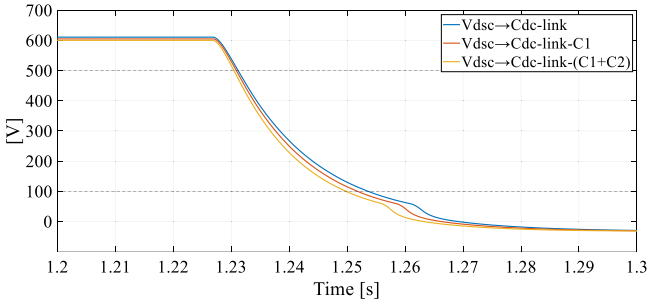

FIGURE 9. Voltage discharge profiles of three capacitors, measured with the H-bridge embedded voltage sensor, when $R_{DSC} = 200\ \Omega$. The discharge voltage profiles are integrated between $V_{start} = 500$ V and $V_{end} = 100$ V.

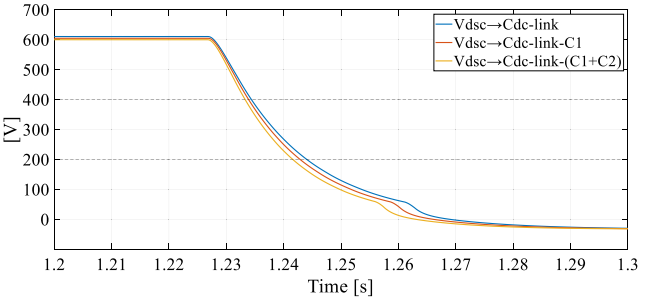

FIGURE 10. Voltage discharge profiles of three capacitors, measured with the H-bridge embedded voltage sensor, when $R_{DSC} = 200\ \Omega$. The discharge voltage profiles are integrated between $V_{start} = 400$ V and $V_{end} = 200$ V.

Fig. 9 shows the discharge voltage profiles of the capacitors (i.e., 150, 140, 130 μF) measured by the MCU. The capacitors are precharged to 600 V, a typical voltage in EV battery systems, using an external dc power supply.

Then, the dc-link is disconnected from the power supply, and the condition monitoring test is performed by turning ON the MOSFET M_2, and by integrating the discharging voltage profile. In this first test, the integral is calculated between $V_{start} = 500$ V and $V_{end} = 100$ V, thus providing the necessary measurement sensitivity.

The obtained values of K are reported in Table 4. The ratio $\frac{K_{aged}}{K_{new}}$ for the first and second steps are 0.9336 and 0.8678, respectively, which matches $\frac{C_{aged}}{C_{new}}$, thereby confirming the validity of (6). Comparing the *LCR* meter values and these ratios according to Table 4 shows that the estimation error in this case is almost negligible.

Regarding Fig. 9, it must be observed that the voltage sensor of the converter shows a nonlinearity when the measured voltage drops below 50 V. This behavior is typical of dc-link voltage sensors in power converters, which are not designed for low-voltage operation. Therefore, the value of V_{end} must be appropriately chosen to exclude the nonlinear region from the integral calculation, preventing it from influencing the test results. Even when using a more advanced sensor capable of maintaining linearity across the entire measurement range, integrating the low-voltage region should still be avoided due to the poor signal-to-noise ratio at low voltages. For instance, measuring a voltage of 10 V with a sensor that has a noise level of 5 V would produce highly unreliable readings.

In Fig. 10, the same test is repeated using a reduced voltage integration range, with $V_{start} = 400$ V and $V_{end} = 200$ V. In this case, the number of samples decreases, leading to reduced accuracy in the results. For this test, the values of K are also presented in Table 4. Ratio $\frac{K_{aged}}{K_{new}}$ for the first and second capacitance steps are 0.9325 and 0.8642, respectively, which results in estimation error of –0.147% and –0.424% . These results indicate that reducing the integral limits will result in a slightly lower accuracy, since it decreases the number of data samples. However, even in this condition, the results are still accurate, and the estimation error is acceptable.

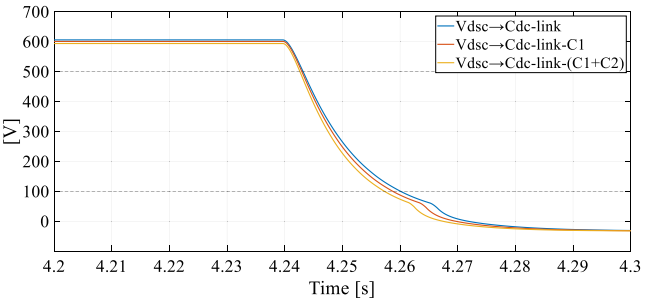

FIGURE 11. Voltage discharge profiles of three capacitors, measured with the H-bridge embedded voltage sensor, when $R_{DSC} = 150\ \Omega$. The discharge voltage profiles are integrated between $V_{start} = 500$ V and $V_{end} = 100$ V.

To evaluate the effect of the resistance value of the discharging resistor, the experiment is repeated with a 150 Ω resistor. Fig. 11 indicates the discharging voltage profiles of the three capacitors. In this case, based on Table 4, the ratio $\frac{K_{aged}}{K_{new}}$ for the first and second steps are 0.9311 and 0.8694, respectively. The capacitance values of emulated aged capacitors can be calculated based on (6), and the estimation errors with respect to the values measured by *LCR* meter are −0.297% and 0.174% . Comparing Fig. 9 with Fig. 11 proves that the capacitor will be discharged faster, if R_{DSC} is reduced. Therefore, with a shorter discharging time and the same sampling rate, lower number of data samples are collected for the calculation, which leads to lower accuracy. This verifies the results of the simulations in PLECS, and emphasizes on the importance of choosing the appropriate resistance during component selection.

The same experiment is repeated in another case, where the integral is calculated between 200 and 400 V. According to Table 4, $\frac{K_{aged}}{K_{new}}$ ratios for both steps are equal to 0.9325 and 0.8642. In this case, the estimation errors for the two capacitance steps are 0.452% and 0.451% , respectively. It can be seen that this case shows the highest estimation error. This is because the lower resistance value as well as smaller integral range leads to collecting lower data samples to calculate the value of K, which results in a higher estimation error.

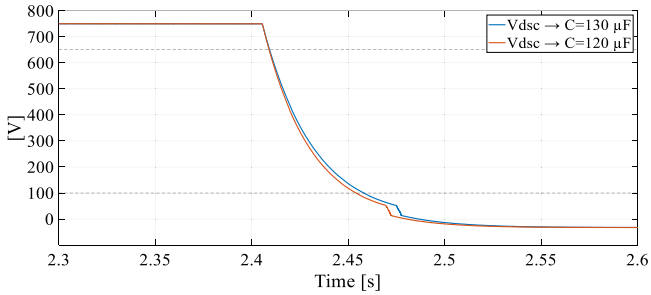

FIGURE 12. Voltage discharge profiles of both 130 and 120 μF capacitors measured with the H-bridge embedded voltage sensor. The discharge voltage profiles are integrated between $V_{start} = 650$ V and $V_{end} = 100$ V.

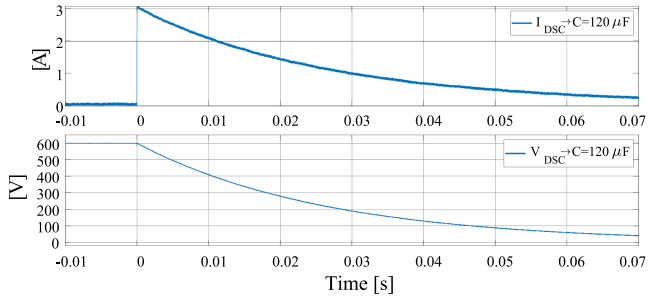

FIGURE 13. Voltage and current discharge profiles of the 120 μF capacitor measured with the oscilloscope.

To further confirmation of the methodology, an additional test is conducted, in which the capacitances and the voltage integration range are changed. In this additional test, the dc-link capacitance is approximately 130 μF and then it is reduced to 120 μF to emulate the aging of the capacitor, while the discharging resistor is 200 Ω. In this test, the initial voltage of the capacitor is considered to be 750 V, while the integration voltage range is set between $V_{start} = 650$ V to $V_{end} = 100$ V. Fig. 12 shows the discharging profiles of both capacitors. The measured K_{new} and K_{aged} are 14.3799 and 13.2700, respectively. $\frac{K_{aged}}{K_{new}}$ is equal to 0.9228 thus corresponding to an estimation error of 0.0283% . It can be seen that in this case the estimation error is almost negligible, since the integral range is wide and the resistor value is high enough to provide a great accuracy in the test.

Fig. 13 shows the discharging voltage and current profiles, measured with an oscilloscope, for the 120 μF capacitor in the additional test. In this case, there is no voltage nonlinearity caused by the embedded voltage sensor. In addition, the peak discharge current is approximately 3 A. This is particularly significant, as it highlight that a low-current discharge switch can be used, offering substantial cost benefits.

V. CONCLUSION

This article presents a *robust and cost-effective* methodology for assessing the health of film capacitors in power converters, requiring only a low-current switch and a resistor. The proposed technique has been analytically and experimentally validated under various operating conditions, demonstrating to be highly accurate in measuring any capacitance variation with a high noise immunity. One of the main strengths of the proposed technique is that there is no need for a precise resistor or a calibrated voltage sensor, as long as their characteristics remain constant over time. A standard, and relatively low-accuracy voltage sensor (also not perfectly linear) used for dc-link voltage measurement is sufficient. Thanks to the integration of the voltage over a large number of samples the impact of the measurement noise (i.e., white noise) can be virtually eliminated. It must be highlighted that the proposed test does not aim at estimating the absolute capacitance value but aims at evaluating its variation.

In practical applications, an end-of-life criterion for film capacitors is typically defined when the capacitance falls below 95% of its initial value. The proposed condition monitoring test should be performed periodically to monitor capacitor health. The voltage integration should always be conducted over the same range, with the initial voltage set sufficiently below the battery's nominal voltage to allow testing even when the battery is not fully charged. When capacitance approaches a critical threshold, the system can alert the user, enabling timely maintenance and reducing the risk of unexpected component failure. Since a sudden failure of the dc-link capacitor could be costly and potentially life-threatening, the minor expenses associated with the additional hardware components required for this technique are a worthwhile investment.

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