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29 November 2026

SET: Substrate Extraction Tool for Predicting Substrate Noise in SOI Smart Power ICs

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***Abstract*—Substrate noise propagation is a critical issue in smart power SOI design, as the switching noise generated by power circuits can couple with sensitive analog circuitry causing malfunctions. This work presents SET, a lightweight tool for extracting SPICE-like netlists to provide a rapid estimation of aggressor-victim coupling through the substrate. By implementing a local mesh refinement, SET reduces the simulation time while preserving accuracy. Validation on elementary test structures shows good agreement with commercial tools in terms of spreading resistance and substrate coupling, making SET a practical solution for early-stage architecture exploration and design definition.**

***Index Terms*—Smart Power ICs, substrate coupling, substrate modeling, self-immunity, integrated power circuits.**

I. Introduction

Silicon On Insulator (SOI) processes are widely adopted in smart power ICs to integrate high-voltage power transistors with low-voltage circuitry. Despite improved isolation compared to bulk technologies, SOI smart power ICs still suffer from substrate coupling issues. The fast switching of on-chip power transistors, which typically occupy a significant area, inject large currents through the buried oxide into the common substrate, where they propagate and induce voltage variations in analog circuits, as shown in Fig. 1. As a result, system-level malfunctions may occur, e.g., offset in band-gap references due to substrate noise demodulation [1]–[3] or high conducted electro magnetic interference due to noise from on-board DC-DC converters [4]. To address such issues, substrate coupling must be assessed from early design stages to define layout partitioning and effective grounding and isolation strategies.

Substrate modeling has been widely studied in mixed-signal bulk-isolated ICs, where digital circuitry is typically the dominant aggressor [5]. Given the distributed and layout-specific characteristics of substrate coupling, these effects are commonly analyzed using 3D discretization techniques, such as Finite Element (FEM) or Finite Difference Method (FDM). However, general-purpose FEM tools are not specifically intended for substrate modeling, meaning that they do require a manual definition of the geometry to be simulated. Conversely, substrate extraction tools embedded in commercial CAD tools are intended for post-layout usage, where a layout-vs-schematic is already available, which is often not the case during design exploration.

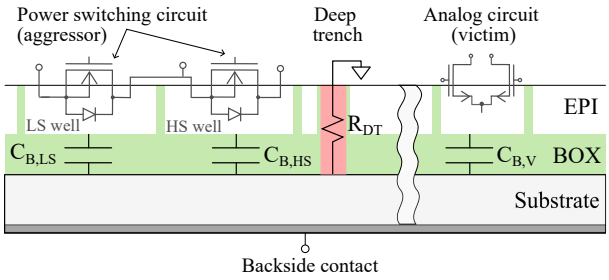

Fig. 1. Cross-section of an SOI smart power IC.

As far as substrate modeling for smart power ICs is concerned, prior research focused mainly on bulk technologies, where minority carriers should be accounted for [6], [7]. Conversely, only a few works addressed substrate modeling in smart power SOI. Amongst them, [8] proposed a simplified π-model for the handle wafer resistance. Despite the ease of integration in the design flow, it does not account for the voltage gradient nearby the injection point. In [9], a model based on DPI measurements and fitting was proposed, but it requires dedicated measurement for each test structure, which limits its applicability. To sum up, a substrate extraction tool tailored for SOI processes, capable of operating on preliminary layouts with low computational effort, is still lacking.

This paper introduces SET, a Substrate Extraction Tool for smart power SOI processes, targeting the assessment of substrate coupling from early design stages. The preliminary architecture and validation on elementary structures is discussed in this work, posing the basis for future developments of the tool. The paper is organized as follows. Sect. II introduces the FDM discretization model, and the SET discretization algorithm is described in Sect. III. Validation results are reported in Sect. IV, with conclusions in Sect. V.

II. Substrate FDM model

To model the substrate coupling in an SOI-isolated IC, FDM can be used to discretize the substrate beneath the Buried Oxide Layer (BOX) into a set of parallelepipeds, as shown in Fig. 2(a). While FEM includes complex meshing to handle irregular geometries, FDM exploits a cartesian grid onto which the rectangular layout geometries can be directly

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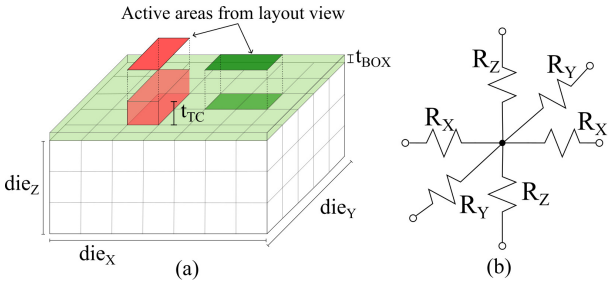

Fig. 2. (a) 3D structure discretized according to FDM model, and (b) electrical equivalent of elementary parallelepiped.

mapped, resulting in a better trade-off between accuracy and computational cost compared to FEM.

The substrate is assumed to be uniformly doped, meaning that its resistivity (ρ_{SUB}) is constant. With ρ_{SUB} in the 1 to $20\,\Omega\cdot\mathrm{cm}^{-1}$ range, the substrate cutoff frequency is 7.5-150 GHz [5]. Recalling Fig. 1, the rise/fall time associated with the switching of integrated power transistors is typically higher than 1 ns, meaning that the bandwidth of the aggressor source is below 350 MHz. Thereby, the substrate can be considered as purely resistive. The equivalent electrical model associated with each parallelepiped the substrate is discretized into is shown in Fig. 2(b). It comprises six star-connected resistances, between the parallelepiped center and the center of the top/bottom/left/right/front/back faces. The value of the resistance along the x-axis (R_{X}) is evaluated as

$$R_{\mathrm{X}} = \frac{1}{2}\rho_{\mathrm{SUB}}\frac{step_{\mathrm{X}}}{step_{\mathrm{Y}}\cdot step_{\mathrm{Z}}}, \tag{1}$$

where $step_{\mathrm{X-Z}}$ is the parallelepiped size along the X-Z dimension. The R_{Y},R_{Z} values can be obtained similarly.

In addition, the substrate must be contacted in correspondence of aggressors, victims and substrate ties. Thus, capacitive and resistive contacts are considered to connect the substrate resistive mesh to the remainder of the circuit. The former models the capacitive coupling through the BOX, as for the aggressor and victim wells in Fig. 1 ($C_{\mathrm{B,LS}}, C_{\mathrm{B,HS}}, C_{\mathrm{B,V}}$), while the latter models a deep-trench contacts used to bias the substrate or as guard rings (R_{DT}). In both cases, the 2D input geometry is discretized into rectangles using the same grid exploited for the substrate. For resistive contacts, the vertical resistance associated with each rectangle is

$$R_{\mathrm{CONT}} = \rho_{\mathrm{TC}}\frac{t_{\mathrm{TC}}}{stepX\cdot stepY}, \tag{2}$$

where ρ_{TC} (t_{TC}) is the resistivity (thickness) of the deep trench contact. Similarly, the BOX capacitance associated with each parallelepiped is

$$C_{\mathrm{CONT}} = \varepsilon_0\varepsilon_{\mathrm{R,BOX}}\cdot\frac{stepX\cdot stepY}{t_{\mathrm{BOX}}}, \tag{3}$$

where t_{BOX} is the BOX thickness and $\varepsilon_{\mathrm{R,BOX}}$ its relative dielectric constant. As a result, the overall $C_{\mathrm{B,LS}}$ capacitance (R_{DT} resistance) is modeled in SET by placing as many capacitances or resistances in parallel as the number of parallelepipeds beneath the area. Another boundary condition can be set at the backside surface of the chip to account for its connection to an exposed pad once it is encapsulated. For the sake of simplicity, the backside is modeled as a resistive contact with resistivity ρ_{BS} and thickness t_{BS}. Thus, each parallelepiped whose bottom face is in contact with the backside is assigned a contact resistance evaluated as in (2).

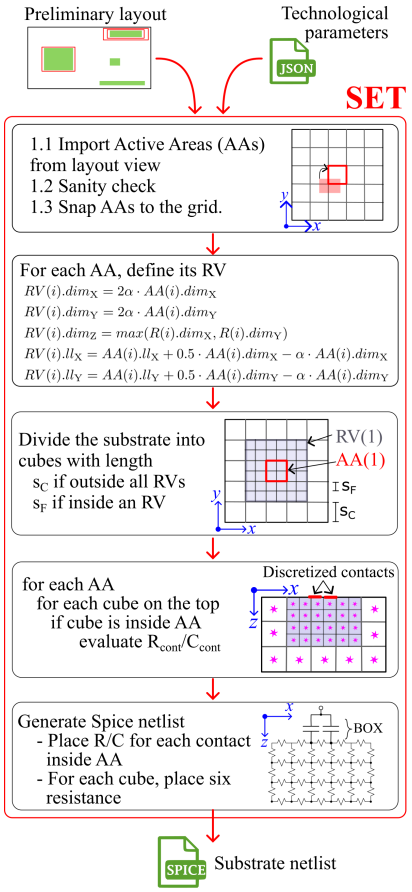

Fig. 3. Flowchart of the discretization algorithm in SET.

III. SET DISCRETIZATION ALGORITHM

Given the FDM substrate model shown in Fig. 2(a), the aim of SET is to extract a SPICE-like netlist that includes both the resistive network of the discretized parallelepipeds and the capacitive/resistive contacts. Once the substrate netlist has been generated, simulations including the remainder of the circuit can be carried out, allowing one to assess the substrate coupling between different blocks.

The flowchart of the algorithm implemented in SET is shown in Fig. 3, and it includes five steps. The tool takes as input a set of technology parameters, including die dimensions, ρ_{SUB}, ρ_{TC} and t_{BOX}, from a JSON file. Concerning the IC layout, a simplified version identifying the aggressor/victim wells and the substrate ties is sufficient, meaning that the full detailed IC layout is not mandatory.

In the first step, the layout is imported as a set of rectangular active areas ($AA(i)$). A sanity check then performed on the

TABLE I
STRUCTURE PARAMETERS

Symbol	Parameter	Value
$die_{X,Y,Z}$	Die dimensions (XYZ)	$2\,\text{mm} \times 2\,\text{mm} \times 0.7\,\text{mm}$
ρ_{SUB}	Substrate resistivity	$2\,\Omega \cdot \text{cm}^{-1}$
ρ_{TC}, ρ_{BS}	Contact and backside resistivity	$0\,\Omega \cdot \text{cm}^{-1}$
t_{BOX}	BOX thickness	300 nm
t_{TC}	Trench thickness	5 µm

TABLE II
ACCURACY VS. SIMULATION TIME.

	100 µm contact		50 µm contact	
Tool	**Error**	**Simulation time**	**Error**	**Simulation time**
EM field solver	0%	6.5 min	0%	6.5 min
TCAD	-6%	36 min	-22%	16 min
SET	+7%	6 min	+15%	1.5 min

imported geometries, which are snapped to the mesh grid. Thus, each active area is discretized as shown in Fig. 2(a) into an integer number of parallelepipeds. In the second step, a mesh refinement volume ($RV(i)$) is associated to each area to encompass both the snapped geometry and its surroundings. The refinement volume keeps the same aspect ratio of the related $AA(i)$, but with dimensions scaled by a factor α.

The substrate is then discretized into cubes. Outside all refinement volumes, a coarse mesh step (s_C) is used for $step_{X-Z}$. Conversely, inside each $RV(i)$, the grid is refined using a fine step (s_F), allowing a more accurate modeling of regions where the voltage potential is expected to vary the most. In the fourth step, substrate contacts are discretized by identifying all parallelepipeds beneath each active area and assigning the corresponding value evaluated using (2) or (3).

Finally, the extracted SPICE netlist is generated. Each node is labeled according to its physical position in the 3D structure, expressed as a set of three integer coordinates. All nodes remain internal to the netlist except those associated with the imported $AA(i)$ areas, meaning that the external interface only includes the net labels assigned to the corresponding contacts.

IV. VALIDATION RESULTS

To assess the accuracy and the simulation time of SET, preliminary validation was carried out on elementary structures to compare results from SET with those from commercial tools. Specifically, an FEM solver suited for Electro-Magnetic (EM) field analysis and a Technology Computer-Aided Design (TCAD) tailored for semiconductor processes and devices were employed. The parameters of simulated structures are reported in Tab. I.

A. Spreading resistance

The first validation structure is shown in Fig. 4(a) and consists of a backside contact and a centered top contact of variable size. In this case, the substrate can be modeled as an equivalent spreading resistance (R_{SPREAD}) between the two contacts, with extracted values shown in Fig. 4(b)

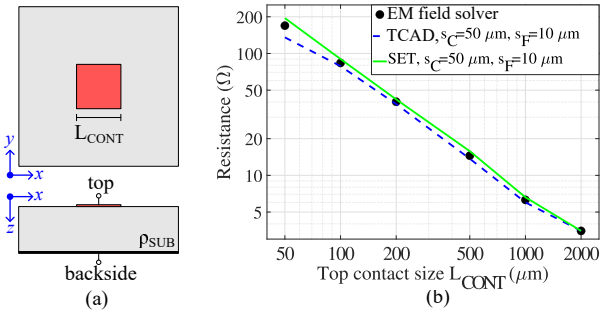

Fig. 4. (a) Simulated structure and (b) extracted spreading resistance by different tools for the one-top contact.

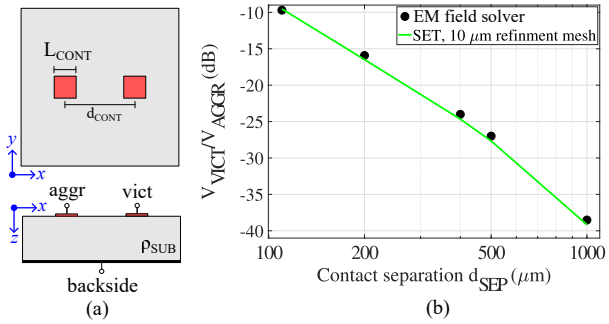

Fig. 5. (a) Two-contacts structure and (b) corresponding results in terms of aggressor to victim transfer function.

for EM field solver (circle), TCAD (cross) and SET (no markers). For L_{CONT}=2 mm, all tools estimate a substrate resistance of 3.5 Ω, consistent with the analytical solution for an homogeneous parallelepiped. As L_{CONT} decreases, discrepancies increase. With the EM field solver, the mesh is automatically refined near the top contact during iterations until a target convergence tolerance of 1% is achieved. Reducing the target error to 0.2% results in a 0.28 % discrepancy for L_{CONT}=100 µm, but at the cost of threefold increase of simulation time. In the TCAD tool, no adaptive mesh was used, and a minimum step size as that in SET. Results from SET and the TCAD tool approach those from EM field solver provided that the mesh step is sufficiently low, as shown in solid line for s_C=25 µm. Overall, SET leads to results closer to those from the EM solver, especially for small L_{CONT}.

Simulation time and accuracy were compared using the EM field solver as a reference and reported in Tab. II for L_{CONT}=50,100 µm. For the TCAD tool and SET, identical mesh parameter, i.e., s_C=50 µm and s_F=10 µm, were used. For L_{CONT}=100 µm, they both achieved the same accuracy, but SET was six times faster. Conversely, for L_{CONT}=50 µm, accuracy degrades for both tools, but SET remained the fastest.

B. Two top contacts structure

The single top-contact configuration is not representative of the target application, i.e., substrate noise coupling between an aggressor and a victim. Therefore, two identical, aligned 100 µm × 100 µm contacts separated by varying distances

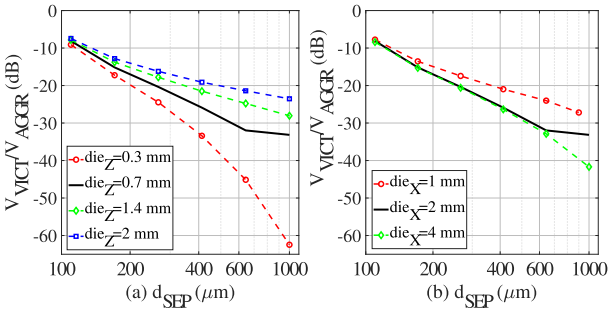

Fig. 6. Sweep of (a) die thickness and (b) die width for the two-contact structure shown in Fig. 5(a).

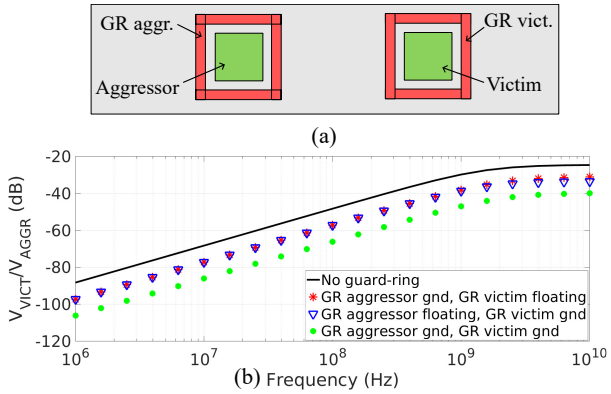

Fig. 7. (a) Two-contacts structure with guard-rings and (b) corresponding results in terms of aggressor to victim transfer function as a function of guard rings connection.

(d_{CONT}) were considered, as shown in Fig. 5(a). A current excitation was applied between the aggressor and backside contacts, and the ratio between victim and aggressor voltages was evaluated in the EM field solver and SET. The results are shown in Fig. 5(b), showing an exponential decrease of the coupling with d_{CONT}. SET shows good agreement with the EM field solver (circle marker), with a maximum deviation of 0.6 dB with a fine 10 µm mesh, while keeping a comparable simulation time.

SET also allows one to assess the impact of physical parameters on substrate coupling. Starting from the reference values in Tab. I, the die thickness (die_{z}) and width ($die_{\mathrm{X}} = die_{\mathrm{Y}}$) were swept, as shown in Fig. 6(a) and (b), respectively. While all curves agree with the reference one (solid line) for low d_{SEP}, larger variations occur when $d_{\mathrm{SEP}} >> d_{\mathrm{CONT}}$. With the backside metalized, and thus equipotential, reducing the substrate thickness increases the current flowing from the aggressor directly to the backside, as shown by circle markers. Conversely, varying the substrate width and length has a limited impact around 5 dB.

C. Isolation structures

In previous cases, top contacts were assumed to be ideal resistive contacts. However, as shown in Fig. 1, aggressor and victim are capacitively coupled to the substrate. To this end, the structure was modified as shown in Fig. 7(a), with the aggressor and victim capacitively coupled to the substrate. In addition, 20 µm-wide substrate ties separated by 20 µm were placed around each contact to investigate the effect of a guard ring. These deep-trench active areas were modeled as ideal resistive contacts. Using SET, the transfer function is that of a first-order high-pass filter, as shown in Fig. 7(b). Connecting the guard ring near the aggressor (star) or the victim (triangle markers) reduces the transfer function magnitude by about 10 dB compared to floating trenches (solid line), while connecting both guard rings provides 15 dB reduction. The phase is around 90°(0°) for frequencies where the capacitive coupling is predominant (negligible), i.e., below (above) 1 GHz.

V. Conclusion

This work proposes SET, a lightweight tool to extract SPICE-like netlists for substrate coupling analyses. By implementing local mesh refinement, SET achieves results consistent with commercial tools, while avoiding the need for manual 3D geometry definition. This makes SET suitable for integration with widely used CAD toolchains. As the simulation time cost is expected to increase for large layouts, adaptive mesh strategies and netlist reduction can be adopted to limit the netlist size without compromising accuracy. In the future, SET will be applied to representative design to assess its effectiveness in a practical smart power IC.

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