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(Article begins on next page)

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A Comparison of Low-Complexity Iterative Algorithms for Adaptive Active Gate Drivers

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***Abstract*—Adaptive Active Gate Drivers (AGDs) improve the trade-off between switching losses and transient overshoots by dynamically shaping the gate current. However, their implementation requires the optimization controller to run on limited computational resources while coping with fast load variations. This work compares three low-complexity algorithms for adaptive AGDs, analyzing their computational cost and convergence behavior. The algorithm performance are evaluated on a real AGD test case, showing that steepest gradient descend provides the best trade-off between speed and complexity.**

***Index Terms*—Active Gate Driver (AGD), adaptive AGD, gate driving, power transistor, stability, tracking speed.**

I. Introduction

The control of fast power transistors is a critical aspect in hard-switched power converters, as they are prone to overshoots, undershoots, and oscillations during switching transients. Conventional gate drivers typically address such an issue by increasing the gate resistance, but at the cost of higher losses.

Conversely, Active Gate Drivers (AGDs) dynamically modulate the gate current during the commutation to shape the switching trajectory, thus achieving a better trade-off between power losses and overshoot [1], [2]. The AGD architecture and the corresponding switching waveforms are shown in Fig. 1, where the AGD drives the low-side transistor T_{LS}. A resistance-modulated AGD typically consists of N independently controlled pull-up and pull-down branches, each associated with a different resistance and selected through switches $S_{\mathrm{ON/OFF}}$. Considering the turn-on transition of T_{LS}, the driver initially selects a low resistance ($R_{G,\mathrm{ON},1}$ in Fig. 1(b)) to speed up the current transition. As the drain current approaches I_{LOAD}, a higher resistance is applied to damp the resonance between the power loop parasitic inductance (L_{LOOP}) and the output capacitance of the high-side switch (D_{HS}). Finally, the driver switches back to a low resistance to complete the transition quickly. The resulting sequence of activated branches, referred to as the modulation profile, determines the gate-current waveform and the switching trajectory, eventually. The selection of the proper modulation profile is a key challenge, as fixed profiles degrade under varying operating conditions, device spread, and aging [3]. Adaptive AGDs address this aspect by iteratively updating the profile after each commutation, based on the measured switching performance [4]–[6]. However, the convergence speed and stability of iterative algorithms have received little attention, despite their importance in resource-constrained adaptive AGDs.

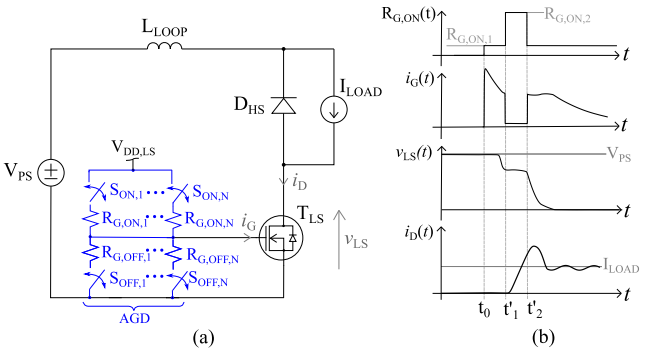

Fig. 1. (a) Half-bridge in which T_{LS} is driven by a resistance-modulated AGD, comprised of N pull-up and N pull-down branches. In (b), switching waveforms at the T_{LS} turn on.

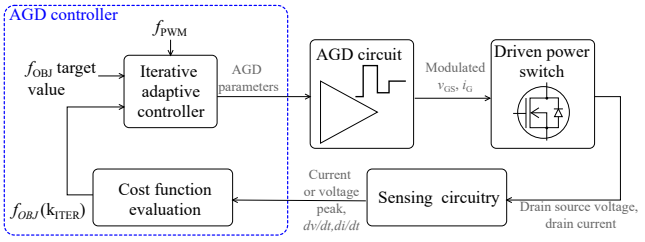

Fig. 2. Scheme of an adaptive active gate driver.

This paper provides a comparative analysis of the stability and convergence speed of low-complexity algorithms for adaptive AGDs, highlighting the trade-offs between convergence speed and computational complexity.

II. Adaptive AGD and Iterative Control

Given a resistance-modulated AGD as that shown in Fig. 1(a), the modulation profile is defined by M parameters, corresponding to the delays and durations of the activated branches. The typical architecture of an adaptive AGD is shown in Fig. 2. The controller evaluates a cost function $f_{\mathrm{OBJ,SYS}}(\boldsymbol{x})$ after each commutation and updates the modulation parameters $\boldsymbol{x} \in \mathbb{R}^M$ to minimize it. The cost function can represent a switching constraint, e.g., overshoot, or a weighted combination of switching speed and losses. The optimization process continues commutation by commutation until $f_{\mathrm{OBJ,SYS}} < f_{\mathrm{OBJ,THR}}$.

This problem can be formulated as a minimization task. Since the closed-loop system is nonlinear and its analytical

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TABLE I
COMPUTATION COMPLEXITY OF THE CONSIDERED ALGORITHMS.

Parameter	CCD	SDG	NCG
No. $f_{\mathrm{OBJ,SYS}}$ per iteration	2	M+1	M+4
No. sum per iteration	5	3M+1	4M+4
No. multiplication per iteration	2	3M	5M+4
No. square root per iteration	0	1	2

TABLE II
EXPONENTIAL STABILITY RESULTS ($1/\lambda$ IN UNITS OF k_{iter}).

	$\boldsymbol{x_E}$ @ 5 A		$\boldsymbol{x_E}$ @ 0.2 A	
	c	$1/\lambda$	c	$1/\lambda$
Cyclic Coordinate Descent	3.6	26.3	1.95	13.7
Steepest Gradient Descent	4	10	3.25	4.3
Nonlinear Conjugate Gradient	12.8	12.3	3.8	4.4

model is generally unknown, its stability is assessed through the exponential convergence of the equilibrium point $\boldsymbol{x_E}$:

$$||\boldsymbol{x}(t) - \boldsymbol{x_E}|| \leq c\, e^{-\lambda t} ||\boldsymbol{x_0}(t) - \boldsymbol{x_E}||, \ \forall ||\boldsymbol{x_0}(t) - \boldsymbol{x_E}|| \leq \epsilon. \tag{1}$$

The parameters (λ, c) can be exploited to provide an estimation of the AGD capability to track the optimal modulation profile under operating condition variations.

To identify $\boldsymbol{x_E}$, three low-complexity iterative algorithms suitable for resource-constrained controllers are compared, which are the Cyclic Coordinate Descent (CCD), the Steepest Gradient Descent (SGD), and the Nonlinear Conjugate Gradient (NCG). Their computational complexity, reported in Tab. I, depends on M, with CCD requiring the lowest computational effort per iteration. The convergence time of these algorithms is $t_{\mathrm{conv}} = k_{\mathrm{iter}} t_{\mathrm{iter}}$, where k_{iter} is the number of iterations and t_{iter} is the iteration execution time. As t_{iter} is an integer multiple of the power converter switching period $(1/f_{\mathrm{SW}})$, the objective function evaluations impose a lower bound

$$t_{\mathrm{conv}} > k_{\mathrm{iter}} \frac{No.Eval}{f_{\mathrm{SW}}}. \tag{2}$$

III. RESULTS ON A REAL TEST CASE

The adaptive AGD proposed in [5] was selected as test case, with $M = 2$ parameters defining the delay (d_{ON}) and duration (t_{ON}) of an auxiliary pull-down branch active during the Miller plateau (see Fig. 1). The objective function was the drain-source voltage undershoot. Measurements were first performed to obtain the objective-function map as a function of the two parameters. For $f_{\mathrm{OBJ,THR}} = 1.4\,\mathrm{V}$, the equilibrium regions for load currents of 0.2 A and 5 A are reported in Fig. 3(a).

The three optimization algorithms were then applied to the measured maps, starting from the same initial condition. CCD required the highest number of iterations to converge ($k_{\mathrm{ITER}} = 24$), since it updates one parameter at a time. Conversely, SGD and NCG achieved faster convergence ($k_{\mathrm{ITER}} = 4$), with SGD providing the best trade-off between convergence speed and computational complexity.

The exponential stability of the equilibrium points was

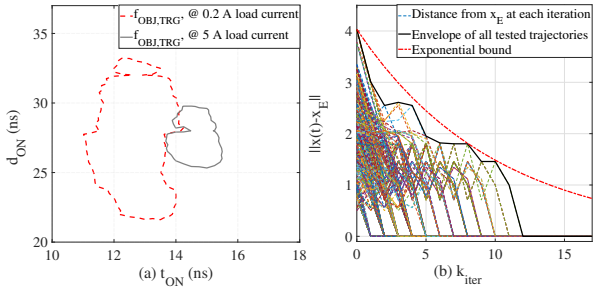

Fig. 3. In (a), equilibrium regions ($f_{\mathrm{OBJ,SYS}} \leq f_{\mathrm{OBJ,THR}}$) for load currents of 0.2 A (dashed) and 5 A (solid). In (b), simulated convergence trajectories for a 5 A load current.

evaluated as per (1). The resulting convergence rates, extrapolated from Fig. 3(b), are reported in Tab. II, where $1/\lambda$ is the convergence time in iterations. For both load conditions, CCD exhibited the slowest convergence, while SGD and NCG showed similar performance. Conversely, CCD resulted in the lowest c, meaning closer to the equilibrium point.

To experimentally validate the analysis, the SGD algorithm was implemented on the prototype of [5] with $f_{\mathrm{SW}} = 100\,\mathrm{kHz}$ and $t_{\mathrm{iter}} = 40\,\mu\mathrm{s}$. Step load variations between 0.2 A and 5 A were applied, resulting in convergence times of approximately $240\,\mu\mathrm{s}$ ($k_{\mathrm{ITER}} \approx 6$) and $480\,\mu\mathrm{s}$ ($k_{\mathrm{ITER}} \approx 12$), respectively. The experimental results agree with the estimated convergence rate, validating λ as a predictor of AGD convergence speed under load transients.

IV. CONCLUSION

This paper compared low-complexity iterative algorithms for adaptive AGDs, highlighting the impact of algorithm selection on convergence speed and computational requirements. Amongst the investigated approaches, SGD achieved the best complexity/speed trade-off, as confirmed experimentally. The presented analysis provides insights for the implementation of real-time self-adaptive gate drivers.

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