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On the Use of the Delay Compensation Technique to Reduce the Volume of Traction Inverter EMI Filters

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***Abstract*—The mitigation of conducted EMI is a major challenge in traction inverters, as bulky input filters are often required. Targeting the reduction of the filter volume, this work combines the four-leg topology with the delay compensation technique to maximize the cancellation of the common-mode current at the inverter output during switching transients. An iterative algorithm allows one to find the optimal delays for the switching legs for each commutation, resulting in around $30\,\mathrm{dB}$ EMI reduction in the $150\,\mathrm{kHz}$-$1\,\mathrm{MHz}$ range. By relaxing the required insertion loss of the input filter, a conventional two-stage EMI filter can be replaced by single-stage solution with reduced inductance, resulting in a 70 % lower filter volume.**

***Index Terms*—Common-mode Electro Magnetic Interference (EMI), EMI filter, four-leg inverter.**

I. Introduction

Conducted Electro Magnetic Interference (EMI) is a significant issue in traction Voltage Source Inverters (VSIs), where strict automotive electromagnetic compatibility (EMC) standards limits must be met. In such systems, Common-Mode (CM) EMI is dominant in most cases, as high dv/dt switching transitions of the VSI legs inject a large CM current into the chassis through the motor parasitic capacitance.

To comply with limits imposed by Original Equipment Manufacturers (OEMs), e.g., [1], passive EMI filters are typically installed at the inverter DC input. These filters combines Y-capacitors and CM chokes to provide the required attenuation in the low-frequency regulated range, i.e., from 150 kHz to a few MHz [2]. However, in high-power traction applications, the large current levels require busbar-mounted one-turn CM chokes, which significantly limit the achievable inductance per unit volume. As a consequence, input EMI filters may occupy up to one third of the inverter volume, becoming a major limitation for power density improvement in traction drives [3].

To reduce the filter size, active EMI filtering techniques have been investigated, in which CM disturbances generated by VSIs are sensed, inverted, and reinjected to cancel the CM current at the inverter input [4], [5]. Although effective in some applications, these solutions remain challenging for traction inverters due to bandwidth limitations and limited current injection capability.

An alternative approach consists in reducing CM disturbances directly at the source through modulation and topology-level modifications [6], [7]. Amongst them, spread-spectrum modulation is a well established solution for DC-DC converters, but it shows a limited effectiveness in traction systems due to the restricted frequency modulation allowed [8], [9].

A promising EMI reduction strategy effective at the source is the Delay Compensation Technique (DCT), which exploits the cancellation of CM current contributions generated by complementary transients. By finely adjusting the delays of switching edges, the CM currents injected through parasitic capacitances coupling high dv/dt nodes with the reference ground can be ideally canceled. This technique has shown significant CM EMI reduction in full-bridge converters [10], trapezoidal-modulated motor drives [11], as well as DC-DC converters [12].

To apply the DCT to traction motor drives, four-leg three-phase inverter topology can be explored, as it allows for the complementary commutation of switching legs [13]–[15]. In this scenario, the approach proposed in [16], where the fourth leg only drives a dummy impedance, is promising for high-current traction application, as it does not require bulky output filters. However, the direct application of the DCT to three-phase VSIs is not straightforward, as a practical implementation should account for load-dependent switching conditions and component mismatches, thus requiring an adaptive delay control strategy.

In this context, this work investigates the application of the adaptive algorithm for DCT proposed in [17] to four-leg three-phase traction inverters, with the objective of reducing CM EMI at the source and assessing the reduction in the required input EMI filter. To this purpose, the filter design procedure representative of traction applications is first presented, highlighting the relationship between the CM EMI reduction and the required filter inductance. The DCT is then experimentally validated on a four-leg traction inverter, with the achieved EMI reduction translated into passive filter requirements. A comparison with a conventional three-leg VSI demonstrates that CM EMI reduction at the source allows for a lower CM choke inductance, thus resulting in a more compact filter.

The paper is organized as follows. Sect. II introduces the CM EMI model and filter design procedure. The four-leg topology is introduced in Sect. III, and the DCT algorithm in Sect. IV. Experimental setup and results are reported in Sect. V, with concluding remarks in Sect. VI.

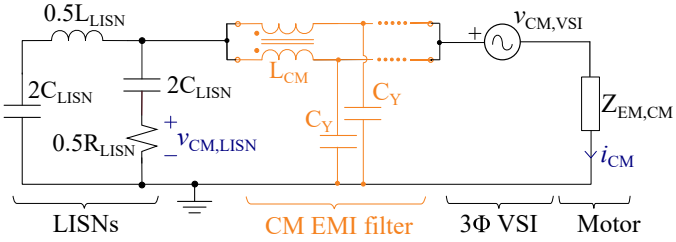


Fig. 1. CM EMI model of a motor drive system. The input EMI filter is placed between the LISNs and the device under test, i.e., the inverter and the motor.

II. Design of Input Filter for CM EMI

To assess the efficacy of the fourth leg combined with the DCT in reducing the volume of the input EMI filter, this Sect. recalls the EMI filter design procedure focusing on the low-frequency regulated range.

For a conventional three-phase VSI, the equivalent CM model shown in Fig. 1 is commonly exploited to evaluate conducted EMI at the receiver side. The VSI is represented by the voltage source $v_{\mathrm{CM,VSI}}$, i.e., the CM voltage at the inverter output. The motor is modeled by its CM equivalent impedance $Z_{\mathrm{EM,CM}}$. According to standards [1], [18], two HV Line Impedance Stabilization Networks (LISNs) are connected between the HV supply (V_{HV}) and the device under test. For CM analysis, the LISN outputs are tied together, as shown in Fig. 1. High-frequency parasitics, such as those related to cables, are neglected since they marginally affect LF components.

The input EMI filter, placed between the LISNs and the motor drive, is designed to provide sufficient attenuation, so that CM disturbances at the LISN measurement ports are below limits imposed by OEMs. The minimum insertion loss (IL) required by the filter can be estimated provided that CM source spectrum ($v_{\mathrm{CM,VSI}}$), source impedance ($Z_{\mathrm{EM,CM}}$) and the CM LISN impedance are known.

As far as three-phase VSIs implementing the Space Vector Modulation (SVM) are concerned, the frequency spectrum of $v_{\mathrm{CM,VSI}}$ is bounded by that of trapezoidal waveform with 50% duty cycle and V_{HV} amplitude [19]. The spectrum envelope is characterized by two breakpoint frequencies associated with duty cycle and rise time. In traction inverters, the switching frequency (f_{SW}) is typically 10-50 kHz, while rise/fall times are in the order of tens of ns, meaning that in the low frequency regulated range, i.e., from 150 kHz up to a few MHz, the $v_{\mathrm{CM,VSI}}$ spectrum can be approximated as

$$|V_{\mathrm{CM,VSI}}(f)| \approx V_{\mathrm{HV}} \cdot \frac{2f_{\mathrm{SW}}}{\pi f}, \tag{1}$$

Assuming no EMI filter is present, from Fig. 1 the transfer function between $v_{\mathrm{CM,VSI}}$ and $v_{\mathrm{CM,LISN}}$ is

$$H_{\mathrm{CM}}(j\omega) \approx \frac{C_{\mathrm{EM,CM}}}{C_{\mathrm{LISN}}} \cdot \frac{1 - L_{\mathrm{LISN}}C_{\mathrm{LISN}}\omega^2}{1 + \frac{L_{\mathrm{LISN}}}{R_{\mathrm{LISN}}}j\omega - L_{\mathrm{LISN}}C_{\mathrm{EM,CM}}\omega^2}, \tag{2}$$

TABLE I
CM EMI model values

Parameter	Value	Parameter	Value	Parameter	Value
V_{HV}	400 V	f_{SW}	32 kHz	$C_{\mathrm{EM,CM}}$	10 nF
C_{LISN}	100 nF	L_{LISN}	5 µH	R_{LISN}	50 Ω
M	6 dB	$\sum C_{\mathrm{Y}}$	400 nF	L_{dB}	[1]

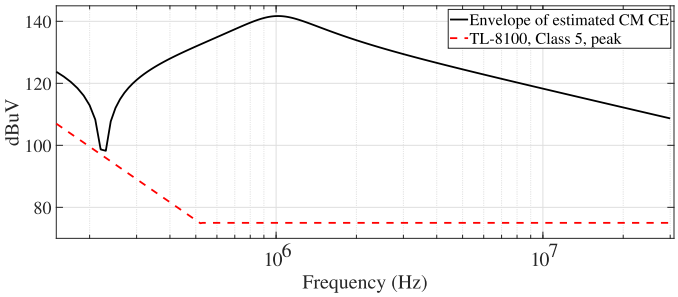


Fig. 2. Estimated envelope of CM EMI for a traction motor drive (solid) based on the values reported in Tab. I.

where $Z_{\mathrm{EM,CM}} = (j\omega C_{\mathrm{EM,CM}})^{-1}$ since previous studies have reported a capacitive behavior of the motor CM impedance up to a few MHz for traction motors [20].

Thus, CM conducted EMI at the LISNs can be estimated as

$$|V_{\mathrm{CM,LISN}}(j\omega)| = |H_{\mathrm{CM}}(j\omega)| \cdot |V_{\mathrm{CM,VSI}}(j\omega)|. \tag{3}$$

With the parameter values reported in Tab. I, the estimated CM EMI envelope is shown in Fig. 2 in solid line. Such a spectrum largely exceeds the TL-8100 limit reported in dashed line. The required filter insertion loss is thus

$$IL_{\mathrm{req,dB}} = |V_{\mathrm{CM,LISN}}|_{\mathrm{dB}} - L_{\mathrm{dB}}(f) + M, \tag{4}$$

where $L_{\mathrm{dB}}(f)$ is the target mask and M is for design margin.

With $IL_{\mathrm{req,dB}}$ known, the EMI filter must ensure $IL_{\mathrm{fil,dB}} > IL_{\mathrm{req,dB}}$ over the entire regulated frequency range. To design a passive filter, topology (CL or LC), number of stages, and component values must be selected. The filter IL can be analytically evaluated from its ABCD parameters [21] using the CM model in Fig. 1. Due to safety constraints, the total Y-capacitance is limited by OEM requirements, typically 200-400 nF for 400 V DC buses. The design proceeds iteratively to determine the required CM choke inductance L_{CM} and the number of stages [2]. As a reference case, the filter was designed in accordance with the values in Tab. I. The resulting inductance values for different topologies are shown in Fig. 3 in dark bars. CL topology is generally preferred over LC because it results in a lower L_{CM} as the source impedance is mostly capacitive. Increasing the number of stages further reduces total inductance due to the higher IL slope.

The preliminary design must then be refined to include component non-idealities. In the low-frequency range, the dominant non-ideality is the frequency-dependent permeability of the CM choke core. Even for nanocrystalline materials, permeability can drop significantly in the MHz range. By

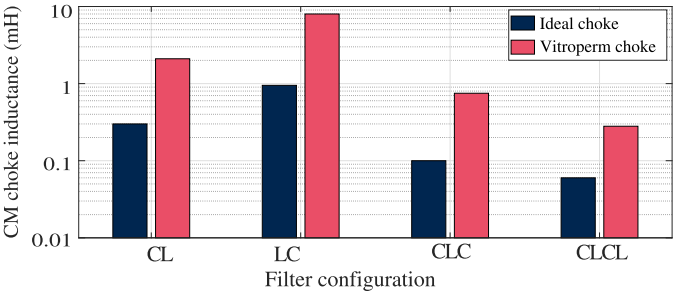


Fig. 3. Required inductance for different filter topology/number of stages with a constant Y-capacitance. Dark bars refer to ideal chokes, light bars to real chokes where permeability is frequency dependent.

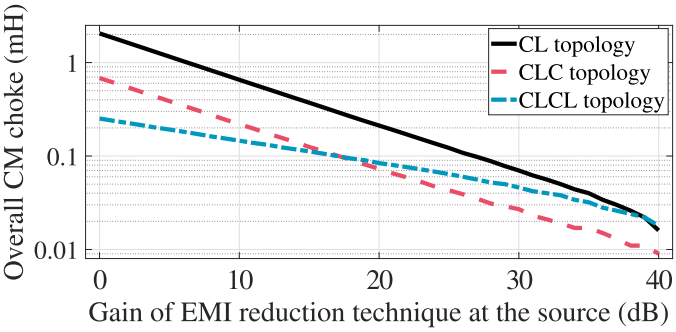


Fig. 4. Required inductance for CL (solid), CLC (dashed) and CLCL (dashed-dot line) input filter as a function of the G_{dB} achievable by adopting a CM EMI reduction technique at the source.

repeating the filter design to accounting for such an issue in commercial chokes [22], the required inductance becomes roughly eight times larger than the ideal estimate, as shown by the light bars in Fig. 3.

In traction inverters, one-turn CM chokes are often placed around DC busbars, thus limiting the achievable inductance. For such a reason, two- or three-stage CL filters are commonly adopted to achieve IL_{req} while minimizing the inductance.Since the filter volume is mainly determined by the CM chokes, reducing L_{CM} also directly reduces the filter volume.

This work investigates CM EMI mitigation at the source to reduce IL_{req}, thus L_{CM}. Independently from the specific technique applied, if the spectrum of $v_{\mathrm{CM,VSI}}$ is reduced by G_{dB}, the required filter insertion loss decreases by the same amount as per (3) and (4). Aiming to quantify the impact of a EMI reduction technique at the source on the input filter design, Fig. 4 shows the resulting choke inductance for CL (solid), CLC (dashed), and CLCL (dashed-dot line) filters as a function of G_{dB}. For CL and CLC topologies, L_{CM} is approximately inversely proportional to G, whereas CLCL shows a sub-inverse dependence. Therefore, source-side EMI mitigation is highly effective for reducing input filter volume, since even moderate CM reduction significantly lowers the required choke inductance.

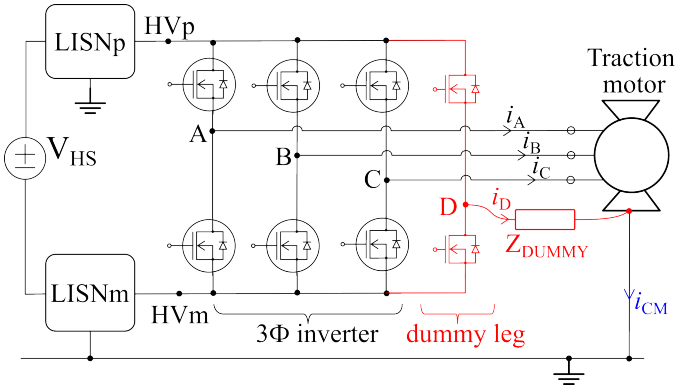


Fig. 5. Four-leg VSI driving a three-phase motor without the output filter. The fourth leg is connected to the dummy impedance Z_{DUMMY} to control the injected CM current.

III. Four-leg Three-Phase Inverter With AZSPWM-3

Amongst CM EMI reduction techniques effective at the source, four-leg three-phase VSIs are a well-known topology for motor drives, allowing for the cancellation of the output CM voltage through complementary commutations of the four switching legs [7].

As far as traction inverters are concerned, they are characterized by high currents, thus requiring busbars connected between the inverter output phases and the motor terminals. In this scenario, a suitable four-leg topology is that proposed in [16] and shown in Fig. 5. Here, the dummy leg drives a passive impedance Z_{DUMMY} connected to the motor chassis. To achieve CM current cancellation at the inverter output, Z_{DUMMY} must be properly selected to ensure the CM current injected by one of the three main legs is equal in magnitude to that by the dummy leg, thus resulting in $i_{\mathrm{CM}} = 0$.

From analysis of the circuit shown in Fig. 5, the required condition is that

$$Z_{\mathrm{DUMMY}} = 3 \cdot Z_{\mathrm{EM,CM}}, \tag{5}$$

where $Z_{\mathrm{EM,CM}}$ is the CM motor impedance. Possible implementations of the RLC network for Z_{DUMMY} are reported in [16], [17], which include a limited number of passive components to achieve a good matching up to a few MHz. For the harmonics of the switching frequency, it results that the dummy leg must only drive a capacitive load with a value of a few nF, in place of the large output currents provided by the three main legs as per the required motor torque. Since the power rating of the fourth leg is much lower than those of the main legs, more compact devices can be used for that, resulting in an estimated volume overhead of the inverter of around 5 %.

To achieve CM current cancellation at the inverter output, besides introducing the fourth leg, also the PWM modulation must be revised to ensure all legs switch complementary. To this purpose, Active Zero State PWM (AZSPWM-3) is considered, which can be obtained directly from SVM provided

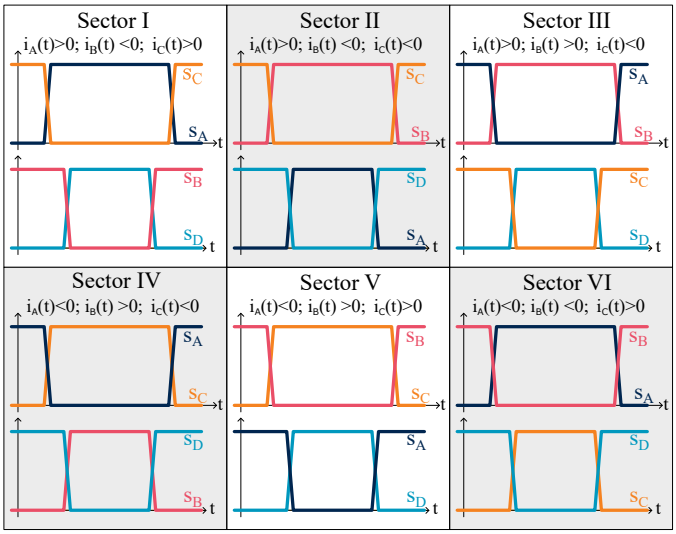


Fig. 6. Control signals of the four legs according to AZSPWM-3 for the six sectors.

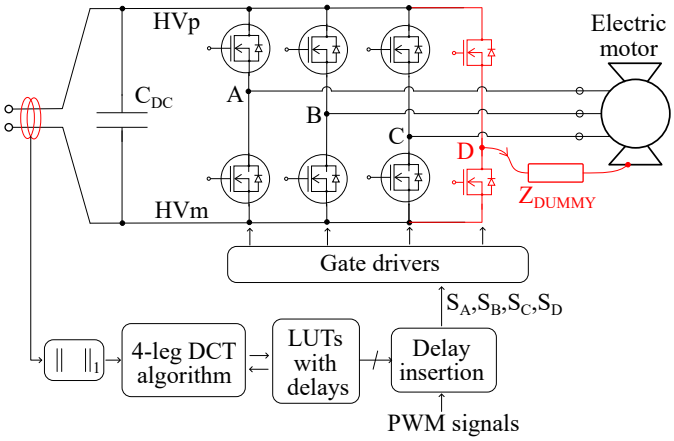


Fig. 7. Block scheme of the proposed solution to apply DCT to four-leg VSIs.

that, for specific legs and sector, the PWM signal is generated by either the positive, or negative, triangular carrier [23]. More precisely, the control signals for the main three legs ($S_{\mathrm{A-C}}$) and that of the dummy leg (S_{D}) according to AZSPWM-3 are shown in Fig. 6 for all six sectors.

Assuming a sinusoidal modulation of the phase currents shifted by 120°, the duty cycles of $S_{\mathrm{A-C}}$ are almost sinusoidal, with 0.5 mean value. It is worth noting that, in each sector, there is leg whose duty cycle is closed to the maximum, one whose duty cycle is closed to the minimum, and the third leg has the duty cycle varying the most. With AZSPWM-3, the legs whose duty cycle is almost constant are grouped together and associated with a positive/negative triangular carrier at f_{SW}, so that the resulting control signals commutate opposite. This is shown in Fig. 6 for legs A-C (sector I), B-C (sector II) and A-B (sector III). The remaining leg is then associated with the dummy leg, so that the control signal S_{D} is generated by negating the control signal of leg B, A and C in sector I, II and III, respectively.

By adopting such a modulation scheme, the complementary commutations of the control signal can be achieve, which in principle should be directly translated as complementary commutations of the output phase voltages at AC side of the inverter. However, the switching waveforms may be different from those shown in Fig. 6. Indeed, the phase voltages are not well aligned during commutations due to mismatches and load-dependent delays. As a result, CM current cancellation at the inverter output is impaired, leading to a lower gain of the EMI reduction.

IV. DCT ALGORITHM

To ensure all the switching leg commutation are finely aligned, this work applies the Delay Compensation Technique (DCT) to the four-leg inverter according to the block-level scheme shown in Fig. 7.

The proposed solution is an adaptive delay optimization system. It is based on the isolated measurement of the CM current, performed at the inverter input. The acquired signal is processed, and its 1-norm computed after windowing the signal around the switching transition to be optimized, i.e.,

$$M = \int_0^{t_{\mathrm{wind}}} |i_{\mathrm{CM}}(t)|dt. \tag{6}$$

The variable M represents the cost function used by the optimization algorithm. The algorithm determines the delays between the rise and fall edges of the control signals associated with the four legs to minimize M, thus the CM current. These delays are stored in Look Up Tables (LUTs) and added to the PWM signals generated by the motor controller, immediately before being sent to gate drivers.

In order to define the size and populate the contents of the two LUTs, i.e., one for rise edges and one for fall edges, Fig. 6 can be considered. For each PWM cycle, there are two pairs of legs switching opposite. Therefore, two rise delays and two fall delays must be optimized for each PWM period. Multiplying these by the number of PWM periods within one sector and by the number of sectors, the size of the delay tables grows significantly. Since the delays depend on the operating conditions under which the legs switch, it can be observed that in even (odd) sectors the main pair of legs switches with positive (negative) currents. A similar consideration applies to the current flowing through the leg compensated by the dummy leg.

Therefore, the possible scenarios can be reduced to four configurations, two for the main leg pairs and two for the pair involving the fourth leg, which are reused across different sectors since the leg currents are the same. As a result, the LUT size becomes 4 rows by N_{PWM} columns, where N_{PWM} is the number of PWM cycles within each sector.

The proposed algorithm for populating the LUTs is based on an initial coarse phase, followed by a fine phase, as shown in the flowchart in Fig. 8. During the coarse phase, only the central PWM cycle corresponding to each configuration is

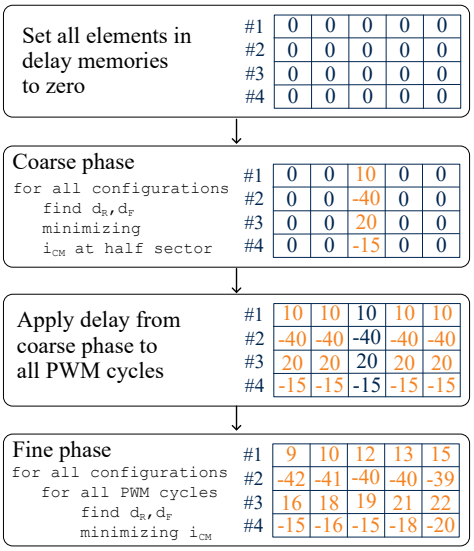


Fig. 8. Flowchart of the proposed algorithm to populate the delay LUTs shown in Fig. 7.

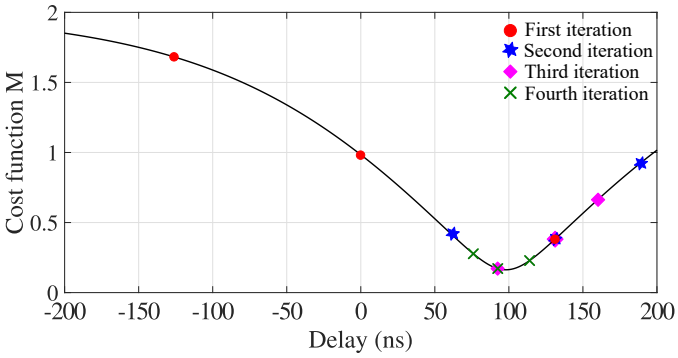


Fig. 9. Ternary search algorithm to determine the optimal delay in two complementary switching legs.

optimized, i.e., the column with index $\lceil N_{\mathrm{PWM}}/2 \rfloor$. The delays obtained are then applied to the entire sector, i.e., to the whole row of the LUT. Since the delays may vary from one PWM cycle to another due to the variation of the load current within the sector, the delays are further refined one by one during the fine phase.

The optimization of the delays for a pair of legs switching opposite is performed iteratively using a ternary search algorithm. The defined cost function M exhibits a local minimum corresponding to the delay to be applied to the control signal to properly align the commutations of complementary switching legs, as shown in Fig. 9 in solid line. Starting from an initial estimate of the optimal delay, the algorithm evaluates M corresponding to the initial estimate, as well as those obtained by subtracting and adding the step width (circle markers). Among the three candidates, the one corresponding to the lowest value of M is selected, and the procedure is repeated while halving the step width at each iteration, as shown in Fig. 9 in star and diamond markers. With the final iteration (cross markers), the optimal delay is attained. Thereby, this approach

TABLE II
NOMINAL TESTBENCH PARAMETERS.

Parameter	Value
Switching frequency (f_{SW})	32 kHz
Electrical modulation frequency (f_{LOAD})	666 Hz
Input supply voltage (V_{HV})	96 V
Phase peak current	25 A
Motor	100 kW PMSM in hairpin technology

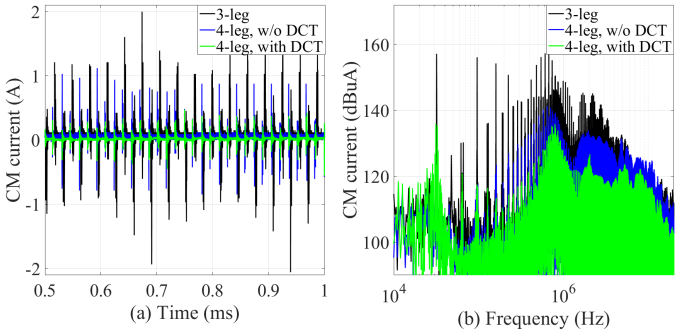


Fig. 10. Measured CM current in (a) time-domain and (b) frequency-domain for the prototype used as a conventional three-leg VSI (black), as four-leg with AZSPWM-3 without (blue) and with (green) the DCT applied.

allows one to estimate the optimal delays in a finite number of iterations while maintaining low computational cost, as only sums and comparisons are required.

V. Experimental Results

To assess the impact of the DCT on the required input EMI filter, measurements were carried out on a motor-drive prototype comprising of a four-leg VSI and a traction motor. The inverter can either operate as a conventional three-leg VSI with SVM modulation, or as four-leg VSI as that in Fig. 5 with AZSPWM-3 and DCT. The nominal operating conditions are reported in Tab. II. In what follows, the DCT effectiveness in reducing the CM current and conducted EMI is firstly assessed. Then, based on the measured conducted EMI, the required passive input filters are designed and compared to quantify the achievable reduction in filter volume.

A. DCT effectivness

With the prototype operating as a conventional VSI, the commutations of the switching legs cause large CM current pulses as shown in black in Fig. 10(a). Such a CM current was measured using an isolated 20 MHz-bandwidth probe placed around the inverter DC supply, as shown in Fig. 7.

The i_{CM} peaks are around 2 A and repeat every 250 µs, which is one sixth of the electrical period, i.e., the duration of one SVM sector. The corresponding frequency spectrum is shown in Fig. 10(b). Additional investigations revealed that the 1 MHz resonance is mainly associated with the CM motor impedance, with the equivalent LF capacitance $C_{\mathrm{EM,CM}}$=6.6 nF resonating with one third of the phase inductance.

With the fourth leg enabled and the modulation set to AZSPWM-3, the CM current is reduced, as shown by blue

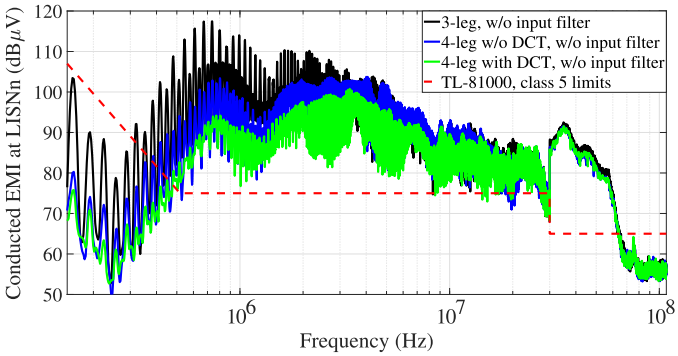


Fig. 11. Measured conducted EMI for three-leg VSI with SVM (black), four-leg VSI without (blue) and with (green) DCT applied.

waveforms. Concerning the frequency content, a significant reduction up to 5 MHz is observed. After executing the DCT algorithm, i_{CM} is further reduced, as shown green waveforms in Fig. 10. Compared to the four-leg case without DCT (blue), the magnitude of the CM current spectrum exhibits an additional reduction, especially in the 500 kHz-10 MHz range.

To quantify the reduction in the filter insertion loss (IL_{req}), conducted EMI measurements with no input filter were carried out according to the setup prescribed by [1]. The measured spectra are shown in Fig. 11 for the reference three-leg VSI (black), the four-leg VSI with AZSPWM-3 before (blue) and after (green) applying the delay optimization discussed in Sect. IV. Additional measurements confirmed that conducted EMI is mainly attributed to CM disturbances. As expected, the envelope of three-leg VSI case closely matches the analytical model presented in Sect. II, with EMI level being lower than that in Fig. 2 as both the DC supply voltage and the motor CM capacitance are lower than those estimated in Tab. I.

Although none of the tested configuration meet the TL-81000 limits (dashed line in Fig. 11) without an input EMI filter, the DCT allows one to reduce conducted EMI by approximately 30 dB up to a few MHz with respect to the conventional case, thus assessing the effectiveness of the proposed delay optimization in mitigating CM EMI at the source.

B. Filter design and voltage scaling

Based on the conducted EMI shown in Fig. 11, the design procedure described in Sect. II was adopted to determine the required passive EMI filter. Since the experimental prototype operates at 96 V, whereas the target traction application is typically based on a 400 V DC bus, the measured conducted EMI must first be scaled to the target operating voltage. As per (1), the magnitude of the CM voltage source $V_{\mathrm{CM,VSI}}$ is directly proportional to V_{HV}. Thereby, the CM EMI measured at the LISN scales proportionally with the supply voltage. More precisely, for a target voltage of V_{HV}=400 V, the expected conducted EMI is 12 dB higher than the measured spectrum.

The proposed solution, corresponding to the green spectrum in Fig. 11, was first considered for the filter design. The total Y-capacitance was fixed to $\sum C_{\mathrm{Y}}$=200 nF, and commercial

TABLE III
INPUT CM EMI FILTERS

Filter topology	CLC	CLC
Y-capacitance	2 x 2 x 50 nF	2 x 2 x 50 nF
CM choke	1 x 30 uH	2 x (30 uH + 60 uH)
Choke volume	30 cm^3	120 cm^3
Filter cost	21 $	80 $

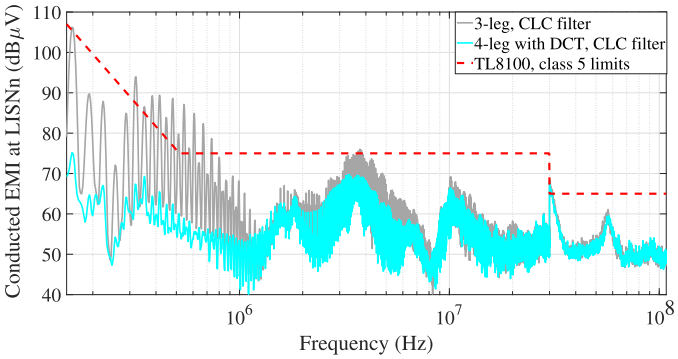


Fig. 12. Measured conducted EMI with the CLC filter inserted for the inverter operating as three-leg VSI with SVM (gray) and as a four-leg VSI with DCT applied (light blue spectrum).

one-turn chokes suitable for bus-bar mounting were selected [22]. The result is a CLC filter, whose component values are reported in Tab. II. The filter was then inserted and conducted EMI measurement repeated, with the corresponding spectra shown in Fig. 12. The proposed four-leg VSI with DCT (light blue) satisfies the target mask (dashed red) with adequate margin. However, the same filter does not provide sufficient attenuation when the DCT is disabled or when the inverter operates as a conventional three-leg VSI. In the latter case (grey), the conducted EMI would exceed the limit by approximately 15 dB at 500 kHz, corresponding to the frequency range more demanding in terms of insertion loss.

To achieve compliance for the conventional three-leg VSI, the input filter was redesigned following the same procedure. The resulting solution is a two-stage CLCL filter, whose component values are reported in the third column of Tab. II. The corresponding conducted EMI is shown in Fig. 13 in fucsia. Despite achieving emission levels comparable to those obtained with the proposed DCT solution (light blue), the conventional inverter requires a significantly larger passive filter to meet the same EMI limits.

C. Discussion

With the two input filters reported in Tab. II assessed as shown in Fig. 13, a comparison between the two solutions, i.e., traditional 3-leg with CLCL filter and proposed 4-leg with DCT and CLC filter, can be carried out, as they result in similar CE levels. Looking at the CM choke inductance values, i.e., 180 uH inductance for 3-leg case and 30 uH for the DCT case, these values are in agreement with Fig. 4. Indeed, as

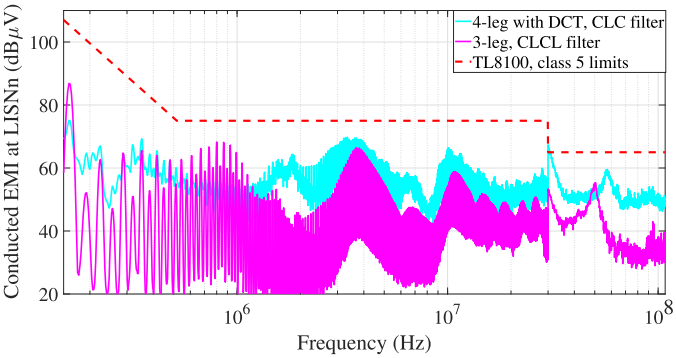


Fig. 13. Measured conducted EMI with the inverter operating as three-leg VSI with SVM and the CLCL filter (fucsia) and as four-leg VSI with DCT and CLC filter (light blue spectrum).

TABLE IV
SOLUTION COMPARISON

Solution	3-leg with CLCL filter	4-leg with DCT, CLC filter
Inverter volume	1270 cm^3	1330 cm^3
Inverter cost	293 $	310 $
Assembled filter volume	468 cm^3	144 cm^3
Filter cost	80 $	21 $
Total volume	1.74 dm^3	1.47 dm^3 (-15%)
Total cost	373 $	331 $ (-12%)

the proposed technique allow one to significantly reduce CE at the source, the required IL for the filter reduces, especially in the lower frequency range, i.e., from 150 kHz to around 1 MHz, which is where either large CM choke inductances or multi stage filters are needed to achieve the target attenuation.

It is worth noting that, besides the input filter reduced inductance and thus the filter volume, as reported in Tab. II, the use of CM reduction techniques at the source also provide other benefits to the filter design, as it allows for reduced current stress in the Y-capacitors and reduces the requirement of saturation current for the CM chokes.

Finally, a system-level comparison is reported in Tab. IV, where the contributions of the inverter and the input filter are separated. Although the proposed solution introduces a slightly larger inverter due to the additional leg, this increase is more than compensated by the significant reduction in filter size. Overall, the proposed solution achieves a reduction of approximately 15% in total system volume and 12% in total cost compared to the conventional three-leg solution with a bulkier EMI filter.

VI. Conclusion

The proposed four-leg traction inverter combined with the DCT was experimentally validated, resulting in 30 dB (15 dB) lower CM EMI at 160 kHz (2 MHz) compared to the traditional SVM configuration without any input EMI filter. Such a reduction lowered the insertion loss required from the input EMI filter, allowing for the replacement of a two-stage topology featuring 180 uH CM chokes with a one-stage one having a single 30 uH choke. Such a reduction translated into a four fold decrease in both the choke volume and in the choke cost.

From a system level perspective, the implementation of the DCT slightly increased the inverter volume and cost. However, the reduction of the EMI filter more than compensated for this increase. Indeed, the proposed solution achieved an overall volume reduction of approximately 15% and a cost reduction of approximately 12% compared with the conventional SVM-based solution when considering the overall assembly. These experimental results demonstrated the reducing CM disturbances directly at the source effectively reduced EMI filter requirements while improving the overall volume and cost of the traction inverter system.

VII. Acknowledgment

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