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Design, Control and Experimental Validation of an 800 V Wide-Bandgap Power Converter for Fuel Cell Traction Applications

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Declaration

I hereby declare that, the contents and organization of this dissertation constitute my own original work and does not compromise in any way the rights of third parties, including those relating to the security of personal data.

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2026

* This dissertation is presented in partial fulfillment of the requirements for **Ph.D. degree** in the Graduate School of Politecnico di Torino (ScuDo).

To my grandfather, whose path unexpectedly became my own.

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Abstract

Fuel cell electric vehicles represent a promising solution for high-efficiency and zero-emission transportation, but their adoption strongly depends on the availability of high-performance power electronic converters. In particular, the low and variable output voltage of fuel cell stacks requires efficient, compact, and reliable high-voltage conversion stages capable of interfacing with modern traction inverters.

This dissertation presents the analysis, design, control, and experimental validation of a high-voltage wide-bandgap power conversion system for fuel cell traction applications. The work focuses on a multilevel interleaved DC/DC converter based on GaN devices, complemented by a high-power SiC-based DC/AC traction inverter. A systematic analytical approach is developed to evaluate magnetic and electric stresses of active and reactive parts, demonstrating that the proposed four-leg multilevel interleaved architecture achieves a sixteen-fold reduction in the maximum peak flux ripple of the equivalent inductive path compared with the conventional bidirectional switching cell, together with a fourfold increase in effective ripple frequency. These characteristics enable reduced passive component size while preserving high efficiency and low current ripple.

A fully digital multi-loop control architecture is proposed for the DC/DC stage, including dedicated loops for differential current balancing and split DC-link voltage regulation. Small-signal modeling provides straightforward tuning guidelines and ensures stable operation and fast dynamic response. The control strategy is experimentally validated on a 75 kW prototype, achieving efficiencies above 98%.

The thesis further addresses the design and validation of a 150 kW SiC-based traction inverter and introduces an innovative back-to-back testing methodology for mapping full-power efficiency. Experimental results confirm the effectiveness of the proposed architectures and control strategies, demonstrating their suitability for high-power fuel cell electric powertrains.

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Nomenclature

AC	Alternating Current	ISR	Interrupt Service Routine
B2B	Back-to-back	MBC	Model Based Control
BBC	Buck-Boost Converter	MLBC	Multilevel boost Converter
BDC	Bidirectional DC/DC Converter	MPC	Model Predictive Control
CAN	Controller Area Network	PEMFC	Proton Exchange Membrane Fuel Cell
CM	Common Mode	PHEV	Plug-in Hybrid Electric Vehicle
CUT	Converter Under Test	PHIL	Power Hardware in the Loop
DC	Direct Current	PWM	Pulse Width Modulation
DM	Differential Mode	SEPIC	Single Ended Primary Inductor Converter
DMA	Direct Memory Access	TIM	Thermal Interface Material
EMI	Electromagnetic Interference	TLBDC	Three-Level Bidirectional DC/DC Converter
EV	Electric Vehicle	UART	Universal Asynchronous Receiver/Transmitter
FCEV	Fuel Cell Electric Vehicle	WBG	Wide Bandgap
FEM	Finite Element Method		
GaN	Gallium Nitride		
IBC	Interleaved Boost Converter		

Chapter 1

Introduction

The long-term effects of CO₂ emissions have sparked significant interest in the research of sustainable and green alternatives to conventional energy sources [1]. In this context, the *European Green Deal* [2] represents a bold challenge, aiming to make Europe the first carbon-neutral continent by 2050. Among the various sectors contributing to global CO₂ emissions, transportation ranks third after industry [3] with an increased contribution of 79% since 1990 [4]. This has led to substantial growth in the electric vehicle (EV) market. However, despite this growth, EVs still represent a minority share of the overall vehicle market [5]. This limited adoption can be attributed to critical challenges, particularly related to range extension and charging time. To address these limitations, several solutions have been proposed [6]. One promising approach is the integration of fuel cells in parallel with batteries [4]. Fuel cells offer clear advantages in terms of zero-emission output, producing only water as a byproduct, and lightweight design. However, they present significant challenges, such as lower efficiency compared to batteries and low output voltage [7]. Indeed, a hybrid solution composed of a fuel cell and a battery could represent a viable approach for electric vehicles, offering the feasibility for long-distance travel based on the fuel cell and urban mobility supported by the battery [8].

A key element in this hybrid system is the power converter, which bridges the gap between the energy source and the electric motor. In particular, an efficient high-voltage power converter is essential to step up the low output voltage of the fuel cell to meet the higher voltage requirements of modern electric motors.

Therefore, **this work focuses on the design, analysis, and experimental validation of high-power, high-efficiency DC/DC + DC/AC power converters for fuel cell electric powertrains.** The power converter is treated not as an auxiliary subsystem, but as a key enabling technology that directly impacts system efficiency, power density, reliability, and fuel cell lifetime. Particular attention is devoted to converter architectures capable of handling large voltage conversion ratios, high current levels, and stringent efficiency requirements, while ensuring low current ripple and controlled dynamic interaction with the fuel cell stack.

1.1 State of the Art of Fuel Cell Electric Vehicles

The global imperative to decarbonize transportation has intensified research into alternative powertrains. Fuel cell electric vehicles (FCEVs) are a promising zero-tailpipe-emission technology that converts hydrogen into electricity via electrochemical cells [8, 4]. FCEVs complement battery electric vehicles (BEVs) and hybrid engines by offering high energy density fuel and rapid refueling [4, 8]. Major climate initiatives, such as the European Green Deal, explicitly support hydrogen and fuel cell development to achieve carbon neutrality [2]. Concurrently, the rapid growth of electric mobility [5] demonstrates that oil demand from light-duty vehicles has already peaked, underscoring a shift towards clean alternatives. In this context, FCEVs are gaining attention both for passenger cars and for heavy-duty transport where long range and fast refueling are valued.

1.1.1 Principles of FCEV Operation

Fuel cell vehicles operate by combining a hydrogen fuel cell stack with an electric drivetrain. In a typical Proton Exchange Membrane Fuel Cell (PEMFC), compressed hydrogen stored onboard reacts with oxygen from air across catalyst-coated membranes, producing electricity, water, and heat. A single fuel cell produces only about 0.6–0.8 V, so a significant number of cells are stacked to reach a useful voltage. The DC output of the stack feeds an electric motor, usually via an inverter, optionally assisted by a battery or supercapacitor to buffer transient loads. FCEVs thus resemble BEVs in having an electric propulsion system, but the primary energy source is hydrogen rather than a battery [8, 4]. Typical fuel cell stack efficiencies

are on the order of 50–60%, and the overall fuel-to-wheel efficiency (including the electric drivetrain) may reach 40–50% under optimal conditions. However, the total well-to-wheel efficiency depends strongly on the hydrogen supply chain (electrolysis, compression, etc.) [9, 4].

Indeed, fuel cell operation presents specific engineering challenges. The stack voltage varies with load, temperature, and state-of-health, often in the range of only tens to a few hundred volts. Thus, a high-gain DC/DC converter is required to boost and regulate the voltage to the vehicle's DC bus (commonly 400–800 V) [10, 11]. Furthermore, the control of the fuel cell current is critical for safety and durability: rapid load changes can stress the membrane and catalysts, while shutdown and restart cycles can cause degradation [12]. To mitigate these issues, FCEVs typically include a secondary energy storage (battery or supercapacitor) that handles peak power during acceleration or regenerative braking, allowing the fuel cell to operate near its steady-state optimum. Some modern designs even use multiple fuel cell stacks (multi-stack architectures) managed in parallel or series to achieve higher power and redundancy [13].

1.1.2 Technological Developments

Recent years have seen significant improvements in fuel cell and related technologies. In the fuel cell stack itself, advances in catalyst materials and membrane durability have reduced the required platinum loading and extended lifetime. Automotive PEMFC systems now typically use less than 30–50 mg of Pt per kW of power, roughly an order of magnitude less than early prototypes, reducing cost and resource demand. Stack designs have become more compact and are often integrated with heat and water management systems to improve resilience across a wide temperature range [13]. Multi-stack configurations allow FCEVs to flexibly meet transient and peak power demands; control strategies allocate load among stacks to maintain optimal operating points and to compensate for any degraded cells [13, 11]. Onboard hydrogen storage has also evolved. Current FCEVs typically store hydrogen at 700 bar in lightweight carbon-fiber composite tanks, achieving high storage energy densities. Newer tank designs and materials aim to improve safety and weight further. Hydrogen fueling infrastructure remains limited, so research is also focusing on efficient ways to compress or liquefy hydrogen for refueling stations.

A key area of development is power electronics. The inherently low and variable fuel cell voltage requires high-gain DC–DC converters. State-of-the-Art FCEV power converters exploit advanced topologies to maximize efficiency, power density, and reliability. For instance, interleaved boost converters split the fuel cell current among multiple phases, reducing input current ripple [14, 10]. Coupled-inductor interleaved designs have been shown to further reduce ripple and stress by sharing magnetic coupling between phases [10, 15]. High-frequency switching (in the hundreds of kHz) is now achievable thanks to wide-bandgap semiconductors (WBG) (e.g. SiC MOSFETs and GaN), enabling converters with very high power density. Soft-switching techniques (e.g. resonant or clamped circuits) are also employed to minimize switching losses at high frequency.

Topologies such as multilevel and multi-stage converters are used to handle the high voltage ratio from fuel cell to DC bus. Diode-clamped and cascaded multilevel converters can achieve very high gain without extreme duty cycles [16, 17]. In [17] an ultra-high-gain interleaved converter is presented, tailored for fuel cells, showing low current ripple and voltage stress even at high boost ratios. Another important aspect that needs to be considered is the energy management between the fuel cell and auxiliary storage. Two-stage converter architectures are often used: a front-end converter handles fuel cell-to-bus voltage boosting, while a second stage interfaces a battery or supercapacitor for bidirectional power flow, as presented in [18, 1]. These hybrid architectures allow the fuel cell to be oversized for continuous power while letting the battery cover short peaks. Control algorithms coordinate the power split to keep the fuel cell in its high-efficiency operating window and to avoid sharp load transients. Recent literature emphasizes integrated approaches where converters and control are co-designed to minimize current ripple, maximize efficiency, and ensure fail-safe operation [11, 13].

1.1.3 Market Trends

Despite the technical progress, FCEV market deployment remains limited compared to BEVs. Table 1.1 summarizes the main fuel cell powertrains that are commercially available and prototyped. As of 2024, only on the order of tens of thousands of fuel cell cars and light vehicles have been sold worldwide, a small fraction of the millions of BEVs and ICE vehicles on the road. Early FCEVs such as the Toyota Mirai, Hyundai Nexo, and Honda Clarity have demonstrated ranges around 600 km per fill,

Table 1.1 Fuel Cell Electric Vehicles: commercially available and prototype/demo models.

Manufacturer	Model	Year	Power [kW]	Range [km]	H ₂ [kg]
Commercially available models					
Toyota	Mirai (Gen II)	2020	114	647 (EPA)	5.6
Hyundai	Nexo	2018	95	666 (WLTP)	6.33
Honda	Clarity Fuel Cell	2016	103	~650	5.0
Prototype and demo models					
BMW	iX5 Hydrogen (pilot)	2022	295 (total) / 125 (FC)	504 (WLTP)	6.0
Mercedes	GLC F-Cell	2018	155	~437	4.4
Audi	A7 h-tron (concept)	2015	170	~540	5.0

validating the concept. Industry analysts note that several new hydrogen-powered car models are in development, some claiming ranges up to about 800 km [19].

Moreover, FCEVs are also targeting heavier segments. Several companies are developing fuel cell buses, trucks, and vans [20]. The choice to adopt FCEVs is often supported by policy incentives. Regional initiatives like California's hydrogen highway or the EU's hydrogen strategy (part of the European Green Deal) provide subsidies for stations and vehicles, acknowledging hydrogen's role in decarbonizing transport [2]. As a consequence, hydrogen refueling infrastructure is expanding but remains sparse. As of 2024, there are only a few hundred public hydrogen stations worldwide (mostly in California, Japan, Germany, and South Korea). Deploying a comparable network to gasoline or electric charging is challenging. Furthermore, hydrogen network costs are currently higher than those for electricity networks, but both systems can be developed in parallel to serve different needs [7].

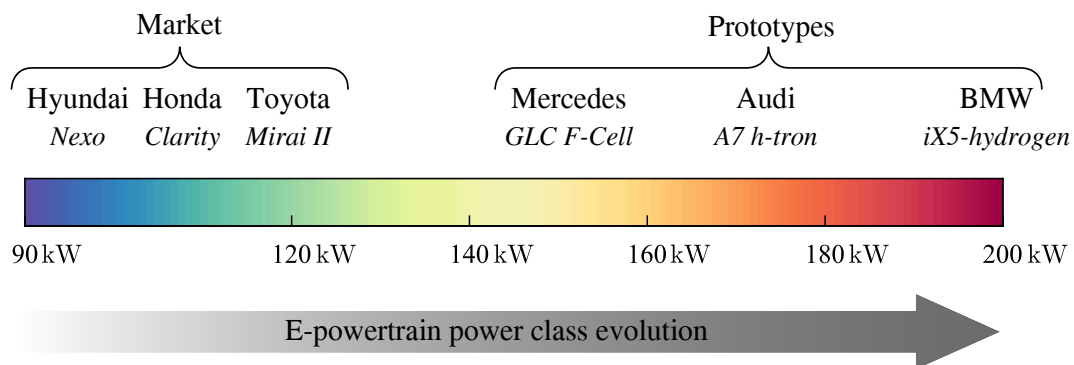


Fig. 1.1 Market and prototype trends for fuel cell electric vehicles.

1.2 Requirements and Challenges

Despite their potential, FCEVs face significant technological and infrastructural challenges. High system costs—mainly related to platinum catalysts and complex balance-of-plant—remain a barrier. Stack durability under dynamic operating conditions, lower overall well-to-wheel efficiency compared to BEVs, and the limited availability of hydrogen refueling infrastructure further hinder large-scale adoption [4, 7, 12]. Analyses suggest that in the long term, hydrogen can become economically viable if supported by scale-up and fleet deployment [20]. Addressing these barriers requires advances in material science, manufacturing, and infrastructure investment.

At the technical core of these challenges lies the role of power electronics and energy management. The inherently low and variable output voltage of fuel cells stacks (tens to a few hundred volts) requires efficient high-gain DC–DC converters to interface the stack with the vehicle’s high-voltage DC bus (typically 400–800 V). As a consequence, based on the previous market trends analysis, there is a clear gap between the commercially available fuel-cell electric powertrains and the prototyped ones, visually represented in Fig.1.1.

Indeed, the proposed challenge is to investigate the gap between industry and prototypes. State-of-the-Art research has developed a variety of topologies tailored for FCEVs: multi-phase interleaved converters to reduce input current ripple [14, 21], coupled-inductor designs to improve performance [10], and ultra-high-gain or multilevel converters to achieve the large voltage ratios required [17, 16, 22], as well as bidirectional converter topologies which are also essential to support regenerative braking and hybrid storage systems [23, 24]. In this manner, the use of wide-bandgap devices (SiC, GaN) enables high-frequency operation with efficiencies above 95% [25, 26] and also represents an important opportunity to reduce the size of magnetic components. Last but not least, the power density of the full powertrain will also improve.

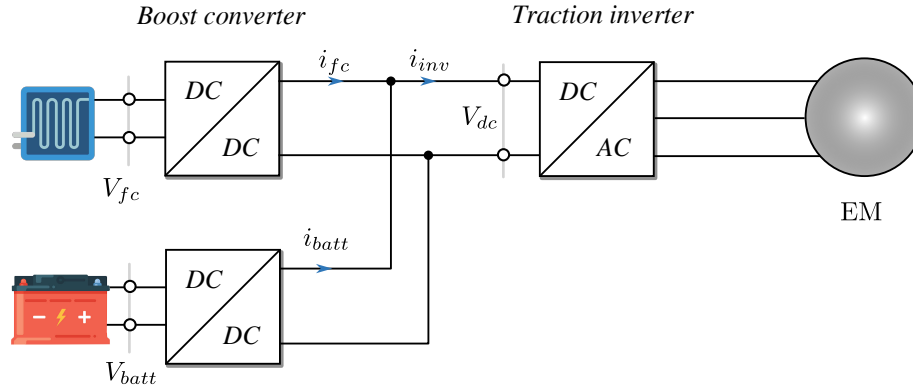


Fig. 1.2 System architecture of the proposed solution for the electrical powertrain.

1.3 System architecture

The proposed powertrain system is designed to interface a low-voltage fuel cell stack with a high-performance traction inverter, providing efficient DC voltage conversion and AC power delivery for electric propulsion. As illustrated in Fig. 1.2, the system consists of two identical DC/DC converter modules and a three-phase inverter, forming a modular and scalable architecture suitable for medium and high power fuel cell electric vehicles. This modular approach enables flexible adaptation to different vehicle power levels while maintaining high efficiency and compactness.

The fuel cell stack typically operates within a variable voltage range of 200–400 V, which must be boosted to the intermediate DC-link voltage of 400–800 V required by the traction inverter. This conversion is achieved by two interleaved multilevel DC/DC converters connected in parallel on the output side, enabling both high current handling and high voltage operation. The complete system is rated for up to 150 kW of output power, achieving an efficiency above 98% under nominal operating conditions. In addition to high efficiency, the design targets compactness and fast transient response, which are made possible by adopting WBG devices, in particular GaN for the DC/DC converter and SiC for the inverter. These features ensure stable operation during the rapid load variations typical of fuel cell systems, while also contributing to reduced volume and mass compared to conventional silicon-based converters.

The DC/DC conversion stage, implemented with GaN transistors, performs high-efficiency voltage step-up and intermediate energy buffering. It consists of two cascaded interleaved converters, referred to as the *P* and *N* units, each composed

of two magnetically coupled interleaved legs. This configuration provides effective current sharing and ripple minimization. The split DC-link capacitors, C_P and C_N , are symmetrically arranged to sustain bidirectional power flow and maintain voltage balance across the split bus.

Downstream, a SiC-based three-phase inverter converts the DC-link voltage into AC power for the traction motor. The inverter employs a compact half-bridge module topology, integrating gate-driver and control boards directly above the power module to minimize parasitic inductance and improve electromagnetic performance.

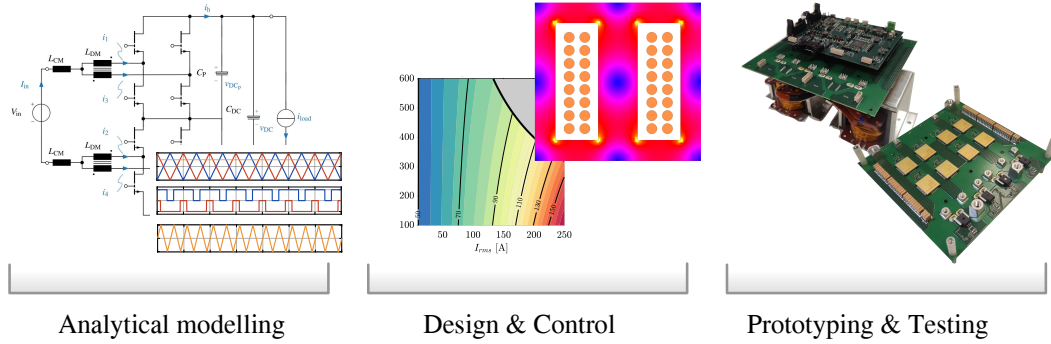


Fig. 1.3 Overview of the main subject of this dissertation: converter analysis and modeling, converter control and design with experimental validation.

1.4 Goals and contributions

The main contribution of this thesis lies in the comprehensive analysis, design, and control of the DC/DC stage (Part I), complemented by the inverter stage, which is discussed mainly in the context of testing (Part II). A final chapter presents the full powertrain DC/DC + DC/AC stage feeding an electric load, validating the full system communication setup and continuous operation. The detailed list of contributions is provided below:

- *DC/DC Converter analysis and modeling.* A systematic analytical approach is presented for the derivation and evaluation of the stress of active and reactive components of the DC/DC converter. The proposed four-leg interleaved architecture demonstrates a sixteen-fold reduction in the maximum peak flux ripple of the equivalent inductive path compared with the conventional bidirectional switching cell, together with a fourfold increase in effective ripple frequency. Furthermore, analytical considerations are also included for the design of a DC/AC inverter, including final modeling and packaging. These analytical considerations provide essential design guidelines for magnetic components and capacitor selection for the described application.
- *DC/DC Converter control.* A high-performance digital control strategy for a multilevel interleaved DC/DC converter is described, implemented and validated. A multi-loop control architecture is developed, incorporating specialized inner loops for differential current balancing and capacitor voltage regulation to ensure stable operation under all conditions. Small-signal modeling techniques provide straightforward tuning procedures for all control loops,

optimizing dynamic performance and disturbance rejection capabilities. The complete digital control system is implemented and experimentally validated, demonstrating excellent voltage regulation and robust converter operation.

- *DC/DC and DC/AC Hardware design and prototype validation* The design of the proposed multilevel interleaved DC/DC converter and a DC/AC converter is presented and described, achieving high efficiency and the expected low ripple. For the DC/DC, magnetic components, including coupled differential inductors, are sized using analytical models and FEM validation to meet peak current ripple constraints and avoid core saturation. DC-link capacitors are sized according to simulated charge ripple and voltage stress to guarantee stable operation. A prototype is built and tested accordingly. Moreover, an inverter powertrain stage is designed and fully tested through an innovative back-to-back testing solution.
- *Back-to-Back testing methodology validation* A novel B2B testing methodology is developed and validated, enabling high-fidelity characterization of power converters under realistic loading conditions. The setup features two independently controlled converters—one as the Converter Under Test (CUT) and one as an active load—interfaced through inductors and a transformer. This configuration ensures isolation, suppression of common-mode currents, and full-rated voltage and current testing, while maintaining high modularity and minimal grid power consumption. The methodology allows flexible, independent operation of both converters with minimal coordination via a CAN interface. Experimental validation confirms its effectiveness for comprehensive efficiency mapping and robust performance assessment of both prototype and full-scale converters.

1.5 Thesis outline

DC/DC Converter

► Chapter 2: Analysis

This chapter conducted an analytical derivation of the chosen high-power DC/DC converter topology for automotive fuel-cell applications. The study concluded that a non-isolated, bidirectional architecture is optimal. Moreover, the two-level converters are unsuitable for this application, as they usually lead to excessive stress for the components. Interleaved and multilevel topologies were identified as superior alternatives, leading to the proposal of a combined multilevel-interleaved converter. This topology achieves high voltage gain, reduced device stress, and minimized passive component size. The core analysis progressed from fundamental switching cells to the complete four-phase structure. The proposed converter achieves the lowest flux ripple, directly enabling a significant reduction in magnetic component size and mass. The effective ripple frequency is quadrupled, further simplifying filtering requirements. This analytical foundation confirms the proposed converter's suitability for high-performance traction systems and provides the basis for its detailed design.

► Chapter 3: Control

This chapter presented the design and implementation of a fully digital control routine for a multilevel interleaved DC/DC boost converter operating at 100 kHz. A small-signal model was derived to support the tuning of five cascaded feedback loops, including voltage and current regulation as well as auxiliary loops for capacitor voltage and current balancing. An interleaved N-type modulation scheme with 90° phase shift was adopted to improve efficiency, EMI performance, and capacitor lifetime. Particular emphasis was placed on synchronization of PWM carriers and current sampling to ensure reliable operation. The proposed strategy achieves stable voltage regulation, accurate current sharing, and robust DC-link balancing, experimentally validated.

➤ **Chapter 4: Hardware design and testing**

This chapter reports the implementation and experimental validation of the multilevel interleaved DC/DC converter. The converter was implemented using GaN power devices to ensure fast switching and high efficiency. Magnetic components and DC-link capacitors were sized according to the analytical study to achieve low ripple and reduced thermal stress. Experimental tests confirmed the expected performance in terms of voltage regulation, current sharing, and ripple reduction, validating the control strategy and the converter design. The results demonstrate that the proposed topology meets the high-power and compactness requirements for automotive fuel-cell applications.

DC/AC Converter

➤ **Chapter 5: Sizing and Design**

This chapter presented the design and analysis of a 150 kW SiC-based DC/AC traction inverter for automotive fuel-cell applications. A modular three-layer stacked layout was adopted, separating power, driver, and control stages to achieve compactness and ease of integration. A comprehensive comparison of commercial SiC power modules was performed, evaluating electrical, thermal, and packaging characteristics. The DC-link capacitor was sized using detailed simulation sweeps to ensure voltage ripple below 20 V and RMS current handling up to 95 A. The prototype assembly confirmed the feasibility of the proposed layout, providing a solid foundation for subsequent experimental validation.

➤ **Chapter 6: Hardware B2B testing**

This chapter introduces a back-to-back efficiency–mapping methodology for DC/AC converters. After outlining the limitations of conventional regenerative benches and reviewing common– and differential–mode filtering options, it proposes a test topology featuring a high–frequency Δ –Y isolation transformer that decouples the Converter Under Test (CUT) from the active load inverter. The arrangement suppresses circulating common–mode currents and removes the need for any inter–converter communication, while a simple open–loop drive for the CUT and synchronized current imposition by the load inverter enable full–power tests over arbitrary operating points (modulation index,

output frequency, current amplitude, and power factor). The approach is experimentally validated on a 30 kW GaN-based inverter, yielding accurate efficiency maps and demonstrating flexibility and modularity of the bench; results toward the 150 kW system designed are also discussed.

DC/DC and DC/AC converter communication

► Chapter 7: Full Power Conversion Integrated Control and Communication Validation

This chapter presents the validation of the full powertrain control and communication architecture integrating the DC/DC converter and the three-phase inverter. After introducing the control partitioning and distributed implementation across the two microcontrollers, the chapter details the multi-layer communication strategy, including CAN-based command exchange, UART feed-forward streaming, and timer synchronization for deterministic coordination. The control timing structure and state-machine logic ensuring safe startup and fault handling are then described. Finally, the chapter reports the experimental results demonstrating the correct synchronization, coordinated operation, and stability of the integrated system under various operating conditions.

1.6 List of Publications

Journal Papers

- Stefano Savio, Simone Giuffrida, Fabio Mandrile, Fausto Stella, Eric Giacomo Armando, and Radu Bojoi. Digital Control of Multilevel Interleaved GaN DC-DC Converter for Fuel Cell Electric Powertrains. *IEEE Transactions on Industry Applications*, pages 1–12, 2025. ISSN 0093-9994, 1939-9367. doi: 10.1109/TIA.2025.3599817
- Stefano Savio, Fabio Mandrile, Fausto Stella, Eric Armando, and Radu Bojoi. Back-to-back testing platform for inverter efficiency mapping using standard

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DC/DC Converter

Chapter 2

DC/DC Converter - *Analysis*

2.1 Introduction

This chapter focuses on a comprehensive analytical comparison of various DC/DC converter topologies, with particular focus on non-isolated configurations suitable for high-power automotive applications in electric and fuel cell vehicles. The analysis systematically evaluated the performance characteristics of different converter architectures, including conventional bidirectional switching cells, three-level configurations with and without midpoint connection, interleaved structures with common- and differential-mode considerations, and ultimately the complete multilevel interleaved GaN-based converter topology. Through detailed mathematical modeling and simulation, key performance metrics such as inductor flux ripple stress, capacitor current stress, and semiconductor switching stresses are quantitatively assessed under different operating conditions and duty cycle ranges. The analytical framework established in this chapter provides crucial insights into the trade-offs between component stresses, efficiency and implementation complexity.

2.1.1 State-of-the-Art high-voltage DC/DC converter topologies

Selecting an appropriate DC/DC converter topology is critical in electric vehicles and plug-in hybrid vehicles because it directly affects system efficiency, size, and cost [35]. A survey of EV/PHEV converter architectures notes that the choice of topology strongly influences electromagnetic compatibility (EMC), reliability and

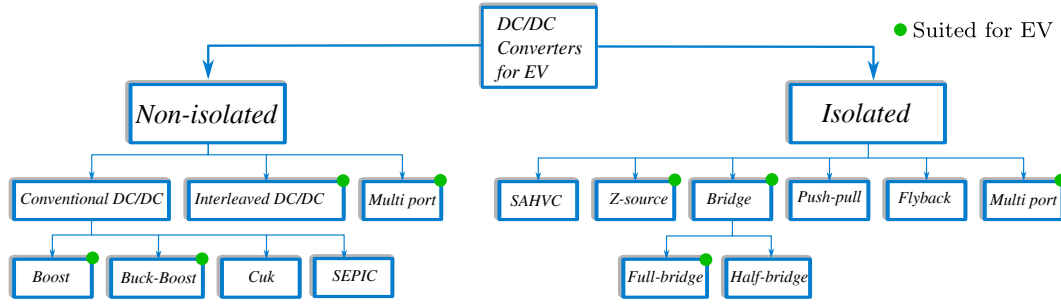


Fig. 2.1 Main DC/DC State-of-the-Art Converter topologies.

power density [36]. Generally, converters can be categorized according to isolation and power-flow direction. Non-isolated converters are often preferred at high-power levels (e.g. >10–50 kW) due to their lower cost and simpler control [37]. For example, [38] presents a review of boost-derived high-gain non-isolated DC/DC converters and discusses the trade-offs in semiconductor voltage stress, component count, and conversion ratio. In contrast, isolated topologies (e.g. forward, flyback, full-bridge) can provide galvanic isolation but typically at the expense of added components and lower power density in high-power traction systems. In parallel with isolation, converters are also categorized by unidirectional or bidirectional power flow. Fig.2.1 presents an overview of the main DC/DC converter topologies. In typical EV architectures, the battery-side converter must be bidirectional to support regenerative braking, while the fuel-cell interface can be unidirectional. However, for design unity and scalability, bidirectional converters are chosen on both sides. Bidirectional converters allow boosting battery voltage during motoring and step it down during regeneration [35]. In [35], it is shown that bidirectional converters are essential in vehicle energy management, and it is noted that three-level bidirectional converters often achieve higher efficiency and smaller magnetic size than equivalent two-level buck/boost converters.

Conventional bidirectional topologies (e.g. synchronous buck–boost cells) can handle moderate voltage differences but suffer when high step-up ratios are needed. Bidirectional Two-switch boost or buck–boost converters exhibit high voltage and current stress at high duty cycles, limiting efficiency and requiring large components [39]. Similarly, single-switch boost or buck–boost converters (non-interleaved) impose high ripple on the input current and require bulky inductors at high power. Even variants such as Cuk or SEPIC converters achieve simultaneous step-up/down, but also suffer from low efficiency and excessive component stress in high voltage

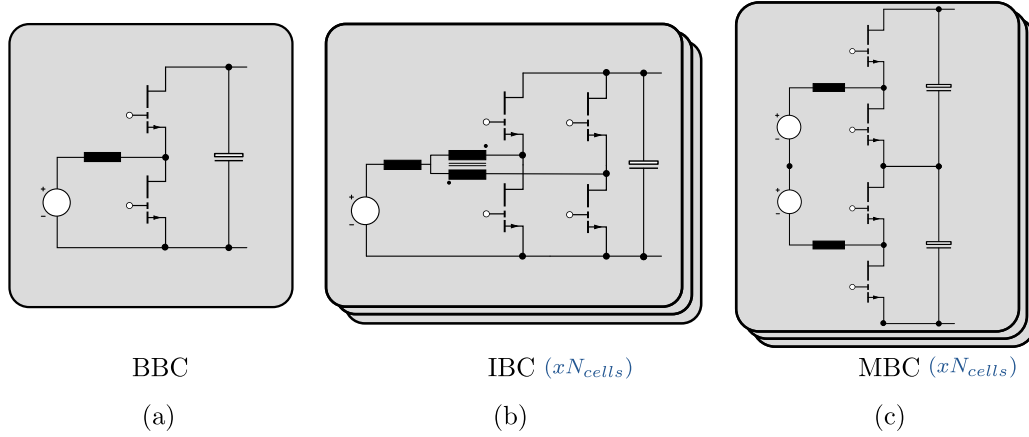


Fig. 2.2 (a) Bidirectional boost converter (BBC), (b) Interleaved boost converter (IBC), (c) Multilevel boost converter (MBC).

ratios [39]. In high-gain traction applications, conventional two-level converters may require extreme duty ratios and are subjected to high current ripple, switching stress, and EMI. The device-voltage-rating constraint is particularly relevant for GaN implementations connected to an 800 V DC bus, whereas suitably rated SiC devices can generally withstand the bus voltage.

To meet the demanding HV step-up (e.g. 48–400V or 400–800V) and power (>50kW) requirements of fuel-cell propulsion, more advanced topologies have been proposed. Fig.2.2 outlines several candidate architectures considered in the literature. A widely studied family is the non-isolated interleaved boost converter (IBC) [40, 41]. An N -phase IBC replicates N standard boost cells in parallel, using phase-shifting of their gate signals. Interleaving distributes the input current among multiple inductors (often coupled) and effectively multiplies the switching ripple frequency (to Nf_{sw}) seen by each magnetic element [42, 43]. For example, a 4-phase IBC can reduce input and output ripples almost as if a much larger single inductor were used, yet with smaller magnetics and faster transient response [44, 43]. In [42], it is demonstrated that using coupled inductors in a four-phase IBC (as in the Honda Clarity fuel-cell vehicle) can drastically shrink the volume and achieve high power density. The phase-shifted architecture also increases the effective switching frequency seen by each phase, yielding lower EMI emissions and enabling smaller filter size [44, 45]. In practice, IBCs are often implemented with multi-phase (4–8 phases) and coupled inductors to optimize the ripple reduction [14, 42]. Such designs have demonstrated efficiencies on the order of 85–95% in laboratory fuel-cell/DC

tests [43]. For example, in [43] an efficiency of $\approx 90\%$ for a 1.2 kW PEMFC using a four-phase IBC is achieved. Overall, interleaving is a mature technique that improves dynamic performance and EMI at the cost of additional inductors, switches and control complexity.

The main drawback of a pure interleaved boost converter for HV is the high voltage gain stress per stage. A single-stage boost converter has a limited gain. To achieve very high step-up ratios, cascaded boost stages must be employed (e.g. two or more boost cells in series) [40, 14]. However, cascading increases component count and conduction paths, raising the cost and reducing power density [38, 46]. In summary, while the IBC topology is simple and effective for moderate gains, in high-voltage automotive applications the device voltage stress and component count become problematic. This motivates exploration of modified boost and multilevel converter families that intrinsically achieve higher gain or distribute stress.

One alternative is the non-isolated multilevel boost converter (MBC). The classical multilevel boost uses stacked capacitors to realize an N -level output with only one inductor and one switch [47]. Such topologies can reach large DC gains without extreme duty ratios, since each level contributes a portion of the voltage. More recent variants include dual-switch and switched-capacitor boost hybrids [48]. These converters improve the static gain and reduce switch stress (dividing voltage across capacitors), they impose tighter capacitor voltage balancing requirements and eventually increase the diode or MOSFET count [47, 49]. Double-frequency multilevel boost schemes, for instance, achieve doubled effective frequency operation by alternating two sub-converters, enhancing efficiency at different loads [48]. In general, multilevel boost converters are promising for large step-up ratios, but their complexity and the need for capacitor voltage balancing networks are challenges. In addition, many MBC designs have only been demonstrated at relatively low power or single-switch count, so their applicability to multi-kW traction systems requires careful evaluation.

Another promising class is the three-level (or higher) interleaved converter. By introducing additional voltage levels (through flying capacitors or stacked half-bridges), one can split the voltage stress across multiple devices. For example, in [35], bidirectional three-level DC/DC converters are compared to two-level buck/boost and interleaved variants, finding that the three-level topology yielded higher efficiency and smaller inductor size under automotive driving profiles. Likewise, [50] analyzed

a 3-level interleaved boost with a coupled inductor, showing improved performance for fuel-cell boost conversion. Other recent works [51, 52] explore three-level interleaved converters with common-leg coupled inductors for medium-voltage applications. These designs can operate as bidirectional interfaces and have been demonstrated at the 10–20kW scale (e.g. 750V bipolar DC-link) with SiC devices. Such multilevel-interleaved converters combine the low ripple of multi-phase operation with reduced device stress of multilevel stages, making them attractive for fuel-cell/battery traction interfaces. However, they require more switches and precise capacitor voltage control, which adds control complexity and parts count.

In summary, the state of the art includes basic boost-based converters (buck, boost, buck–boost, Cuk, SEPIC), interleaved-multi-phase boost converters, and hybrid multilevel or interleaved topologies. Surveys underline that for high-power vehicular use, the most suitable topologies tend to be those with low ripple and modular construction (e.g. multidevice interleaved bidirectional converters) [37]. Figure 2.2 illustrates the subset of topologies considered in this work, focusing on non-isolated, boost-based converters that can achieve the high gains and bidirectional capability needed for fuel-cell traction.

2.1.2 Design challenges

Each DC/DC topology has inherent trade-offs when applied to high-voltage automotive traction. As previously noted, conventional two-level boost or buck–boost converters are simple and robust, but their voltage gain is limited without resorting to very high duty ratios, which in turn increases switch stress and losses [38]. In addition, single-phase converters have large input and output ripples unless oversized inductors and capacitors are used. Thus, they tend to have lower power density and higher EMI when pushed to HV/high-power conditions. Bidirectional versions of these converters further complicate control and may require snubbers or auxiliary switches for efficient soft switching.

Interleaved boost converters address the ripple issue by paralleling phases, but at the cost of more components. Each additional phase adds an inductor, a diode, and an extra switch, increasing gate-drive and control complexity. While interleaving reduces current stress per inductor, it also requires careful current sharing to avoid imbalance. Coupled-inductor variants (e.g. inverters with common-leg coupling)

can save volume but introduce mutual leakage and saturation considerations [42, 52]. Moreover, even interleaved boost requires multiple stages or extremely high duty to reach very high gains; cascading phases multiplies complexity and internal conduction losses. Multilevel converters mitigate voltage stress by splitting the voltage across several capacitors or switches. In a flying-capacitor MBC, for instance, balancing capacitors is nontrivial and the diode/capacitor count grows the number of levels. Fault tolerance is also reduced: a single capacitor failure can unbalance the voltages across the healthy floating capacitors. Moreover, multilevel topologies typically have more parasitic elements and snubbers, making them bulky. Three-level topologies require floating capacitors or modular subunits (e.g. half-bridges), which need active balancing circuits and additional control loops. The PWM schemes become more complex to maintain balanced voltages and bidirectional current. In short, higher-level topologies improve gain and stress but add significant component cost and control overhead.

Isolated converters, not discussed in this dissertation, can isolate voltages and achieve high gain with fewer stages, but their transformers are heavy at power levels exceeding 50 kW and their resonant/forward topologies often operate with lower bandwidth. For on-board automotive use, additional isolation may be unnecessary since the chassis can serve as a ground reference [21]. Table 2.1 summarizes key pros and cons. Table 2.1 provides a detailed qualitative comparison of the considered topologies, while Fig. 2.3 summarizes their relative performance in terms of efficiency, reactive element stress, power density, and implementation simplicity.

In addition to topology-specific issues, all converters must withstand the harsh automotive environment: wide temperature range, reliability demands, and stringent EMI standards. Any topology chosen for fuel-cell traction must be robust to source voltage fluctuation (fuel cell output varies with load) and must efficiently handle both high-current and high-voltage operation. These topologies should be implemented with wide-bandgap devices (SiC/GaN) to push switching frequency while limiting losses. These considerations significantly narrow the field: the topology should minimize stress, minimize passive component size (for power density), and support bidirectional power flow without excessive hardware overhead.

Table 2.1 Comparison of main non-isolated converter topologies

Topology	Pros	Cons
Single-phase boost / buck–boost	Simple, low-cost, well known	High switch stress, large ripple, poor efficiency at high gain [39, 38].
Interleaved boost	Ripple reduction, shared current, better EMI [44, 43]	Requires N inductors/switches, complex control, gain still limited [38, 46].
Multi-stack interleaved	Very high voltage gain [40]	High component count, higher losses, reduced power density [46].
Multilevel boost	High static gain, lower switch stress [47]	Many capacitors/diodes, balancing issues, complex PWM, not easily bidirectional.
Three-level interleaved (bidirectional)	Half switch voltage stress, ripple cancellation, high efficiency, smaller magnetics [35, 53]	More devices, flying capacitors, complex capacitor balancing and bidirectional control.

2.1.3 Benefits of the proposed topology

Based on the previous considerations, the proposed solution is a multilevel-interleaved bidirectional boost converter, implemented with GaN devices. This architecture combines the advantages of multilevel voltage handling with interleaving, directly addressing the aforementioned challenges. Specifically:

- **High voltage gain with reduced component stress:** By stacking half-bridge modules, the total voltage step-up is divided among multiple devices. Each switch only experiences a fraction (e.g. one-half) of the full DC-link voltage. This significantly lowers the voltage rating required per device. As a result, lower-voltage (and lower-conduction-loss) transistors can be used while achieving the same overall HV conversion [35, 36]. For fuel-cell interfacing, this means safely boosting from 200–300V to the 400–800V traction bus without very high duty cycles.

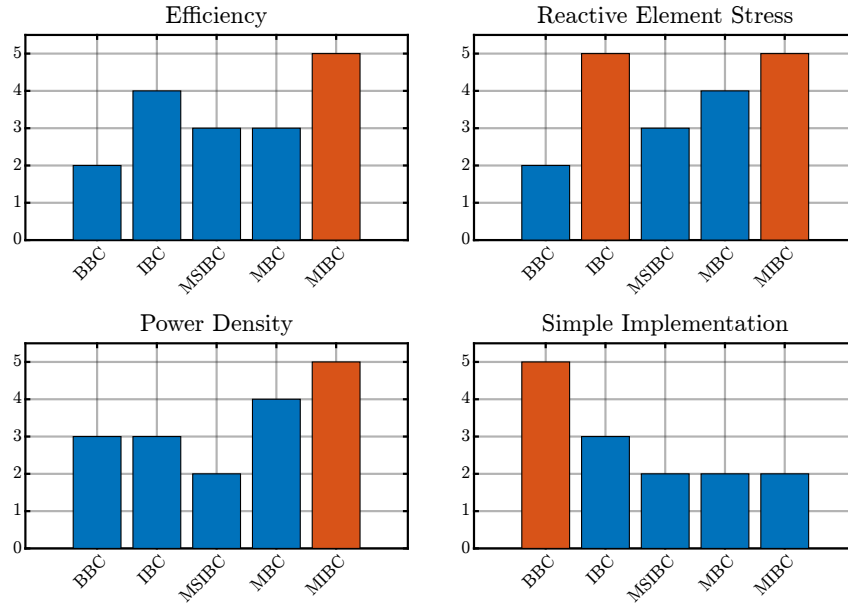


Fig. 2.3 Metric comparison of non-isolated high-voltage DC/DC converter topologies for fuel-cell traction applications, based on four criteria: efficiency, reactive element stress, power density, and simplicity of implementation. The red bars indicate the best-performing topologies for each metric.

- **Ripple reduction and higher effective frequency:** Each bridge or cell is interleaved (phase-shifted) with the others. The input and output ripples from each leg partially cancel, reducing the size of required inductors and capacitors [44, 43]. Effectively, the converter operates at an N -times higher switching frequency as seen by the magnetics, allowing smaller magnetics and better transient response [44]. Reduced ripple improves fuel-cell source stability and makes the DC-link smoother for the inverter.
- **High efficiency with wide-bandgap devices:** The reduced device stress and multi-phase structure facilitate the use of GaN or SiC transistors operating at higher switching frequencies with low losses [36, 30]. Higher switching frequency allows for smaller inductors and capacitors, significantly increasing the overall power density.
- **Bidirectional power flow:** By using symmetrical multilevel bridges, the converter naturally supports bidirectional operation. During traction, it steps up battery voltage to the high-voltage link; during regenerative braking, the same hardware steps down the HV back to the battery. The three-level interleaved bidirectional topology presented in [35] showed 93% peak efficiency

in both directions. Indeed, the multilevel topology presented preserves this bidirectional capability while further reducing stress.

- **Reduced EMI and switching loss through interleaving:** With multiple phases interleaved, each phase can operate at a lower individual current, reducing I^2R losses in inductors. Also, the phase-shifting spreads the EMI spectrum and simplifies filtering [44, 54]. Any common-leg coupling technique (as in [52]) can further mitigate stray inductance and noise.

In conclusion, the multilevel-interleaved topology offers a good compromise: it achieves the high voltage gain and bidirectional capability needed for fuel-cell/battery traction while maintaining high efficiency and reduced ripple. The trade-off is higher component count compared to a single boost, but this is justified by the gains in performance. Compared to other high-gain topologies, the proposed converter uses fewer series stages and better distributes stresses, enabling a more compact, high-density design. By leveraging recent results on coupled inductors and SiC/GaN switching [42, 30], it promises to meet the stringent requirements of automotive fuel-cell powertrains.

Overall, the chosen multilevel-interleaved DC/DC converter represents a state-of-the-art solution, combining the best features of interleaving (low ripple, high effective switching rate) and multilevel conversion (high gain, low device stress) to address the challenges of high-voltage fuel cell interfacing [35, 36, 30].

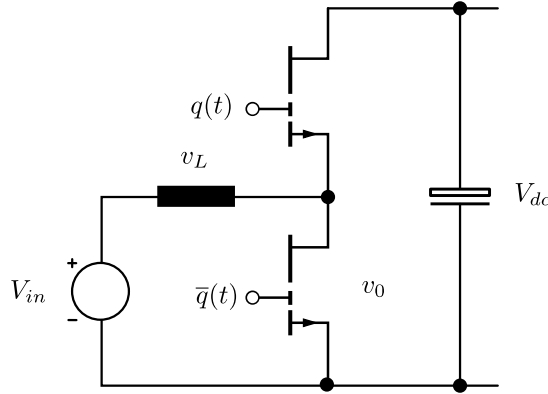


Fig. 2.4 Symbolic representation of a bidirectional switching cell.

2.2 Analysis of inductor flux ripple stress

2.2.1 Base: Bidirectional switching cell

A preliminary analysis of the basic structure is carried out to understand the working principle of the complete DC/DC three-level interleaved GaN architecture. As a first step, a brief explanation of the basic switching cell is provided, presented in Fig. 2.4. The duty cycle d , evaluated according to the buck converter rule [55], and the voltage v_L across the inductor at steady state are defined as (2.1) and (2.2), where $q(t)$ represents the switching function of the converter:

$$d = \frac{V_{in}}{V_{dc}} \quad (2.1)$$

$$v_L = V_{in} - q(t)V_{dc} \quad (2.2)$$

To show the significant current ripple reduction achieved with the DC/DC Three-level interleaved converter, the alternating component of the flux ripple is analytically evaluated. In general, the flux Φ across an inductor L can be expressed by (2.3):

$$\Phi(I_L) = L \cdot I_L + \Delta\Phi_L \quad (2.3)$$

where $\Delta\Phi_L$ denotes the alternating component of the flux ripple across the inductor, while LI_L represents its DC bias, where I_L is the average current flowing through it.

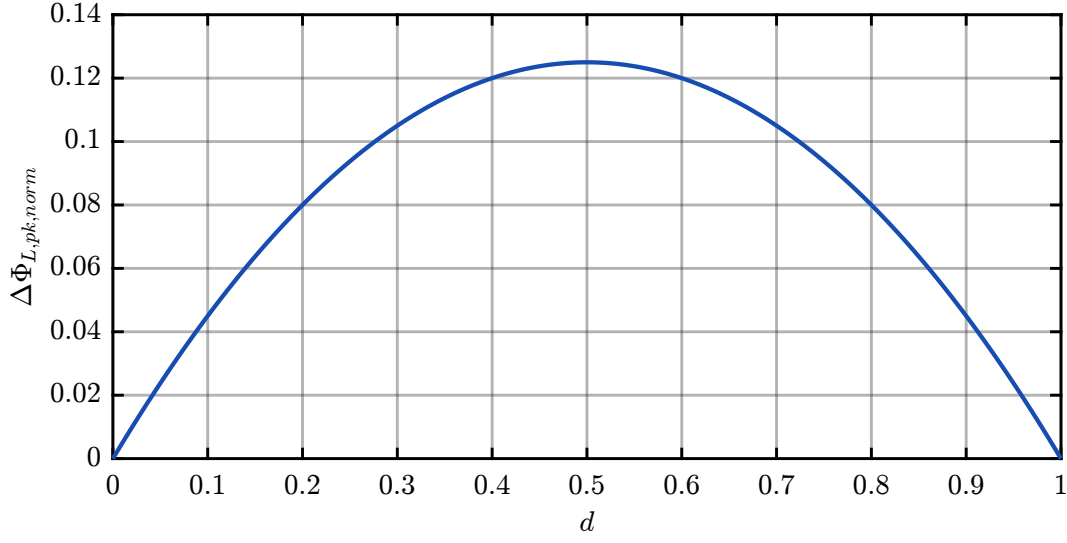


Fig. 2.5 Normalized flux ripple $\Delta\Phi_{L,pk,norm}$ across the inductor L of a bidirectional switching cell as a function of the duty cycle d .

As expected, when $\bar{q}(t)$ is on, the voltage v_L across the inductor is $V_{max,L} = V_{in}$. When $q(t)$ is conducting, $v_L = V_{min,L} = V_{in} - V_{dc}$. As can be noticed, the flux ripple is strictly related to the voltage drop across the inductor L . As is known from the literature [55], the flux can be estimated as:

$$\Phi(t) = \int_0^t v_L(\tau) d\tau \quad (2.4)$$

and the peak inductor flux value can be consequently evaluated as:

$$\begin{aligned} \Delta\Phi_{L,pk} &= (V_{dc} - V_{in}) \frac{T_{on}}{2} \\ &= (V_{dc} - d \cdot V_{dc}) \frac{d \cdot T_{sw}}{2} = V_{dc} \cdot (1 - d) \frac{d}{2} \end{aligned} \quad (2.5)$$

As a result from (2.5), the maximum peak flux value is achieved for a duty cycle $d = 0.5$, and it is equal to:

$$\Delta\Phi_{L,pk|_{max}} = \frac{T_{sw}}{8} \cdot V_{dc} \quad (2.6)$$

Normalizing by $V_{dc} \cdot T_{sw}$ (constant for all the analysis at $V_{dc} = 800V$ and $T_{sw} = 10\mu s$) the flux ripple variation can be expressed as in Fig. 2.5.

Based on the maximum flux ripple and maximum desired current ripple, the minimum inductor value can be designed according to equation 2.7.

$$L = \frac{\Delta\Phi_{L,pk|max}}{\Delta i_{L,pk|max}} \quad (2.7)$$

2.2.2 Step 1: Three-level DC/DC converter with dual voltage supply

Based on the preliminary bidirectional switching cell model, a further step in the modeling can be performed by analyzing the behavior of a three-level boost converter (TLBC) with connected midpoint, as presented in Fig. 2.6. In this configuration, the V_{in} voltage source is divided into two voltage sources in order to provide access to the connection to the midpoint O' . The presented structure can then be presented as two vertically symmetric bidirectional cells, respectively called H and L . In this manner, the voltages v_{01} and v_{02} are balanced and referenced to the midpoint O_1 . Furthermore, the PWM is the same for the two cells. As a consequence, the duty cycle d is applied to the devices $q_H(t)$ and $q_L(t)$. The duty-cycle equation presented for the bidirectional switching cell in the previous section is still valid. Fig. 2.7 presents the key waveforms of the three-level converter with the midpoint connected.

The midpoint connected to the two cells is wired to the source midpoint. As a consequence, $v_O = v_{O'} = v_{01} - v_{02} = 0$. Indeed, the voltages v_{01} and v_{02} experience a voltage drop of $V_{dc}/2$ when the high-side switch is on. As a consequence, the maximum flux ripple across the represented inductors (with $L/2$ inductance each) can be expressed as in (2.6), but is reduced by a factor of 2, as in (2.8).

$$\Delta\Phi_{L,pk|max} = \frac{1}{2} \cdot \frac{T_{sw}}{8} \cdot V_{dc} = \frac{T_{sw}}{16} \cdot V_{dc} \quad (2.8)$$

Fig. 2.8 presents the normalized flux ripple across the inductors as a function of the duty cycle d .

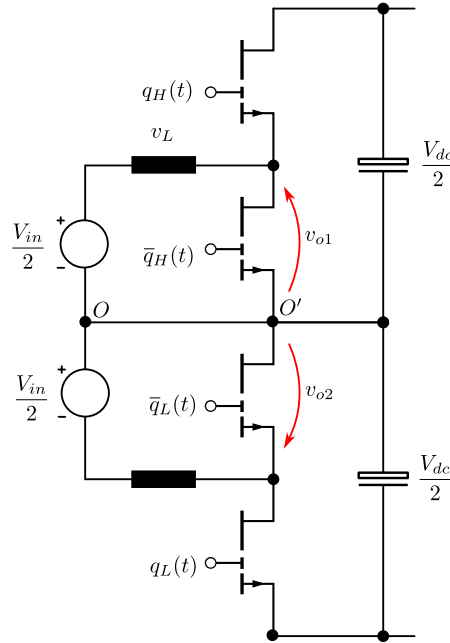


Fig. 2.6 Symbolic representation of a three-level converter with mid-point connected.

2.2.3 Step 2: Three-level DC/DC converter with single voltage supply

As previously discussed, the presented topology does not fully exploit all its degrees of freedom regarding the modulation techniques. In order to take advantage of the additional benefits offered by the structure, the connection between OO' must be removed, and the PWM modulation strategy must be carefully redefined. Building upon the previous analysis, the next step is to investigate the case in which the midpoint connection between O and O' is removed. The corresponding circuit representation is shown in Fig. 2.9.

In this configuration, the structure can still be represented by two symmetric poles (H and L), but the absence of the midpoint connection modifies the modulation strategy as well as the inductor flux behavior.

In this case, the PWM modulation of the two poles is not identical. The triangular carriers are shifted by 180° and compared with the same duty cycle, as illustrated in Fig. 2.10. This modulation scheme results in alternating voltage levels across the poles, while maintaining the same average duty cycle applied to both. As a

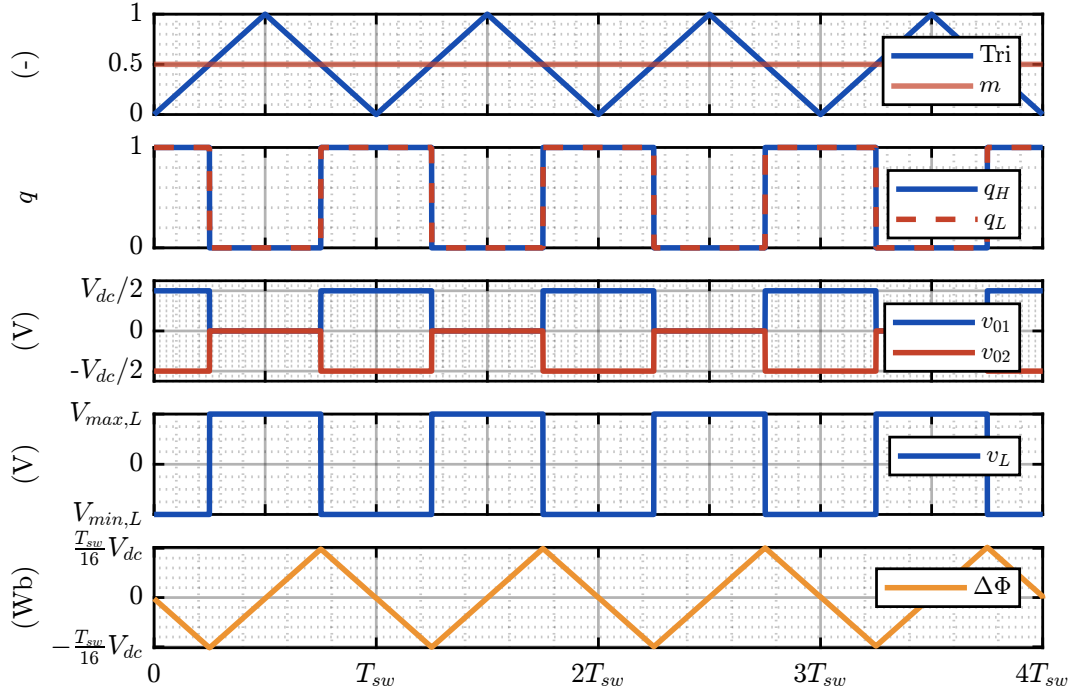


Fig. 2.7 Key waveforms of a three-level converter with the midpoint connected and operated with a duty cycle d . From the top: The triangular carrier is compared to a modulating signal m to generate the PWM signal for H and L . The output voltages v_{01} and v_{02} across the low-side switch of each pole, inductor voltage v_L and differential flux $\Delta\Phi_L$ across the top inductor.

consequence, the inductor flux ripple becomes dependent on the duty cycle in a different manner compared to the midpoint-connected case.

Two operating cases can be distinguished:

- Case 1: $d > 0.5$, $V_{in} > \frac{V_{dc}}{2}$.
- Case 2: $d < 0.5$, $V_{in} < \frac{V_{dc}}{2}$.

Case 1: $d > 0.5$

The peak flux ripple, assuming a single inductor, is expressed as:

$$\Delta\Phi_{L,pk} = \frac{T_{OFF}}{2} \cdot \left(\frac{V_{dc}}{2} - V_{in} \right) = \frac{1}{2} V_{dc} \cdot T_{SW} \cdot (1-d) \cdot \left(d - \frac{1}{2} \right). \quad (2.9)$$

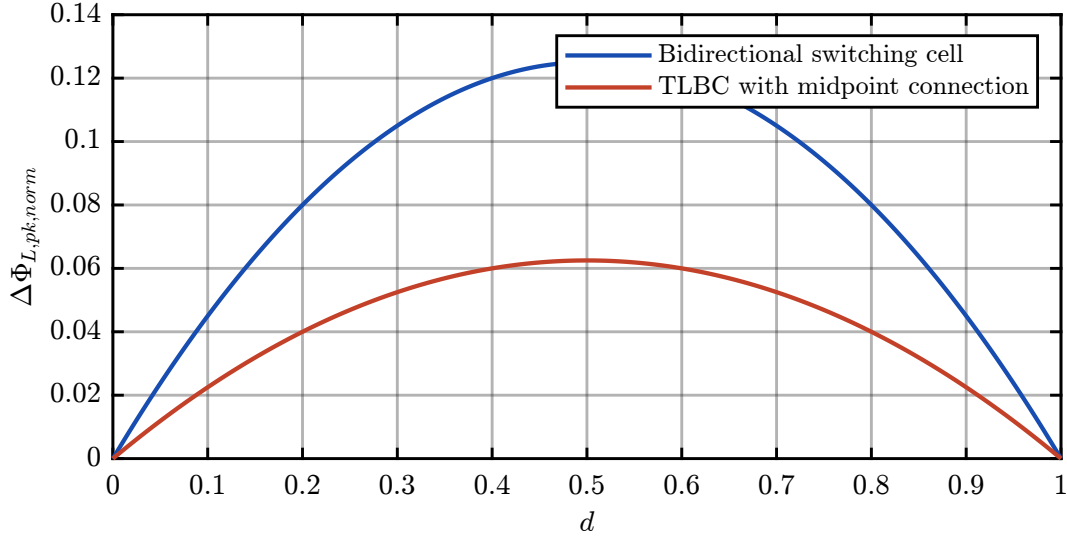


Fig. 2.8 Normalized flux ripple $\Delta\Phi_{L,pk,norm}$ across the inductors L_1 and L_2 of a three-level converter with midpoint O connected as a function of the duty cycle d .

The maximum value is obtained for $d = 0.75$:

$$\Delta\Phi_{L,pk}|_{MAX} = \frac{1}{32}V_{dc} \cdot T_{sw}. \quad (2.10)$$

Case 2: $d < 0.5$

A similar derivation can be carried out for $d < 0.5$:

$$\Delta\Phi_{L,pk} = \frac{T_{ON}}{2} \cdot \left(\frac{V_{dc}}{2} - V_{in} \right) = \frac{1}{2}V_{dc} \cdot T_{sw} \cdot d \cdot \left(\frac{1}{2} - d \right). \quad (2.11)$$

The maximum value in this case occurs at $d = 0.25$:

$$\Delta\Phi_{L,pk}|_{max} = \frac{1}{32}V_{dc} \cdot T_{sw}. \quad (2.12)$$

When two inductors are employed instead of a single one, the maximum flux ripple across each inductor is halved with respect to the values obtained in (2.11) and (2.12):

$$\Delta\Phi_{L,pk}|_{max}(\text{per inductor}) = \frac{1}{64}V_{dc} \cdot T_{sw}. \quad (2.13)$$

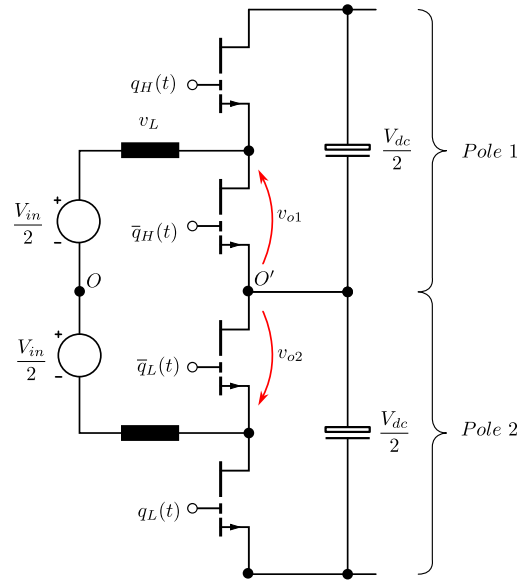


Fig. 2.9 Symbolic representation of a three-level converter without mid-point connected.

Figure 2.10 shows the normalized flux ripple as a function of the duty cycle. The two maximum points occur at $d = 0.25$ and $d = 0.75$.

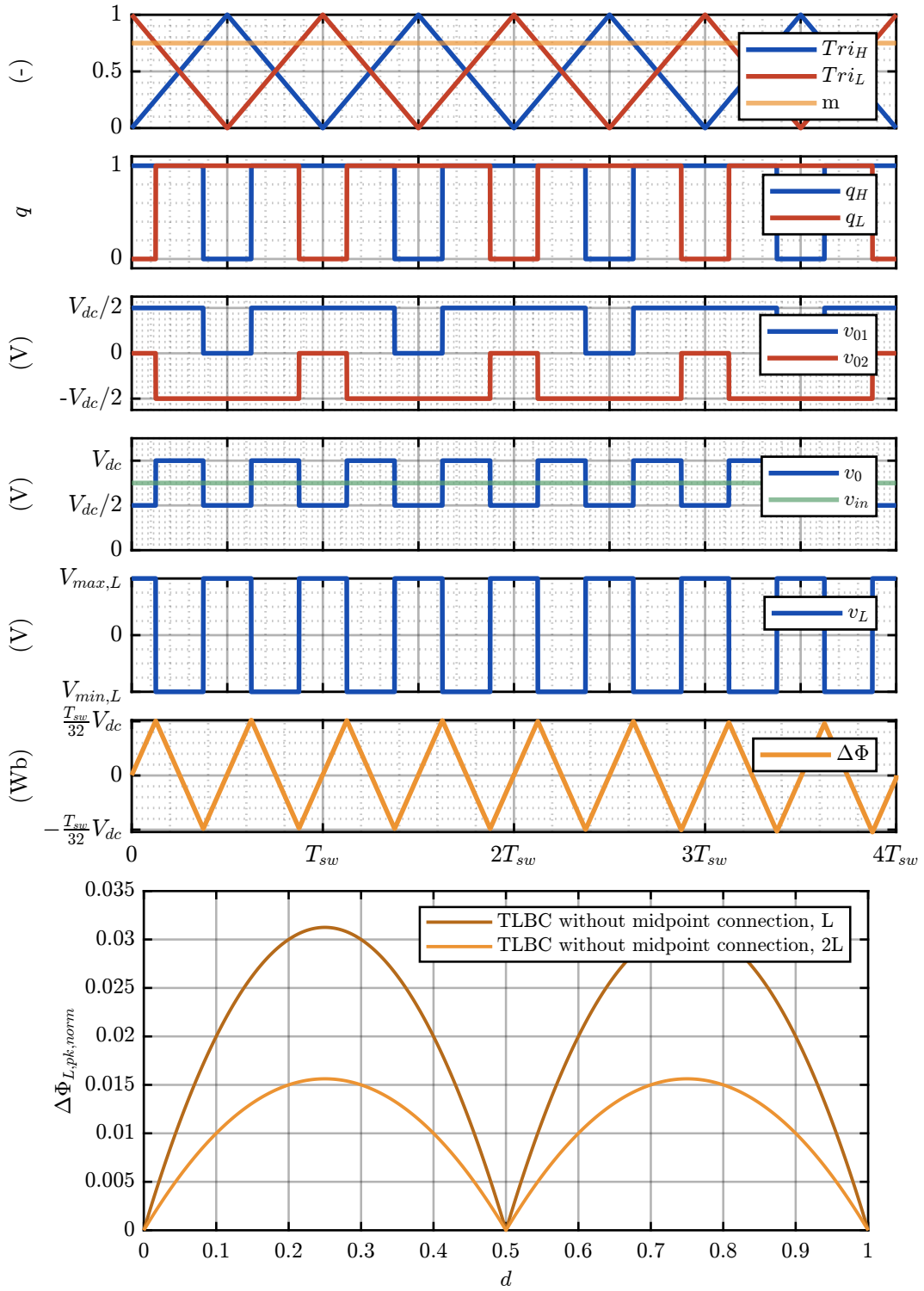


Fig. 2.10 (a) Key waveforms of a three-level converter without the midpoint connected. (b) Normalized flux ripple as a function of the duty cycle for two inductors in series (blue curve) and a single inductor (red curve).

In this case, the PWM modulation applied to *Pole 1* and *Pole 2* is no longer identical. The two triangular carriers are shifted by 180° and compared with the same duty cycle.

2.2.4 Step 3: Interleaved structure: common- and differential-mode inductor considerations

The interleaved structure is a well-established solution to reduce the current ripple in the inductors, thereby allowing a smaller magnetic component design. The considered configuration is illustrated in Fig. 2.11. Two half-bridge legs are connected in parallel, forming a two-phase interleaved system. The coupled inductor consists of two identical windings magnetically coupled through a common core. As a result, the dominant magnetic energy is associated with the differential-mode current component. Specifically, the total output power transfer is associated with the sum of the phase currents, whereas their difference determines the core magnetization.

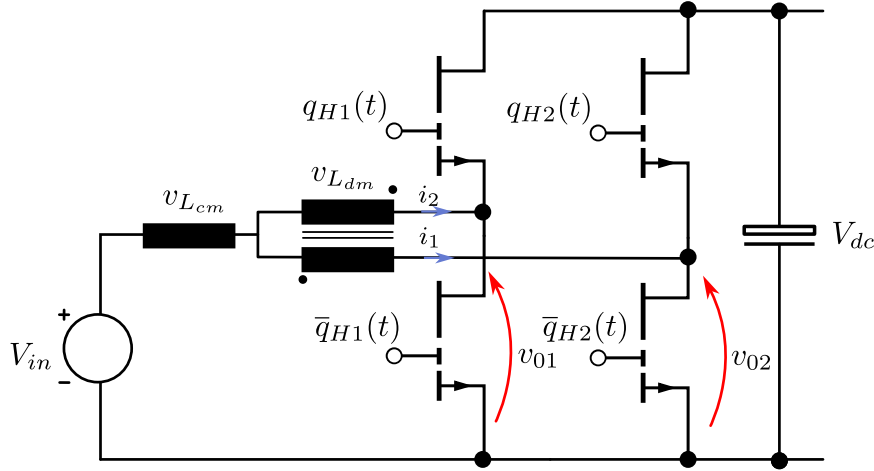


Fig. 2.11 Symbolic representation of an interleaved converter.

To formalize the behavior of the system, it is convenient to introduce the common-mode (CM) and differential-mode (DM) coordinates. The voltages applied to the two half-bridge legs, v_{01} and v_{02} , can be transformed into the equivalent inductor voltages v_{Lcm} and v_{Ldm} by means of the linear transformation

$$\begin{bmatrix} v_{Lcm} \\ v_{Ldm} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} v_{01} \\ v_{02} \end{bmatrix}. \quad (2.14)$$

Equation (2.14) defines the mapping from the physical phase domain into the modal domain of the coupled inductor. The factor $1/2$ defines the common- and differential-mode quantities as the half-sum and half-difference of the corresponding physical variables. With this scaling, the transformation matrix U is symmetric and invertible, but it is not orthogonal, since $U^T U = \frac{1}{2}I$. Its inverse is given in 2.15.

$$U = \frac{1}{2} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}, \quad U^{-1} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} = 2U. \quad (2.15)$$

The same formulation can be consistently applied to flux linkages and currents:

$$\begin{bmatrix} \Phi_{L_{cm}} \\ \Phi_{L_{dm}} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} \Phi_1 \\ \Phi_2 \end{bmatrix}, \quad (2.16)$$

$$\begin{bmatrix} i_{L_{cm}} \\ i_{L_{dm}} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}. \quad (2.17)$$

Accordingly, the modal inductances can be defined as

$$L_{cm} = \frac{\Phi_{cm}}{i_{cm}}, \quad L_{dm} = \frac{\Phi_{dm}}{i_{dm}}. \quad (2.18)$$

This representation highlights the physical role of each mode: the common-mode component represents the flux driven by the in-phase component of the leg currents, while the differential-mode component is excited by their opposing contribution. The interleaving strategy introduces an additional degree of freedom: by modulating the two legs with a 180° phase shift, the ripple components in the inductor fluxes can be substantially reduced.

Depending on the duty cycle d , two operating regions arise. For $V_{in} < V_{dc}/2$ (i.e., $d < 0.5$), the key waveforms are shown in Fig. 2.12. In this condition, the common-mode inductor voltage $v_{L_{cm}}$ exhibits a second-harmonic component at frequency $2f_{sw}$, whereas the differential-mode inductor voltage $v_{L_{dm}}$ displays a first-harmonic behavior with three discrete levels. The corresponding peak flux ripples are:

$$\begin{aligned} \Delta\Phi_{L_{cm},pk} &= \frac{1}{4}d \cdot (1 - 2d) \cdot T_{sw}V_{dc}, \\ \Delta\Phi_{L_{dm},pk} &= \frac{1}{4}d \cdot T_{sw}V_{dc}. \end{aligned} \quad (2.19)$$

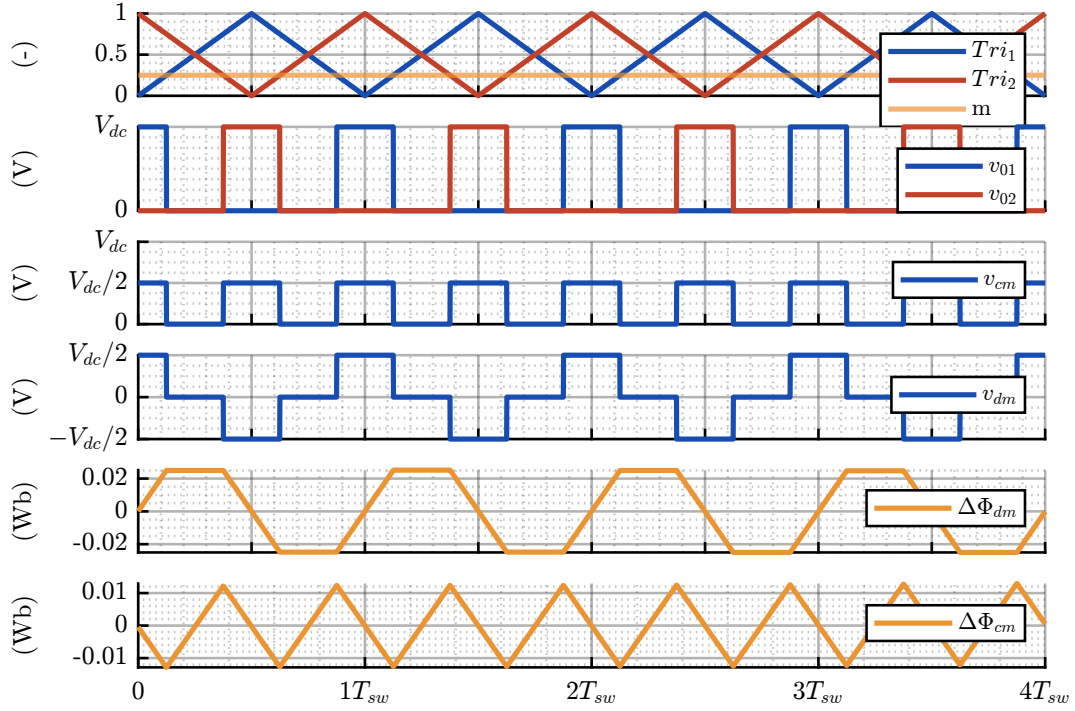


Fig. 2.12 Key waveforms of the interleaved structure with $d < 0.5$. From top to bottom: PWM carriers and modulating signal, pole voltages, common-mode inductor voltage $v_{L_{cm}}$, differential-mode inductor voltage $v_{L_{dm}}$, common and differential flux ripple.

In the middle condition where $V_{in} \approx V_{dc}/2$ the functional waveforms are presented in Fig. 2.13. When $V_{in} > V_{dc}/2$ (i.e., $d > 0.5$), the common-mode inductor voltage oscillates between $V_{dc}/2$ and V_{dc} , while the differential-mode voltage remains unchanged. The resulting flux ripple amplitudes are:

$$\begin{aligned}\Delta\Phi_{L_{cm},pkpk} &= \frac{1}{4}d \cdot (1-d) \cdot (2d-1) \cdot T_{sw}V_{dc}, \\ \Delta\Phi_{L_{dm},pkpk} &= \frac{1}{4}(1-d) \cdot d \cdot T_{sw}V_{dc}.\end{aligned}\tag{2.20}$$

By combining the two regions, the normalized flux ripple in both modes as a function of duty cycle can be summarized as in Fig. 2.14. It is evident that the maximum common-mode flux ripple occurs at $d = 1/4$ and $d = 3/4$, while it becomes zero at $d = 1/2$. Conversely, the differential-mode flux ripple reaches its maximum at $d = 1/2$, as shown in Fig. 2.13. This behavior is consistent with the physical interpretation of the modal decomposition: perfect balance at $d = 0.5$ cancels the common-mode flux, leaving only the differential component, whereas

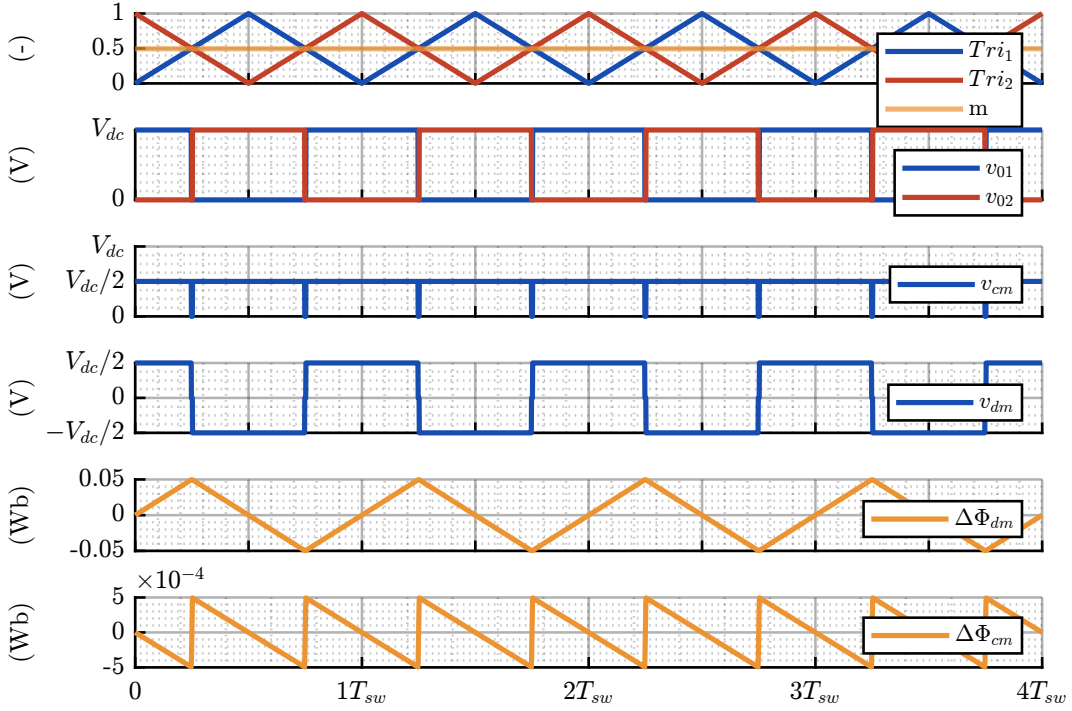


Fig. 2.13 Key waveforms of the interleaved structure with $d = 0.5$. From top to bottom: PWM carriers and modulating signal, pole voltages, common-mode inductor voltage $v_{L_{cm}}$, and differential flux ripple.

imbalance in the duty ratio reintroduces a significant common-mode contribution. Based on Fig. 2.14, the L_{dm} inductance can later be extracted as

$$L_{dm} = \frac{\Delta\Phi_{L_{dm},pkpk}}{\Delta i_{dm}} \quad (2.21)$$

For the sake of clarity, it is important to emphasize the relationship between the modal inductances defined above and the original self- and mutual inductances of the coupled inductor. Considering the inductance matrix in the physical domain

$$\mathbf{L} = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{22} \end{bmatrix}, \quad (2.22)$$

the transformation (2.15) diagonalizes the system into the common-mode (CM) and differential-mode (DM) basis. In the case of a symmetric coupled inductor, where

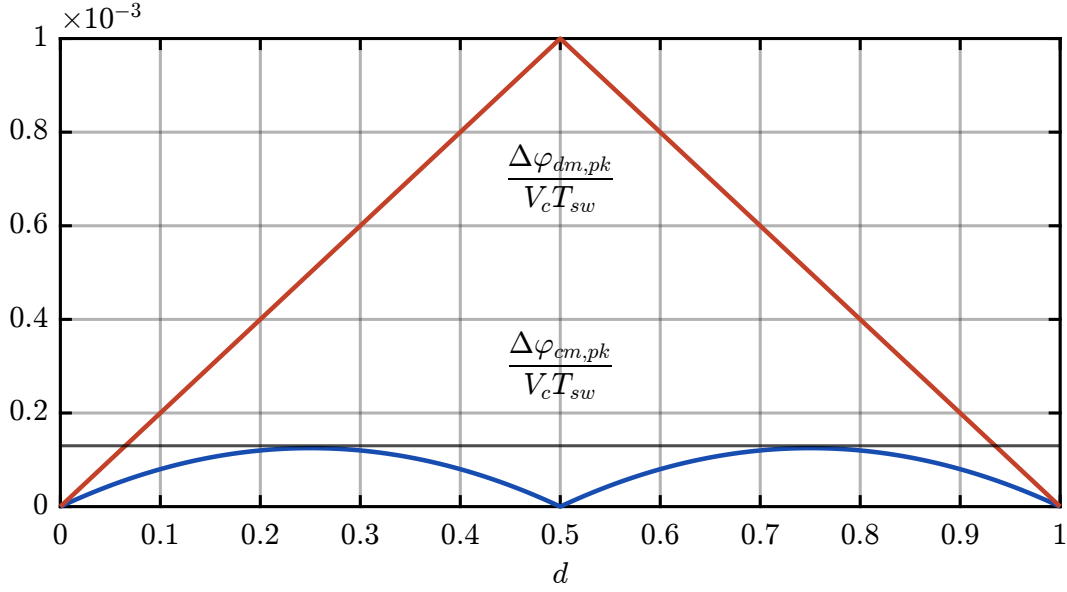


Fig. 2.14 Normalized flux ripple $\Delta\Phi_{L,pk,norm}$ in the common- and differential-mode inductors of the interleaved converter as a function of the duty cycle d .

$L_{11} = L_{22} = L$, the resulting modal inductances are

$$L_{cm} = L + L_{12}, \quad L_{dm} = L - L_{12}. \quad (2.23)$$

These expressions correspond to the inductance *per winding* seen by the common- and differential-mode currents. If referred to the total modal currents as $i_{cm} = i_1 + i_2$ and $i_{dm} = i_1 - i_2$, the equivalent inductances become $2(L + L_{12})$ and $2(L - L_{12})$, respectively. This distinction avoids ambiguities in interpreting whether the inductance is expressed per winding or per mode.

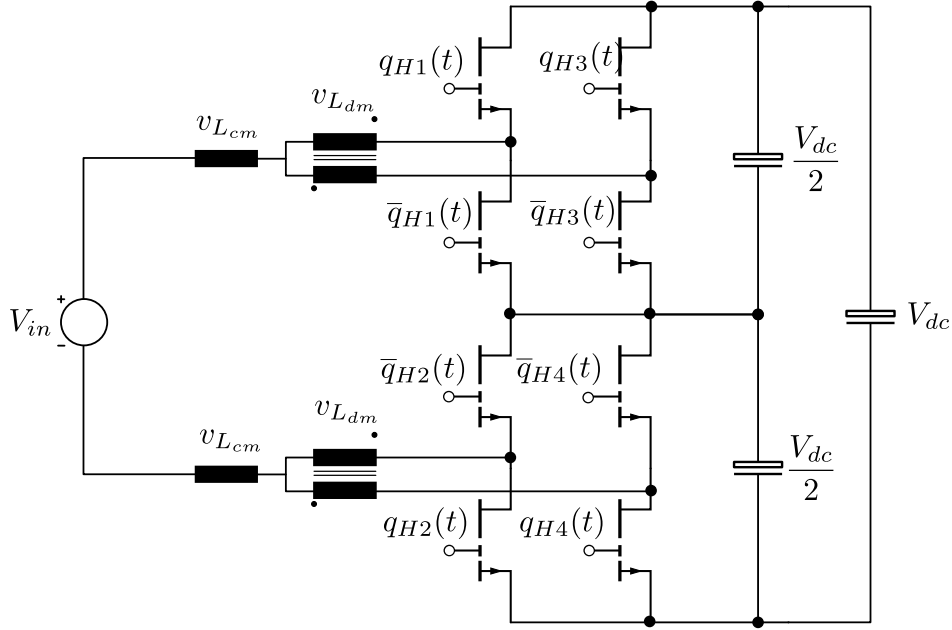


Fig. 2.15 Symbolic representation of a multilevel-interleaved DC/DC converter.

2.2.5 Modeling of the proposed structure

This subsection presents the final modeling of the complete three-level interleaved DC/DC converter. The final structure involves the combination of two poles which are connected in a multilevel configuration plus two additional poles connected in parallel by means of an interleaving configuration, as presented in Section 2.2.4. The complete structure is presented in Fig. 2.15. The four carriers are phase-shifted by 90° from each other. A detailed modeling of the differential-mode flux ripple is carried out in Section 2.2.4. The differential-mode effect that involves the inductor does not directly influence the main behavior of the converter, as it appears as an additional component of the flux ripple for each side of the converter. Fig. 2.16 shows the simplified model of the converter under study.

For the implementation of the DC/DC three-level interleaved GaN converter, two DC/DC units with two poles are involved. The two units use triangular carriers phase-shifted by 90° . The differential-mode effect that involves the inductor cannot be seen from the other DC/DC converter: each converter sees its differential mode without affecting the other one. v_{cm1} represents the voltage across the H-bridge of

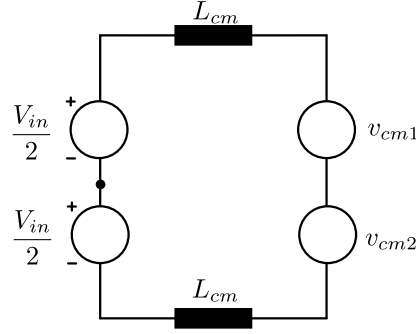


Fig. 2.16 Symbolic representation of the simplified converter model.

the high-side, while v_{cm2} is the voltage on the low-side and $v_{eq} = v_{cm1} + v_{cm2}$, where:

$$\begin{aligned} v_{cm1} &= \frac{V_{dc}}{2} \cdot (q_{H1} + q_{H3}) \cdot \frac{1}{2} \\ v_{cm2} &= \frac{V_{dc}}{2} \cdot (q_{H2} + q_{H4}) \cdot \frac{1}{2} \end{aligned} \quad (2.24)$$

Fig. 2.17a shows the generic waveforms for the triangular carriers of the four legs of the DC/DC converter, the switch commands, and the voltages v_{cm1} and v_{cm2} .

With this configuration, four working conditions can be analyzed:

- Case $0 < d < 0.25$
- Case $0.25 < d < 0.5$
- Case $0.5 < d < 0.75$
- Case $0.75 < d < 1$

Case $0 < d < 0.25$

The ripple expressions are directly related to the duty cycle variation. Considering a duty cycle $0 < d < \frac{1}{4}$, the ripple expressions can be extracted for $L = L_{cm1} + L_{cm2}$.

$$\begin{aligned} \Delta\Phi_L &= \frac{1}{2}d \cdot T_{SW} \cdot \left(\frac{V_{dc}}{4} - d \cdot V_{dc} \right) = T_{SW}V_{dc} \cdot \frac{1}{2}d \cdot \left(\frac{1}{4} - d \right) \\ \Delta\Phi_{L,pk} \Big|_{d=\frac{1}{8}} &= T_{SW}V_{dc} \cdot \frac{1}{2} \cdot \frac{1}{8} \cdot \left(\frac{1}{4} - \frac{1}{8} \right) = \frac{1}{128} \cdot T_{SW}V_{dc} \end{aligned} \quad (2.25)$$

And, since there are two inductors, each one will see a flux ripple of:

$$\Delta\Phi_{L,pk} \Big|_{d=\frac{1}{8}} \text{ (single inductor)} = \frac{1}{256} \cdot T_{SW} V_{dc} \quad (2.26)$$

Case $0.25 < d < 0.5$

Figure 2.17a shows the generic waveforms for $0.25 < d < 0.5$.

Using the same reasoning applied in the previous case, the ripple expression can be extracted as follows:

$$\begin{aligned} \Delta\Phi_L &= \frac{1}{2} T_{SW} \cdot \left(d - \frac{1}{4}\right) \cdot \left(\frac{V_{dc}}{2} - d \cdot V_{dc}\right) = T_{SW} V_{dc} \cdot \frac{1}{2} \cdot \left(d - \frac{1}{4}\right) \cdot \left(\frac{1}{2} - d\right) \\ \Delta\Phi_{L,pk} \Big|_{d=\frac{3}{8}} &= T_{SW} V_{dc} \cdot \frac{1}{2} \cdot \left(\frac{3}{8} - \frac{1}{4}\right) \cdot \left(\frac{1}{2} - \frac{3}{8}\right) = T_{SW} V_{dc} \cdot \frac{1}{128} \end{aligned} \quad (2.27)$$

$$\Delta\Phi_{L,pk} \Big|_{d=\frac{3}{8}} \text{ (single inductor)} = T_{SW} V_{dc} \cdot \frac{1}{256} \quad (2.28)$$

Case $0.5 < d < 0.75$

Using the same reasoning applied in the previous case, the ripple expression can be obtained as follows:

$$\begin{aligned} \Delta\Phi_L &= \frac{1}{2} T_{SW} \cdot \left(d - \frac{1}{2}\right) \cdot \left(\frac{3V_{dc}}{4} - d \cdot V_{dc}\right) = T_{SW} V_{dc} \cdot \frac{1}{2} \cdot \left(d - \frac{1}{2}\right) \cdot \left(\frac{3}{4} - d\right) \\ \Delta\Phi_{L,pk} \Big|_{d=\frac{5}{8}} &= T_{SW} V_{dc} \cdot \frac{1}{2} \cdot \left(\frac{5}{8} - \frac{1}{2}\right) \cdot \left(\frac{3}{4} - \frac{5}{8}\right) = T_{SW} V_{dc} \cdot \frac{1}{128} \end{aligned} \quad (2.29)$$

$$\Delta\Phi_{L,pk} \Big|_{d=\frac{5}{8}} \text{ (single inductor)} = T_{SW} V_{dc} \cdot \frac{1}{256} \quad (2.30)$$

Case $0.75 < d < 1$

Using the same reasoning applied in the previous case, the ripple expression can be extracted through the equations:

$$\Delta\Phi_L = \frac{1}{2}T_{SW} \cdot \left(d - \frac{3}{4}\right) \cdot (V_{dc} - d \cdot V_{dc}) = T_{SW}V_{dc} \cdot \frac{1}{2} \cdot \left(d - \frac{3}{4}\right) \cdot (1 - d)$$

$$\Delta\Phi_{L,pk} \Big|_{d=\frac{7}{8}} = T_{SW}V_{dc} \cdot \frac{1}{2} \cdot \left(\frac{7}{8} - \frac{3}{4}\right) \cdot \left(1 - \frac{7}{8}\right) = T_{SW}V_{dc} \cdot \frac{1}{128} \quad (2.31)$$

$$\Delta\Phi_{L,pk} \Big|_{d=\frac{7}{8}} \text{ (single inductor)} = T_{SW}V_{dc} \cdot \frac{1}{256} \quad (2.32)$$

The flux ripple can be represented graphically as a function of the duty cycle as shown in Fig. 2.17b, where the maximum ripple points are highlighted.

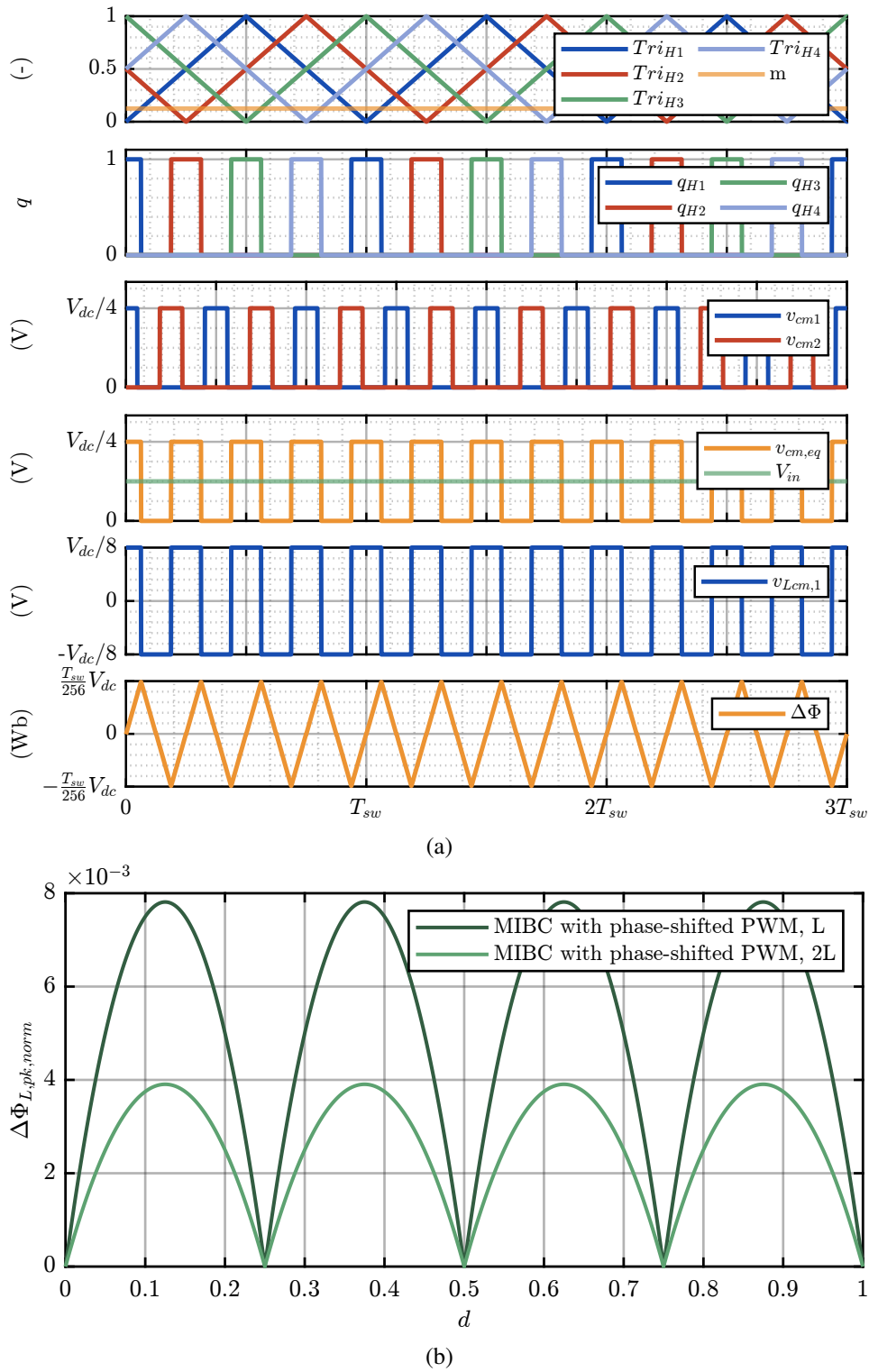


Fig. 2.17 (a) Generic waveforms with a duty cycle $d < \frac{1}{4}$, (b): Behavior of the normalized flux with respect to the duty cycle for the interleaved four-leg structure with phase shift, for the total inductors (dark green curve) and a single inductor (light green curve).

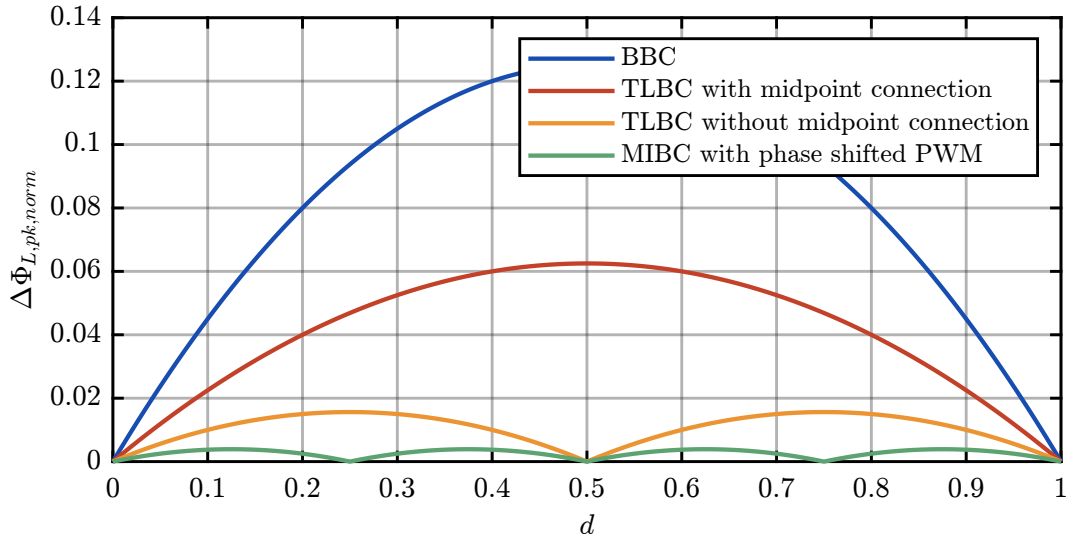


Fig. 2.18 Comparison of the flux ripple in the analyzed structures.

2.2.6 Summary

A comparison between the four presented structures is performed in Fig. 2.18, considering the definition of the duty-cycle as:

$$d = \frac{V_{in}}{V_{dc}} \quad (2.33)$$

The comparison in 2.18 is performed between the single inductor of the conventional bidirectional switching cell and the equivalent inductive path of the studied converters. As a consequence, the ripple frequency is increased by a factor of four, significantly reducing the sizing of the reactive components, as will be shown in the next chapters.

2.3 Analysis of Capacitor Current Stress

This section provides an analytical evaluation of the capacitor current ripple in the proposed multilevel-interleaved DC/DC converter. It is worth noting that these currents are not influenced by the adoption of the multilevel architecture with coupled inductors. Instead, the ripple depends only on the behavior of the single converter cell.

2.3.1 Capacitor Stress in the interleaved structure

The analysis starts from a simplified two-leg DC/DC converter, whose structure was previously presented in Fig. 2.11.

The initial assumption is that the leg currents i_1 and i_3 remain constant and equal to $\frac{I_{m,max}}{2}$. The RMS value of the current flowing into the capacitor can be evaluated for two different ranges of the duty cycle.

► Case $0 < d < 0.5$:

The RMS current is defined as:

$$I_{C_{RMS}} = \sqrt{\frac{1}{T} \int_0^T i^2 dt} \quad (2.34)$$

After some manipulation, the RMS capacitor current becomes

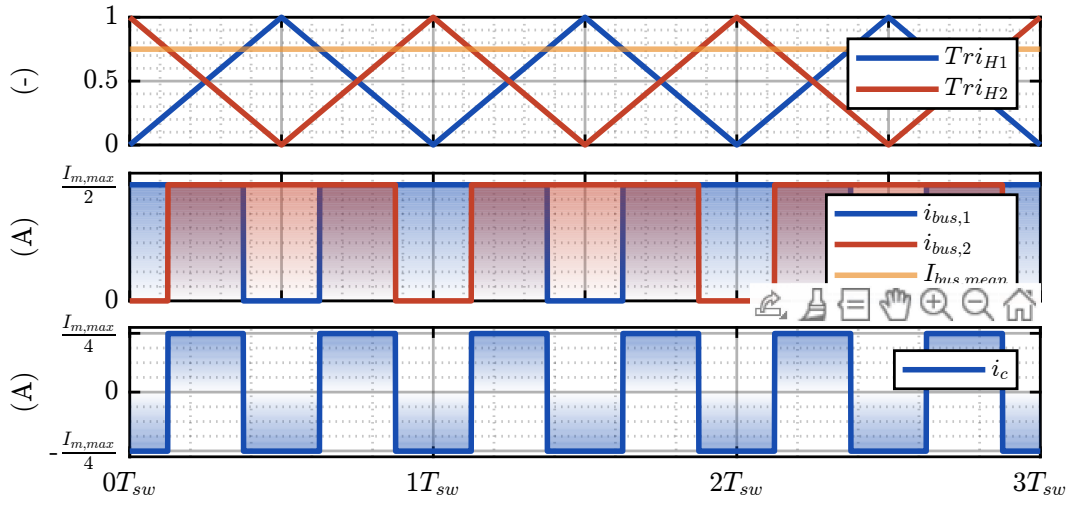
$$I_{C_{RMS}} = \sqrt{\frac{1}{\frac{T_{SW}}{2}} \left[\int_0^{\frac{T_{SW}}{2}} (I_{in,max} \cdot (\frac{1}{2} - d))^2 dt + \int_{\frac{T_{SW}}{2}}^{\frac{T_{SW}}{2}} (I_{in,max} \cdot d)^2 dt \right]}$$

$$I_{C_{RMS}} = I_{in,max} \cdot \sqrt{\frac{1}{2}d + d^2} \quad (2.35)$$

► Case $0.5 < d < 1$:

In this case, the capacitor current assumes the waveform reported in Fig. 2.19. Starting again from (2.34), the analytical expression of the RMS value is derived as

$$I_{C_{RMS}} = I_{in,max} \sqrt{-\frac{1}{2} + \frac{3}{2}d - d^2} \quad (2.36)$$

Fig. 2.19 Capacitor current for $d > 0.5$.

The resulting trend of $I_{C_{RMS}}$ with respect to the duty cycle is reported in Fig. 2.20. Two maximum points can be observed at $d = 0.25$ and $d = 0.75$.

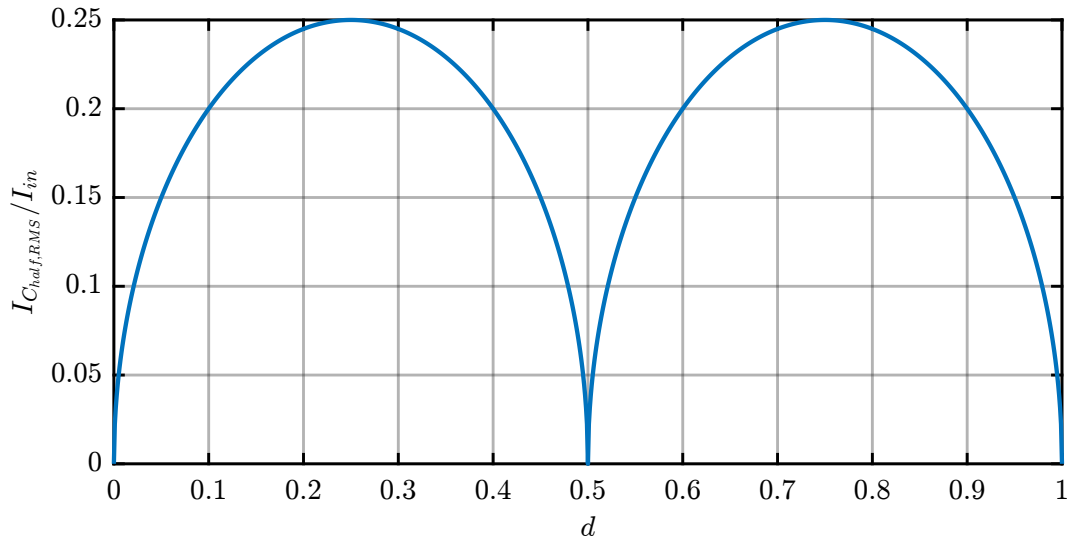


Fig. 2.20 RMS value of the capacitor current as a function of the duty cycle.

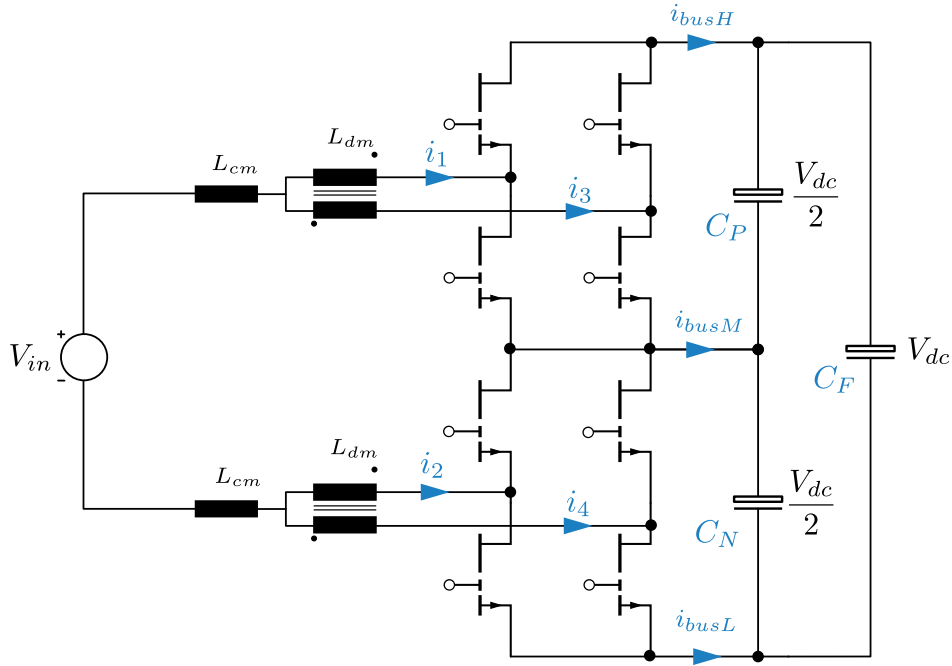


Fig. 2.21 Full DC/DC three-level interleaved GaN converter structure including the three DC-link capacitors.

2.3.2 Full DC/DC three-Level Interleaved GaN Converter Structure

The complete structure of the three-level interleaved GaN-based DC/DC converter, including the DC-link capacitors, is illustrated in Fig. 2.21.

Two types of capacitors are distinguished within the system:

- C_P and C_N : The index denotes the position of the capacitor. These capacitors are responsible for filtering the current in each single DC/DC converter cell. The dominant ripple component in their current has a frequency of $2f_{SW}$, i.e., twice the converter switching frequency.
- C_F : The index “F” denotes “Full”. This capacitor filters the overall ripple of the complete converter. Its main ripple component occurs at $4f_{SW}$, while it does not participate in the attenuation of the $2f_{SW}$ harmonics.

In order to correctly design these capacitors, a detailed evaluation of the current stress is required. The equivalent DC-link structure of the studied converter is

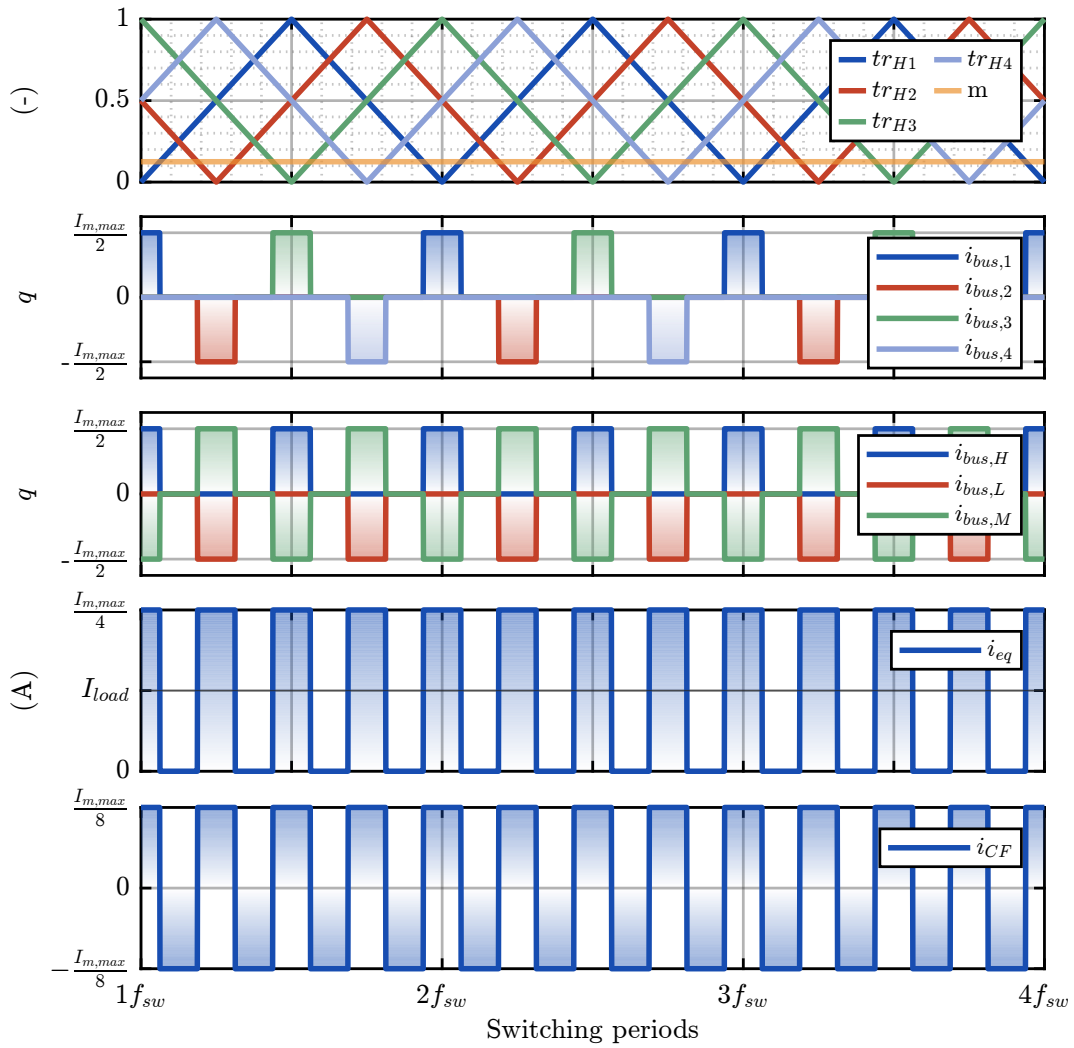


Fig. 2.22 Phase-shifted triangular carriers and current waveforms for the case $0 < d < 0.25$.

reported in Fig. 2.21. The highlighted DC-link currents, namely i_{busH} , i_{busM} , and i_{busL} , can be derived from the branch currents i_1 , i_2 , i_3 , and i_4 depending on the operating duty cycle. Four distinct operating cases are considered:

Case 1: $0 < d < 0.25$

The switching configuration for duty ratios lower than 0.25 is shown in Fig. 2.22, together with the phase-shifted triangular carriers and the corresponding bus currents.

In this condition, the bus currents can be expressed as

$$\begin{aligned} i_{busH} &= i_{bus1} + i_{bus3} \\ i_{busL} &= i_{bus2} + i_{bus4} \\ i_{busM} &= -(i_{bus1} + i_{bus3} + i_{bus2} + i_{bus4}). \end{aligned} \quad (2.37)$$

Referring to Fig. 2.22 and under the assumption $C_H \ll C_F$, the current flowing through the equivalent capacitor can be approximated as

$$i_{eq} = \frac{i_{busH} - i_{busL}}{2}. \quad (2.38)$$

The RMS value of the current flowing into capacitor C_F can thus be evaluated as

$$\begin{aligned} I_{CF_{RMS}} &= \sqrt{\frac{1}{\frac{T_{SW}}{4}} \int_0^{\frac{T_{SW}}{4}} i_{CF}^2 dt} \\ &= \sqrt{\frac{4}{T_{SW}} \left[\int_0^{dT_{SW}} \left(\frac{1}{4} I_{in_{max}} - I_{in_{max}} \cdot d \right)^2 dt + \int_{dT_{SW}}^{\frac{T_{SW}}{3}} \left(-I_{in_{max}} \cdot d \right)^2 dt \right]} \\ &= 2I_{in_{max}} \cdot \sqrt{\frac{1}{3} \left(\frac{1}{4} - d \right) d}. \end{aligned} \quad (2.39)$$

For example, at $d = 0.125$, the RMS current results in

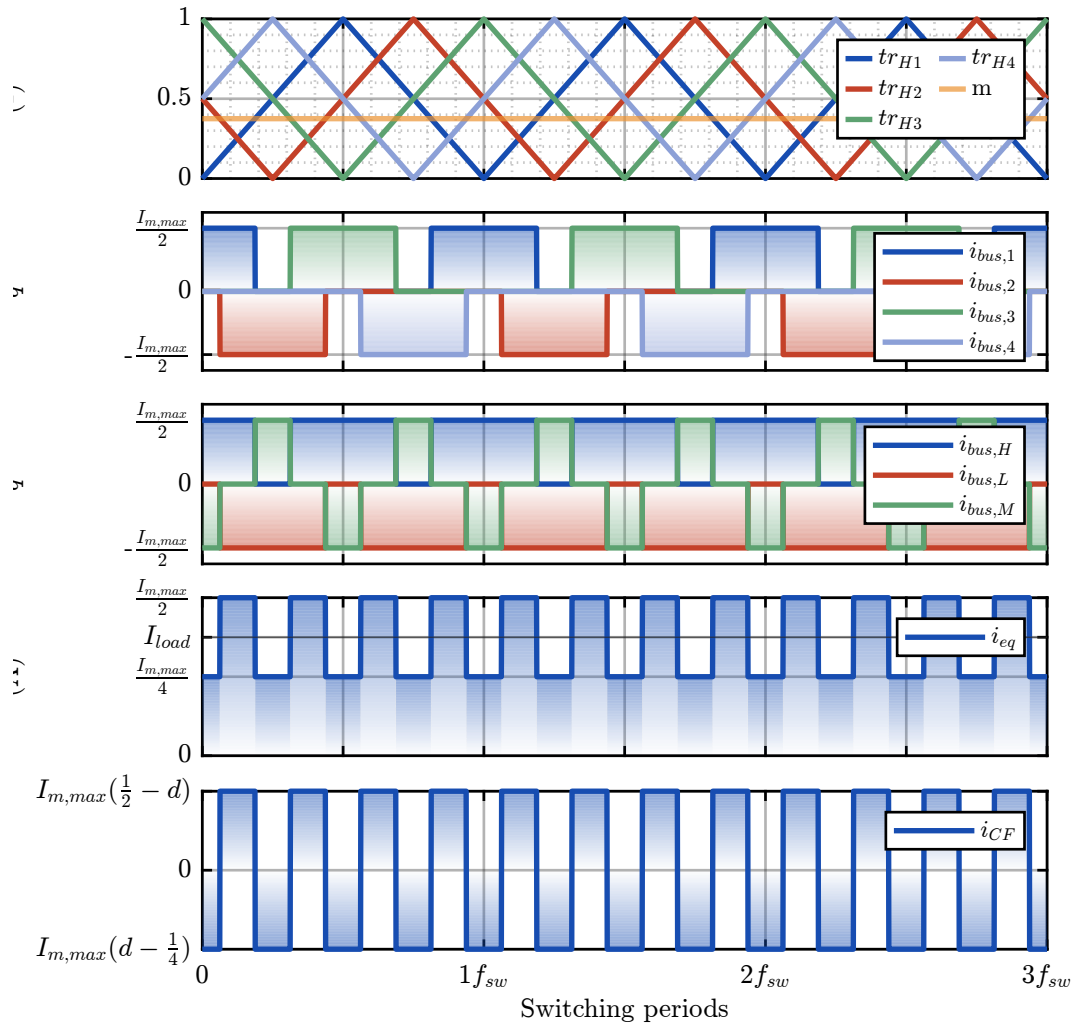
$$I_{CF_{RMS}} = 0.125 I_{in_{max}}.$$

Case 2: $0.25 < d < 0.5$

The general current waveforms for this duty range are illustrated in Fig. 2.23.

The RMS current of C_F is obtained as

$$\begin{aligned} I_{CF_{RMS}} &= \sqrt{\frac{4}{T_{SW}} \left[\int_0^{T_{SW} \left(d - \frac{1}{4} \right)} \left(I_{in_{max}} \left(\frac{1}{2} - d \right) \right)^2 dt + \int_{T_{SW} \left(d - \frac{1}{4} \right)}^{\frac{T_{SW}}{4}} \left(I_{in_{max}} \left(d - \frac{1}{4} \right) \right)^2 dt \right]} \\ &= 2I_{in_{max}} \cdot \sqrt{-\frac{d^2}{4} + \frac{3}{16}d - \frac{1}{32}}. \end{aligned} \quad (2.40)$$

Fig. 2.23 Current waveforms and mean load current for $0.25 < d < 0.5$.**Case 3:** $0.5 < d < 0.75$

The RMS capacitor current expression becomes

$$\begin{aligned}
 I_{CF_{RMS}} &= \sqrt{\frac{4}{T_{SW}} \left(\int_0^{T_{SW}(d-\frac{1}{2})} (I_{in_{max}} \cdot (\frac{3}{4} - d))^2 dt + \int_{T_{SW}(d-\frac{1}{2})}^{\frac{T_{SW}}{4}} (-I_{in_{max}} \cdot (d - \frac{1}{2}))^2 dt \right)} \\
 &= 2I_{in_{max}} \cdot \sqrt{-\frac{d^2}{4} + \frac{5}{16}d - \frac{3}{32}}.
 \end{aligned} \tag{2.41}$$

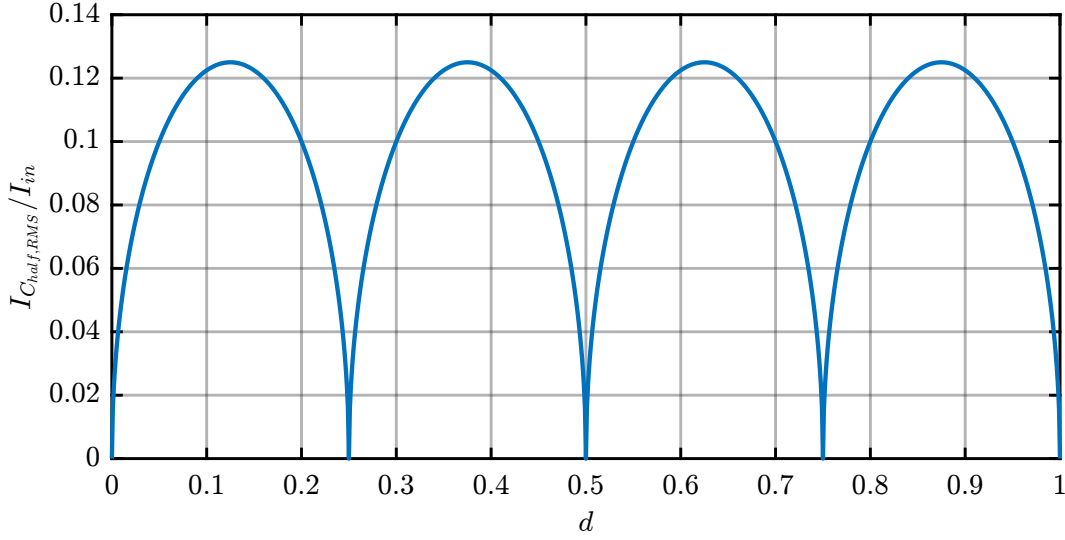


Fig. 2.24 Normalized RMS current of C_F as a function of the duty cycle.

Case 4: $0.75 < d < 1$

The RMS current in C_F can be evaluated as

$$\begin{aligned}
 I_{CF_{RMS}} &= \sqrt{\frac{4}{T_{SW}} \left(\int_0^{T_{SW}(d-\frac{3}{4})} (I_{in_{max}} \cdot (1-d))^2 dt + \int_{T_{SW}(d-\frac{3}{4})}^{\frac{T_{SW}}{4}} (-I_{in_{max}} \cdot (d-\frac{3}{4}))^2 dt \right)} \\
 &= 2I_{in_{max}} \cdot \sqrt{-\frac{d^2}{4} + \frac{7}{16}d - \frac{3}{16}}.
 \end{aligned} \tag{2.42}$$

2.3.3 Summary

Fig. 2.24 summarizes the normalized RMS current flowing through the capacitor C_F as a function of the duty cycle. The plot, obtained for $I_{in_{max}} = 25 \text{ A}_{rms}$, clearly highlights four maximum points corresponding to the four duty ranges previously analyzed.

2.4 Analysis of Semiconductor Stress

In the proposed interleaved three-level DC/DC converter topology, the voltage stress across the semiconductor devices is significantly reduced compared to conventional boost converters. Each switching device experiences a maximum voltage stress of:

$$V_{sw,max} = \frac{V_{dc}}{2} \quad (2.43)$$

This reduced voltage stress is a direct result of the multilevel structure, where the total DC-link voltage V_{dc} is divided equally across the switching cells. For a target output voltage of 800V, each semiconductor device needs to withstand only 400V, allowing the use of lower-voltage-rated devices with better switching characteristics.

Due to the proposed topology, each cell can be modeled as a bidirectional switching cell that commutates only half of the DC-link voltage. Furthermore, due to the interleaved structure, each cell will take care of only half of the total I_{in} current.

$$I_{sw} = \frac{I_{in}}{2} \quad (2.44)$$

Switching Losses

Based on the device datasheet, the switching losses can be estimated from the turn-on and turn-off switching energy curves. The switching power loss of a single device is given by

$$P_{sw} = f_{sw} [E_{on}(i_{sw}) + E_{off}(i_{sw})] \quad (2.45)$$

where E_{on} and E_{off} are the turn-on and turn-off switching energies evaluated at the operating current i_{sw} , and f_{sw} is the switching frequency.

The total switching losses of the proposed topology can therefore be evaluated as

$$P_{sw,tot} = 4 f_{sw} [E_{on}(i_{sw}) + E_{off}(i_{sw})]. \quad (2.46)$$

Conduction Losses

The conduction losses are proportional to the square of the RMS current and present the resistive behavior of the device. For a single power switch:

$$p_{cond} = R_{ds,on} \cdot I_{rms}^2 \quad (2.47)$$

This, for all the devices of the topology, becomes:

$$P_{cond,tot} = 4 \cdot R_{ds,on} \cdot I_{rms}^2 \quad (2.48)$$

2.5 Summary

This chapter presented a comprehensive analytical comparison of DC/DC converter topologies for high-power automotive applications. The analysis started from basic bidirectional switching cells to increasingly sophisticated configurations, culminating in the proposed multilevel interleaved GaN-based converter.

Key findings demonstrate that the complete topology achieves superior performance through:

- Sixteen-fold reduction in the maximum peak flux ripple of the equivalent inductive path compared with the conventional bidirectional switching cell.
- Four-times higher effective ripple frequency enabling smaller passive components
- Half semiconductor voltage stress (400V vs 800V for 800V output)
- Distributed current stress among multiple phases
- Reduced capacitor current stress through harmonic cancellation

The analytical framework established the design guidelines for component selection and optimization, providing the foundation for the practical implementation detailed in subsequent chapters. The significantly reduced stresses enable efficient operation with GaN devices at higher switching frequencies, supporting the development of compact, high-power-density converters for automotive traction systems.

Chapter 3

DC/DC converter - *Control Design*

3.1 Introduction

The use of interleaved multilevel topologies in combination with WBG devices introduces specific challenges for the control system. Higher switching frequencies demand faster sampling rates, precise phase synchronization, and robust current sharing. Magnetic design becomes more critical, and the balancing of voltages and currents across phases must be ensured to prevent performance degradation. These requirements are especially relevant when switching frequencies exceed 100 kHz, where the implementation of cascaded control loops, PWM synchronization, and current balancing strategies must be carefully optimized.

Over the past few years, various control methodologies have been proposed for three-level boost converters. Dual-loop PI-based schemes [56] have proven effective in managing DC-link voltage asymmetries caused by leakage currents, though often validated only at lower frequencies and power levels. Model-based control (MBC) [57] and model predictive control (MPC) [58] can improve dynamic response but require accurate models and significant computational resources, limiting their applicability in high-frequency interleaved architectures. Takagi-Sugeno fuzzy (TSF) control [59–61] offers robustness against nonlinearities but remains challenging to implement in fast-switching systems.

Another key aspect is current sharing among interleaved phases. In ideal conditions, symmetric modulation ensures equal current distribution, but in practice non-ideal dead times, component mismatches, and layout asymmetries can lead to

imbalance, risking magnetic core saturation and potential system failure [62–64]. Sensorless techniques [65, 66] can address this while reducing hardware complexity, but often with a penalty in dynamic performance. Precise synchronization between PWM and ADC sampling [67] is also essential for accurate feedback acquisition, especially in the presence of current ripple and noise.

Although many publications address new converter topologies and modulation techniques, detailed and experimentally validated control routines for high-frequency, high-power, multilevel interleaved converters remain rare. Most studies focus on theoretical schemes or simplified implementations, often without addressing both voltage balancing and coordinated current control.

In this context, the present chapter focuses on the implementation and validation of a fully digital control scheme for a multilevel, interleaved GaN-based DC/DC converter operating at 100 kHz. The discussion includes a complete analysis of the converter structure, the control strategy, and its experimental validation, with particular emphasis on DC-link voltage balancing and current sharing among interleaved phases.

Part of the content of this chapter has been published in [27].

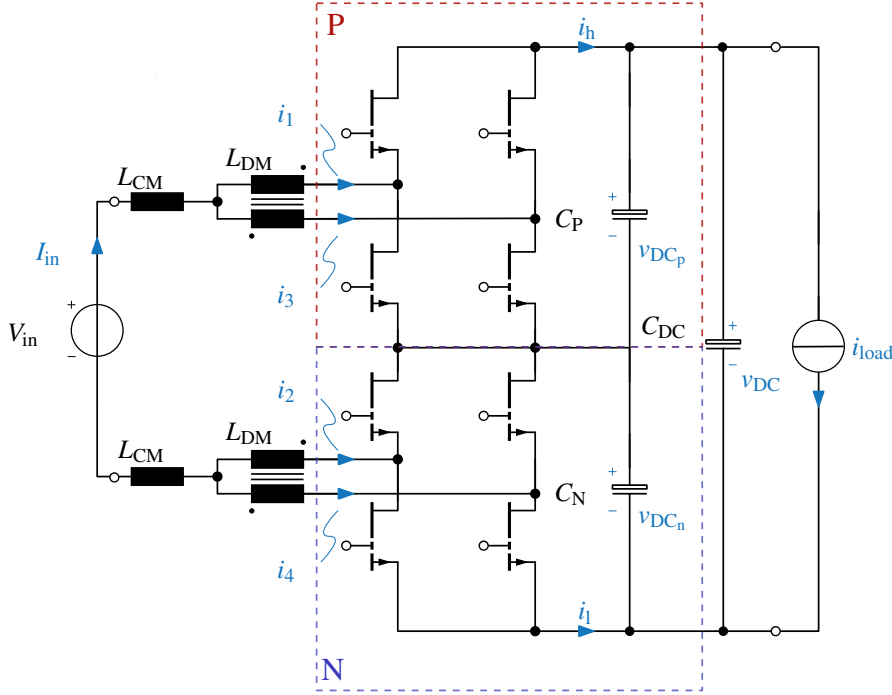


Fig. 3.1 Considered multilevel-interleaved DC/DC converter.

3.2 Control Design and Analysis

As shown in Fig. 3.1, the proposed DC/DC converter topology consists of two cascaded power stages previously presented, here denoted as P and N .

The proposed digital control architecture is depicted in Fig. 3.2. The design combines common-mode and differential-mode controllers in a cascaded arrangement with an external voltage control loop. Due to the split DC-link inherent in the cascaded structure, an additional voltage balancing loop is required. Furthermore, the control system integrates inner common-mode and differential-mode current loops for enhanced dynamic performance.

In total, five feedback loops are implemented to ensure stability and optimal dynamic response:

- Two main loops: an external voltage control loop and an external current control loop, responsible for regulating the output voltage and load current, respectively.

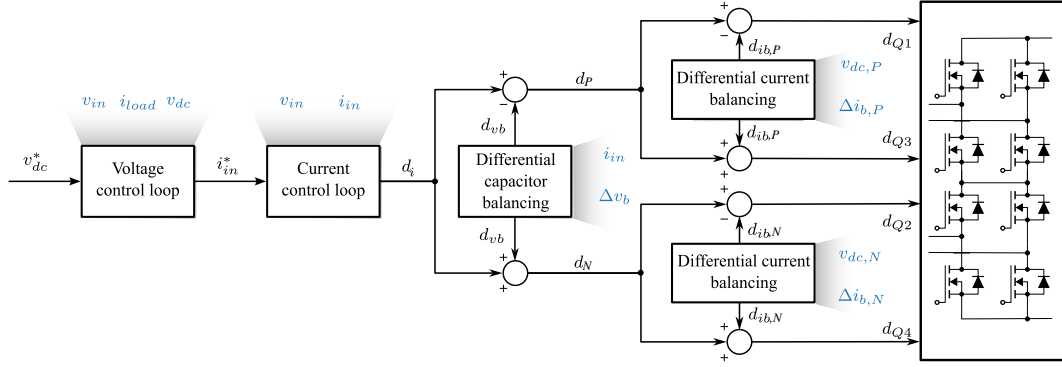


Fig. 3.2 Proposed DC/DC converter control loop.

- Three auxiliary loops: two dedicated to differential current balancing and one to differential voltage balancing. These inner loops ensure capacitor voltage equalization and proper current sharing between converter legs, preventing issues such as inductor saturation, which could otherwise degrade efficiency and reliability.

Referring to Fig. 3.2, the voltage control loop generates a current reference i_{in}^* for the internal current control stage. The current loop output is a duty ratio d_i , common to all converter legs. The differential voltage balancing loop then applies a corrective term d_{vb} to d_i , producing two separate duty cycles, d_{iP} and d_{iN} , for the upper and lower converter sections. Finally, a further current balancing stage refines these duty ratios by $d_{ib,P}$ and $d_{ib,N}$. The measured signals include inductor currents (i_1, i_3, i_2, i_4), the input voltage v_{in} , and the capacitor voltages v_{dcP} and v_{dcN} . Accurate acquisition of these quantities is essential for precise loop operation and safe system performance. The input current i_{in} is obtained from the sum of the differential inductor currents as

$$i_{in} = i_1 + i_3 = i_2 + i_4 \quad (3.1)$$

The total DC-link voltage v_{dc} is estimated as $v_{dc} = v_{dcP} + v_{dcN}$.

To tune the control loops, a small-signal model of the converter is derived following the methodology in [68]. The small-signal approach linearizes the nonlinear system around its steady-state operating point, enabling analysis of stability margins, frequency response, and transient behavior under small perturbations.

Based on the simplified equivalent circuits in Fig. 3.3, the state-space equations

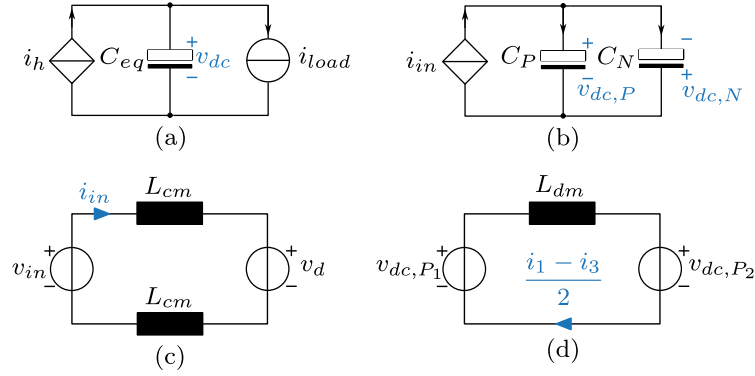


Fig. 3.3 Equivalent circuit representation of the system state-space equations: **(a)** Voltage loop, **(b)** Voltage capacitor balancing, **(c)** Current loop, **(d)** Differential inductor current balancing.

are:

$$\begin{cases} 2L_{cm} \frac{di_{in}}{dt} = v_{in} - v_d \\ C_{eq} \frac{dv_{dc}}{dt} = i_h - i_{load} \\ C_P \frac{dv_{dc,P}}{dt} - C_N \frac{dv_{dc,N}}{dt} = i_{vb} \\ L_{dm} \frac{di_{ib}}{dt} = v_{dc,P1} - v_{dc,P2} \end{cases} \quad (3.2)$$

where C_{eq} is the equivalent output capacitance, v_d is the average leg midpoint voltage, i_h is the sampled high-side current, i_{vb} is the DC-link midpoint current, and i_{ib} is the differential current circulating between the upper and lower converter halves. The auxiliary component definitions are:

$$\begin{cases} C_{eq} = \left(\frac{C_P \cdot C_N}{(C_P + C_N)} + C_{dc} \right) \\ v_d = d_i v_{dc} \\ i_{vb} = 2i_{in} d_{vb} \\ i_{ib,P,N} = \frac{i_1 - i_3}{2} \end{cases} \quad (3.3)$$

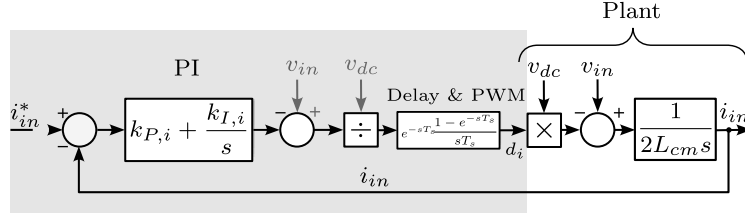


Fig. 3.4 Detailed block diagram of the main current control loop.

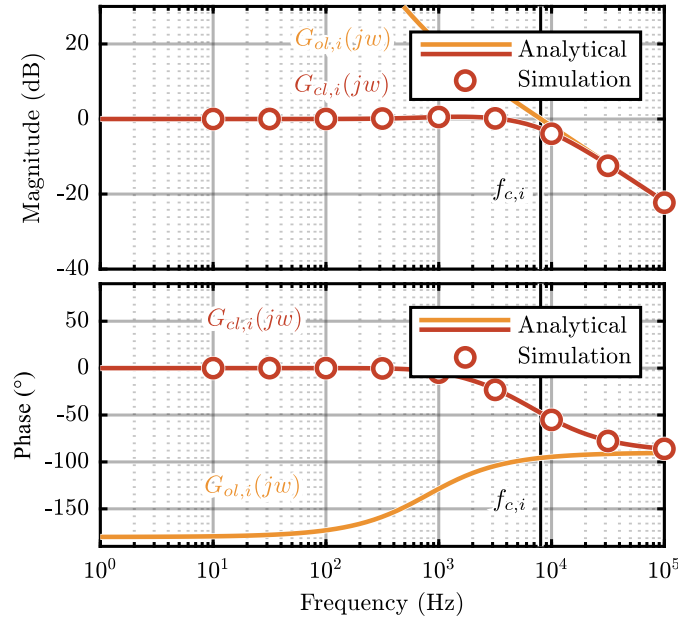


Fig. 3.5 Bode plots of the external current control loop: open-loop magnitude and phase (orange) and closed-loop magnitude and phase (red).

3.2.1 Current control loop

The external current loop, shown in Fig. 3.4, enforces zero steady-state error between the reference input current and the measured one from (3.1).

From (3.2), the voltage-to-current transfer function is:

$$G_{p,i} = \frac{i_{in}(s)}{v_d(s)} = \frac{1}{s2L_{cm}} \quad (3.4)$$

Disturbance effects are neglected in the plant derivation and mitigated in practice by a feed-forward term. In the digital implementation, control delays arise from both

computational processing and the PWM zero-order hold (ZOH), resulting in:

$$G_{d,i} = e^{-sT_s} \frac{1 - e^{-sT_s}}{sT_s} \quad (3.5)$$

A proportional-integral (PI) regulator is adopted:

$$G_{c,i}(s) = k_{P,i} + \frac{k_{I,i}}{s} \quad (3.6)$$

with proportional gain $k_{P,i}$ and integral gain $k_{I,i}$. The open-loop transfer function is:

$$G_{ol,i}(s) = G_{p,i}(s)G_{d,i}(s)G_{c,i}(s) \quad (3.7)$$

Tuning is performed via the open-loop method, selecting a target crossover frequency $\omega_{c,i}$ for a 0 dB magnitude crossing. To ensure stability, the integral gain is set to one-tenth of the proportional gain [69]:

$$\begin{cases} k_{P,i} \approx \omega_{c,i} 2L_{cm} \\ k_{I,i} = \frac{\omega_{c,i}}{10} k_{P,i} \end{cases} \quad (3.8)$$

For this design, $f_{c,i} = 8 \text{ kHz}$ is selected. Fig. 3.5 illustrates the resulting Bode plots.

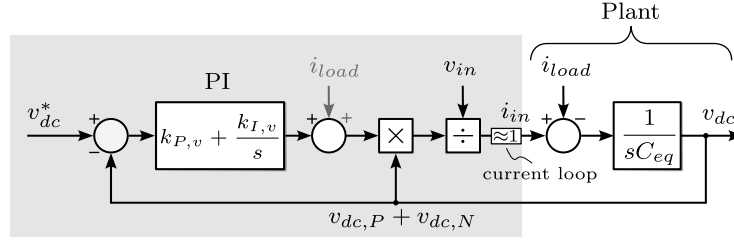


Fig. 3.6 Detailed block diagram of the main voltage control loop.

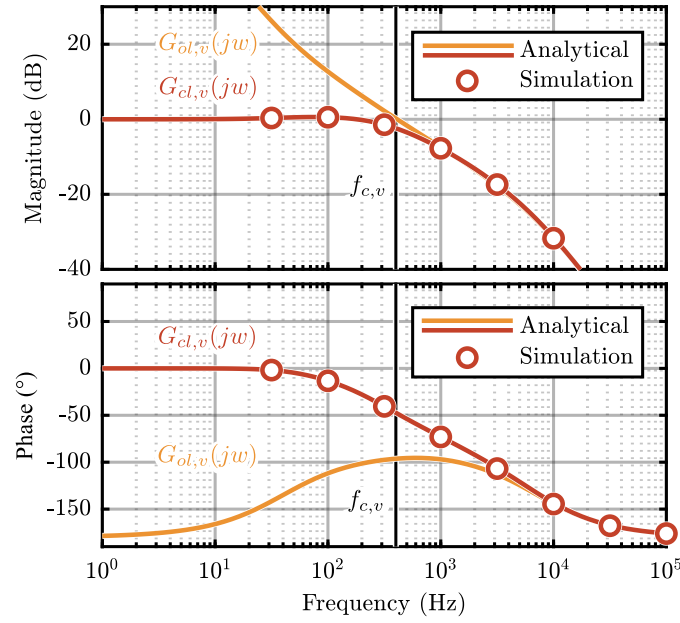


Fig. 3.7 Bode plots of the external voltage control loop: open-loop magnitude and phase (orange) and closed-loop magnitude and phase (red).

3.2.2 Voltage control loop

The voltage regulation stage, represented in Fig. 3.6, consists of a PI controller, a feed-forward term, a gain-adjustment block, and the plant dynamics. Since the DC/DC converter input power is accurately known, the load current i_{load} can be estimated and directly injected as a feed-forward signal to improve disturbance rejection.

From the small-signal model in Fig. 3.3(a) and the state equations in (3.2), the plant transfer function is obtained as:

$$G_{p,v} = \frac{v_{dc}(s)}{i_h(s)} = \frac{1}{sC_{eq}} \quad (3.9)$$

The PI regulator is expressed as:

$$G_{c,v}(s) = k_{P,v} + \frac{k_{I,v}}{s} \quad (3.10)$$

where $k_{P,v}$ and $k_{I,v}$ denote the proportional and integral gains, respectively.

Because the inner current loop operates with much higher bandwidth with respect to the voltage loop, it can be modeled as an ideal unity-gain block for the voltage loop design. Thus, the open-loop transfer function becomes:

$$G_{ol,v}(s) = G_{p,v}(s)G_{c,v}(s) \quad (3.11)$$

Tuning follows the same approach as in the current loop:

$$\begin{cases} k_{P,v} \approx w_{c,v}C_{eq} \\ k_{I,v} = \frac{w_{c,v}}{10}k_{P,v} \end{cases} \quad (3.12)$$

where a crossover frequency $f_{c,v} = 400\text{ Hz}$ is selected. The corresponding open-loop and closed-loop frequency responses are shown in Fig. 3.7.

3.2.3 Voltage capacitor balancing

Multilevel converters inherently feature a split DC-link. Given the well-documented variation of capacitance values with operating conditions [70], a dedicated voltage balancing control is introduced to maintain equal voltages across the upper and lower DC-link capacitors. This inner loop, shown in Fig. 3.8, enforces a zero steady-state differential voltage error.

From (3.2), a proportional regulator is defined as:

$$k_{P,vb} = w_{c,vb}C_{vb} \quad (3.13)$$

where

$$C_{vb} = \frac{C_P + C_N}{2} \quad (3.14)$$

The balancing signal is applied additively and subtractively to the duty cycles of the upper and lower converter sections, as indicated in Fig. 3.2. To ensure separation from the main voltage loop bandwidth, a crossover frequency of $f_{c,vb} = 100\text{Hz}$ is used.

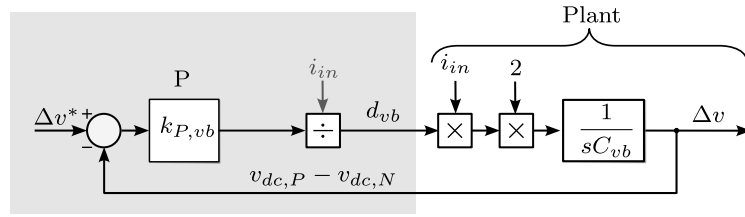


Fig. 3.8 Detailed block diagram of the voltage balancing control loop.

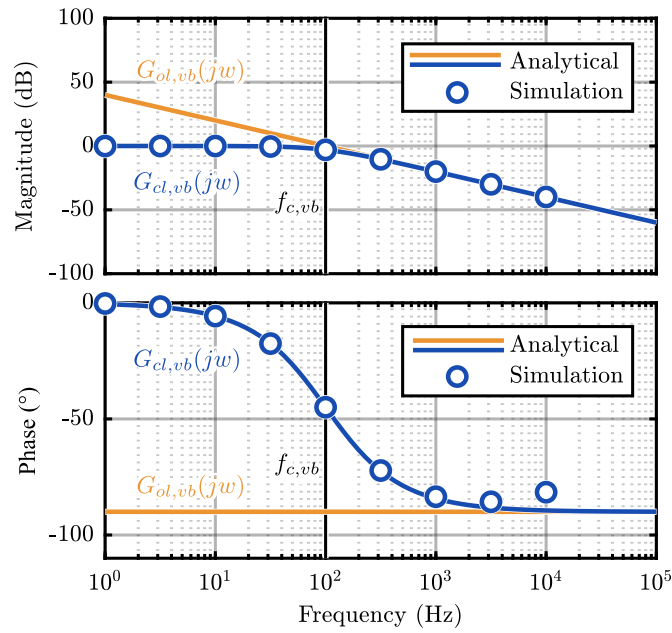


Fig. 3.9 Bode plots of the voltage balance loop: open-loop magnitude and phase (orange) and closed-loop magnitude and phase (blue).

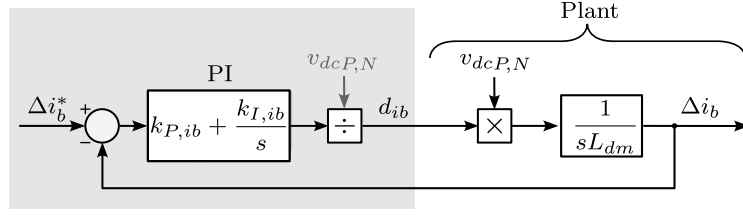


Fig. 3.10 Detailed block diagram of the current balancing control loop.

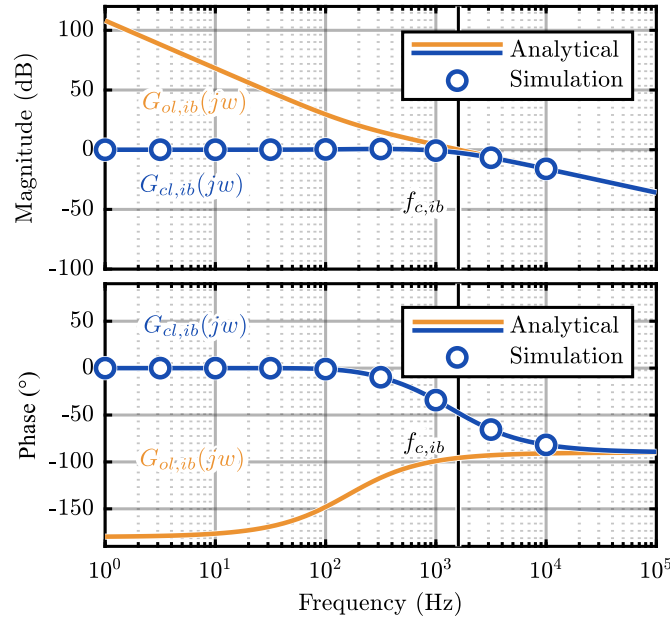


Fig. 3.11 Bode plots of the current balancing loop: open-loop magnitude and phase (orange) and closed-loop magnitude and phase (blue).

3.2.4 Differential current balancing

In interleaved converter legs, current mismatch can cause undesirable effects [71], such as uneven thermal stress, phase voltage imbalances, and increased conduction losses. These effects can degrade efficiency and reduce the reliability of power devices.

To address this, two identical current balancing loops—one for the upper section and one for the lower section—are implemented. Their structure is shown in Fig. 3.10.

Table 3.1 Loop control parameters

	External current control	External voltage control	Internal current control (differential mode)	Internal voltage control (balancing loop)
f_c	8 kHz	400 Hz	1.7 kHz	100 Hz
ω_c	$2\pi f_{c,i}$	$2\pi f_{c,v}$	$2\pi f_{c,ib}$	$2\pi f_{c,vb}$
Plant parameter	$L_{cm} = 6.28 \mu\text{H}$	$C_{eq} = 16.5 \mu\text{F}$	$L_{dm} = 75.79 \mu\text{H}$	$C_{vb} = 33 \mu\text{F}$
k_P	$2L_{cm}\omega_{c,i}$	$\omega_{c,v} \left(\frac{C_P C_N}{C_P + C_N} + C_{dc} \right)$	$L_{dm}\omega_{c,ib}$	$C_{vb}\omega_{c,vb}$
k_I	$\frac{\omega_{c,i}k_{P,i}}{10}$	$\frac{\omega_{c,v}k_{P,v}}{10}$	$\frac{\omega_{c,ib}k_{P,ib}}{10}$	None

From the model in Fig. 3.3(d) and equations (3.2), the PI controller parameters are defined as:

$$\begin{cases} k_{P,ib} \approx \omega_{c,ib} L_{dm} \\ k_{I,ib} = \frac{\omega_{c,ib}}{10} k_{P,ib} \end{cases} \quad (3.15)$$

A crossover frequency of $f_{c,ib} = 1.7 \text{ kHz}$. The corresponding Bode plots are presented in Fig. 3.11.

3.2.5 Control loop summary

Table 3.1 summarizes the selected parameters for all control loops implemented in the converter.

The parameters reported in Table 3.1 correspond to the measured inductance values and to the nominal installed capacitances of the prototype. With reference to Fig. 3.1, the currents i_{in} , i_h , and i_l correspond, respectively, to the differential input current, the high-side circulating current, and the low-side circulating current, which are the key feedback quantities for the external control loops.

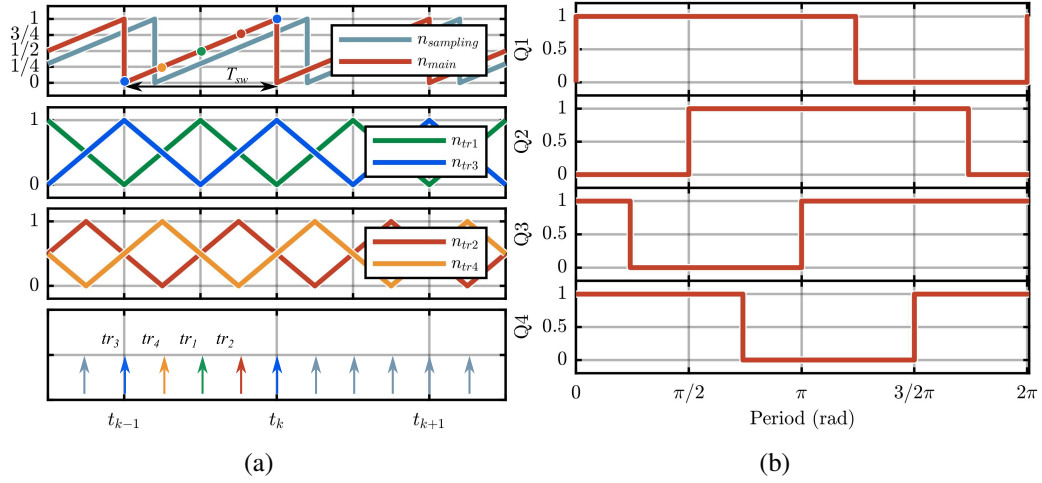


Fig. 3.12 (a): Synchronization of PWM carriers. (b): switching functions for the four legs.

3.3 Digital Implementation of the Control Architecture

The PI controller design was initially performed in the continuous-time domain using Bode plots, allowing precise shaping of the system frequency response and phase margin optimization. The controller was then discretized for implementation on the microcontroller, adopting the backward Euler method for the integral term. This discrete-time realization preserves the characteristics of the continuous-time design with high fidelity, thanks to the high sampling frequency of 200 kHz. Such a high sampling rate ensures that the discretization introduces negligible error, maintaining the stability and dynamic performance of the converter control loop.

For the modulation strategy, an interleaved scheme is implemented, with a 90° phase shift between the four DC/DC converter legs. Depending on the switching sequence, two main modulation types can be defined [15]. In this study, an N-type modulation is adopted, as it provides several practical advantages: increased converter efficiency, extended lifetime of the capacitive elements, and reduced electromagnetic interference noise [62]. These benefits make it particularly suitable for high-power, multi-phase converters such as the one considered in this work. Figure 3.13 highlights the importance of correctly sampling the currents for each leg. The presented current corresponds to a PWM phase shifted by 90° with respect to the others, linked to its specific PWM carrier and ADC sampler. As mentioned,

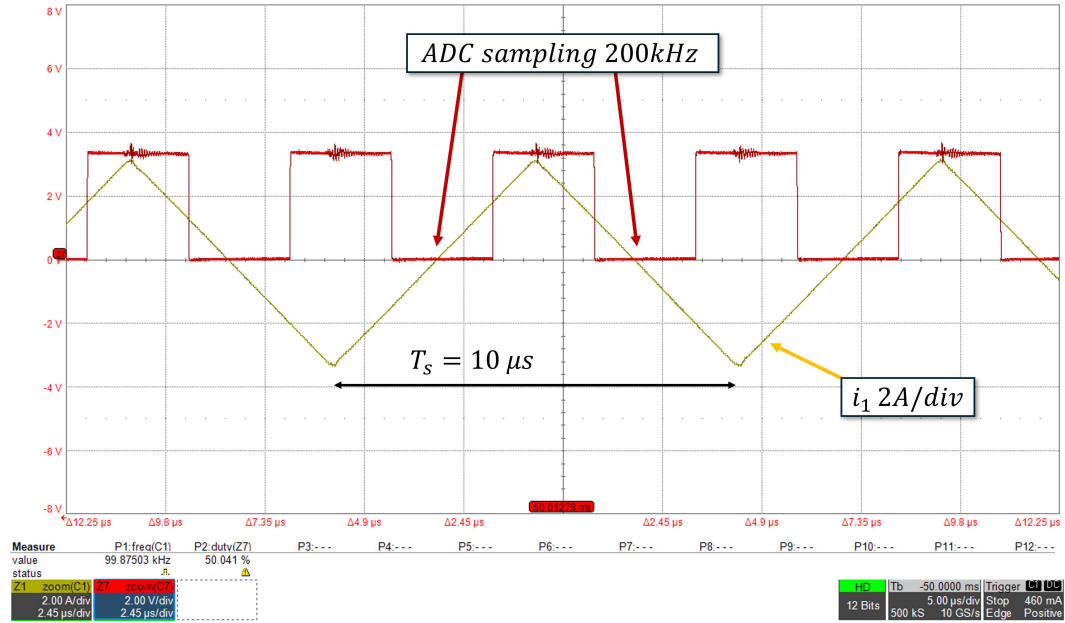


Fig. 3.13 Current sampling trigger detail for one of the leg current of the converter.

the ADC sampling of the current should be performed precisely, exactly at the mean value of the current. Indeed, double sampling is implemented to minimize the error.

Furthermore, the four duty cycles presented in Fig. 3.12a are compared with four different carriers (amplitude equal to unity) phase-shifted by 90° to generate the switching functions of the power switches, as shown in Fig. 3.12b. The acquisition trigger is synchronized with the triangular carriers, and each physical quantity is associated with a specific carrier. Furthermore, the update of the compare register of the PWM modulator must occur at a precise instant, different for each switching pole.

A robust solution for synchronizing all necessary processes is to define a primary timer n_{main} , whose period is set according to the desired switching frequency. Sampling instants must align with the PWM carrier peaks, as shown in Fig. 3.12a. To compensate for delays introduced by analog sensors and conditioning circuitry, a secondary counter $n_{sampling}$ is employed with a specific lag. The triggers for the A/D converters are determined by particular $n_{sampling}$ values, allowing two samples per feedback quantity per PWM period. Additionally, the Interrupt Service Routine (ISR) for DC/DC control must complete execution before the next ISR instance begins, ensuring the availability of the latest sampled data at T_{sw} , as presented in Fig. 3.14.

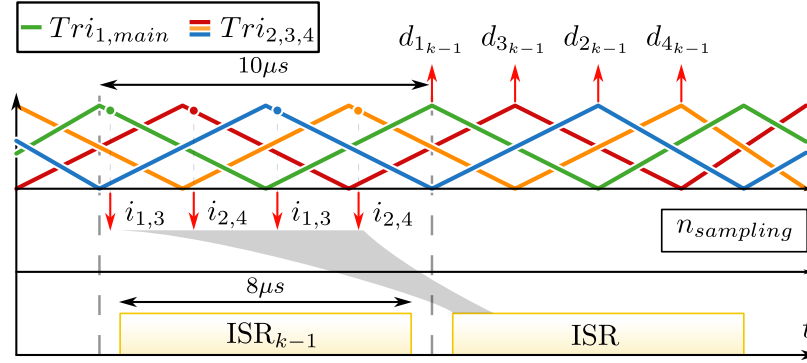


Fig. 3.14 Timing diagram of the sampling, the ISR control loop execution and duty cycle update.

3.4 Experimental Validation and Results

This section presents the experimental validation of the proposed control strategy, implemented and tested on the final converter prototype. A comprehensive experimental campaign was conducted to assess the operational performance of the system and to verify the accuracy of both the theoretical analysis and the simulation models. The complete test setup, shown in Fig. 3.15, is powered by two ITECH IT6090D programmable power supplies, which emulate the battery and load, respectively. This configuration allows controlled variation of the input voltage and load current, enabling validation at different operating points under realistic operating conditions.

Waveform acquisition is carried out using a Teledyne LeCroy HDO8038A eight-channel oscilloscope, allowing simultaneous monitoring of multiple quantities of interest. Voltage measurements were performed using three isolated differential probes (HVD3000A), capturing the input voltage (v_{in}) and the split DC-link voltages ($v_{dc,P}$ and $v_{dc,N}$). Currents through the four half-bridge legs were measured with Teledyne LeCroy CP150A probes, while the input current (i_{in}) was recorded with a CP500A probe.

The control algorithm was executed on an STM32 microcontroller with a sampling frequency of 200 kHz and a switching frequency of 100 kHz. Complementary switches were driven with a 100-ns dead time, ensuring safe operation without shoot-through, while introducing negligible distortion and losses. Any residual dead-time effects were effectively compensated by the control scheme, eliminating the need for additional dead-time compensation logic.

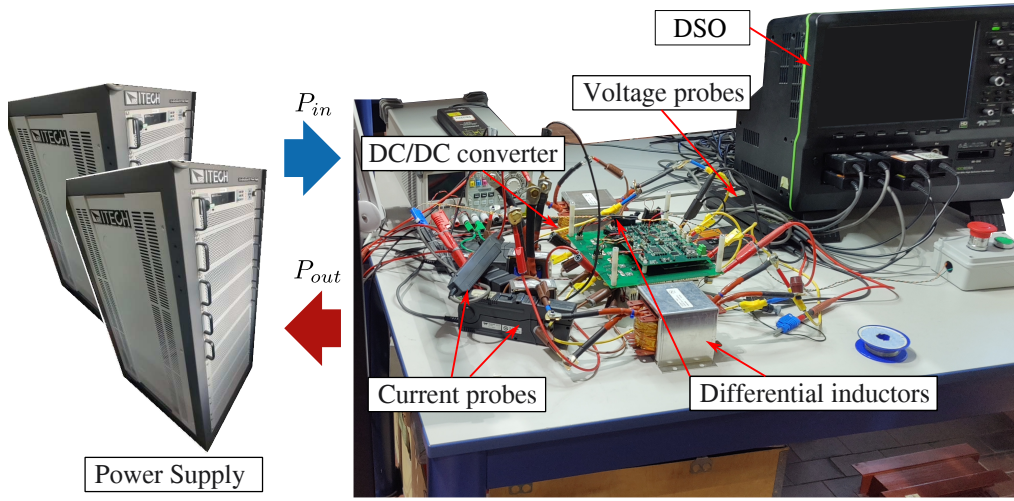
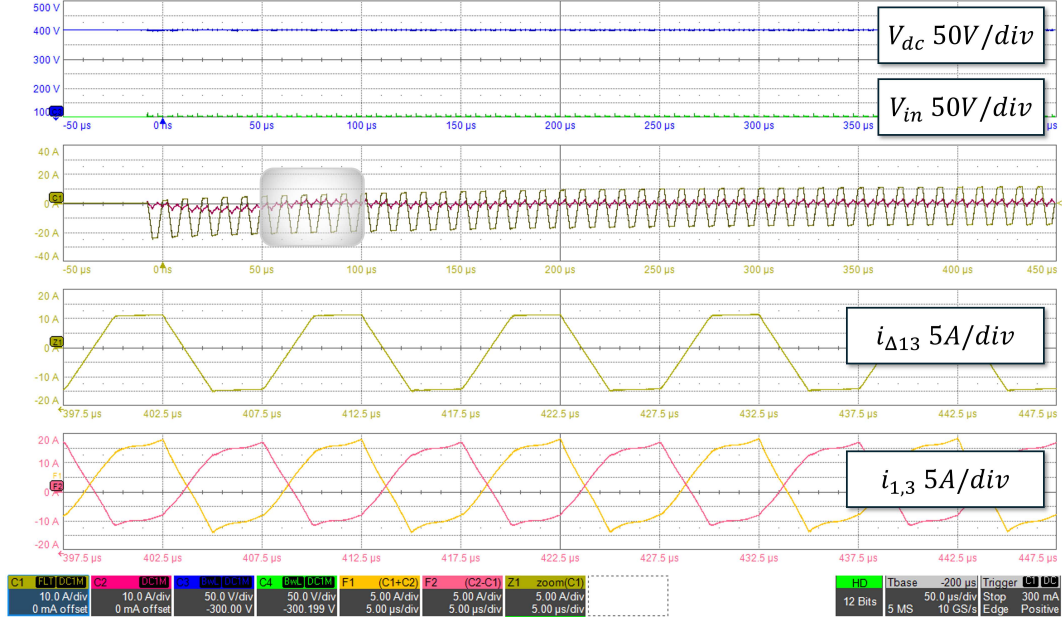


Fig. 3.15 Experimental setup for DC/DC converter control.

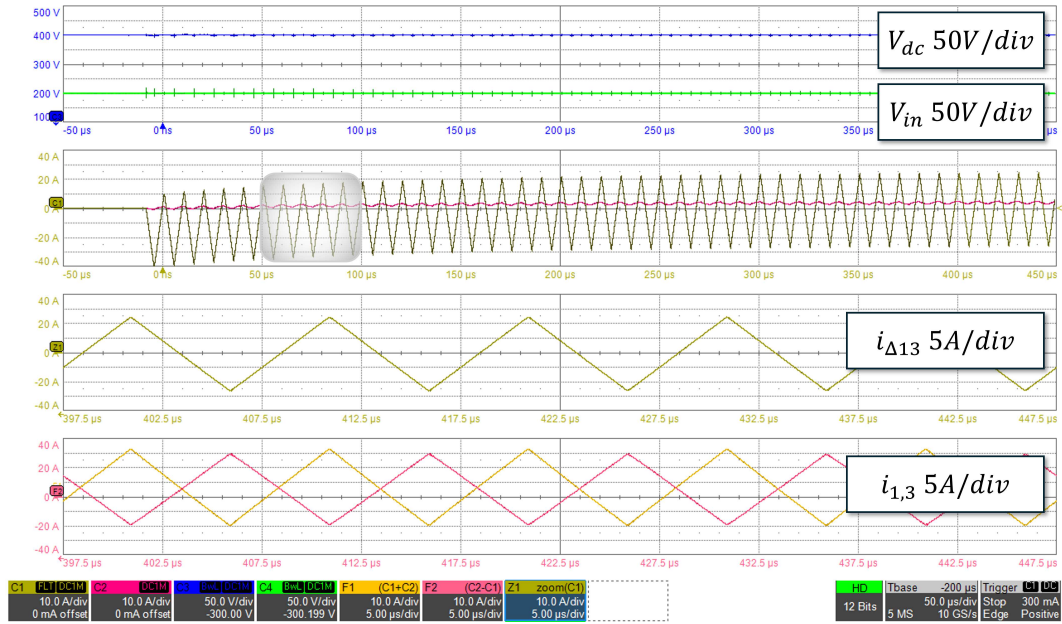
3.4.1 Interleaving current balancing

The first set of experimental tests aims to validate the interleaving balancing performance of the proposed multilevel converter at start-up and steady-state conditions, presented in Fig. 3.16 and Fig. 3.17. For this test, the interleaving stage of the converter was tested independently. Fig. 3.15 presents an overview of the test setup. The measured waveforms in Fig. 3.16a–3.17 show the DC-link voltage $v_{dc,P}$, the input voltage v_{in} , the battery current i_{in} , and the differential current Δi_{13} .

The three plots correspond to different duty-cycle conditions, all regulating the battery current i_{in} to zero. As expected, the ripple of the differential current Δi_{13} occurs at the switching frequency $f_{sw} = 100$ kHz, consistent with the behavior of the leg currents i_1 and i_3 . The shape of these currents directly depends on the phase shift between the legs and the applied duty cycle, in agreement with the analytical waveforms derived in Chapter 2. In Fig. 3.16a, corresponding to a duty cycle of $d = 0.25$, the leg currents i_1 and i_3 exhibit a non-triangular profile, resulting in a trapezoidal differential current Δi_{13} . No noticeable unbalancing is observed, confirming the effectiveness of the differential current balancing loop. Similar performance is obtained for $d = 0.75$, as shown in Fig. 3.17, where the current waveforms are practically identical. The most critical operating condition for the differential current occurs at a duty cycle of $d = 0.5$, where the overlap between the leg currents maximizes the current ripple amplitude, presented in Fig. 3.16b.



(a)



(b)

Fig. 3.16 Interleaving test results for two operating conditions, at (a) $V_{dc,P} = 400V$, $V_{in} = 100V$, (b) $V_{dc,half} = 400V$, $V_{in} = 200V$.

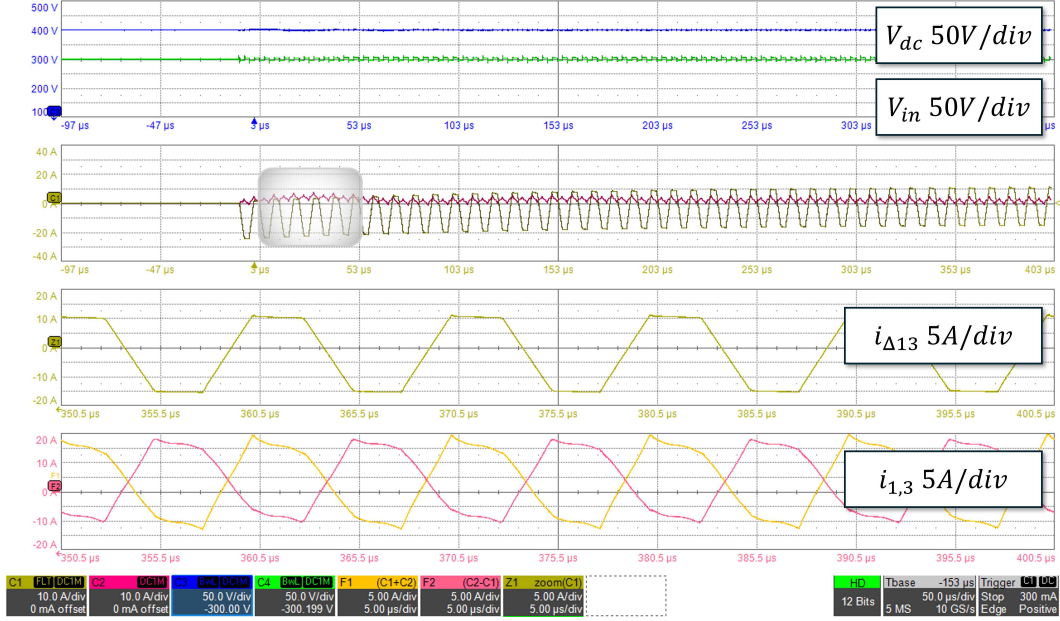


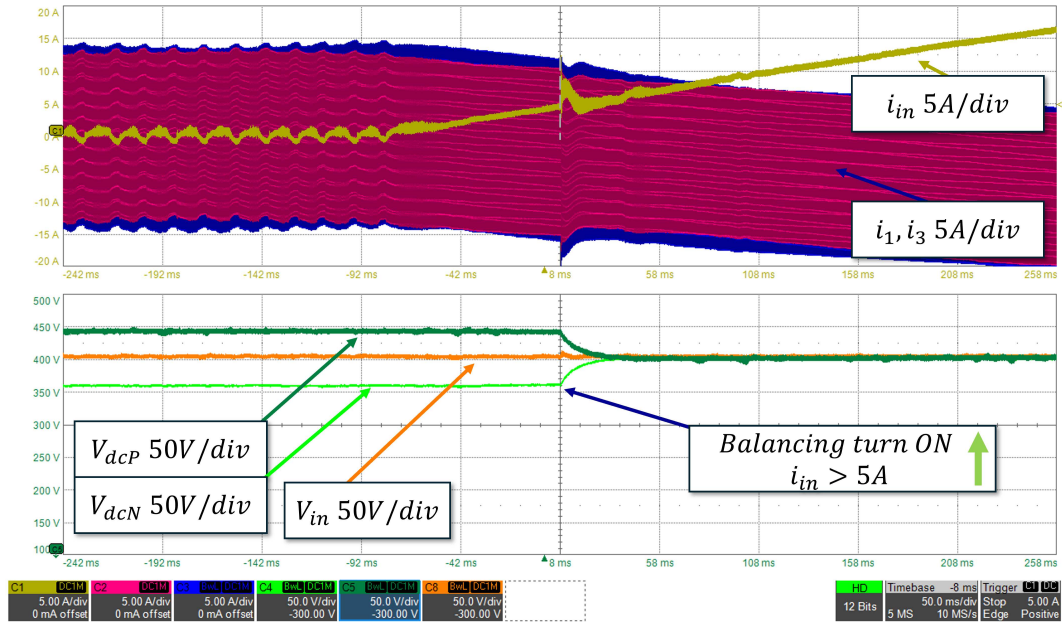
Fig. 3.17 Interleaving test result at $V_{dc,P} = 400\text{ V}$, $V_{in} = 300\text{ V}$.

3.4.2 Capacitor Voltage Balancing

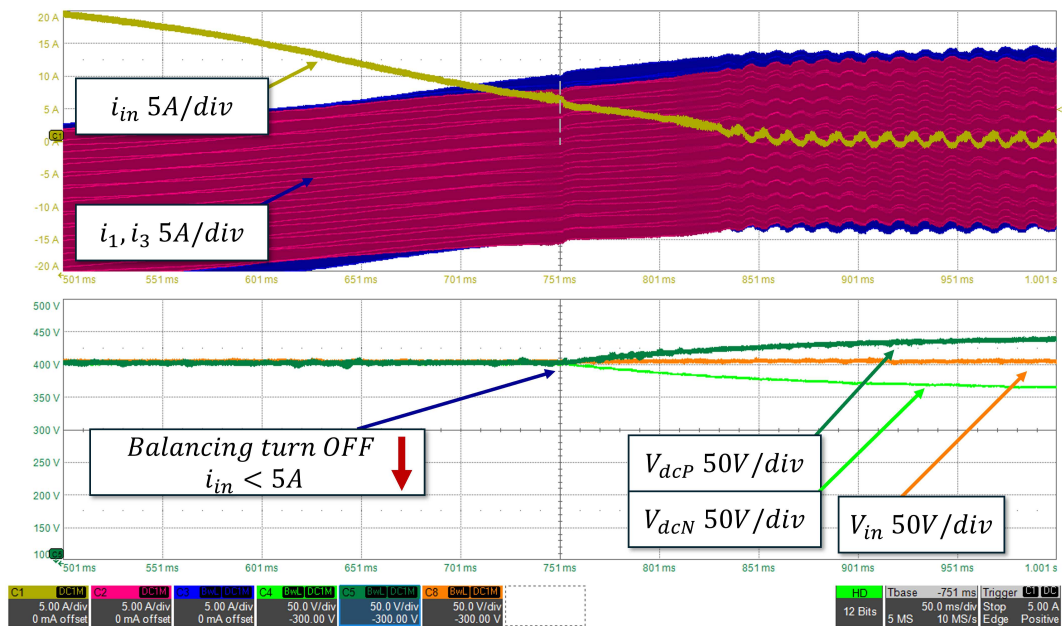
Figure 3.18 illustrates the details of a load transient performed at $V_{dc} = 800\text{ V}$ and $V_{in} = 400\text{ V}$. This operating point at $V_{dc} = 800\text{ V}$ represents the most demanding condition for the proposed converter, as it leads to a maximum unbalance between the split DC-link voltages, with $v_{dc,P} - v_{dc,N} \approx 100\text{ V}$. This unbalance is directly related to the voltage V_{dc} and is directly dependent on the crosstalk between the differential inductors. This could lead to significant unbalanced voltage sharing between the split DC-Link capacitors. An accurate design of the inductors would significantly mitigate this effect. In particular, Figure 3.18a shows the instant at which the capacitor balancing control contribution, denoted as d_{vb} , is activated. This control term becomes effective only when a sufficient load current is circulating through the converter (in this test, $\approx 5\text{ A}$), ensuring that the balancing action contributes to equalizing the capacitor voltages without interfering with the main current control loop. Conversely, when the load current is regulated to zero, the same control term would act as a disturbance, and thus it is automatically disabled.

As observed in Figure 3.18a, only a few milliseconds are sufficient for the balancing loop to restore the voltage symmetry across the split DC-link capacitors, confirming the fast dynamic response of the proposed strategy. Figure 3.18b depicts

the opposite transition: once the balancing contribution is deactivated, the DC-link voltages gradually return to their initial unbalanced condition, as expected. This experimental evidence validates the effectiveness and stability of the implemented balancing mechanism, as well as its capability to dynamically adapt to different load conditions without introducing additional perturbations into the system.



(a)



(b)

Fig. 3.18 Comparison of voltage balancing behavior at $V_{dc} = 800\text{ V}$ and $V_{in} = 400\text{ V}$. Activation (a) and deactivation (b) of the voltage balancing control contribution.

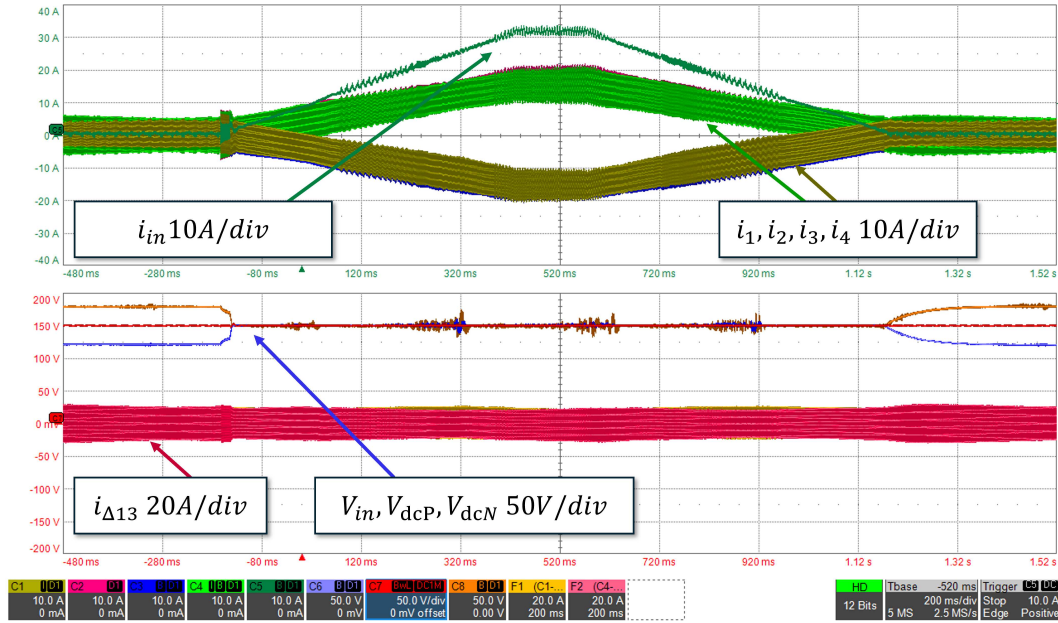


Fig. 3.19 Load step response at $V_{dc} = 600$ V, $V_{in} = 300$ V.

3.4.3 Load Transient Response

For the sake of completeness, a waveform acquisition of a full load transient is presented. To experimentally validate the dynamic performance of the proposed control strategy, a load step is applied to the converter output, varying the input current from zero to a rated load condition of $i_{in} = 30$ A. The corresponding transient waveforms of the input current i_{in} , the four leg currents (i_1, i_2, i_3, i_4), the split DC-link voltages ($v_{dc,P}, v_{dc,N}$), the differential currents ($\Delta i_{13}, \Delta i_{24}$), and the capacitor voltages are shown in Fig. 3.19.

The system exhibits stable and well-damped behavior throughout the entire transient. The current transition occurs smoothly, without overshoot or noticeable oscillations, demonstrating the robustness of the implemented control. Moreover, the DC-link voltages remain well regulated during the load variation, confirming the correct coordination between the current control and the voltage balancing loops. These results validate the capability of the proposed control strategy to maintain steady operation and fast dynamic response under abrupt load changes.

3.5 Summary

This chapter has presented the comprehensive control design and experimental validation of a multilevel interleaved GaN-based DC/DC converter. The proposed control architecture successfully addresses the key challenges of high-frequency operation, including precise current sharing, voltage balancing, and dynamic performance.

The implemented control strategy features a multi-loop structure consisting of five coordinated feedback loops:

- External voltage and current control loops for main power regulation
- Internal voltage balancing loop for split DC-link capacitor equalization
- Two differential current balancing loops for interleaved phase current sharing

Experimental results demonstrate excellent performance across various operating conditions:

- Effective current balancing between interleaved phases with minimal differential current ripple
- Rapid voltage balancing capability (within milliseconds) for split DC-link capacitors
- Stable operation during load transients with smooth current transitions
- Robust performance at 100 kHz switching frequency with 200 kHz sampling rate

The experimental validation confirms that the proposed control approach effectively manages the complexities of multilevel interleaved converters while maintaining stability and performance across the entire operating range, providing a solid foundation for high-power automotive applications.

Chapter 4

DC/DC converter - *Design and Testing*

4.1 Introduction

The successful integration of fuel cell systems into electric vehicle powertrains requires careful attention to the design of the associated power electronics, with the DC/DC converter playing a central role as the interface between the low-voltage fuel cell stack and the high-voltage traction inverter [21, 16]. The high energy density of fuel cells allows for long-range transportation, yet the inherently low voltage output and nonlinear behavior of the stack pose significant challenges for reliable and efficient operation [72, 73, 25, 26, 74]. A properly designed step-up converter is thus essential, often complemented by an auxiliary battery to manage transient power peaks and regenerative braking energy.

Traditional non-isolated, two-level DC/DC converters are simple and cost-effective, but their performance is limited when voltage and power requirements increase [75, 13]. As presented in 2, interleaved converter topologies provide an effective solution, distributing the current across multiple stages to reduce input and output current ripple, increase the effective switching frequency, and improve dynamic response [62, 23, 47, 48]. This also enhances thermal management and system reliability, as heat generation is spread across several conversion stages.

Wide bandgap devices, particularly GaN transistors, enable operation at high switching frequencies with lower losses compared to Si and SiC devices [76, 77]. However, the current handling limitations of commercially available GaN devices pose challenges for high-power applications typical of automotive traction systems.

Solutions include using multiple devices in parallel and employing interleaved converter stages, which address current limitations and improve ripple, thermal performance, and redundancy.

Voltage limitations of GaN devices represent another design constraint, with commercial high-power transistors typically rated up to 650 V. Multilevel converter topologies help overcome these restrictions, though they introduce additional design and control complexity [77]. Similarly, the design of magnetic components is critical, as high switching frequencies increase core and winding losses. Coupled inductors and careful magnetic design improve power density and reduce losses [75], but require advanced control strategies to synchronize interleaved stages, manage low sampling periods, and implement multiple cascaded feedback loops.

Extensive research has focused on interleaved multilevel DC/DC converters for automotive applications [47, 48, 15, 49, 78, 53, 50, 79, 80]. These studies primarily address operating principles and experimental validation, rather than providing a detailed design methodology.

This chapter presents a complete design of a three-level, interleaved boost DC/DC converter for fuel cell automotive powertrains, including the evaluation of converter losses using GaN device characterization and thermal design, the comprehensive stress analysis of passive components, the DC link design, and the experimental validation of a full-scale prototype, including the converter's efficiency map.

4.2 Specifications and performance requirements

As previously presented in Section 2, the proposed DC/DC converter stage is characterized by an interleaved multilevel structure. In particular, the converter is designed for a nominal output power of 75 kW, with a target efficiency above 98% under the operating conditions specified in Table 4.1. During the experimental characterization, the prototype was also operated up to approximately 80 kW under selected operating conditions.

Considering the stringent requirements of fuel cell electric powertrains, a multi-level interleaved boost topology is adopted. As discussed in Section 2, the low and variable output voltage of the fuel cell stack (typically around 200-300 V) requires a high-efficiency step-up stage to reach the DC-link voltage range of 400–800 V.

Table 4.1 Main specifications of the DC/DC converter.

Symbol	Description	Nominal
V_{in}	Input voltage	100-500 V
V_{out}	Output voltage (nominal)	400-800 V
I_{in}	Input current, bidirectional	± 200 A
P_n	Reference power @ $V_{in} = 400$ V, $V_{out} = 800$ V	75 kW
f_{sw}	Switching frequency	100 kHz
η	Target efficiency @ $0.8P_n$, $V_{in} = 400$ V, $V_{out} = 700$ V	$> 98\%$

Moreover, the adoption of wide bandgap devices, specifically GaN transistors, enables switching frequencies up to 100 kHz, thereby improving power density and dynamic performance.

The schematic of the considered multilevel interleaved GaN boost DC/DC converter is illustrated in Fig. 4.1. The split DC-link capacitors C_P and C_N , together with the external capacitor C_{dc} , form the output stage, which is regulated by the digital control system presented in Section 3. Thanks to the cascaded and interleaved structure, the converter is capable of maintaining accurate voltage regulation and capacitor voltage balancing while achieving the expected efficiency.

Part of the content of this chapter has been published in [31]

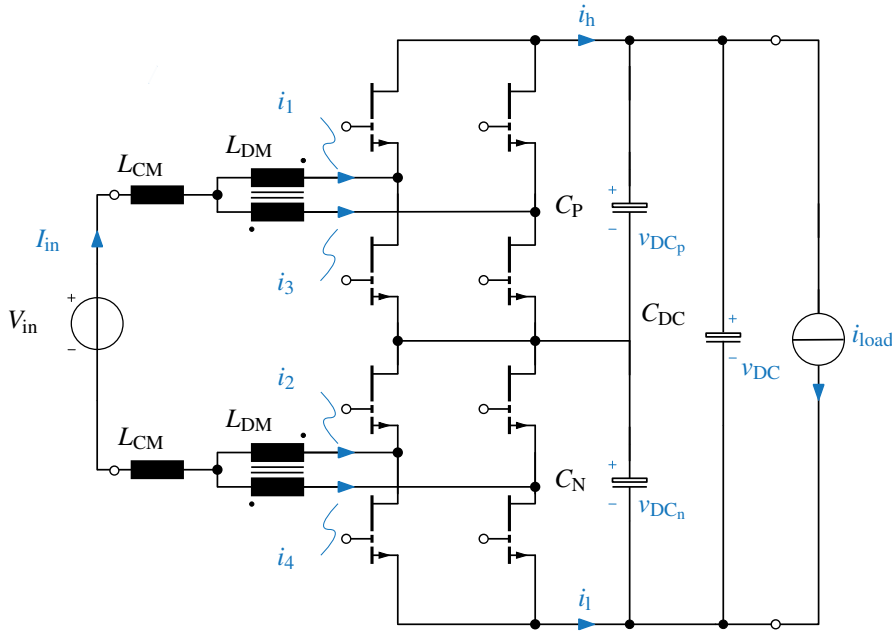


Fig. 4.1 Equivalent circuit schematic of the considered multilevel interleaved GaN boost DC/DC converter for fuel cell applications.

4.3 Semiconductor devices selection

The selection of appropriate power semiconductor devices represents one of the most crucial design decisions in the development of high-performance power electronic converters, especially for electric vehicle traction inverters, where the competing demands of efficiency, power density, reliability, and cost must be carefully balanced. The emergence of WBG semiconductors has fundamentally altered the performance landscape of power electronics, offering substantial advantages over conventional silicon technologies [81–83].

This analysis focuses on the 400/500 V device class, which presents particular strategic importance for the next-generation power converter. These devices enable operation in both 400 V and 800 V DC-link architectures when deployed in advanced multilevel converter topologies [84–86]. Among WBG technologies, GaN devices have demonstrated exceptional theoretical performance characteristics but remain at an earlier stage of technological maturity compared to SiC MOSFETs. However, the fundamental material properties of GaN, including higher electron mobility (2000 cm²/V·s versus 900 cm²/V·s for SiC and 1400 cm²/V·s for Si) and higher electron

saturation velocity, make them particularly suitable for high-frequency switching applications [87–89].

Figure-of-Merit Analysis

To quantitatively evaluate and compare different semiconductor technologies, the Hard Switching Figure-of-Merit (HSFOM) was selected for this analysis, as it comprehensively accounts for both conduction and switching losses, including the critical reverse recovery behavior, while maintaining dependence on actual operating conditions (switching frequency and junction temperature) [90]. The HSFOM is defined as:

$$\text{HSFOM} = \frac{1}{\sqrt{R_{\text{ds,on}}Q_{\text{oss}} + k_i\sqrt{f_{\text{sw}}V_{\text{sw}}\tau_{\text{rr}}}}} \quad (4.1)$$

where:

- $R_{\text{ds,on}}$ is the on-state resistance,
- Q_{oss} is the output charge,
- f_{sw} is the switching frequency,
- V_{sw} is the switched voltage,
- τ_{rr} is the reverse recovery time constant,
- k_i is a current waveform-dependent coefficient ($\sqrt{2}/\pi$ for sinusoidal operation).

The analysis of commercially available 600/650 V devices from major manufacturers reveals several important trends. SiC MOSFETs generally exhibit superior $R_{\text{ds,on}}Q_{\text{oss}}$ product characteristics at room temperature compared to most GaN devices [90]. However, GaN devices, particularly direct-drive d-mode HEMTs from VisIC and e-mode HEMTs from Infineon (GIT technology), demonstrate competitive and in some cases, superior performance, especially when considering the complete loss model encapsulated by the HSFOM.

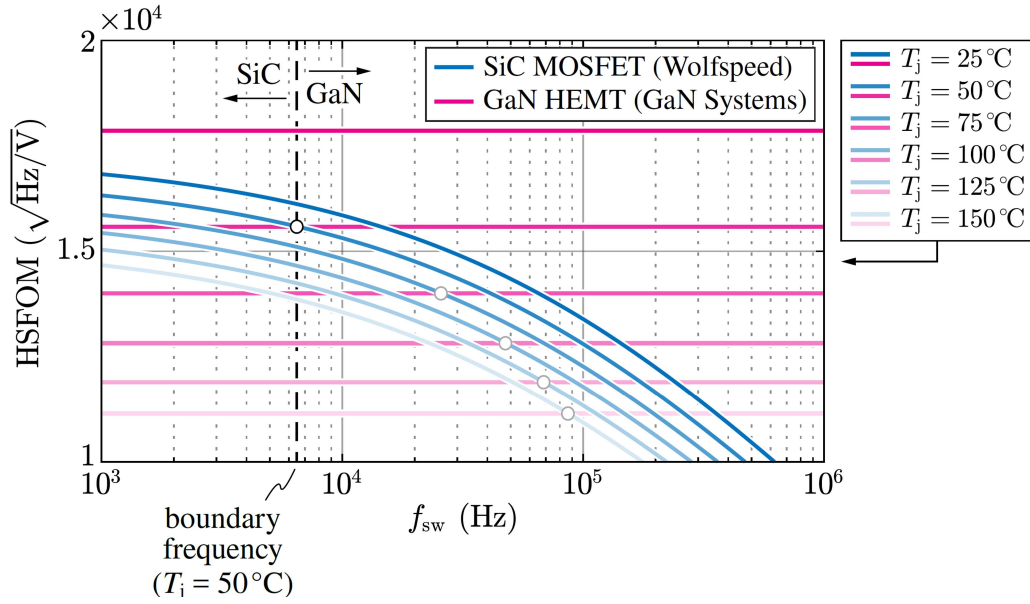


Fig. 4.2 HSFOM comparison showing the performance advantage of GaN vs SiC devices above the crossover frequency [90].

Notably, GaN devices exhibit greater sensitivity to junction temperature variations compared to SiC devices. The $R_{ds,on}$ of GaN devices typically increases by a factor of 1.8-2.2 between 25 °C and 150 °C, while SiC devices show a more moderate increase of 1.4-1.6 over the same temperature range [90]. This temperature dependence must be carefully considered in the design of automotive traction inverters, where junction temperatures can vary significantly during operation.

The HSFOM analysis reveals a crucial crossover phenomenon: for switching frequencies above a certain boundary (which depends on junction temperature), GaN devices from VisIC outperform SiC MOSFETs. As shown in Figure 4.2, at a junction temperature of 50 °C, this crossover occurs at approximately 6 kHz. Given the target switching frequency of the proposed converter (which exceeds this crossover point) and the expected junction temperature profile, VisIC's direct-drive devices demonstrate clear superiority in terms of theoretical performance, as presented in [90]. Fig. 4.3 shows the conduction characteristic and the ON/OFF energy curves extracted from the V08 datasheet.

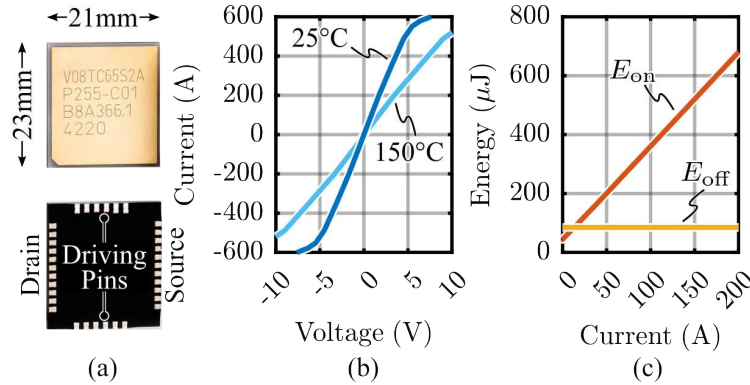


Fig. 4.3 VisIC V08TC65S2A GaN switch: (a) package and dimensions, (b) conduction characteristics, (c) switching losses provided by the datasheet [31].

GaN Semiconductor Technologies

GaN power devices are based on a specific semiconductor structure that makes them very different from conventional silicon devices. At the interface between aluminum gallium nitride (AlGaN) and GaN, strong spontaneous and piezoelectric polarization effects create a two-dimensional electron gas (2DEG). This 2DEG allows very high electron mobility and carrier density, which is the key property behind the superior performance of GaN devices [91–93]. Although all commercial GaN devices rely on this principle, their design can differ significantly depending on the gate structure and the way they are driven.

One important category is the enhanced-mode (e-mode) high electron mobility transistor (HEMT). These devices are designed to be normally off, which is preferred for power applications. Different techniques, such as recessed gates, plasma treatment, or p-doped GaN gate structures, are used to achieve this behavior [94, 95]. E-mode HEMTs switch very efficiently, but they also bring challenges. Their threshold voltages are usually very low (around 1–2 V), and the safe gate voltage range is narrow (typically up to 5–6 V). This means that even small voltage overshoots or oscillations at the gate can cause serious device failure, making careful circuit layout and advanced gate driving strategies essential [96–99].

Another widely used solution is the cascode configuration. In this case, a depletion-mode GaN HEMT is combined with a low-voltage silicon MOSFET in series [100, 101]. This arrangement also provides normally-off operation but with gate driving requirements similar to those of standard silicon MOSFETs, which

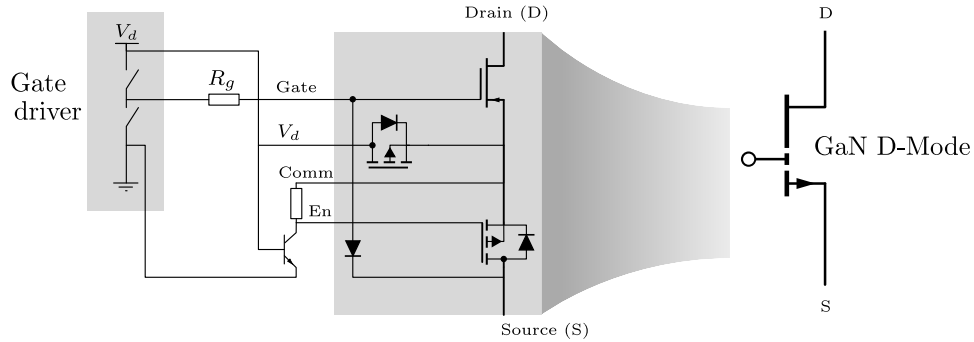


Fig. 4.4 Simplified schematic of VisIC's direct-drive architecture showing the integrated enabling circuit and direct gate drive connection.

makes it easier to use. On the other hand, the cascode structure increases packaging complexity and parasitic inductance, which can reduce the switching speed. In addition, the silicon MOSFET's body diode contributes to reverse recovery losses, though these losses remain much lower than in traditional high-voltage silicon devices [100].

Direct-Drive Architecture

The direct-drive architecture represents an innovative approach that combines the benefits of both conventional cascode and e-mode HEMT configurations while mitigating their respective limitations [102, 103]. This technology maintains the depletion-mode GaN HEMT structure, but incorporates an integrated enabling circuit that ensures normally-off operation without the switching-related drawbacks of traditional cascode configurations.

The operational principle of the direct-drive architecture provides several significant advantages that make it particularly suitable for automotive traction applications. First, it eliminates the reverse recovery losses associated with the Si MOSFET body diode in conventional cascode configurations, as the enabling circuit does not participate in the switching operation [104]. Second, it maintains the robust gate driving characteristics of cascode devices, with higher threshold voltage and greater noise immunity compared to e-mode HEMTs [102]. The architecture provides inherent protection against common failure modes, including undershoot conditions during start-up or auxiliary power loss events [104, 105].

Furthermore, the combination of controlled switching behavior (achievable through external gate resistance adjustment R_g) and the absence of reverse recovery

ery losses results in favorable electromagnetic compatibility (EMI) characteristics [97], which is particularly important in automotive applications where strict EMI standards must be met. The lateral structure of GaN devices also enables more efficient heat extraction from both sides of the die, potentially improving thermal management compared to vertical devices [88]. This characteristic is valuable in high-power-density converter designs and contributes to the system-level benefits of GaN technology, including reduced passive component sizes due to high switching frequency capability and improved efficiency that reduces thermal management requirements [96, 106].

Experimental Characterization of Power Devices

The switching energies $E_{sw,on}$ and $E_{sw,off}$ were experimentally characterized by means of the Double Pulse Test (DPT) method. The schematic of the DPT setup is shown in Fig. 4.5(a). The test circuit consists of a half-bridge leg, where a resistive shunt R_{shunt} is inserted between the source terminal of the DUT and the negative DC-link rail for current measurement. An external inductor L_{ext} is connected between the positive DC link and the upper GaN device, acting as the energy storage element required to generate the load current. In addition, the setup allows the integration of a heater to control the junction temperature T_j of the DUT, thus enabling the investigation of temperature-dependent switching behavior.

The experimental campaign was carried out using a commercial Keysight PD1500 DPT system, which provides automated calibration and measurement routines. During the tests, the main electrical quantities monitored were the drain-source voltage v_{ds} , the drain current i_d , and the gate current i_g at turn-on. For all tests, the turn-on and turn-off gate resistances were set to 0.4Ω . The resulting switching energies at $V_{dc} = 400\text{ V}$, obtained for different load currents and junction temperatures, are reported in Fig. 4.5a. These experimental results provide a reliable basis for the converter loss analysis presented next.

Based on the evaluated E_{on} and E_{off} obtained through a DPT procedure, a PLECS model has been constructed and different simulations are performed to evaluate the component stress under all the different operating conditions. Fig. 4.6 presents the average switching losses of the high-side and low-side devices of one of the four half-bridge legs of the converter, varying V_{dc} over the operating range. As expected, the distribution of the losses is based on the current direction of the

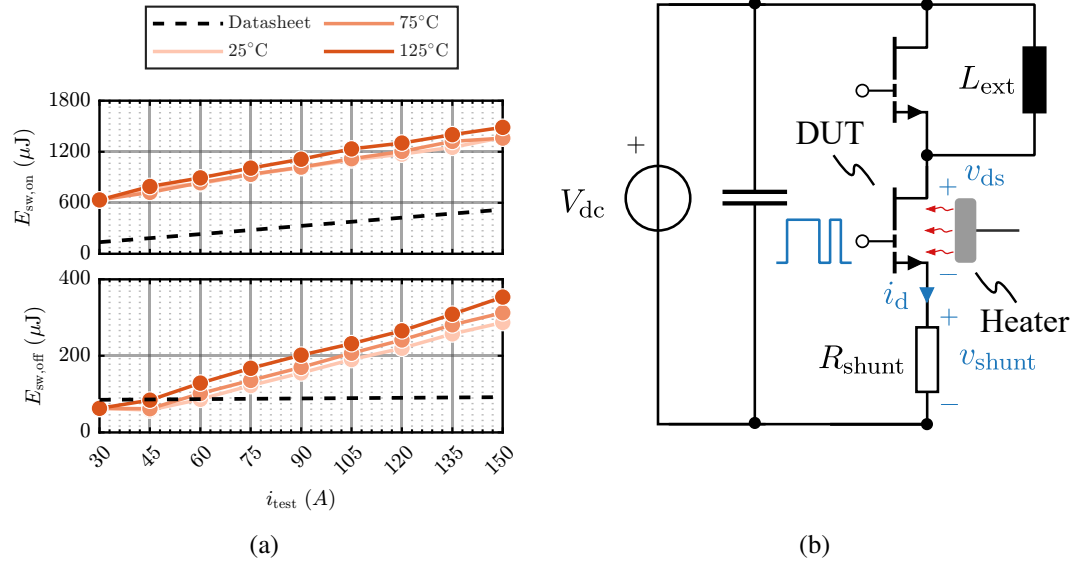


Fig. 4.5 (a) Experimental turn-on and turn-off switching energies for V08TC65S2A; (b) DPT setup circuit diagram [31].

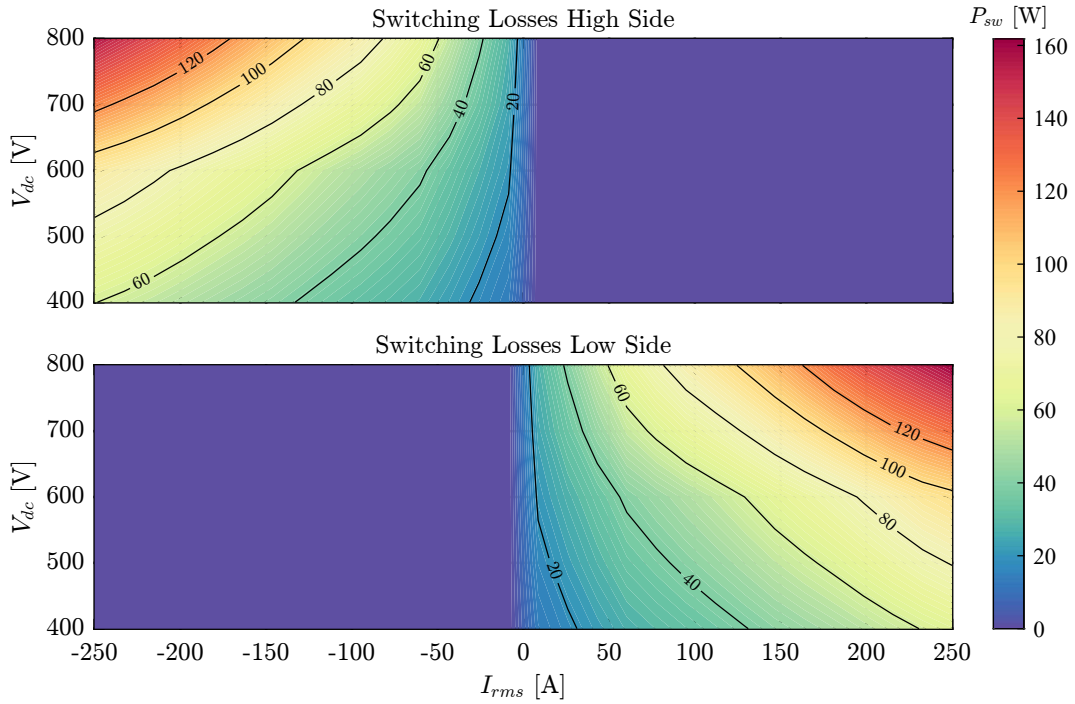


Fig. 4.6 Comparison of the switching losses for the high-side and low-side devices at $f_{sw} = 100kHz$.

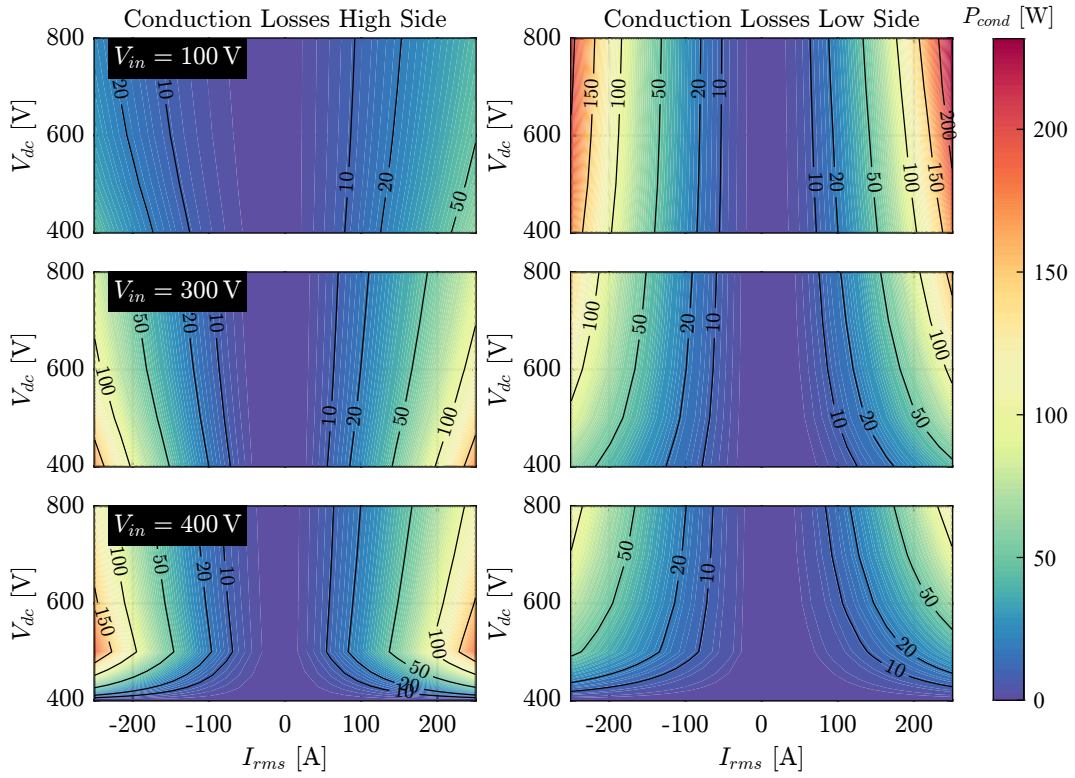


Fig. 4.7 Comparison of the conduction losses for the high-side and low-side devices for different V_{in} at $f_{sw} = 100\text{kHz}$.

converter, defined by the buck or boost operation. For the sake of completeness, Fig.4.7 presents the evaluated conduction losses. As can be noticed, the conduction losses are significantly dependent on the achieved duty cycle. When the boosting step-up is too high, a significant imbalance in the loss distribution occurs.

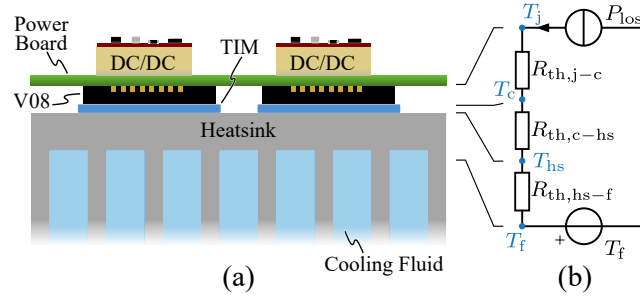


Fig. 4.8 (a) Arrangement of the power devices on the heatsink. (b) Steady-state thermal network of the switches [31].

4.4 Heatsink design and Thermal management

Most commercially available GaN switches exhibit a significant dependence of their on-state resistance on temperature. Typically, the on-state resistance measured at 25°C increases by a factor of 2 to 2.5 when the junction temperature reaches 150°C [107]. For the selected V08TC65S2A GaN device, as shown in Fig. 4.3(b), the on-state resistance at 150°C is approximately twice the value observed at 25°C.

This temperature dependence necessitates a careful design of the heatsink to achieve a low junction-to-fluid thermal resistance, $R_{th,j-f}$, in order to limit the device temperature rise and, consequently, the conduction losses. The total thermal resistance $R_{th,j-f}$ consists of three contributions, as illustrated in the thermal network depicted in Fig. 4.8:

- The junction-to-case thermal resistance, $R_{th,j-c}$, is primarily determined by the device package and is typically provided in the datasheet. For the V08TC65S2A, the junction-to-case thermal resistance of a single device is 0.1°C/W, resulting in an equivalent $R_{th,j-c}$ of 0.0125°C/W for the configuration used. Notably, the GaN device case is already electrically insulated, so no additional insulation between the case and the heatsink is required.
- The case-to-heatsink thermal resistance, $R_{th,c-hs}$, is associated with the Thermal Interface Material (TIM). In this study, HY510 thermal grease is selected as TIM, with a thermal conductivity λ of 1.9 W/(mK). The equivalent thermal resistance is calculated according to (4.2), where S is the total contact area of the GaN devices ($8 \times 21 \text{ mm} \times 23 \text{ mm}$) and a TIM thickness x of 100 μm is assumed. The resulting $R_{th,c-hs}$ is 0.0167°C/W.

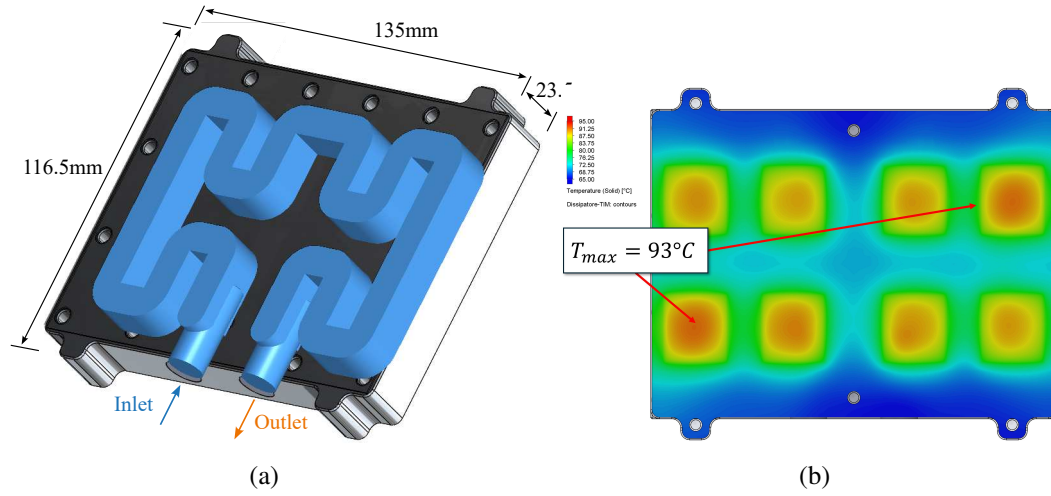


Fig. 4.9 Heatsink 3D structure (a) and corresponding FEM thermal simulation results (b).

- The heatsink-to-fluid thermal resistance, $R_{th,hs-f}$, characterizes the ability of the heatsink to dissipate heat to the cooling fluid. The maximum required value, $R_{th,hs-f}^{max}$, is computed by solving the thermal network in Fig. 4.8, as reported in (4.3). Assuming a fluid temperature $T_f = 60^\circ\text{C}$, a maximum allowable junction temperature $T_{j,max} = 140^\circ\text{C}$, and a minimum nominal efficiency of 98% (corresponding to maximum converter losses of 1500 W), the resulting $R_{th,hs-f}^{max}$ is 0.0275°C/W .

$$R_{th,c-hs} = \frac{x}{\lambda \cdot S} \quad (4.2)$$

$$R_{th,hs-f}^{min} = \frac{T_{j,max} - T_f}{P_{loss}} - R_{th,j-c} - R_{th,c-hs} \quad (4.3)$$

A custom heatsink has been designed, and its 3D layout is shown in Fig. 4.9a, where the external dimensions and the fluid path are highlighted. The heatsink-to-fluid thermal resistance is evaluated using Finite Element Method (FEM) simulations in FlowSim-SOLIDWORKS, assuming a fluid flow rate of 8 L/min, a fluid temperature of 60°C , and 200 W of losses per GaN device. The temperature distribution on the heatsink surface is shown in Fig. 4.9b.

The resulting $R_{th,hs-f}$ is approximately 0.01°C/W , calculated as the ratio of the difference between the average surface temperature and T_f to the total power losses. Based on these results, an estimate of the internal junction temperature can be

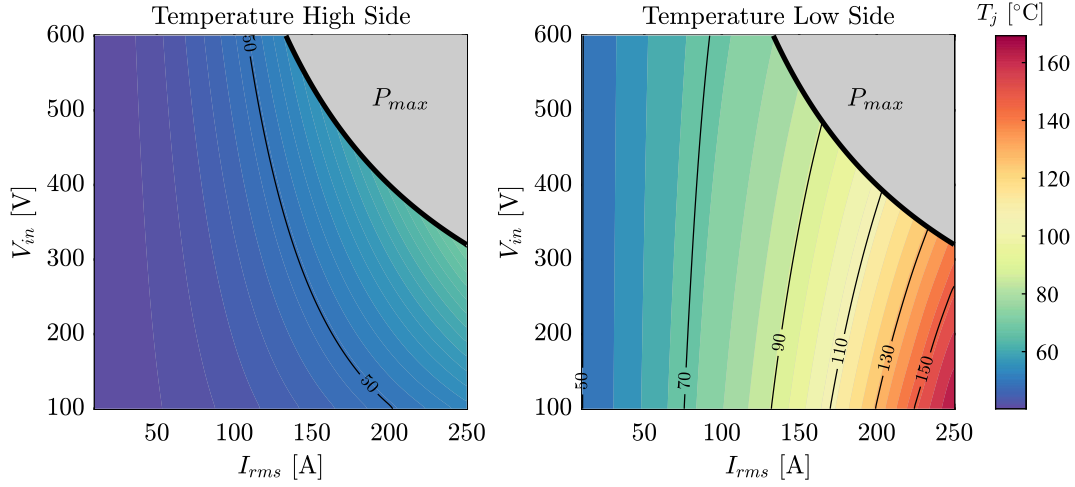


Fig. 4.10 Comparison of the device junction temperatures for the high-side and low-side devices at $V_{dc} = 800V$ and variable V_{in} .

obtained through PLECS simulation, as presented in Fig. 4.10 at nominal V_{dc} . This value satisfies the previously determined minimum thermal resistance requirement.

4.5 Design of Magnetic Components

The design of the magnetic components is a critical step in the development of the proposed converter, as the inductors largely determine current ripple, associated losses, and overall power density. Both differential-mode (DM) and common-mode (CM) inductances must be designed to comply with the current-ripple specifications across the full operating range of the fuel-cell system.

In the previous chapter, an analytical extraction of the peak-to-peak flux ripples for the DM and CM components as functions of the duty cycle and input voltage was performed. Those flux ripples, denoted here as $\Delta\Phi_{L_{dm}}$ and $\Delta\Phi_{L_{cm}}$, provide the starting point for the inductor design.

The maximum values of the flux ripple for the common and differential modes can be evaluated as:

$$\Delta\Phi_{L_{cm},max,pk} = \frac{1}{128} T_{SW} V_{dc} = 62.5 \mu Wb \quad (4.4)$$

$$\Delta\Phi_{Ldm,pk|_{max}} = \frac{1}{8}T_{sw}V_{dc,half} = 0.005 \text{ Wb} \quad (4.5)$$

Consequently, to limit the current ripple to a prescribed maximum ΔI_{max} , the inductances must satisfy

$$L \geq \frac{\Delta\Phi_{Ldm,pk|_{max}}}{\Delta I_{pk|_{max}}}, \quad (4.6)$$

Based on the desired maximum current ripple of $\Delta i_{cm,pk} = 5 \text{ A}$ and $\Delta i_{dm,pk} = 7 \text{ A}$, the minimum inductance values can be evaluated as:

$$\begin{aligned} L_{cm,min} &= \frac{\Delta\Phi_{Lcm,pk|_{max}}}{\Delta i_{cm,pk}} = 12.5 \mu H \\ L_{dm,min} &= \frac{\Delta\Phi_{Ldm,pk|_{max}}}{\Delta i_{dm,pk}} = 71.4 \mu H \end{aligned} \quad (4.7)$$

4.5.1 Modal vs per-winding notation (conventions)

To avoid ambiguity it is necessary to state explicitly the adopted conventions. Let

- L_m denote the magnetizing inductance *per winding* (i.e. the portion of the self-inductance that is coupled through the core and thus responsible for the core flux);
- L_ℓ denote the leakage inductance *per winding* (i.e. the uncoupled portion associated with external/leakage flux).

The self- and mutual-inductances

$$L_{11} = L_{22} = L_m + L_\ell, \quad L_{12} = L_m,$$

with the sign of L_{12} chosen consistently with the winding orientation used in the layout.

Using the modal decomposition introduced in Section 2.2.4 (with $i_{cm} = (i_1 + i_2)/2$, $i_{dm} = (i_1 - i_2)/2$), the *modal inductances* that enter the flux/current relations for the CM and DM modes are (for the winding polarity adopted here, where the DM excites the core and the CM ideally cancels the core flux):

$$L_{cm} = L_\ell, \quad L_{dm} = (2L_m + L_\ell). \quad (4.8)$$

These expressions mean:

- the common-mode *modal* inductance is determined only by leakage (two windings contribute);
- the differential-mode *modal* inductance contains the strong magnetizing contribution plus the leakage contribution from both windings.

4.5.2 Minimum inductance requirements and numerical values

Using the flux ripple expressions of Section 2.2.4 and Eq. (4.6), the minimum required modal inductances (worst case over the operating range) are estimated as presented in (4.7).

As the multilevel structure will present two differential inductors, each passive component should have a minimum L_ℓ of

$$L_\ell = \frac{12.5}{2} = 6.25\mu H \quad (4.9)$$

Indeed, the minimum magnetizing inductance L_m is:

$$L_m = \frac{(L_{dm} - L_\ell)}{2} = 32.5\mu H \quad (4.10)$$

4.5.3 Magnetic structure selection, analytical and FEM validation

A coupled inductor is adopted to obtain a large DM inductance within a compact volume. In the chosen topology both windings are placed on the central leg of the core so that the DM flux is largely confined within the core (magnetizing path), while the CM flux ideally cancels and only leakage flux remains. The selected core and winding parameters are summarized in Table 4.2. The final inductor is presented in Fig.4.11. The magnetizing (DM coupled) inductance can be estimated from the core reluctance $\mathcal{R}$ as

$$\mathcal{R} = \frac{l_c}{\mu_0 \mu_r A_c}, \quad L_{DM,coupled} = \frac{(2N)^2}{\mathcal{R}}, \quad (4.11)$$

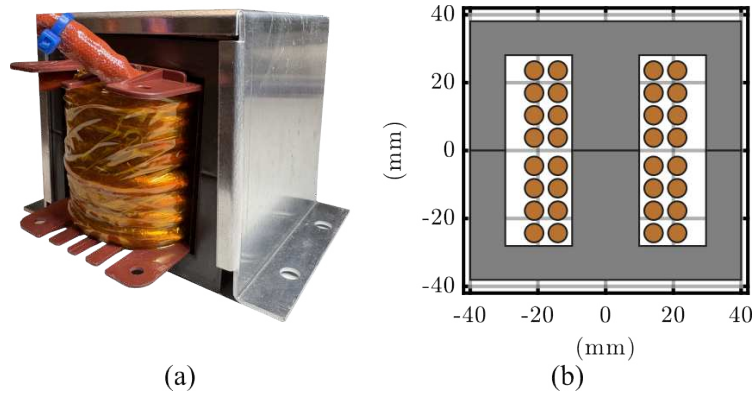


Fig. 4.11 (a) Final Inductor design and (b) 2D section of the inductor.

Table 4.2 Main parameters of the designed inductor.

Part	Parameter	Value
Core	Parallel cores	4
	Shape	EE 8038
	Material	High Flux 26
Winding	Turns N	8
	Type	Litz wire
	Strands n_s	1400
	Strand diameter d_{Cu}	$100 \mu m$

where N is the number of turns per winding.

The leakage inductance is estimated from the magnetic energy stored in the external (leakage) region:

$$L_\ell = \frac{2W_\ell}{I^2}, \quad (4.12)$$

where W_ℓ is extracted from FEM (or analytical fringe estimates) and I is the test current used for the extraction.

With the chosen geometry, the computed values are:

$$L_m = 36.17 \mu H, \quad L_\ell = 3.46 \mu H.$$

The resulting modal totals are

$$L_{dm} = 2L_m + L_\ell = 72.34 \mu H, \quad L_{cm} = 2 \cdot L_\ell = 6.24 \mu H,$$

which satisfy the minimum requirements presented in (4.7).

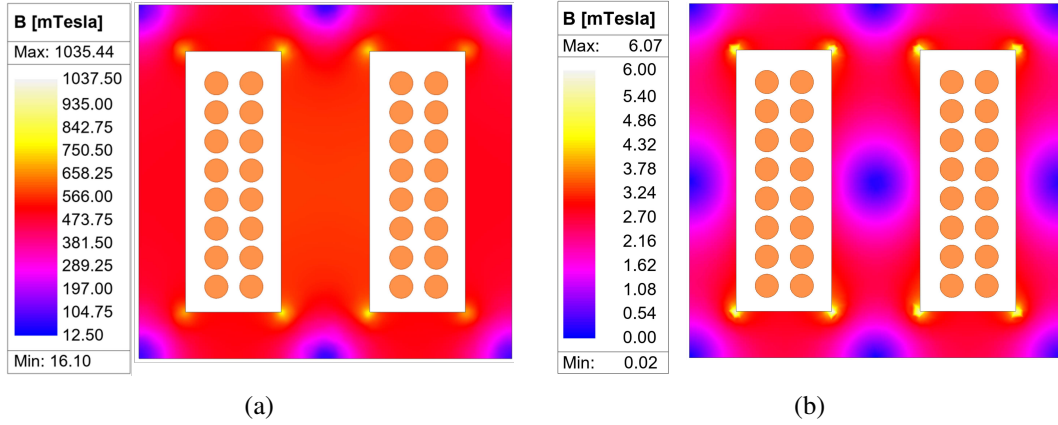


Fig. 4.12 Comparison of flux distributions in the differential inductor: (a) Common-mode flux distribution over the differential inductor core at $I = 100$ A, $\Delta I_{\text{pkpk}} = 10$ A and $f_{\text{sw}} = 100$ kHz; (b) Differential-mode flux distribution over the differential inductor core at $\Delta I_{\text{pkpk}} = 15$ A and $f_{\text{sw}} = 200$ kHz.

Finite-element simulations are used to validate the analytical predictions. The leakage inductance is extracted from the external field energy and compared with the analytical/approximate estimation. The FEM model also confirms that the core operates below saturation, as reported in Fig. 4.12, which shows the worst operating point of the converter and the flux distribution over the differential inductor. The analytical and simulation results are compared with LCR meter measurements of the inductor. The results are reported in Table 4.3.

Table 4.3 Comparison between estimated and measured inductances (modal values).

Parameter	Estimated (FEA+MATLAB)	LCR Meter Measurement
L_{dm}	72.3 μH	75.79 μH
L_{cm}	4.24 μH	6.28 μH

4.5.4 Loss estimation

The inductor losses are estimated as the sum of winding conduction losses and core losses. Conduction losses are computed in the frequency domain:

$$P_{\text{cond}} = 0.5 \sum_{k=1}^n R_{\text{ac}}(f_k) \hat{i}_{\text{L}}^2(f_k), \quad (4.13)$$

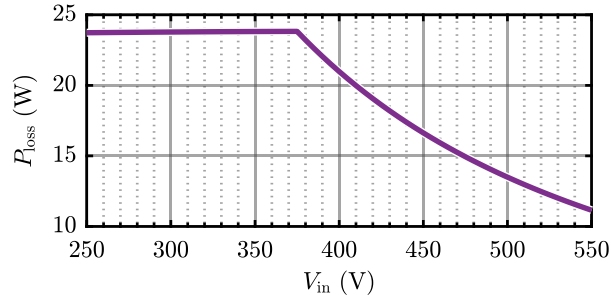


Fig. 4.13 Estimated power losses of the designed inductor as a function of the input voltage.

where $R_{ac}(f_k)$ accounts for skin and proximity effects and $\hat{i}_L(f_k)$ is the spectral content of the inductor current. Core losses are estimated using the improved Generalized Steinmetz Equation (iGSE) [108]:

$$P_{core} = \frac{k_i}{T} \int_0^T \left| \frac{dB(t)}{dt} \right|^\alpha \Delta B^{\beta-\alpha} dt, \quad (4.14)$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos \theta|^\alpha 2^{\beta-\alpha} d\theta}.$$

Fig.4.13 reports the estimated total power losses of the designed inductor at rated power, for different input voltages.

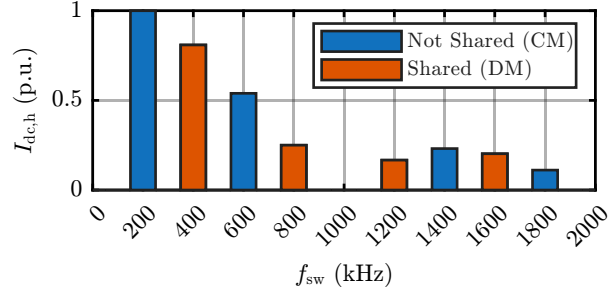


Fig. 4.14 Fourier harmonic spectrum of the DC-link current, emphasizing the CM (not shared) and DM (shared) components.

4.6 DC-link Design

The design of the DC-link capacitors is driven by the charge ripple requirements derived from the converter operation. The total DC-link charge ripple waveform $\Delta Q_{DC}(t)$ is computed by integrating the high-frequency (HF) component of the DC-link current, which includes both common-mode (CM) and differential-mode (DM) contributions:

$$\Delta Q_{DC}(t) = \int_0^T i_{DC,HF}(t) dt. \quad (4.15)$$

The waveform of $i_{DC,HF}(t)$ has been obtained from time-domain simulations and through analytical computation, as described in Section 2.3. The harmonic spectrum of the DC-link current is reported in Fig. 4.14.

The interleaved operation of the converter divides the harmonic content into two groups: 1. *Not-shared harmonics* (CM), which independently affect v_{DC_P} and v_{DC_N} . 2. *Shared harmonics* (DM), which simultaneously contribute to v_{DC_P} , v_{DC_N} , and v_{DC} .

The adopted DC-link consists of two parallel capacitor branches: one associated with the half DC-link voltages ($C_P = C_N = C_{P|N}$), and one across the full DC-link voltage (C_{DC}). The distribution of shared harmonics depends on the sharing ratio k :

$$k = \frac{C_{DC}}{C_{P|N}}. \quad (4.16)$$

Accordingly, the charge ripple expressions for the capacitor banks are:

$$\begin{aligned}
Q_{C_{P|N}}(t) = & \underbrace{\sum_{h=1}^n \hat{Q}_{DC,ns}(2h) \sin(\omega_h t + \phi_h)}_{\text{Not-shared}} \\
& + \underbrace{\sum_{h=1}^n \hat{Q}_{DC,s}(4h) \frac{1}{1+2k} \sin(\omega_h t + \phi_h)}_{\text{Shared}},
\end{aligned} \tag{4.17}$$

$$Q_{C_{DC}}(t) = \underbrace{\sum_{h=1}^n \hat{Q}_{DC,s}(4h) \frac{k}{1+2k} \sin(\omega_h t + \phi_h)}_{\text{Shared}}. \tag{4.18}$$

The methodology adopted to size the capacitors combines analytical derivations with simulation-based data extraction. The procedure was implemented in MATLAB and PLECS, where parametric sweeps of the input voltage V_{in} and the sharing coefficient k were performed. At each operating point, the instantaneous capacitor charge waveforms $Q_{C_{P|N}}(t)$, $Q_{C_{DC}}(t)$ and their corresponding RMS currents were extracted. Post-processing in MATLAB computed the peak-to-peak charge ripple. This workflow allowed the construction of capacitor stress maps such as those reported in Fig. 4.15, where the ripple charge of $Q_{C_{P|N}}$ and $Q_{C_{DC}}$ versus V_{in} and k is presented. As expected from the previous analytical evaluation, the charge ripple stress across the capacitors is zero at $d = 0.5$. The charge ripple map is not symmetrical because of the effective power profile. As a consequence, in order to achieve a maximum power of 75 kW, a current derating is performed for $d > 0.5$.

The minimum capacitances were derived by imposing maximum voltage ripple constraints on both the half and full DC-link voltages:

$$\Delta v_{DC_{P|N}} = 0.9\% \cdot \frac{v_{DC}}{2}, \quad \Delta v_{DC} = 0.3\% \cdot v_{DC}.$$

The optimization criterion was the minimization of the total installed capacitive energy, presented in Fig.4.16:

$$E_C = \frac{1}{2} C_P v_{DC_P}^2 + \frac{1}{2} C_N v_{DC_N}^2 + \frac{1}{2} C_{DC} v_{DC}^2. \tag{4.19}$$

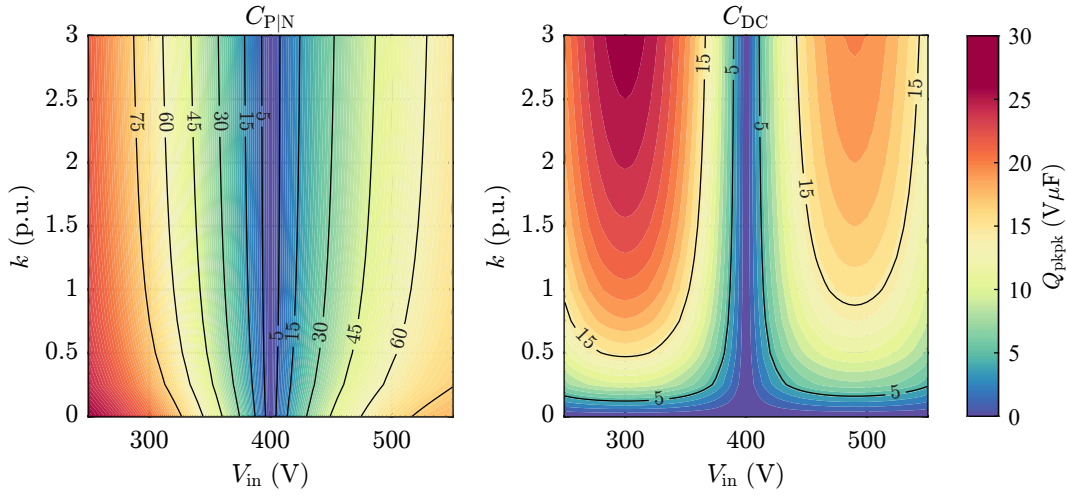


Fig. 4.15 Capacitor charge ripple of $C_{P|N}$ and C_{DC} at different k and V_{in} at $V_{dc} = 800V$

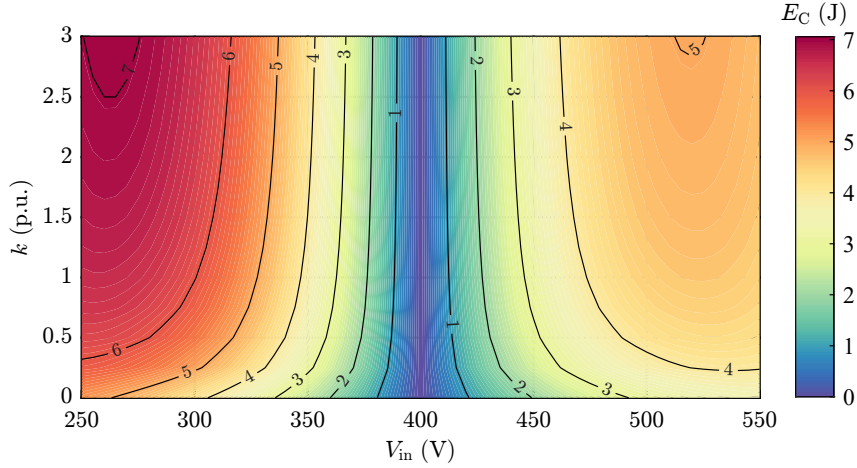


Fig. 4.16 Total capacitor energy storage at different k and V_{in} .

From the results, the optimal sharing coefficient was $k = 0$, leading to a required minimum capacitance of $C_{P|N} \geq 32.1 \mu F$ and $C_{DC} = 0 \mu F$. Fig. 4.17 presents the capacitance maps for both $C_{P|N}$ and C_{DC} based on different k and V_{in} .

For the implementation, PLZT ceramic capacitors were selected due to their high resonant frequency, excellent RMS current capability, high volumetric energy density, and stable performance at elevated temperatures. In particular, the FA10 and FA3 CeraLink[®] series from TDK (500 V rated) were adopted. Table 4.4 summarizes the main electrical parameters of the selected components. To fulfill the capacitance requirement, each $C_{P|N}$ bank consists of three FA10 and one FA3 in parallel, providing a total capacitance of $33 \mu F$.

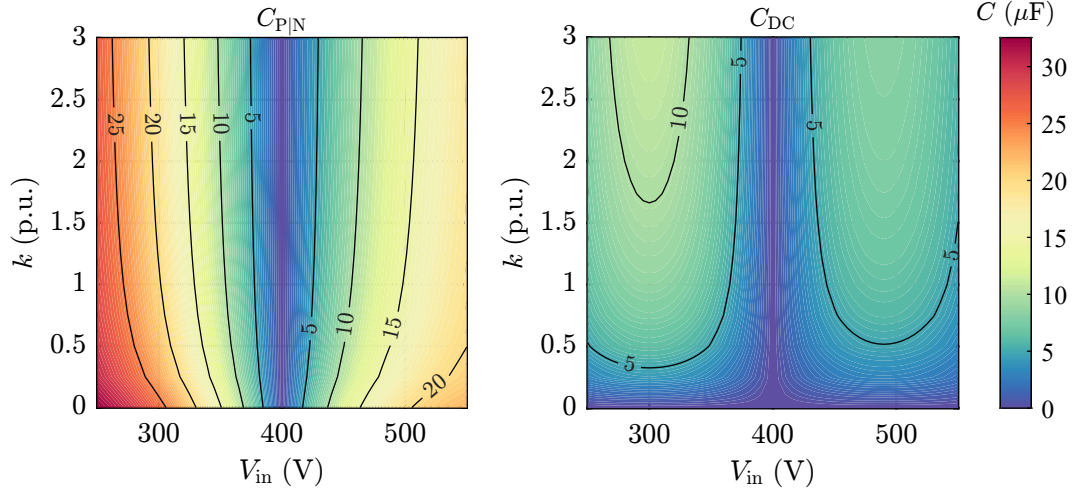


Fig. 4.17 Minimum capacitance for $C_{P/N}$ and C_{DC} at different k and V_{in} .

Finally, capacitor losses were estimated by combining the frequency-dependent equivalent series resistance (ESR) curves (Fig. 4.18a) with the harmonic current spectrum. The capacitor loss model was implemented as:

Table 4.4 Main parameters of the selected DC-link capacitors taken from datasheet.

Capacitor	V_{rated}	C_{nom}	f_{res}	I_{RMS} at 85°C / ESL
FA3 PLZT	500 V	3 μ F	$\simeq 1.7$ MHz	20 A / 3 nH
FA10 PLZT	500 V	10 μ F	$\simeq 1.1$ MHz	47 A / 2 nH

$$P_{loss} = \frac{n_c}{2} \sum_{k=1}^n R_{ESR}(f_k) \left[\frac{\hat{I}_C(f_k, V_{in})}{n_c} \right]^2, \quad (4.20)$$

where n_c is the number of capacitors in parallel. The resulting power losses and corresponding hot-spot temperatures are estimated by (4.21)

$$T_{hs} = T_0 + \frac{R_{th,hs-amb}}{n_p} \cdot P_{loss}, \quad (4.21)$$

The analysis confirmed the feasibility of the proposed capacitor bank in terms of both thermal and electrical constraints.

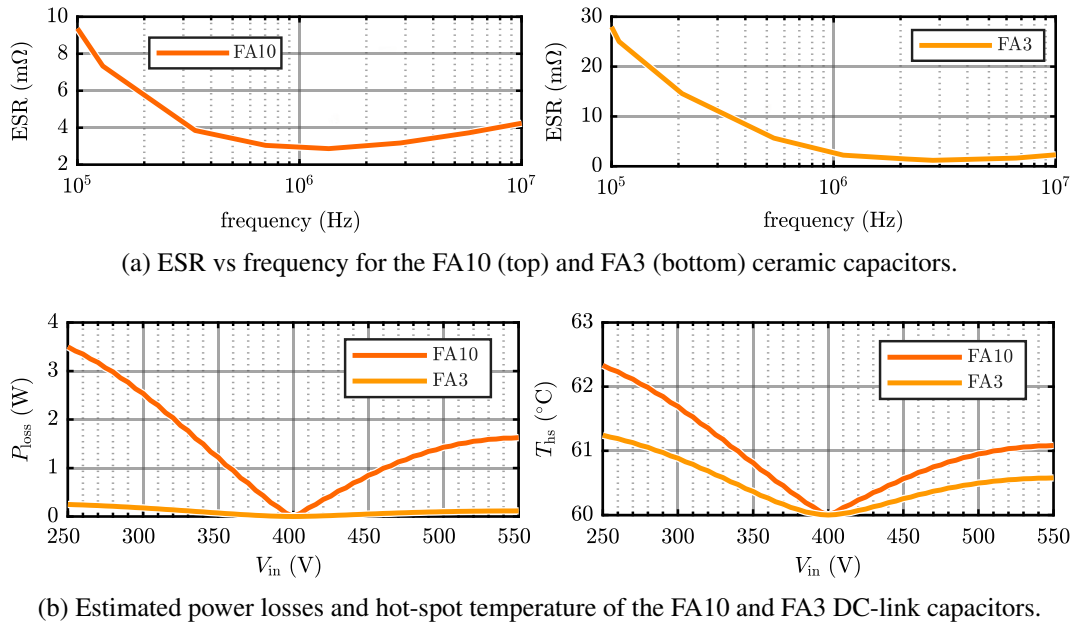


Fig. 4.18 Comparison between the selected ceramic capacitors: (top) ESR vs frequency and (bottom) estimated losses and hot-spot temperature.

4.7 Prototype assembly

To validate the theoretical analysis and the proposed design methodology, a high-power DC/DC converter prototype rated at 75 kW and operating at a switching frequency of 100 kHz was built. The converter's physical implementation, illustrated in Fig. 4.19, adopts a modular architecture that separates the control, the driver, and the power stages. This modular approach not only enhances the system's flexibility, but also allows for straightforward replacement of the control board and simplifies the debugging process. Moreover, isolating the sensitive control circuitry from the high-power switching elements facilitates thermal management and mitigates electromagnetic interference, ensuring robust and reliable operation under demanding conditions. The power stage of the converter integrates high-performance semiconductors and discrete components, which are cooled via a dedicated liquid-cooling system described in Section 4.4. The key power components and measurement devices employed in the prototype are summarized in Table 4.5 and presented in Fig. 4.20.

The overall assembly occupies a compact volume of $19 \text{ cm} \times 18 \text{ cm} \times 15 \text{ cm}$, corresponding to a volumetric power density of approximately 21 kW/l, when in-

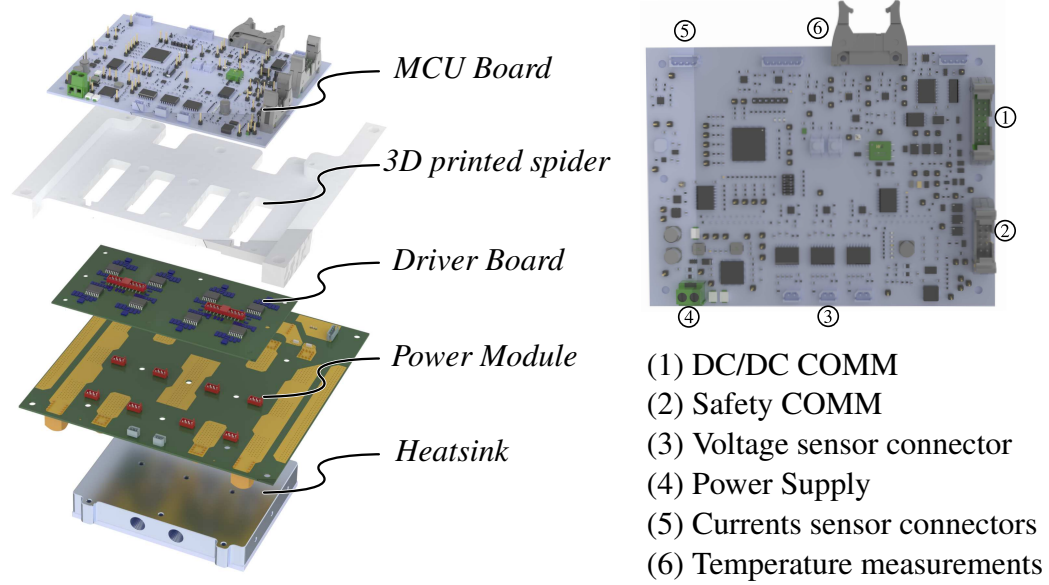


Fig. 4.19 3D render of the power stage, driver board and control/communication board of the converter under study.

Table 4.5 Component ratings and selected devices for the 75 kW prototype DC/DC converter

Components	Required ratings	Selected devices
Main power switches (x8)	400 V, 100 A	VisIC V08TC65S2A 650 V, $R_{on} = 8\text{ m}\Omega$, $I_D = 180\text{ A}$
Local DC-link capacitance	500 V (total $66\text{ }\mu\text{F}$)	B58035U5106M001, ceramic capacitors 500 V, $10\text{ }\mu\text{F}$ Ceralink
Current sensors (x4)	$\pm 200\text{ A}$	ACS772ECB-200B-PFF-T Allegro, accuracy 1%, bandwidth $f_{bw} = 200\text{ kHz}$
Voltage sensors (x3)	0–550 V	AMC3311-Q1, 0 to 2 V input, bandwidth $f_{bw} = 200\text{ kHz}$

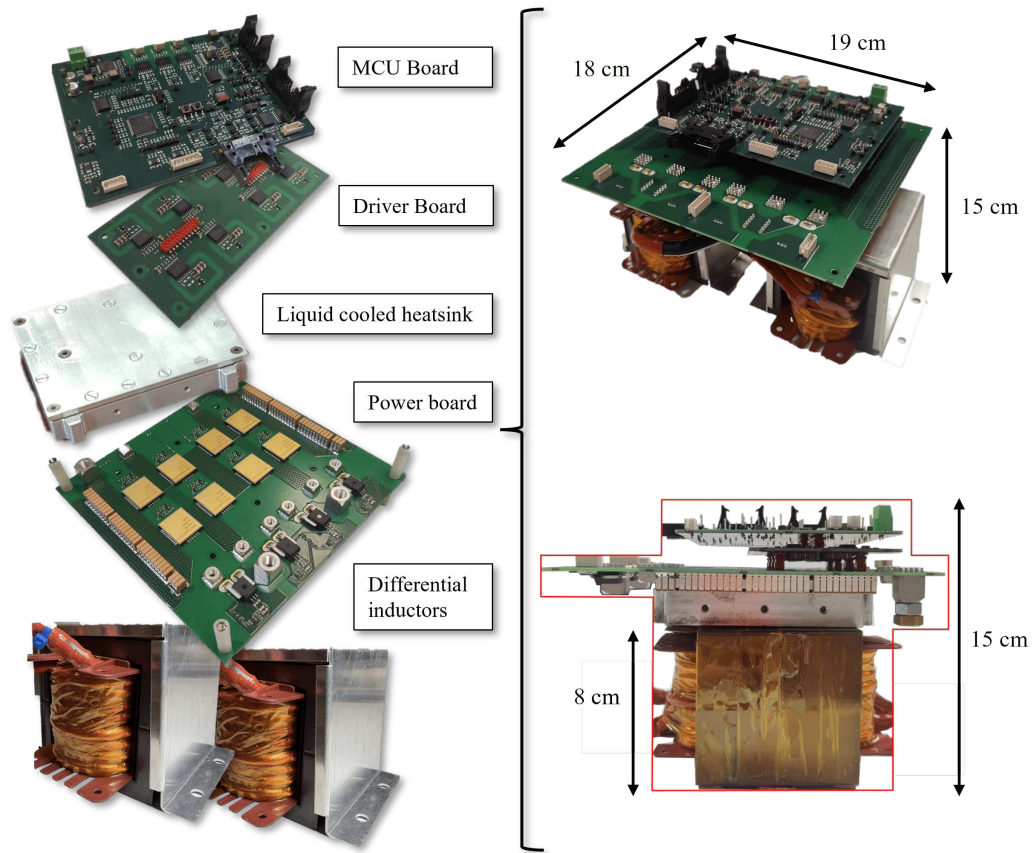


Fig. 4.20 Exploded view of the converter components and dimensions of the assembled converter.

cluding all active devices, control boards, and the heat sink. The gravimetric power density, calculated over the total system mass, is estimated at 15 kW/kg.

Three-quarters of the total mass corresponds to the differential inductors. This emphasizes the significant contribution of magnetic components to the overall weight and suggests that future optimizations in magnetic materials, core design, or winding techniques could substantially improve both volumetric and gravimetric power densities.

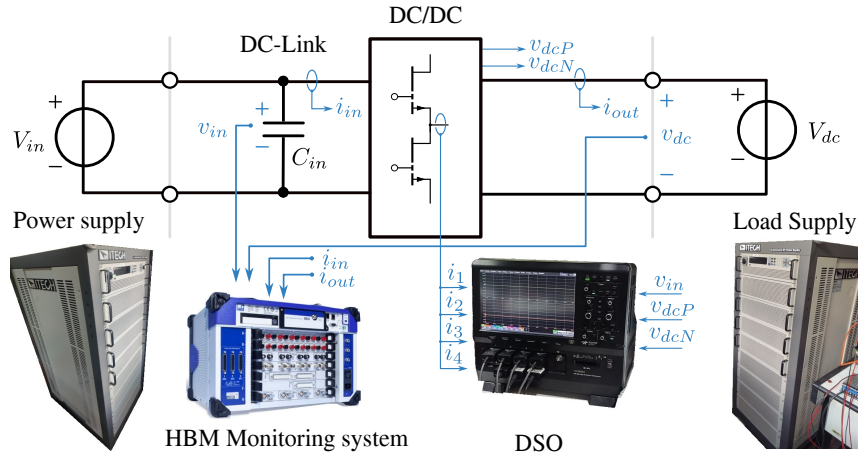


Fig. 4.21 Experimental setup for efficiency and loss characterization.

4.8 Experimental Validation

A comprehensive experimental campaign was carried out to validate the operational performance of the prototype and to verify the accuracy of both the theoretical and simulation models. Fig. 4.22 depicts the laboratory setup, showing the physical layout of the converter and the instrumentation used for measurements. The full test setup, schematically presented in Fig. 4.21, incorporates an HBM monitoring system for precise power and loss measurements and is powered by two ITECH IT6090D programmable power supplies acting as battery and load emulators. This configuration enables controlled variation of input voltage and load current, allowing a thorough mapping of the converter's efficiency characteristics under realistic operating conditions.

Waveform acquisition was performed using a Teledyne LeCroy HDO8038A oscilloscope with eight channels, enabling simultaneous monitoring of multiple signals of interest. Voltage measurements were conducted with three isolated differential voltage probes (HVD3000A), capturing the input voltage (v_{in}) as well as the split DC-link voltages ($v_{dc,P}$ and $v_{dc,N}$). Currents through the four half-bridge legs were measured with Teledyne LeCroy CP150A probes, while the input current (i_{in}) was monitored via a CP500A probe.

The first experimental procedure evaluated the system's response to a load transient under conditions that induce the maximum ripple in the input current i_{in} . The results, presented in Fig. 4.23a, indicate that the control strategy successfully maintains

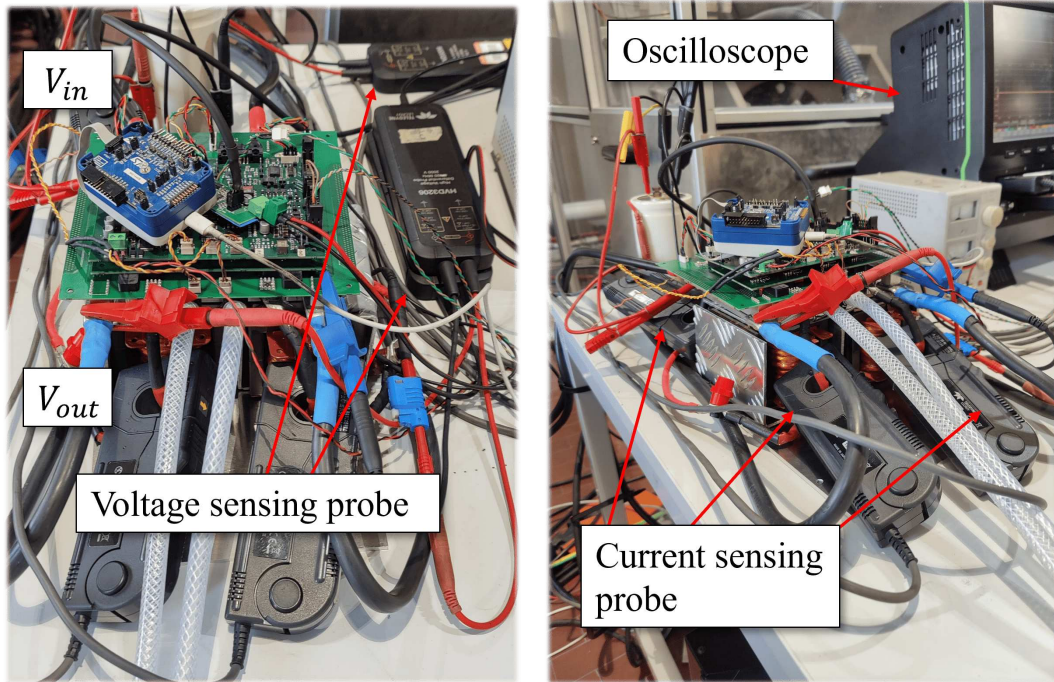


Fig. 4.22 Laboratory setup for experimental testing of the converter.

a balanced differential current across the four converter legs while accurately tracking the target load. Additionally, the split DC-link voltages remain well-balanced throughout the transient, demonstrating the effectiveness of the implemented control algorithm. A detailed comparison between simulation and experimental waveforms at an input voltage of 350 V, output voltage of 800 V, and input current of 100 A is provided in Fig. 4.23b. The experimental data closely follow the simulated waveforms, confirming both the accuracy of the modeling approach and the effectiveness of the control implementation. In particular, the split DC-link voltages $v_{dc,P}$ and $v_{dc,N}$ remain balanced, and the differential currents $i_1 - i_3$ and $i_2 - i_4$ exhibit the expected behavior.

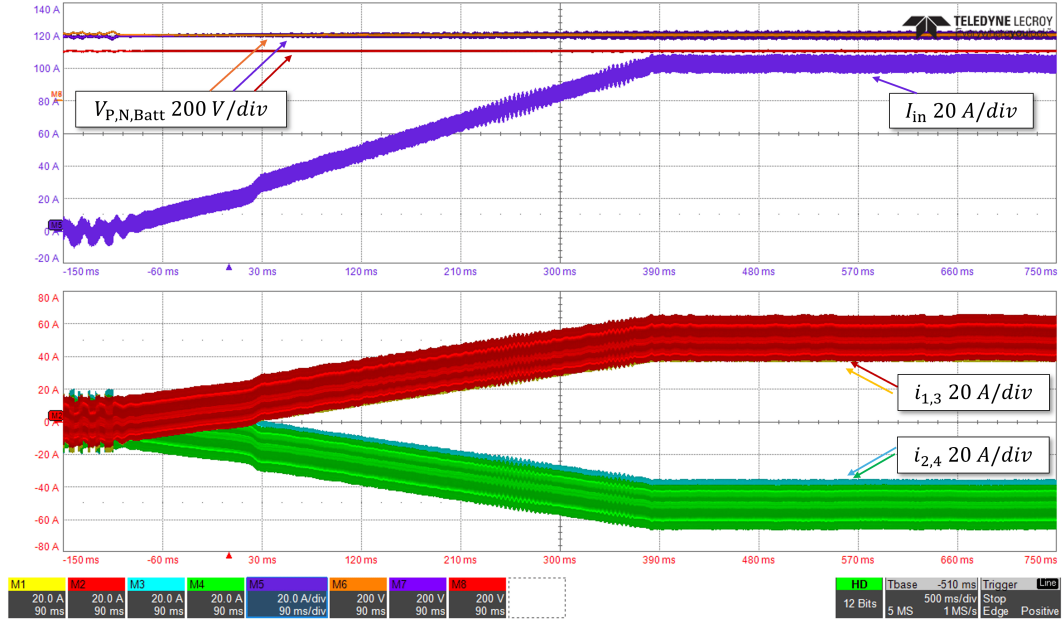
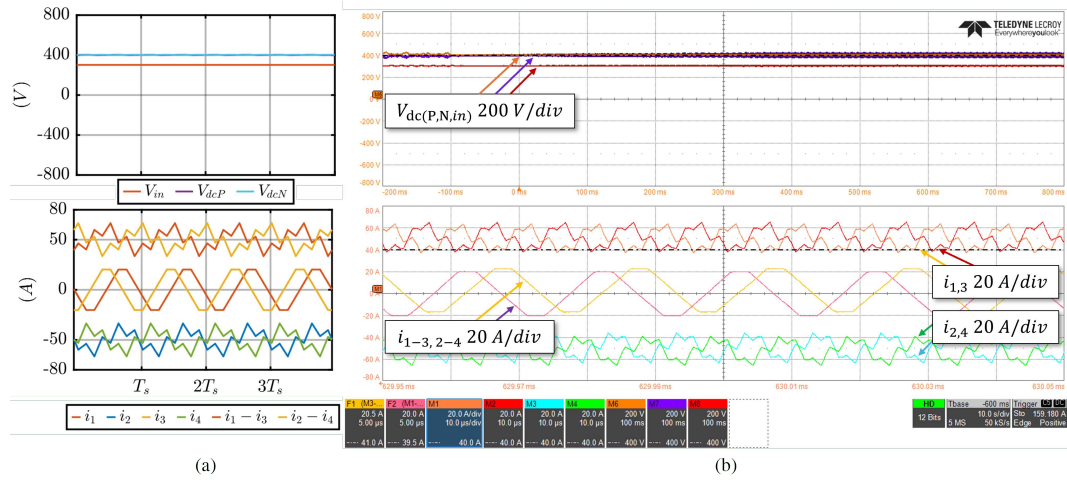
(a) Load transient response at $v_{in} = 350$ V, $v_{dc} = 800$ V, and $i_{in} = 100$ A.(b) Comparison between simulated (a) and experimental (b) waveforms under nominal load conditions: $v_{dc} = 800$ V, $v_{in} = 350$ V, $i_{in} = 100$ A, $f_s = 100$ kHz.Fig. 4.23 Experimental results at $v_{dc} = 800$ V, $v_{in} = 350$ V, and $i_{in} = 100$ A.



Fig. 4.24 Captured waveforms during the converter efficiency mapping. Top plot: input currents for five different power levels. Bottom plot: trigger signal for the data recorder to save data.

Beyond dynamic waveform validation, the experimental campaign also focused on efficiency measurement and loss characterization. Based on the same setup previously presented, a detailed efficiency and power loss estimation mapping is performed. Fig. 4.24 presents the mapping technique involved. For each operating point, the experimental procedure follows a structured and repeatable sequence.

First, the reference values for the current are generated and transmitted to the system. After setting these references, a waiting time is introduced in order to allow the system to reach steady-state conditions.

Once steady-state operation is ensured, data acquisition is triggered using the HBM measurement system, enabling the collection of representative data for the selected operating point. After the acquisition phase, a cool-down interval is applied before proceeding to the next operating condition.

This systematic procedure ensures consistent thermal conditions across all measurements, thereby improving the reliability and repeatability of the resulting operating map. Based on this subsequent load steps, a complete efficiency mapping of the converter is collected, as presented later. For completeness, two detailed oscilloscope acquisitions at the maximum load condition are shown in Fig.4.25 and Fig.4.26.

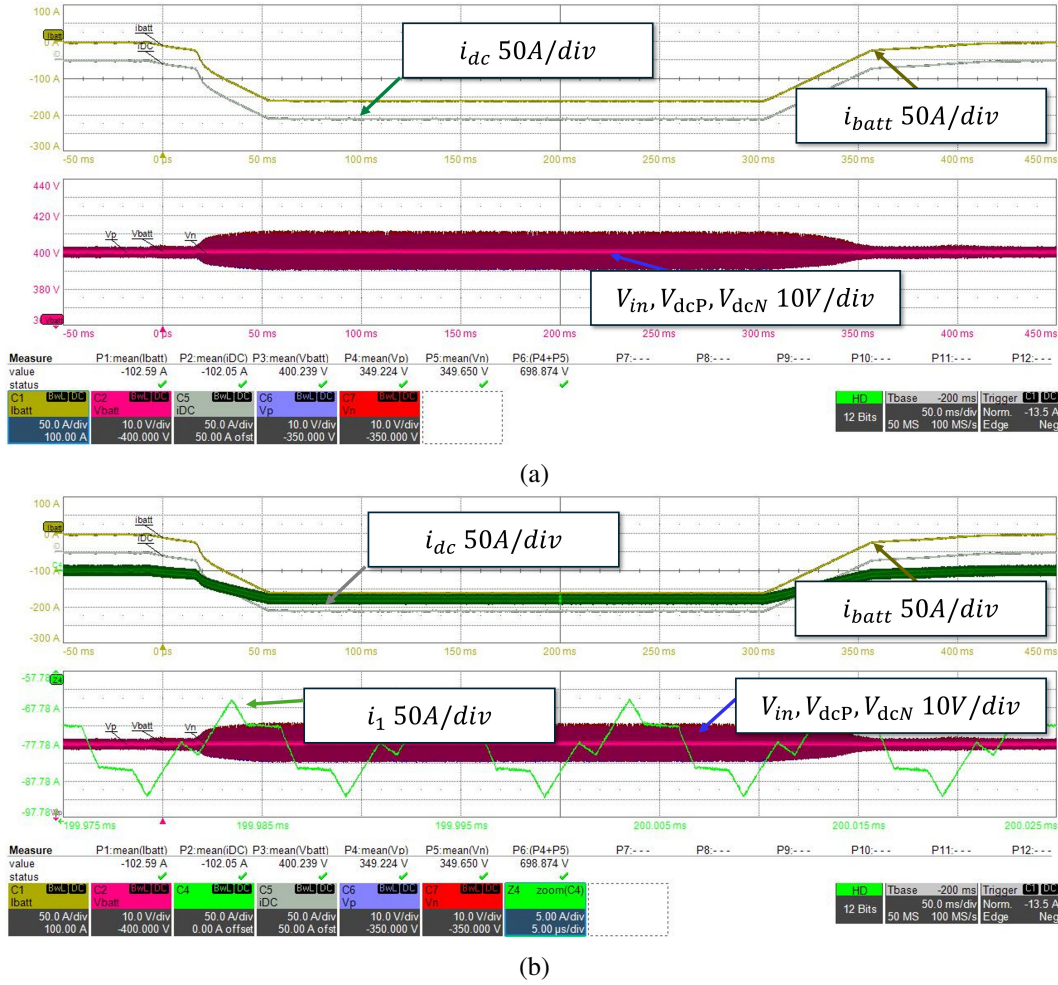


Fig. 4.25 Experimental waveforms at full load: $V_{in} = 400$ V, $V_{dc} = 700$ V, $i_{in} = 180$ A.

The acquisitions highlight the converter behavior at full load for $V_{dc} = 700$ V and $V_{dc} = 800$ V Bus, respectively. The observed current step shows stable operation at rated conditions, while the split DC-link voltages remain properly balanced throughout the transient. These results are particularly relevant because they confirm that the converter preserves correct voltage sharing and controlled dynamic behavior also in the high-power region used for the efficiency characterization.

The experimental campaign was finally extended to a complete steady-state mapping of the converter over the considered operating range. In particular, the measured results were compared with the corresponding simulation outcomes in order to assess the accuracy of the developed loss and performance model under different voltage and power conditions.

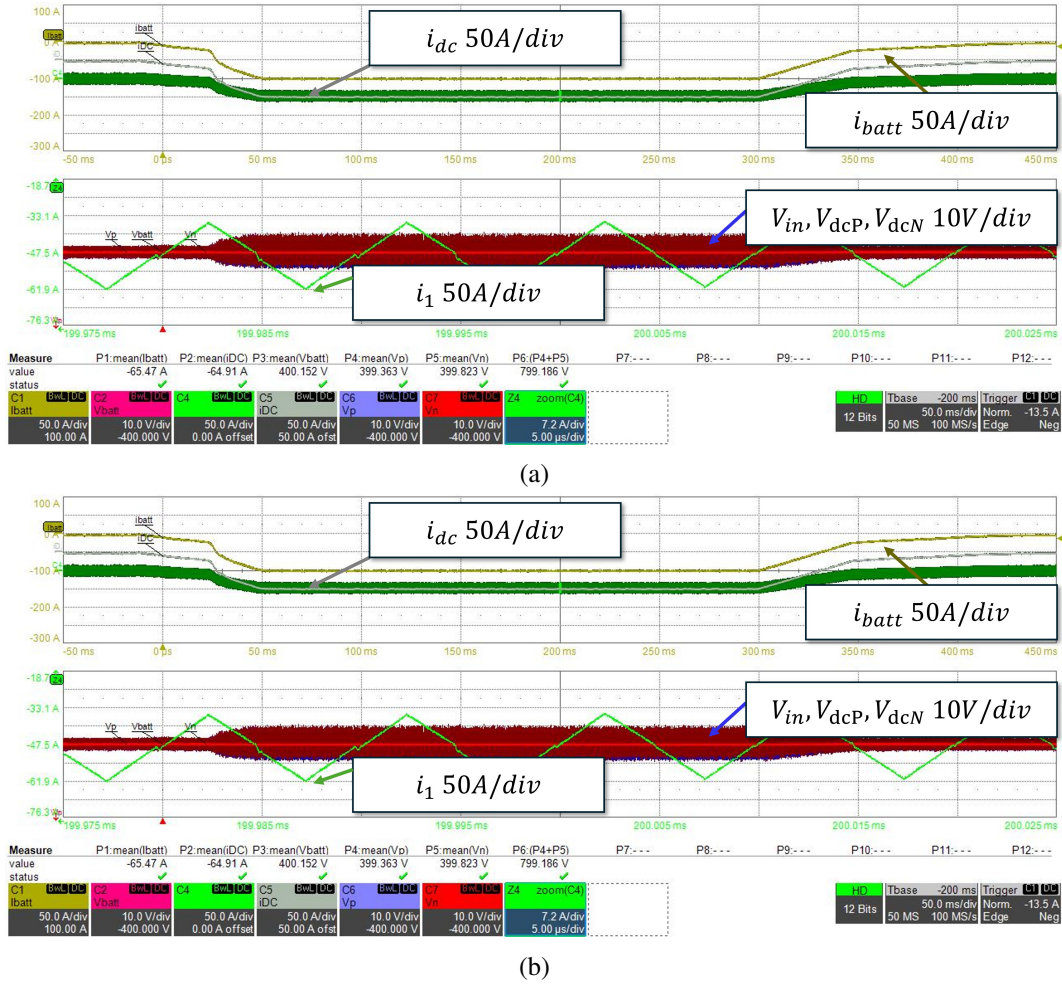


Fig. 4.26 Experimental waveforms at full load: $V_{in} = 400$ V, $V_{dc} = 800$ V, $i_{in} = 180$ A.

Figures 4.27, 4.28, and 4.29 summarize the comparison between experimental measurements (left column) and simulation results (right column) for three different DC-link voltage levels. More specifically, Fig. 4.27 reports the efficiency maps, Fig. 4.28 shows the corresponding input power maps, and Fig. 4.29 presents the total converter loss maps. In all cases, the star symbol highlights the target operating point at 75 kW, which represents the nominal design objective of the prototype.

Although 75 kW represents the nominal design target, the experimental operating envelope extends up to approximately 80 kW for selected voltage and current combinations. These operating points demonstrate the prototype's overload capability and are not considered part of its continuous nominal rating.

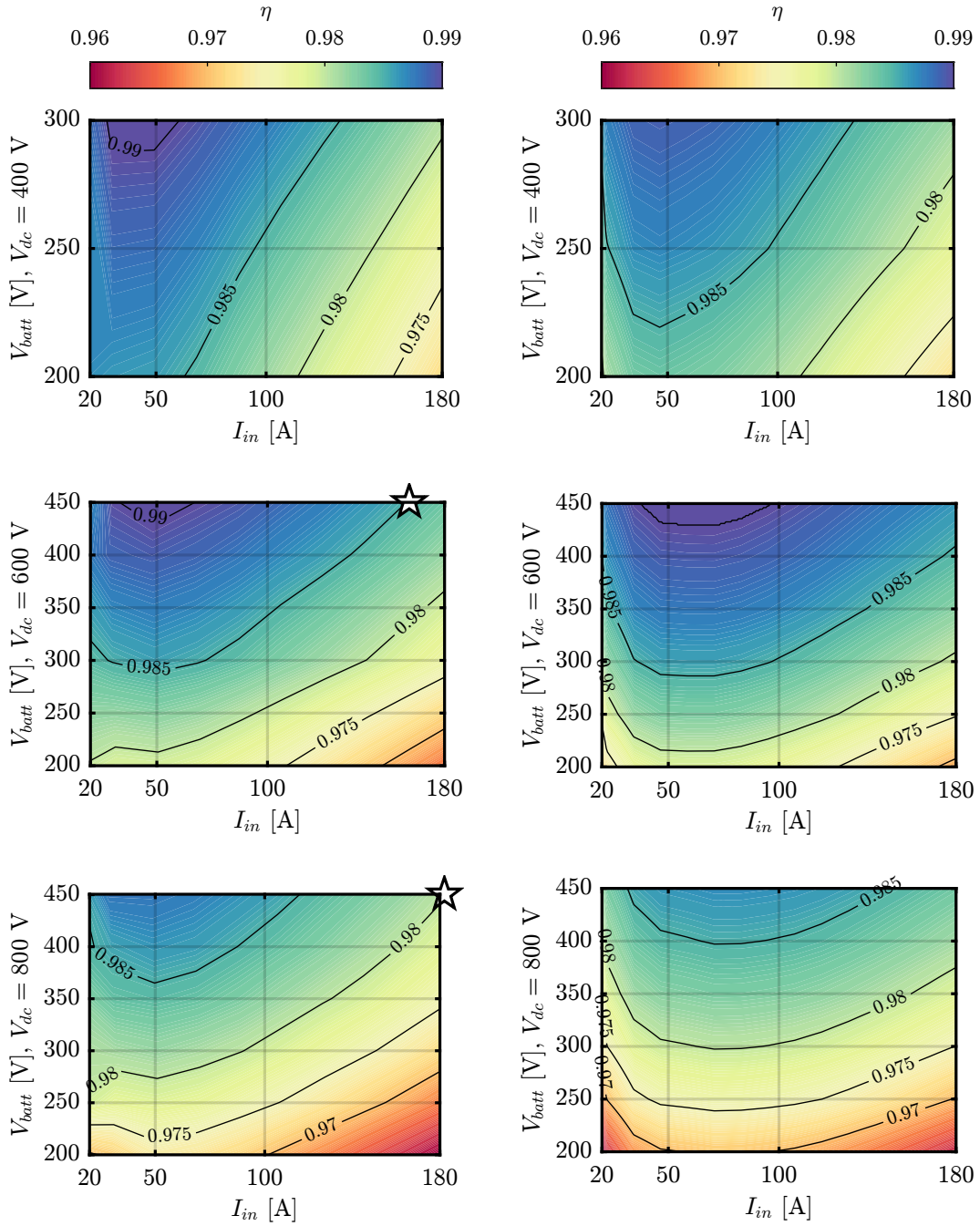


Fig. 4.27 Comparison between experimental (left) and simulated (right) efficiency maps of the converter for different operating voltage conditions. The star symbol marks the target operating point at 75 kW.

The efficiency maps of Fig. 4.27 show that the converter is able to achieve, and in the nominal region also exceed, the target efficiency of 98% at the rated power

of 75 kW. The highest efficiency values are obtained in the central operating region, while a gradual reduction can be observed when moving toward more demanding conversion ratios and current levels. Overall, the experimental results are in good agreement with the simulations, confirming the validity of the adopted design approach and loss estimation procedure.

To complement the efficiency analysis, Fig. 4.28 reports the input power maps, which identify the portions of the operating plane where the required power transfer can actually be sustained. These maps are particularly useful to visualize the effective operating envelope of the converter and to verify that the 75 kW target point is reached under the expected voltage conditions. The comparison with the simulated maps confirms that the model captures the overall power capability of the converter with good accuracy.

Figure 4.29 presents the corresponding total loss maps. As expected, the losses increase with power level and become more significant in the operating regions characterized by larger current stress and higher conversion ratio. The comparison between measured and simulated losses shows a consistent overall trend, although the experimental maps exhibit slightly higher losses than predicted by the model. This discrepancy is reasonably attributed to second-order effects that were only partially included in the simulations, in particular the high-frequency losses of the magnetic components, as well as additional parasitic contributions related to layout, connections, and measurement uncertainty.

Taken together, these maps provide a comprehensive overview of the converter performance. They demonstrate that the proposed prototype not only satisfies the required 75 kW power target, but also maintains high efficiency and acceptable loss levels across a wide operating region, thereby validating both the hardware design and the adopted simulation framework.

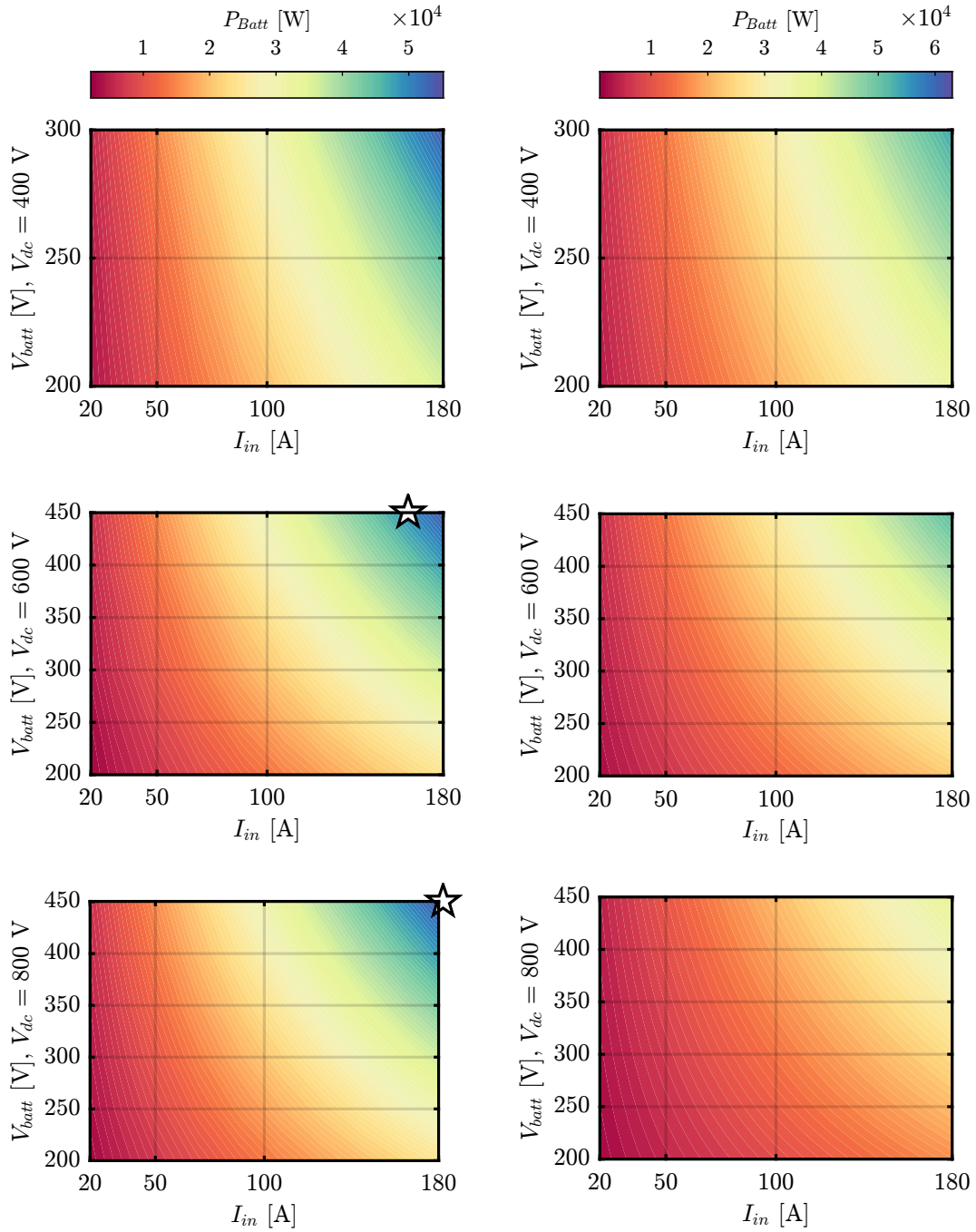


Fig. 4.28 Comparison between experimental (left) and simulated (right) input power maps of the converter for different operating voltage conditions. The star symbol marks the target operating point at 75 kW.

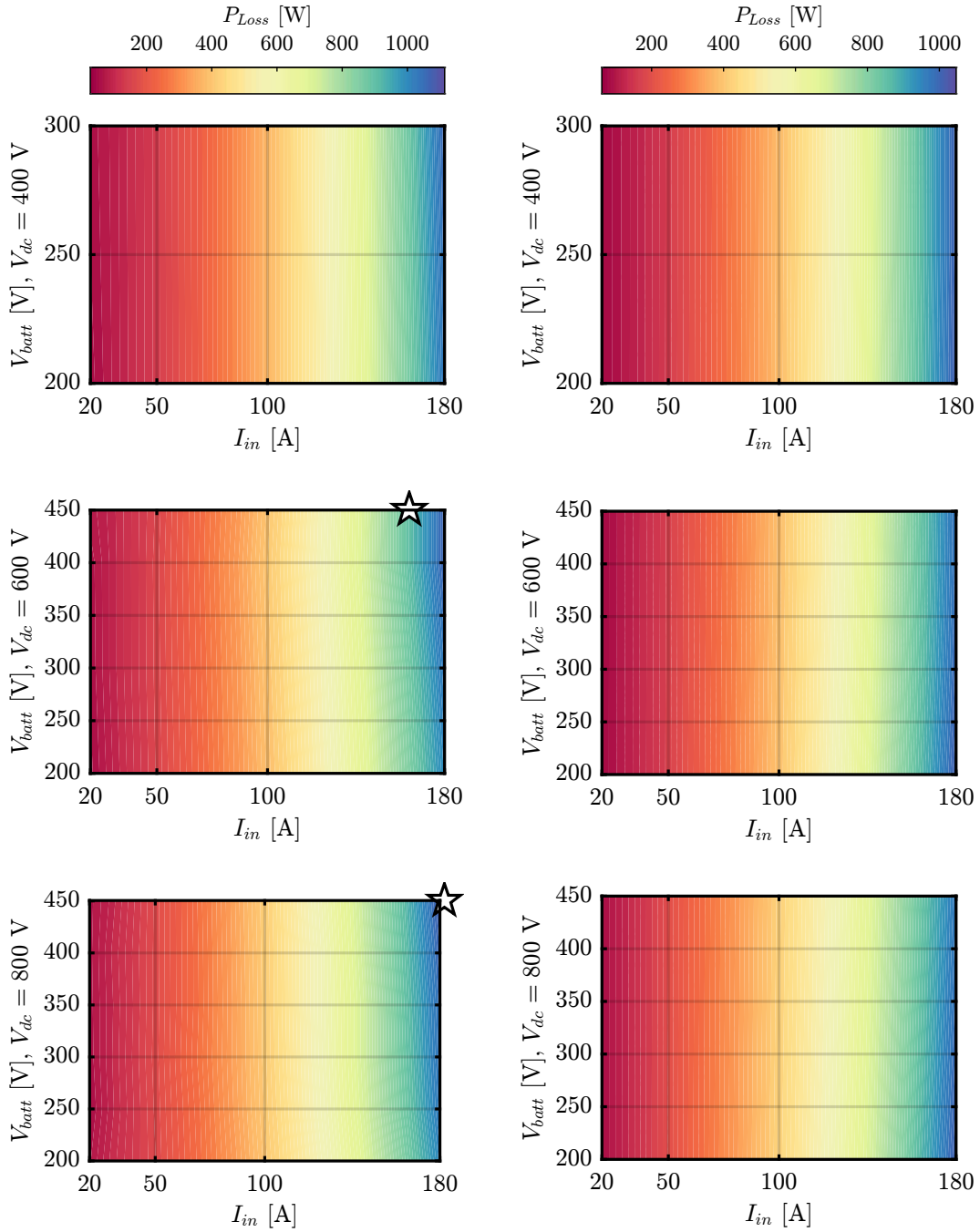


Fig. 4.29 Comparison between experimental (left) and simulated (right) total power loss maps of the converter for different operating voltage conditions. The star symbol marks the target operating point at 75 kW.

Particular attention was given to efficiency performance at partial load, reflecting typical operating conditions in traction applications. Fig. 4.30 presents both the

experimentally measured efficiency (dots) and the computed efficiency (continuous line) as functions of power and input voltage. The computed efficiency accounts for losses in all main components based on the loss model introduced in Section 4.3. The results demonstrate a measured peak efficiency of approximately 98.5%, in agreement with the design specifications reported in Table 4.1. Since the efficiency is evaluated close to unity, the absolute value is inherently sensitive to measurement-system accuracy, residual offsets, thermal variations, and parasitic contact and cable resistances. A complete quantitative uncertainty budget was not available for this experimental campaign; therefore, the reported peak value should be interpreted as the measured estimate under the adopted test conditions. Small differences between nearby operating points or between measured and computed values should consequently not be regarded as significant. The structured acquisition sequence and the cool-down interval between consecutive operating points were adopted to improve measurement repeatability and limit thermal drift. Overall, the experimental

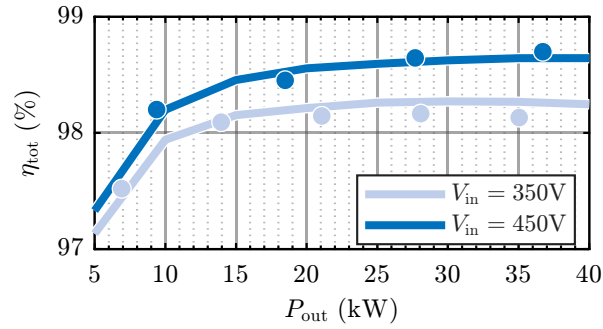


Fig. 4.30 Measured (dots) versus computed (continuous line) converter efficiency at partial load across different input voltages.

results validate the proposed design and control methodology, demonstrating both the high performance and reliability of the 75 kW DC/DC converter prototype under a range of operating conditions. The consistency between simulation and experimental data confirms the robustness of the modeling approach and provides a solid foundation for further optimization and scaling of the system.

4.9 Summary

This chapter presented the complete design and experimental validation of a 75 kW multilevel interleaved GaN boost converter for fuel cell electric vehicles. The prototype exceeded 98% efficiency across the operating range, validating the selected architecture. Key achievements include:

- Coupled inductor design achieving $L_{dm} = 72.3 \mu\text{H}$ and $L_{cm} = 6.24 \mu\text{H}$.
- Optimized DC-link with 33 μF per half-bank using Ceralink capacitors.
- Power density of 21 kW/l and 15 kW/kg.

Experimental results confirmed excellent agreement with simulations and demonstrated robust performance during transients, successfully meeting all design specifications for the automotive target application.

DC/AC Converter

Chapter 5

DC/AC Converter - *Sizing and Design*

5.1 Introduction

The traction inverter is one of the most critical parts in electric vehicles, acting as the interface between the high-voltage DC bus and the AC traction motor. Its design has a direct impact on driving performance, efficiency, thermal behavior, and overall reliability. At the same time, automotive inverters must meet significant constraints in terms of size, weight, cost, and safety, making their design particularly challenging.

Table 5.2 provides an overview of inverters used in several production vehicles over the past decade. Until around 2016, most inverters relied on silicon IGBT technology and were implemented either as discrete devices or as integrated modules. These solutions were robust and cost-effective, but their switching frequency and efficiency were limited. The adoption of wide-bandgap semiconductors such as silicon carbide MOSFETs brought significant advancements. As shown in Table 5.2, vehicles such as the Tesla Model 3, BYD Han, and Lucid Air have introduced SiC-based inverters into production. Compared to traditional IGBT-based designs, SiC modules allow higher switching frequencies and lower conduction and switching losses, significantly improving thermal performance. This has enabled more compact inverter designs capable of higher efficiency and power density.

In this context, the present chapter focuses on the design and analysis of a 150 kW SiC-based DC/AC converter for automotive fuel cell traction applications. The target specifications, summarized in Table 5.2, include an input voltage range of 100–

800 V, an RMS output current of 150 A, and an efficiency above 98% at rated power. Achieving a volumetric power density greater than 40 kW/l is also a primary design objective. The chapter is organized as follows. First, a comparison of available SiC power modules is presented, considering their electrical, thermal, and packaging characteristics. Detailed simulations are carried out to estimate conduction and switching losses and the thermal behavior under different operating conditions. Next, the mechanical and electrical integration of the inverter is discussed, highlighting the three-layer stacked architecture that separates the power stage, gate driver circuits, and control/communication board. The sizing of the DC-link capacitor is also addressed, using analytical calculations and simulation sweeps to ensure proper voltage ripple and current handling. Finally, the assembly of the prototype is shown, providing a foundation for the experimental testing presented in Chapter 6.

Table 5.1 Electric vehicle inverters, topologies and semiconductor technologies.

Tech	Vehicle	Year	Inverter manufacturer	Topology	Modules / devices
Si IGBT	Nissan Leaf	2012	Nissan	2s-1p	3
	Renault Zoe	2013	Continental/Infineon	2s-1p	3
	Mercedes Benz S550	2014	Hitachi	2s-1p	3
	Honda Accord	2014	Fuji Electric	2s-1p	1
	Tesla Roadster	2014	Infineon	TO-247 discrete	54
	Tesla Model S	2015	Infineon	TO-247 discrete	36
	Audi C-Tron PHEV	2015	Bosch	6s-1p	1
	BMW i3	2016	Infineon	6s-1p	1
	Cadillac CT6	2016	Hitachi	2s-1p	3
	Chevrolet Volt	2016	Delphi	1s-1p	12
	Tesla Model X	2016	Infineon	2s-1p	3
	Toyota Prius	2016	Denso/Toyota	2s-1p	3
	Volkswagen ID.3	2018	Infineon	6s-1p	1
	Audi e-tron BEV	2019	Hitachi	6s-1p	1
SiC MOSFET	Tesla Model 3	2018	STMicroelectronics	1s-1p	3
	BYD Han	2020	BYD Semiconductor	6s-1p	1
	Lucid Air	2021	Lucid	6s-1p	1

5.1.1 Specifications and performance requirements

Based on the technology trends and the effectiveness of the benefits of the use of WBG devices, the proposed 150 kW DC/AC converter is characterized by a SiC power module with two boards: one for the driving stage and one for the control stage, located on top of the power module. The required specifications of the considered DC/AC converter are outlined in Table 5.2. In particular, it is assumed that the converter's nominal rated power is achieved at the maximum accepted V_{bus} (i.e., 800 V). Furthermore, a nominal efficiency of $\geq 98\%$ is targeted.

Table 5.2 Specifications and goal performance of the designated converter.

Parameter	Description	Value
V_{bus}	Input Voltage (V)	100 – 800 V
I_{out}	Output Current (A_{RMS})	150 A
P_n	Rated power (kVA) @ 800V, 150A _{RMS}	150
f_{sw}	Switching frequency (kHz)	20 kHz
η	Target efficiency @ P_n	$> 98\%$
Power density	(kW/l) @ P_n	> 40

5.2 Power module selection

For the design of the DC/AC converter, a modular three-layer stacked board has been chosen. Instead of using discrete devices, power modules have been preferred, based also on the automotive market trend.

5.2.1 Module Comparison

Six modules from leading manufacturers were selected for evaluation:

- NVVR26A120M1WST/S - Onsemi;
- EAB450M12XM3 - Wolfspeed;
- ADP360120W3 - STMicroelectronics (direct-cooled);

- MSCSM120AM08T3AG - Microchip;
- FS05MR12A6MA1B - Infineon;
- FS03MR12A6MA1B - Infineon.

Key performance characteristics of these modules, referenced at an ambient temperature of 25°C, should meet the requirements presented in Table 5.3, with best-in-class metrics highlighted in bold. Key observations include the ST module exhibiting the lowest on-state resistance ($R_{DS,on}$) and body-diode threshold voltage (v_{th}), the Microchip module achieving the lowest switching losses, and the Onsemi module featuring the lowest body-diode resistance and junction-to-case thermal resistance ($R_{th,j-c}$), suggesting superior cooling potential.

	OnSemi	Wolfspeed	Microchip
Topology	Half-bridge	Half-bridge	Half-bridge
$V_{ds,nom}$	1200V	1200V	1200V
$I_{dc,nom}$	400A	450A	337A
$R_{ds,on}$	2.6 mΩ	2.6 mΩ	6.3 mΩ
$T_{j,max}$ (cont.)	175°C	175°C	175°C
E_{off} (800V,200A)	≈ 6 mJ	≈ 6 mJ	≈ 2.6 mJ
E_{on} (800V,200A)	≈ 14 mJ	≈ 8 mJ	≈ 5 mJ
v_{th} (rev. cond.)	≈ 3 V	≈ 3.5 V	≈ 3.2 V
R_{on} (rev. cond.)	≈ 2.5 mΩ	≈ 2.7 mΩ	≈ 3.3 mΩ
$R_{th,j-c}$	0.025 °C/W	0.11 °C/W	0.1 °C/W

(a) OnSemi, Wolfspeed, Microchip

	ST	Infineon FS05	Infineon FS03
Topology	3-ph Inverter	3-ph Inverter	3-ph Inverter
$V_{ds,nom}$	1200V	1200V	1200V
$I_{dc,nom}$	379A	200A	400A
$R_{ds,on}$	2.55 mΩ	5.5 mΩ	2.75 mΩ
$T_{j,max}$ (cont.)	175°C	150°C	150°C
E_{off} (800V,200A)	≈ 8 mJ	≈ 4.3 mJ (600V)	≈ 17.6 mJ (600V,400A)
E_{on} (800V,200A)	≈ 13 mJ	≈ 6.0 mJ (600V)	≈ 19.5 mJ (600V,400A)
v_{th} (rev. cond.)	≈ 2.5 V	3.25–4.5 V	3.25–5.55 V
R_{on} (rev. cond.)	≈ 5 mΩ	n.a.	n.a.
$R_{th,j-c}$	0.129 °C/W (j-f)	0.15–0.18 °C/W (j-f)	0.10–0.108 °C/W (j-f)

(b) ST and Infineon FS05/FS03

Table 5.3 Performance overview of the evaluated SiC power modules.

Based on a wide range of power modules, an analysis of the three-phase inverter's performance requires a junction-to-fluid/ambient thermal model. While the ST module's datasheet provides detailed thermal information for its direct-cooled design, only the junction-to-case/junction-to-fluid thermal impedance is available for the other modules. Therefore, additional thermal parameters must be estimated based on module exchange surfaces, considering TIM and heatsink thermal resistance, as illustrated in Fig. 5.1. To simplify the calculations, it is reasonable to consider a unique inverter equivalent surface equal to 6000 mm^2 , which corresponds to a small overestimation of the thermal resistances (worst-case condition). By considering a thermal grease with a thermal conductivity λ of $4 \text{ W/(m}\cdot\text{K)}$ and a thickness x of $100 \text{ }\mu\text{m}$, the case-to-heatsink thermal resistance $R_{th,c-h}$ can be computed as in (5.1).

For a liquid-cooled heat sink, the heatsink-to-fluid thermal resistance $R_{th,h-f}$ depends on many factors, such as the exchange surface, the flow rate, the technology, etc. It is reasonable to assume $R_{th,h-f} = 0.03^\circ\text{C/W}$, which is the same for all half-bridge modules.

$$R_{th,c-h} = \frac{x}{\lambda \cdot S_{exc,inv}} \simeq 0.004^\circ\text{C/W} \quad (5.1)$$

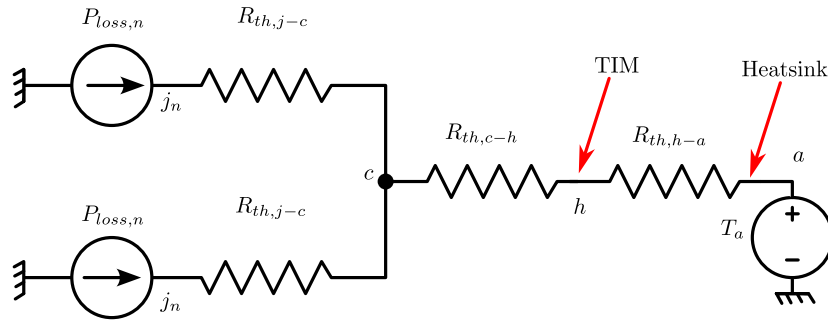


Fig. 5.1 Steady-state thermal model used for the SiC module performance comparison.

5.2.2 Simulation Results

The module comparison was simulated using PLECS, incorporating temperature-dependent loss models based on datasheet curves, linearly scaled for operating voltage and current. The simulation included continuous operation mode (steady-state), synchronous rectification, and a dead time of 500 ns.

Figs. 5.2 present the conduction losses, switching losses, and total average power losses, as well as the estimated junction temperature reached across the switching-frequency range studied. Consistent with Table 5.3, the ST module demonstrates the best conduction performance, extremely close to the Infineon 06, while the Microchip module excels in switching performance. Fig. 5.2 confirms the superior junction-temperature performance of the Infineon 06 power module due to the direct cooling configuration.

The efficiency mapping simulations have been carried out for all the considered SiC modules, by sweeping the modulation index, the RMS output current (from 60 up to the nominal $150 A_{rms}$), and the power factor in the range $\cos \phi = 0.7$ to 1. The obtained results are reported in Fig. 5.3. Beyond electrical and thermal performance, the module package significantly impacts the inverter's mechanical layout, manufacturability, and parasitic behavior. An ideal package facilitates easy mounting (for both debugging and production) and minimizes parasitic elements to limit voltage overshoot and resonance during commutation. Fig. 5.4 shows the packages of the evaluated modules. The ST, Infineon and Onsemi modules feature superior mechanical layouts, with clear separation between power and signal terminals. The Wolfspeed module offers easy-to-mount power terminals, but its gate pins are proximate to the power section, complicating busbar design and increasing cost. The Microchip module utilizes an industrial package not optimized for WBG semiconductors (likely exhibiting high stray inductance) and lacks clear automotive qualification, rendering it unsuitable despite its electrical performance.

Based on the comprehensive analysis of electrical performance, thermal behavior, and packaging, the Infineon 05 module (FS05MR12A6MA1B) was selected, prioritizing its robust thermal performance and superior package layout, despite a marginal efficiency disadvantage.

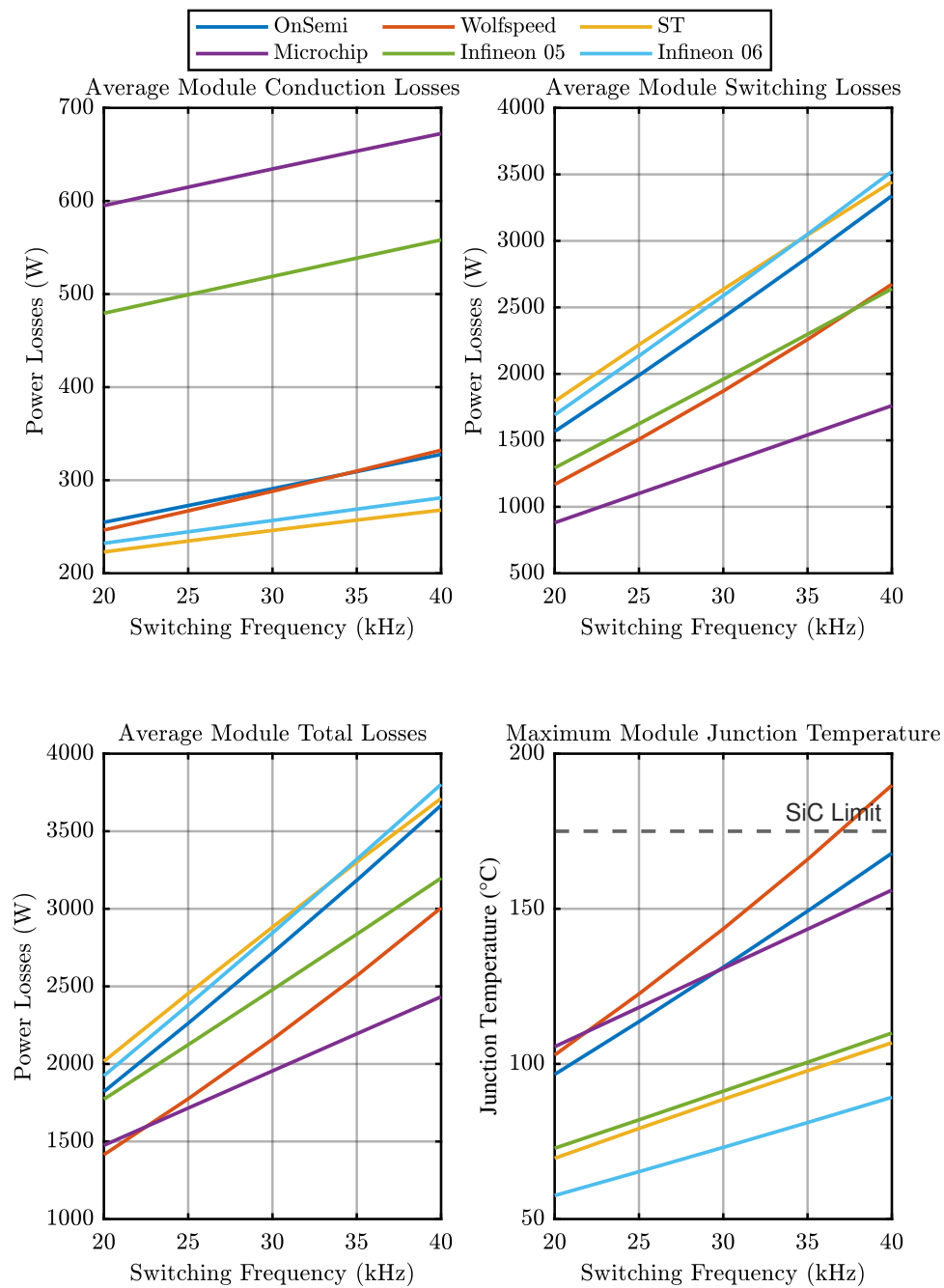


Fig. 5.2 Comparison of conduction losses, switching losses, total losses and Maximum estimated junction temperature.

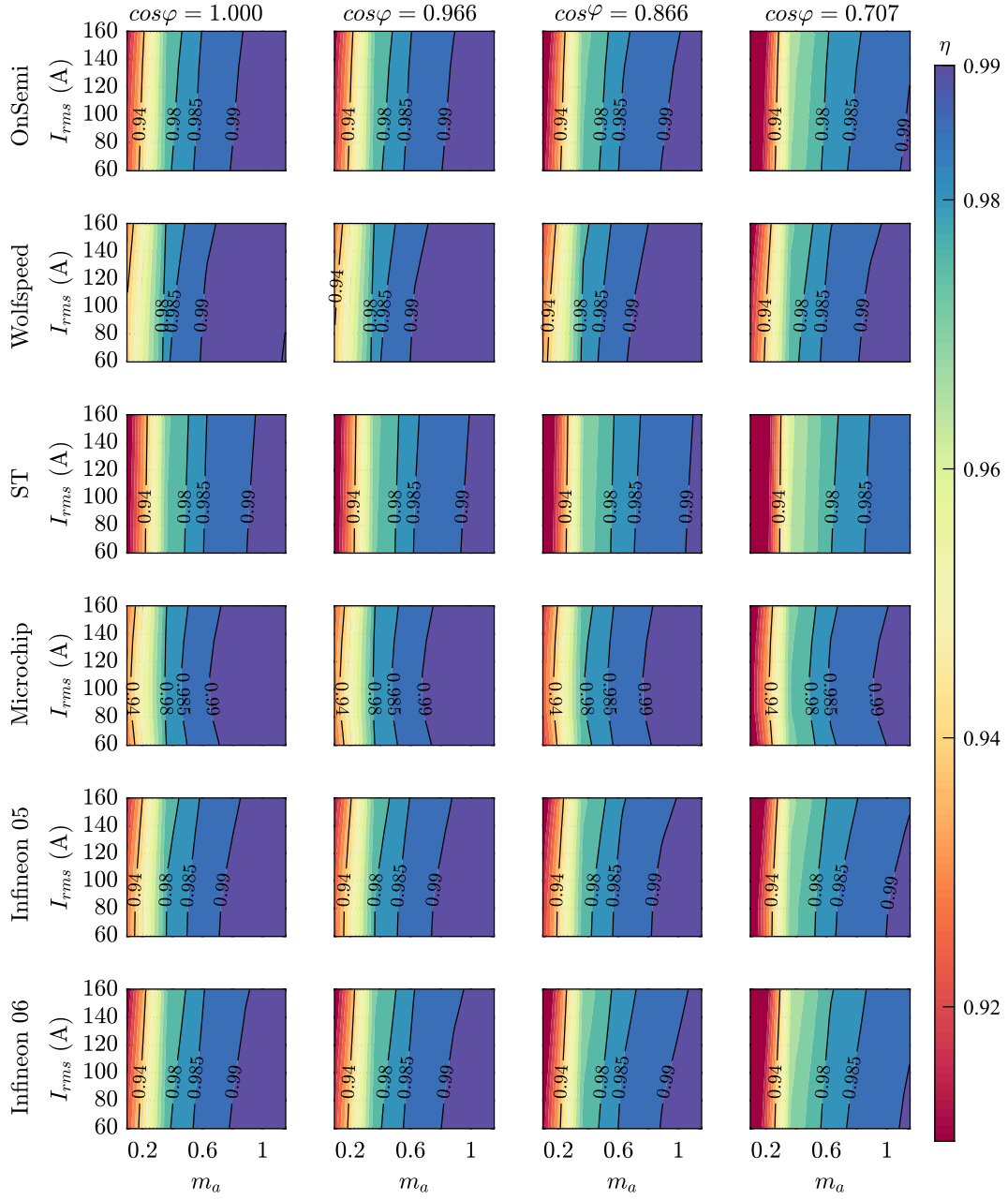


Fig. 5.3 Efficiency comparison of the SiC modules at different modulation indexes, $\cos \varphi$ and currents.

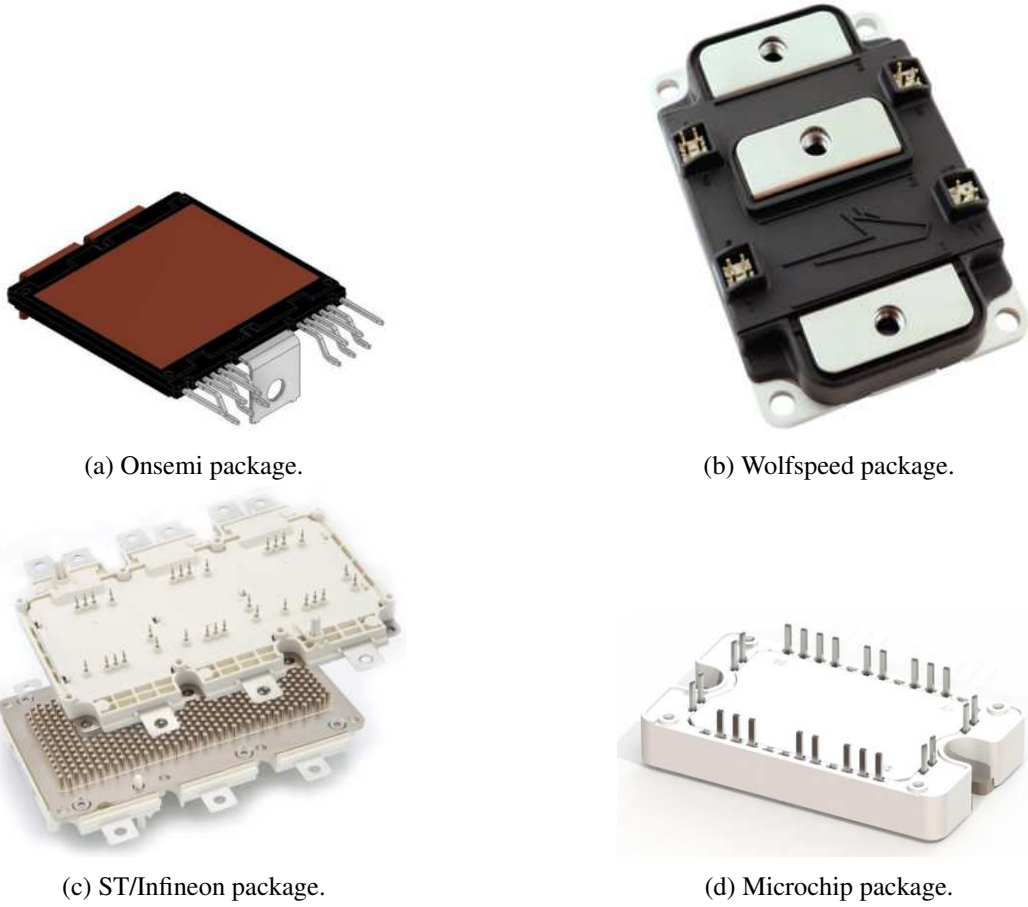


Fig. 5.4 Package comparison of the evaluated SiC power modules.

5.2.3 Converter modeling

The mechanical layout of the prototype converter is presented in Fig. 5.5. A three-layer stacked board arrangement has been adopted to achieve a compact design while keeping the control and driving circuits physically separated from the power stage. The power module is placed at the bottom of the converter, with the dedicated direct cooling system. On top of it, the driver board is mounted, hosting the isolated gate drivers, their auxiliary supplies, and additional voltage measurement circuits for control purposes. The upper board contains the microcontroller and its peripherals and the current sensors, which manage both the overall control of the converter and the communication with the two DC/DC converters. Two dedicated connectors are provided for this internal communication, while an external CAN interface is available for system-level communication.

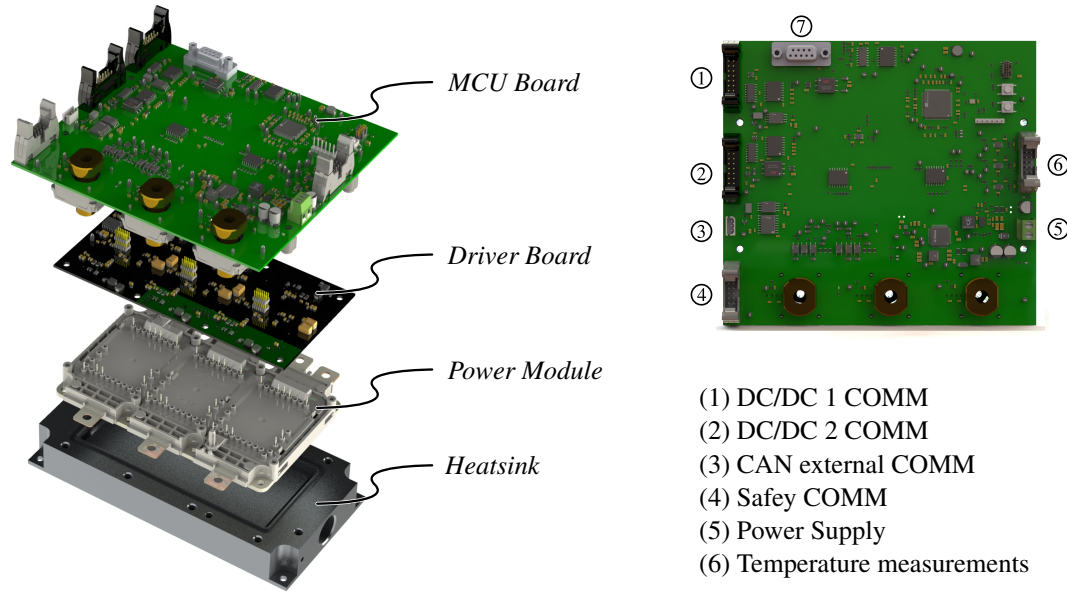


Fig. 5.5 3D render of the power stage, driver board and control/communication board.

5.3 DC-link Capacitor Sizing

The DC-link capacitor is a fundamental component in a voltage source inverter, serving as the primary energy buffer between the DC source and the AC load. Its correct sizing is critical for system performance and reliability. An undersized capacitor leads to excessive voltage ripple on the DC bus, resulting in poor output waveform quality, EMI, and potential over-voltage stress on the semiconductor devices. On the other hand, an oversized capacitor increases the system's cost, volume, and weight without providing a functional benefit. Therefore, the design process aims to determine the minimum capacitance required to maintain the DC-link voltage ripple within acceptable limits while ensuring the capacitor can handle the associated current stress.

The design is governed by the fundamental relationship between charge, current, and capacitance. The instantaneous current $i_c(t)$ through the capacitor is related to the voltage $v_c(t)$ across it by:

$$i_c(t) = C_{dc} \frac{dv_c(t)}{dt}. \quad (5.2)$$

Integrating this equation over a period of time shows that the change in voltage is proportional to the net change of charge in the capacitor. Consequently, the peak-to-

peak voltage ripple ΔV_{pkpk} can be expressed as a function of the peak-to-peak charge ripple ΔQ_{pkpk} demanded by the inverter:

$$\Delta V_{\text{pkpk}} = \frac{\Delta Q_{\text{pkpk}}}{C_{\text{dc}}}. \quad (5.3)$$

Rearranging for the minimum capacitance required to limit the voltage ripple to a specified maximum value $\Delta V_{\text{pkpk,max}}$ (often defined as a percentage of the DC-link voltage V_{dc}) yields the central design equation:

$$C_{\text{min}} = \frac{\Delta Q_{\text{pkpk,max}}}{V_{\text{dc}} \cdot (\Delta V_{\text{pkpk,max}}/100)}. \quad (5.4)$$

A comprehensive analysis is performed to determine the worst-case scenario. This work employs a simulation-based approach, sweeping the modulation index from 0 to the maximum linear modulation limit ($2/\sqrt{3}$) and the phase angle across a meaningful range of power factors ($-60^\circ \leq \phi \leq 60^\circ$). For each operating point (m_a, ϕ) , PLECS simulations are performed to extract the precise capacitor current and charge waveforms.

The results of this sweep are visualized in Figure 5.6, which maps the charge ripple across the entire operating range. Beyond voltage ripple, the RMS current stress $I_{\text{cap,RMS}}$ on the capacitor is a paramount consideration for reliability. This current causes I^2R losses within the capacitor's Equivalent Series Resistance (ESR), leading to internal heating and potential thermal failure. The worst-case RMS current, derived from the same simulation sweep, is presented in a normalized form in Figure 5.7. This value must be compared against the RMS current rating of the selected capacitor to ensure safe thermal operation. Based on $I_{\text{rms}} = 150 \text{ A}$, in the worst-case scenario, $I_{\text{cap,rms}}$ would be equal to $95 A_{\text{rms}}$.

As a consequence of Eq. 5.4, Figure 5.8 provides a direct design tool, illustrating the trade-off between the allowed voltage ripple and the minimum required capacitance.

In order to meet the target specifications for voltage ripple ($\Delta V_{\text{pkpk}} < 20 \text{ V}$), a DC link with an equivalent capacitance greater than $150 \mu\text{F}$ has been selected. Fig. 5.9 shows a 3D rendering of the final DC-link assembly, while Table 5.4 summarizes the main selected components. Two different film capacitor formats were chosen to simplify assembly and ensure sufficient power density on the board. Additional

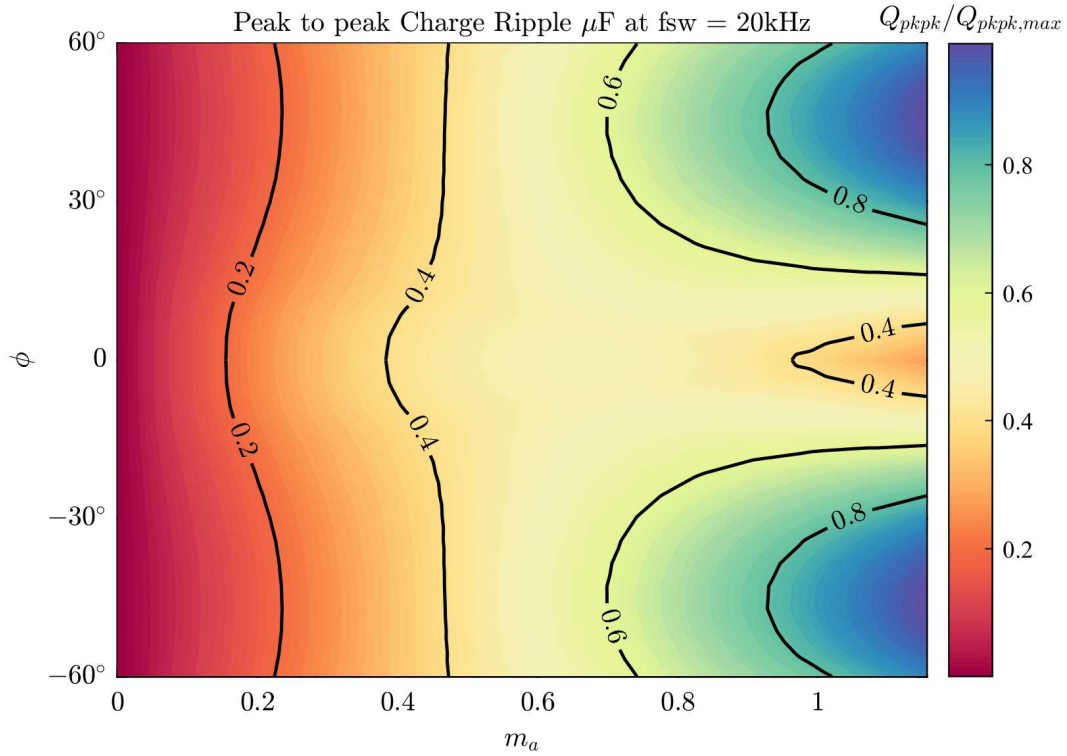


Fig. 5.6 Contour plot of the peak-to-peak charge ripple on the DC-link capacitor as a function of modulation index m_i and load phase angle ϕ . The maximum value $\Delta Q_{pkpk,max}$, used for sizing, is identified from this dataset.

safety capacitors have been included, and a few ceramic capacitors were added to absorb high-frequency current ripple.

Component p.n.	Mfr.	Cap. (μF)	V_{rate} (V)	Type	Qty	A_{rms}
B58035U9754M062	TDK	0.975	900	Ceramic (PLZT)	6	-
C4AQOLW5180M38J	KEMET	18	900	Film	6	17.2
C4AQOBU5100M12J	KEMET	10	900	Film	12	13.8
R413N322050P0K	KEMET	0.22	1200	Film (Safety)	2	-

Table 5.4 List of selected capacitors with manufacturer, capacitance, voltage, current rating, type, and quantity.

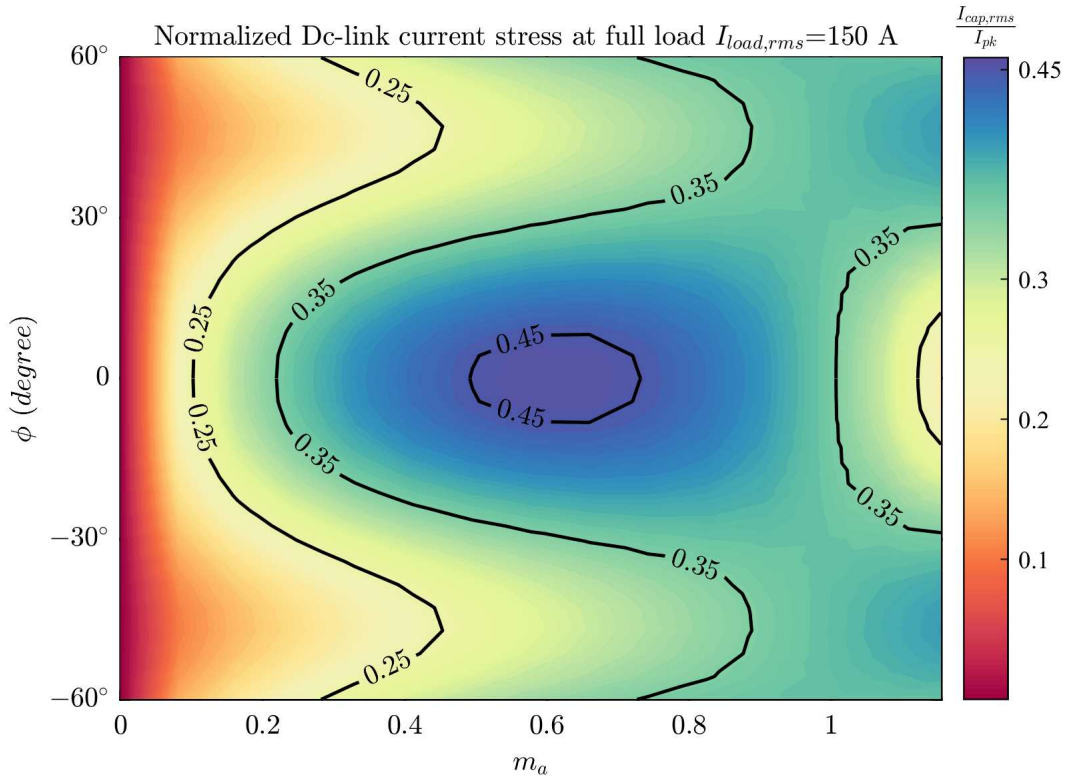


Fig. 5.7 Normalized RMS current stress in the DC-link capacitor.

5.4 Prototyping and Testing

The final assembly of the prototype converter is shown in Fig. 5.10. The complete system integrates the three-layer stacked boards previously described, including the power stage, the gate driver board, and the control/communication board. The DC-link capacitor bank is positioned as close as possible to the power terminals, in order to reduce the current loop area and limit voltage overshoot during fast switching events. Signal and control connectors were routed on the top side, providing straightforward access for both debugging and integration within the test bench. This prototype assembly validated the feasibility of the proposed design and enabled subsequent experimental testing. In order to validate the switching performance of the proposed converter, preliminary tests were carried out on each phase. The tests were performed using a passive inductive load, confirming the capability of the converter to handle up to 150 kVA. Figs. 5.11 and 5.12 report the measured voltage waveforms during the ON and OFF transitions at a peak current of 220 A.

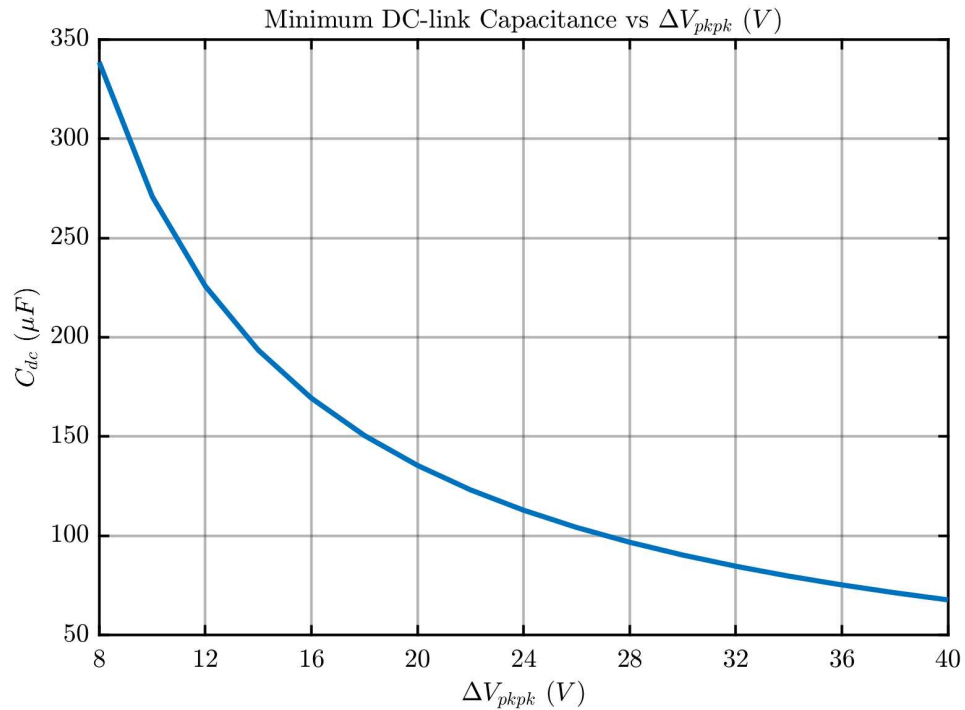


Fig. 5.8 Minimum DC-link capacitance as a function of the allowable peak-to-peak voltage ripple. This curve is derived from the worst-case charge ripple and Eq. 5.4.

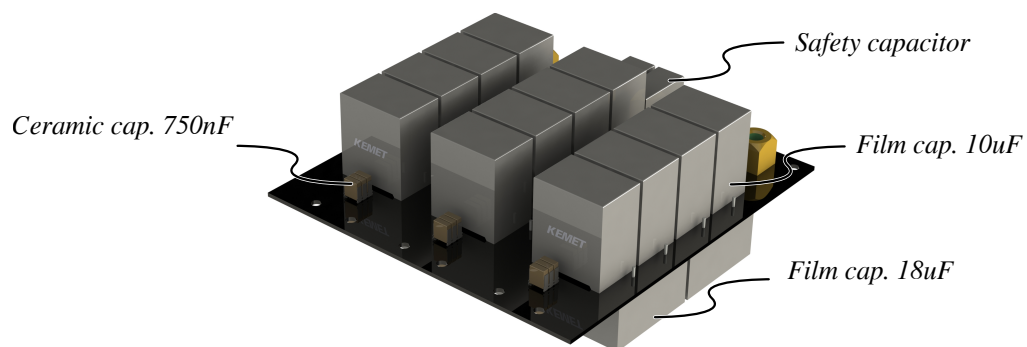


Fig. 5.9 3D render of the designed inverter DC-link.

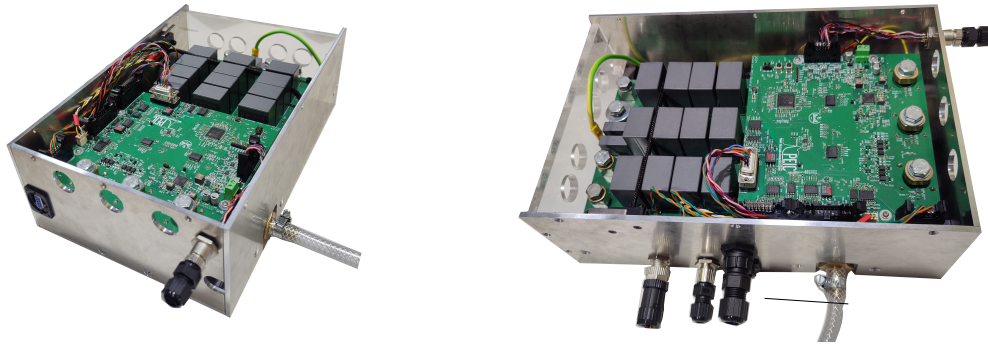
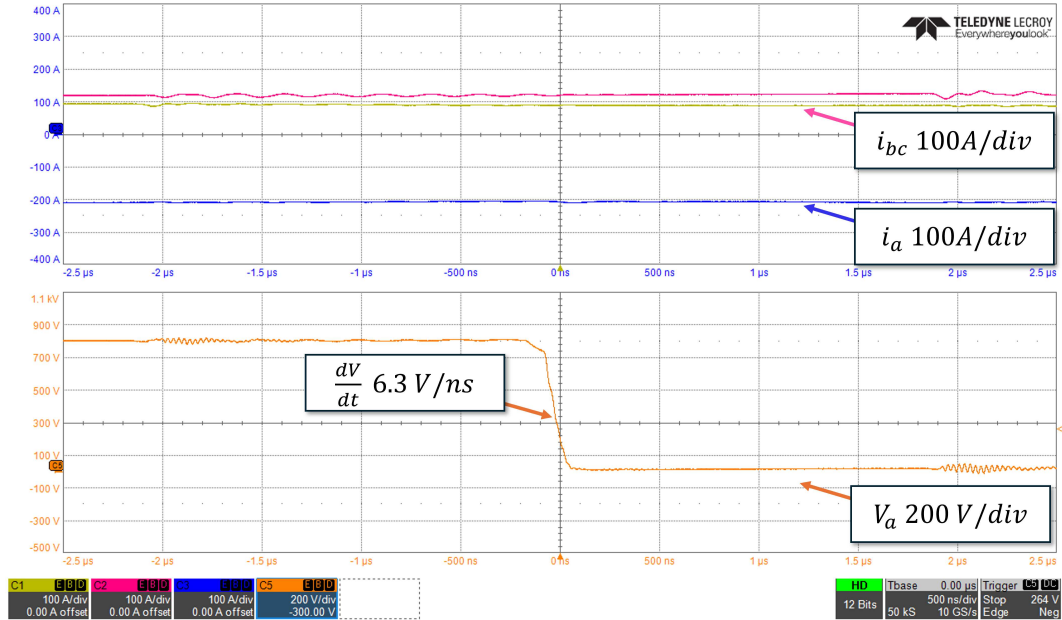


Fig. 5.10 Overview of the full DC/AC converter prototype.

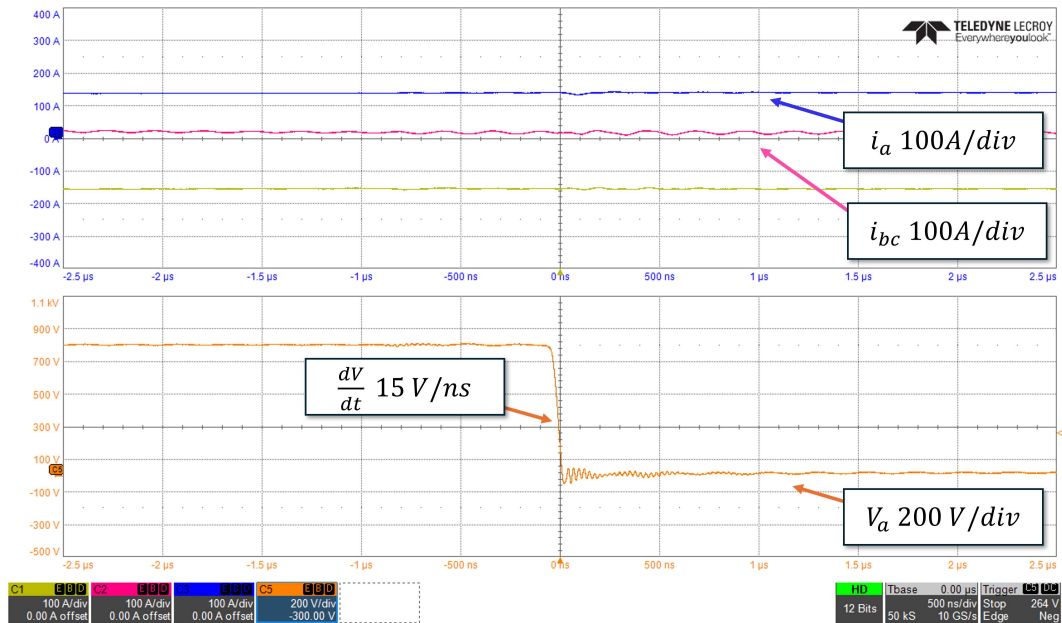
5.4.1 Experimental validation

The testing of the converter has been performed using an inductive load. Fig. 5.11 and Fig. 5.12 show a detailed view of the ON/OFF transitions at the peak current level. It can be observed that the ON transitions are cleaner when the current flowing through the drain is positive, whereas the opposite trend is observed during the OFF transitions. This behavior can be explained by considering the conduction mechanism of the device. In the case of positive drain current, the ON transition occurs through the natural channel conduction, resulting in a smoother switching event. Conversely, when the current is negative, the ON transition takes place while the body diode (or reverse conduction path) is already conducting, leading to additional parasitic interactions and a less clean waveform. For the OFF transition, the situation is reversed: with positive current, the device turns off directly from channel conduction, producing a sharper and more regular event, while negative current conditions involve the commutation of the reverse conduction path, which tends to increase oscillations and waveform distortion.

Subsequently, continuous operation tests were conducted to further assess the performance of the converter under steady-state conditions. Fig. 5.13 and Fig. 5.14 show the three-phase current waveforms and the corresponding output phase voltage for different peak current levels. At lower current levels (e.g., Fig. 5.13), the current waveforms exhibit a nearly sinusoidal shape. However, as the peak current increases (as in Fig. 5.14), noticeable waveform distortion appears. This effect is attributed to the magnetic saturation of the inductors employed during the tests, which were not specifically designed for operation at such current levels.

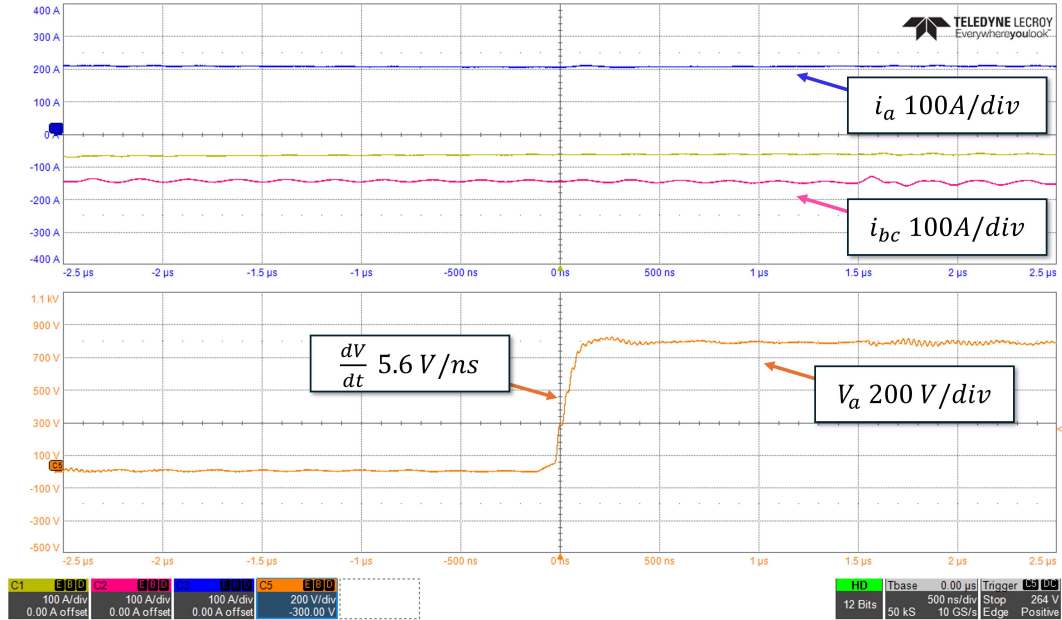


(a) ON transition with positive current flowing through the drain.

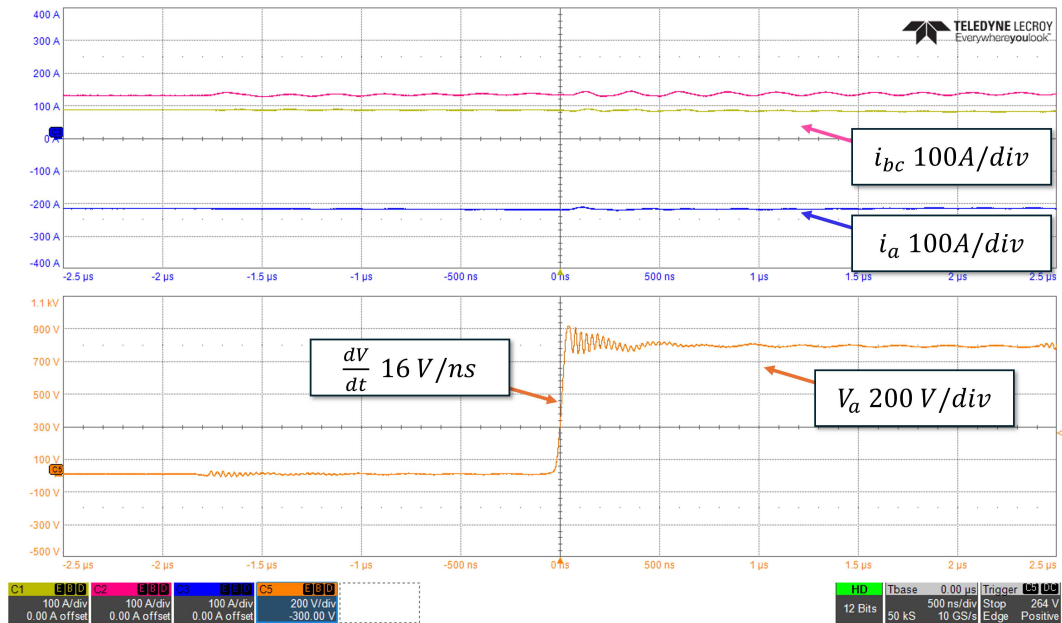


(b) ON transition with negative current flowing through the drain.

Fig. 5.11 Measured voltage waveforms during the ON transition at $V_{dc} = 800\text{ V}$, $I_{pk} = 220\text{ A}$, and $f_{sw} = 20\text{ kHz}$, for both positive and negative drain current conditions.



(a) OFF transition with positive current flowing through the drain.



(b) OFF transition with negative current flowing through the drain.

Fig. 5.12 Measured voltage waveforms during the OFF transition at $V_{dc} = 800\text{ V}$, $I_{pk} = 220\text{ A}$, and $f_{sw} = 20\text{ kHz}$, for both positive and negative drain current conditions.

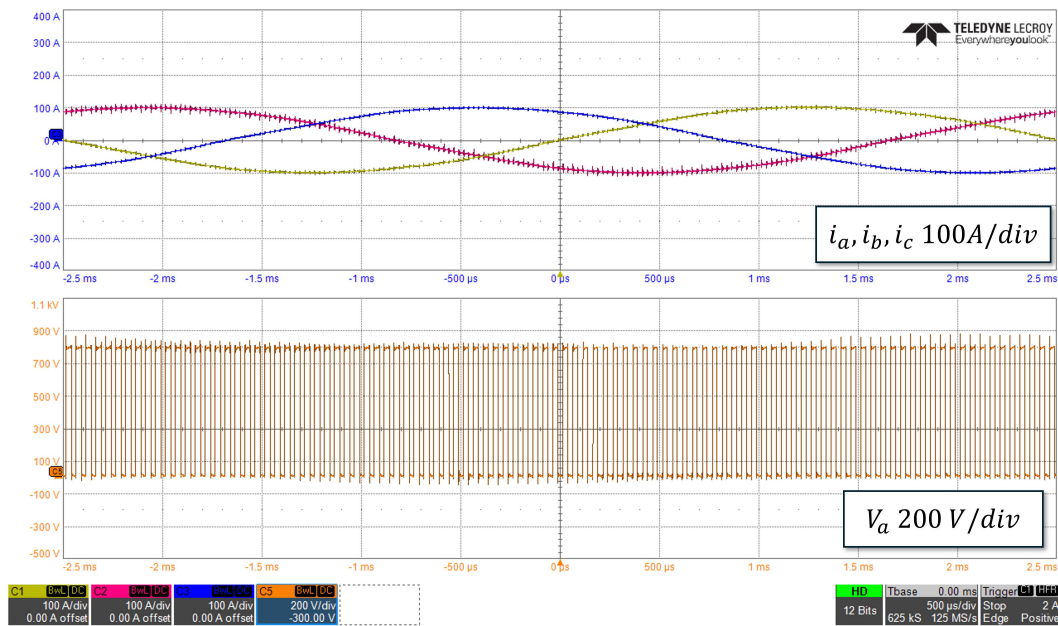


Fig. 5.13 Continuous inverter operation at $V_{dc} = 800$ V, $I_{pk} = 100$ A, and $f_{sw} = 20$ kHz. The three-phase currents and corresponding output phase voltage are shown.

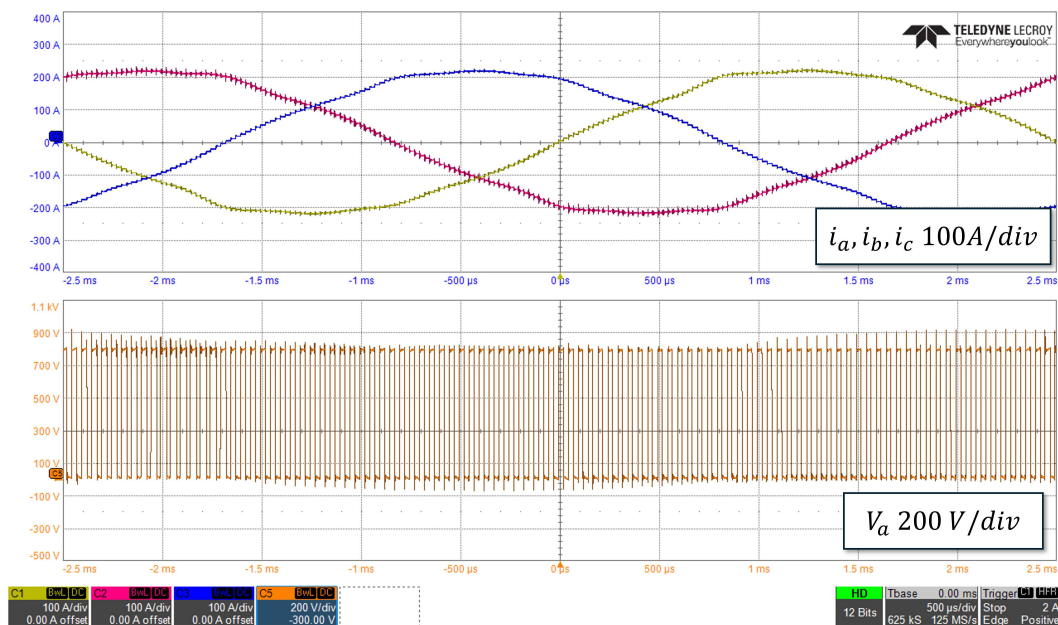


Fig. 5.14 Continuous inverter operation at $V_{dc} = 800$ V, $I_{pk} = 220$ A, and $f_{sw} = 20$ kHz. Current distortion becomes more pronounced, confirming the influence of inductor saturation.

5.5 Summary

This chapter presented the design and prototyping of a 150 kW SiC-based traction inverter for fuel cell electric vehicles. The comprehensive development process covered:

- Comparative analysis of commercial SiC power modules, selecting Infineon FS05MR12A6MA1B based on thermal performance and packaging.
- Three-layer stacked architecture separating power, driver, and control boards.
- DC-link capacitor sizing via simulation sweeps, determining 150 μF minimum capacitance for <20 V ripple.
- Prototype assembly validating the mechanical and electrical design.
- Experimental validation showing clean switching transitions up to 220 A peak current.

The prototype demonstrated stable operation under continuous loading conditions, with waveform distortion at high currents attributed to test inductor saturation rather than converter limitations. The design successfully established the foundation for the full efficiency characterization presented in Chapter 6.

Chapter 6

DC/AC converter - *Back-to-Back* *testing methodology and efficiency* *mapping*

6.1 Introduction

The growing demand for power converters in emerging applications—such as vehicle electrification, energy-smart systems, and high-efficiency power supplies—has significantly increased the need for appropriate testing and functional validation procedures. These procedures must ensure reliable operation under realistic mission profiles and specific operating points. Consequently, the testing and validation of power converters have become increasingly complex and costly. Traditional testing approaches typically rely on passive loads; however, these are affected by major limitations in reproducing realistic operating conditions. In particular, purely inductive loads allow the exploration of only low power factor operating points, which makes them unsuitable for comprehensive efficiency characterization. On the other hand, advanced test setups employing high-power supplies and programmable load banks provide greater flexibility but at the cost of increased hardware complexity and expenses.

To overcome such limitations, several alternative testing methods have been proposed in the literature. For instance, [109] presents a testing configuration based on a back-to-back (B2B) connection of two converters, emulating the behavior of an

induction motor. In this setup, one converter regulates the three-phase voltage V_{abc} , while the other tracks the current references generated by a motor model. Although this approach effectively replicates realistic load conditions, it suffers from circulating common-mode currents i_{cm} between the converters. To mitigate this issue, the authors implemented synchronization of the fundamental waveforms through CAN bus communication [109]. A related research direction explores Power-Hardware-in-the-Loop (PHIL) platforms for machine emulation. For example, [110] investigates the use of LCL coupling networks to ensure stable and accurate emulation of Permanent Magnet Synchronous Machines (PMSMs). Although this approach does not employ a classical B2B configuration, it shares the same goal of reproducing realistic loading conditions for converters. However, it introduces additional challenges related to stability margins and coupling network design.

Furthermore, the test bench proposed in [111] is designed for uninterruptible power supply (UPS) systems and incorporates a step-up transformer. This transformer performs multiple functions: it enables DC-link charging, supports energy recirculation, and introduces leakage inductance that shapes the current waveform, improving the accuracy of the model. A more sophisticated configuration is described in [112], where circulating power is returned to the grid using two electrical machines and additional control hardware for synchronization—an approach that, while effective, increases hardware requirements and overall system complexity. Given these limitations, an increasing research effort has been devoted to enhancing control strategies. The industrial test platform presented in [113] represents a significant step in this direction. It employs dual voltage-source inverters (VSIs) as a virtual load for the converter under test (CUT) in end-of-line testing of industrial drives. In this configuration, a resonant controller allows the virtual load to act as a common-mode active filter, mitigating recirculating currents. However, its effectiveness is confined to predefined frequencies, as the controller bandwidth restricts the attenuation of higher-frequency disturbances.

Among the different B2B configurations, the topology proposed in [119] represents a major advancement, inspired by the open-end winding motor structure. In this setup, two inverters share a common DC-link and are interconnected through three coupling inductors that emulate motor windings. This configuration eliminates the need for external load banks, as power is internally recirculated between the converters, requiring only a small DC supply to compensate for system losses. Nevertheless, several drawbacks remain. First, the shared DC-link prevents full-power

Ref.	Regenerative setup	Proposed solution	Exp. val.	Speed comm	Drawbacks
[114]	no	PWM modulation strategies	no	High	The reduction of the common-mode voltage is achieved by controlling the switching frequencies of both converters.
[115]	yes	Coordinated control strategy between converters	no	High	Common control routine shared by both converters.
[116]	yes	Coordinated control + LCL	yes	–	No discussion on independent control boards.
[117]	yes	Coordinated control + PLL	yes	High	Common controller board shared between converters.
[118]	yes	Hysteresis control	yes	Low	–
[119]	yes	Control + Carrier synchronization	yes	High	External synchronization board required.
[120]	yes	Common-mode choke + carrier synchronization	yes	High	–
[121]	yes	Control routine + synchronization	yes	High	Common controller board shared between converters.
[122]	no	Control routine	no	–	–
[109]	yes	Motor emulator	yes	–	Motor behavior simulated; no discussion of common-mode current suppression.
[112]	yes	Additional converter/motor	yes	–	DFIM-based configuration.
[123]	yes	B2B testing configuration	yes	–	No mention of common-mode current suppression.

Table 6.1 Summary of literature on B2B converter configurations.

testing of the converter under test. Second, common-mode circulating currents become significant in high-power operation, necessitating mitigation techniques. In [119], this issue is addressed through an external synchronization board, while in [117, 121], a common controller board coordinates both converters. Although this simplifies synchronization, it reduces modularity and flexibility. A summary of these solutions, including their validation level and main limitations, is provided in Table 6.1. The table highlights the prevalence of B2B testing setups and the diversity of approaches adopted to overcome their inherent challenges.

Despite the advantages of internal power recirculation and reduced hardware requirements, most existing B2B solutions remain limited in their ability to fully decouple the converter under test from its load—both in terms of power exchange and control architecture. In particular, the use of a shared controller or tight syn-

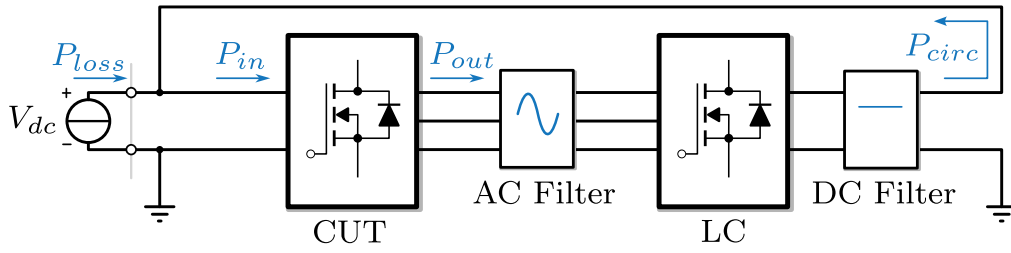


Fig. 6.1 B2B converter test setup scheme.

chronization strategy constrains system modularity and complicates independent testing of different converters. Moreover, the presence of a shared DC-link inherently leads to the generation of common-mode currents, which can cause electromagnetic interference, additional losses, and potential reliability issues, especially at high power or voltage levels.

To address these limitations, this chapter introduces a novel B2B test setup characterized by the following features:

- The converter under test (CUT) and the loading converter operate independently, each with its own control unit, while communicating with an external test manager via a low-speed CAN bus.
- High modularity, allowing the testing of any converter under arbitrary load conditions without the need for firmware-level coordination or shared control hardware.
- Effective suppression of circulating common-mode currents through the use of a transformer, which also enables full-rated voltage and current testing of the CUT—extending the capabilities of the setup beyond conventional B2B architectures.

This configuration provides a highly modular and flexible testing environment, capable of supporting comprehensive and high-fidelity converter validation with minimal hardware complexity. The use of a transformer not only isolates the two converters but also allows operation at full voltage and current ratings, significantly enhancing the applicability of the testbench to a wide range of converter technologies and power levels.

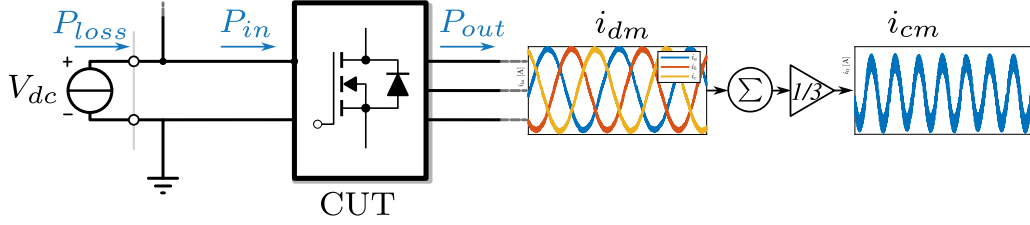


Fig. 6.2 Illustration of common-mode (i_{cm}) and differential-mode (i_{dm}) currents in a B2B configuration.

6.2 Common-Mode and Differential-Mode Filtering Configurations

As previously introduced, the use of a shared DC-link between two converters in a B2B test configuration offers clear advantages in terms of reduced power demand from the external supply. However, this architecture also introduces several critical challenges. The most relevant issue is the presence of undesired low- and high-frequency current components, in particular the common-mode (i_{cm}) and differential-mode (i_{dm}) currents, as illustrated in Fig. 6.2.

The differential-mode current i_{dm} represents the output load current generated by the differential-mode voltage, defined as the voltage difference between any two phase terminals. It contains both the fundamental component at frequency f_0 and additional harmonics resulting from PWM switching and interactions with the load. In contrast, the common-mode current—computed as the average of the three-phase currents—is associated with the common-mode voltage generated by the inverter. This voltage can be intentionally injected, for instance, to increase the modulation index or to implement zero-sequence voltage injection techniques.

In a B2B configuration, the shared DC bus provides a natural return path for common-mode currents, which can reach significant amplitudes. Such currents contribute to higher conduction and switching losses, increased electromagnetic emissions, and degraded measurement accuracy and reliability during testing. The issue becomes particularly severe when testing complete power converters that already include EMI filters at their input stage. These filters are designed to handle limited levels of i_{cm} and may be damaged or operate improperly when exposed to the higher current levels typical of B2B configurations. Moreover, the electrical

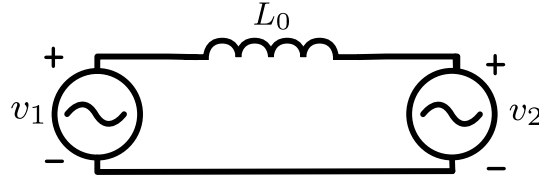


Fig. 6.3 Simplified common-mode equivalent circuit of the B2B test configuration.

coupling between converters through the shared DC-link generates both i_{cm} and i_{dm} ripple components, which must be minimized to ensure stable operation and accurate test results.

As reported in the literature, a major source of i_{cm} arises from the lack of synchronization between the PWM carriers of the two converters and the dead-time of power switches belonging to the same leg [124, 125]. Additionally, third-harmonic injection naturally introduces common-mode recirculating currents.

6.2.1 Common-Mode Equivalent Circuit

To clarify the mechanism behind the generation and suppression of the circulating common-mode current in the adopted B2B configuration, a simple common-mode equivalent circuit can be derived. The proposed model, shown in Fig. 6.3, consists of two common-mode voltage sources, representing the common-mode voltages generated by each inverter (the converter under test and the load converter), and an equivalent common-mode inductance L_0 of the loop. The inductance L_0 accounts for all the elements that contribute to the impedance seen by the common-mode current (coupling inductors, L or LCL filters, transformer leakage inductance, and possible common-mode chokes). The common-mode capacitances are neglected in this analysis, since their values are difficult to estimate or to measure accurately and they do not significantly affect the first-harmonic behavior, which is the focus of this model.

If only the first harmonics of the common-mode voltages v_1 and v_2 are considered, they can be expressed as

$$v_1 = V_{CM} \sin(\omega_1 t + \varphi_1) \quad (6.1)$$

$$v_2 = V_{CM} \sin(\omega_1 t + \varphi_2) \quad (6.2)$$

where V_{CM} is the amplitude of the first harmonic of the common-mode voltage generated by each inverter and ω_1 is the fundamental frequency of the common-mode voltage generated by the converter (for a three-phase two-level inverter, $\omega_1 \approx \omega_{sw}$).

The amplitudes are assumed equal, since the DC-link voltage, modulation index, and switching frequency of the two converters are the same or at least very similar. Without loss of generality, the phase of the first converter common-mode voltage is set to $\varphi_1 = 0$. The resulting common-mode voltage stress across the loop is then given by

$$v_{CM}(t) = v_1 - v_2 = V_{CM} [\sin(\omega_1 t) - \sin(\omega_1 t + \varphi_2)]. \quad (6.3)$$

By applying trigonometric identities, (6.3) can be rewritten as

$$v_{CM}(t) = 2V_{CM} \cos\left(\omega_1 t + \frac{\varphi_2}{2}\right) \sin\left(-\frac{\varphi_2}{2}\right). \quad (6.4)$$

Therefore, the magnitude of the common-mode voltage stress in the loop is proportional to $|\sin(\varphi_2/2)|$ and depends directly on the phase shift φ_2 , which is ultimately dictated by the converters' PWM carriers and switching patterns.

By neglecting the common-mode capacitances, the circulating common-mode current can be approximated as

$$i_{CM}(t) \approx \frac{v_{CM}(t)}{j\omega_1 L_0}, \quad (6.5)$$

so that its peak value is

$$I_{CM,pk} \approx \frac{2V_{CM} \left| \sin\left(\frac{\varphi_2}{2}\right) \right|}{\omega_1 L_0}. \quad (6.6)$$

This design-oriented expression makes it possible to estimate *a priori* the circulating current amplitude from the setup parameters. Given a maximum acceptable common-mode current $I_{CM,max}$, the required equivalent inductance can be directly obtained as

$$L_0 \geq \frac{2V_{CM} \left| \sin\left(\frac{\varphi_2}{2}\right) \right|}{\omega_1 I_{CM,max}}. \quad (6.7)$$

In the proposed setup, this constraint is satisfied by the combination of the coupling inductors, the AC and DC filters, and the transformer leakage inductance,

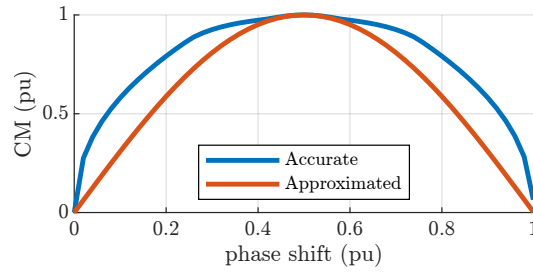


Fig. 6.4 Comparison between normalized common-mode voltage stress obtained from detailed numerical evaluation and from the simplified first-harmonic model as a function of the phase shift between the voltages generated by the two converters.

ensuring that the common-mode current remains well below the admissible limit across the operating range.

Although the model is intentionally simple and only considers the first harmonic of the common-mode voltage, it matches well the numerically obtained results when the actual switching waveforms of both converters are used. This is illustrated in Fig. 6.4, which compares the normalized common-mode voltage stress predicted by the proposed model with the one obtained from a detailed numerical evaluation. The simplified model accurately captures the minima and maxima of the common-mode stress as a function of the phase shift, which is sufficient to identify the phase shifts leading to the worst common-mode conditions and to guide the design of the mitigation techniques discussed in the remainder of this section.

From Figs. 6.3 and 6.4, it is evident that mitigation can be achieved either by reducing the common-mode voltage term $V_{CM} |\sin(\phi_2/2)|$ (through appropriate PWM and carrier synchronization) or by increasing the equivalent inductance L_0 of the common-mode path (through suitable passive filtering and transformer design). The filtering configurations analyzed in the following subsections implement these two design levers in different ways.

To mitigate the impact of the circulating common-mode and differential-mode currents, various filtering and control strategies have been proposed, aiming to suppress or decouple the influence of these disturbances. In this work, five main approaches are considered, selected for their relevance in B2B converter systems:

- **Inductive filter:** a basic configuration using three-phase inductors on the AC side to attenuate high-frequency i_{dm} disturbances, Fig. 6.5(a).

- **LCL filter:** a more advanced topology that provides improved high-frequency attenuation and better decoupling between the two converters, avoiding direct interaction between their PWM signals, Fig. 6.5(b).
- **AC and DC common-mode choke filters:** additional filters that can be integrated with the previous solutions to further suppress i_{cm} currents, Fig. 6.5(c,d).
- **Active filtering:** control-based approaches where inner control loops are implemented to suppress low-frequency recirculating common-mode currents, typically through resonant controllers tuned at the i_{cm} frequency.
- **Transformer:** the most robust solution in terms of electrical isolation, capable of completely blocking common-mode currents and attenuating differential-mode noise through leakage inductance, Fig. 6.5(e). However, practical issues such as magnetic saturation, size, and limited low-frequency performance must be carefully evaluated.

6.2.2 Inductive Filter and LCL Filter

The implementation of an inductive filter in a B2B configuration provides a simple and practical solution to improve power quality. As shown in Fig. 6.5(a), the filter aims to attenuate current ripple and avoid a direct electrical connection between the converters. Despite its simplicity, this configuration offers limited harmonic attenuation due to the impedance $Z_L = sL$, which provides an attenuation rate of only -20 dB/dec [126]. Consequently, very high switching frequencies are required to sufficiently suppress high-frequency harmonics [127]. Furthermore, additional control effort is necessary to compensate for undesired common-mode current components.

Since a single L filter cannot effectively attenuate high-frequency harmonics, multi-stage filtering is often adopted. A standard solution in voltage-source converter (VSC) applications is the LCL filter [126, 128, 129]. The design of such filters has been widely investigated in the literature [130]. In B2B systems, an LCL filter can be easily integrated, as shown in Fig. 6.5(b). Compared to the simpler L filter, the LCL configuration requires a more detailed passive component design but provides stronger attenuation of higher-order harmonics [131]. However, its resonant

behavior can introduce potential stability issues [132], requiring the implementation of additional control strategies for damping and stabilization.

In summary, both L and LCL filters represent valid solutions for suppressing high-frequency differential-mode circulating currents i_{dm} and for decoupling the PWM operation of the two converters. Nevertheless, these filters are not effective in mitigating common-mode current i_{cm} components.

6.2.3 Common-Mode Choke Implementation

The inclusion of a common-mode choke offers an effective means to reduce circulating common-mode currents in a B2B converter configuration [133]. In [133], accurate design guidelines and specifications for common-mode filters are presented. As illustrated in Fig. 6.5(c,d), the common-mode choke can be inserted either on the AC side—between the output terminals of the two converters—or on the DC side, within the recirculation path between them. When placed on the AC side, the common-mode choke attenuates both low- and high-frequency CM currents propagating along the three-phase lines.

Over the years, several designs for integrated chokes have been proposed to simultaneously attenuate both common-mode (i_{cm}) and differential-mode (i_{dm}) current components [134–137], enhancing EMI performance without significantly increasing the system footprint.

6.2.4 Active Filtering

To mitigate common-mode currents i_{cm} , various control-based solutions have been proposed [115, 117–119, 121], many of which originate from research on zero-sequence current suppression in open-end winding machines [138–141]. In [138], three modulation techniques for common-mode current suppression are compared. Compared to the case without compensation, the inclusion of an additional PI control loop can significantly reduce total harmonic distortion, while the best results are achieved using a dead-time compensation technique.

Nevertheless, dead-time compensation presents practical limitations, especially in B2B configurations. As an open-loop approach, it lacks feedback to adapt to changing load conditions, making precise cancellation of the zero-sequence voltage

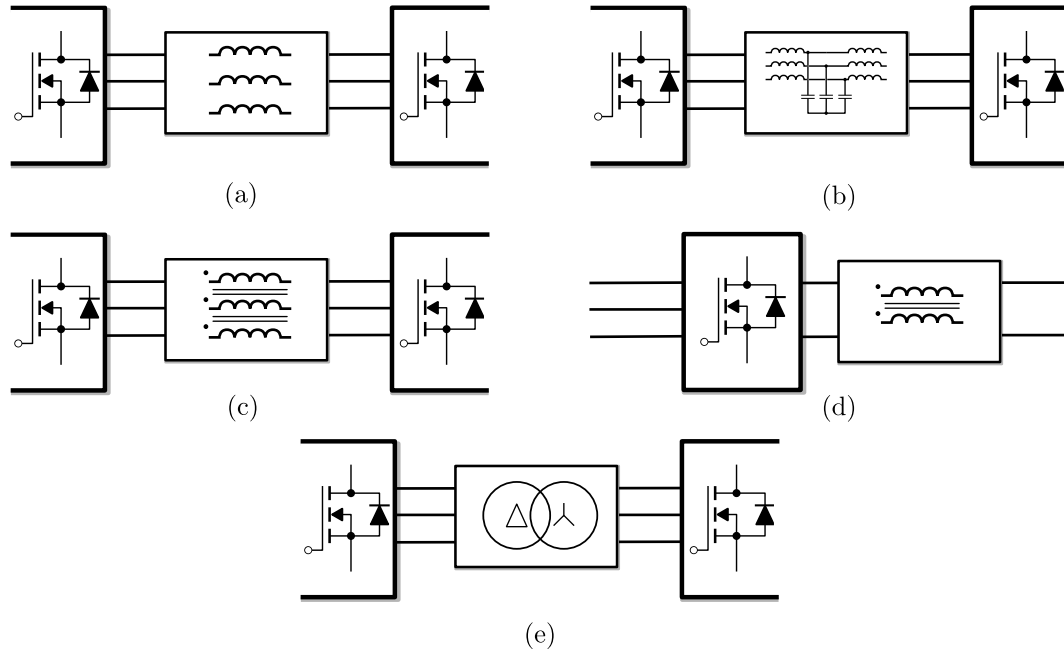


Fig. 6.5 Filter configurations analyzed: (a) L filter, (b) LCL filter, (c) common-mode choke on the AC side, (d) common-mode choke on the DC side, (e) transformer.

difficult [138]. Moreover, it requires high-speed communication between the two converters—typically through a shared control board—which is not always feasible when testing different converter units independently. In [113], common-mode current suppression is achieved through the use of a resonant controller. Its effectiveness is comparable to that of a common-mode choke, although it strongly depends on the converter's fundamental frequency and on accurate tuning of the resonant parameters.

For clarity, the resonant controller used later in this work is briefly detailed here. The controller operates on the measured common-mode current and is designed to attenuate the low-frequency component that appears when the two converters switch at the same frequency but with an uncontrolled PWM phase shift. The tuning frequency of the resonant controller is selected as three times the fundamental frequency, $f_{\text{res}} = 3f_0$, since this harmonic represents the dominant low-frequency component of the circulating common-mode current in a B2B configuration without synchronization.

The controller adopts the standard resonant structure

$$G_{\text{res}}(s) = K_{\text{res}} \frac{2\omega_{\text{res}}s}{s^2 + \omega_{\text{res}}^2}, \quad (6.8)$$

where $\omega_{\text{res}} = 2\pi f_{\text{res}}$. This transfer function provides a very high gain at ω_{res} and negligible gain at DC, which is suitable for selectively suppressing the targeted harmonic of the common-mode current. The continuous-time controller (6.8) is then discretized and implemented following the same sinusoidal-integrator methodology adopted in [113].

6.3 Proposed B2B Testing Solution

The proposed B2B test configuration is illustrated in Fig. 6.6. This solution leverages a common DC link between two converters to exploit the main advantage of reduced power demand from the external supply. The setup consists of the Converter Under Test (CUT) and a load inverter operating as an active load. These two converters are interconnected through a network of three coupling inductors (L or L_{load}) and a three-phase Δ –Y isolation transformer, forming a controlled power recirculation path. A key design objective is to enable comprehensive testing of the CUT while minimizing the amount of additional hardware and avoiding any modification to the CUT's native control scheme. Furthermore, the approach allows the use of any commercially available inverter as the load converter. To ensure coordination between the two converters, communication is established through a CAN interface, enabling the exchange of reference quantities without requiring direct control interconnection.

One of the main advantages of this configuration lies in the significantly reduced power requirement from the DC-link supply. The DC voltage source (V_{dc}) is only required to compensate for the total system losses (P_{loss}), which represent a small fraction of the total recirculating power (P_{rec}). Consequently, the proposed setup enables high-power testing with minimal grid power consumption, achieving high energy efficiency and lower operating costs.

A further key advantage is related to common-mode current mitigation. As discussed in Section 6.2, a major drawback of conventional B2B configurations is the circulation of common-mode current i_{cm} through the shared DC link. The inclusion of a Δ –Y transformer in the proposed setup provides complete suppression of i_{cm} recirculation between the converters, since any common-mode component is confined within the delta side of the transformer and does not flow through the CUT terminals. Any residual circulation inside the delta connection is irrelevant for the CUT operation and does not affect the accuracy or safety of the tests. This

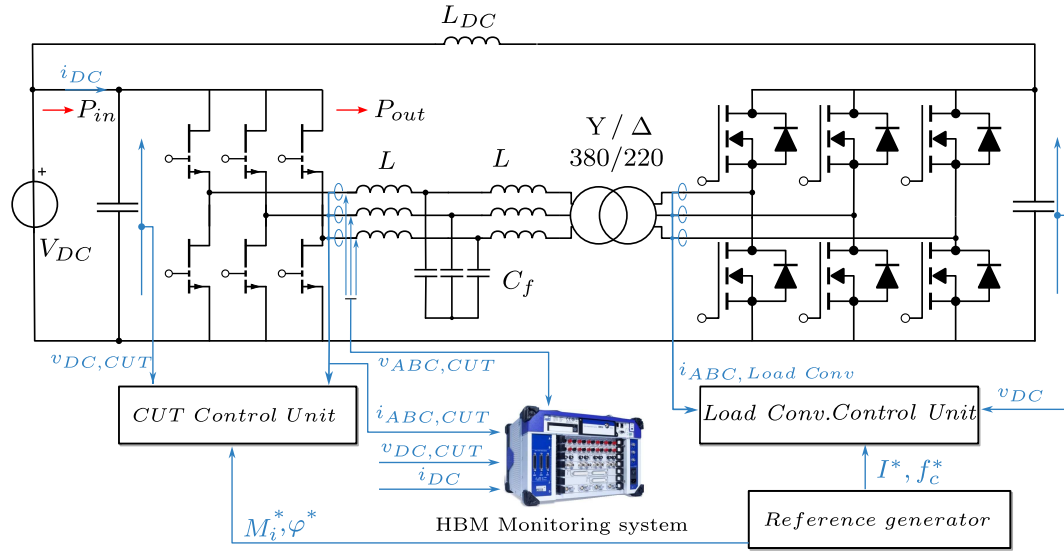


Fig. 6.6 Functional block diagram of the proposed B2B testing configuration with the converter under test and the load converter.

configuration therefore brings significant additional benefits in terms of reduced conducted emissions and improved EMI performance [142], without requiring active common-mode control.

An additional benefit of incorporating the transformer lies in the possibility of increasing the effective modulation range of the CUT. In a conventional B2B configuration with direct connection, both converters generate approximately the same line-to-line voltage for a given DC-link voltage and therefore share the same modulation index limit. By contrast, the voltage transformation introduced by the Δ -Y transformer decouples the line-to-line voltages of the CUT and the load converter. This enables the CUT to operate at a higher modulation index (up to approximately $M_{\text{CUT}} \simeq 1.15$ in the considered implementation), while the load converter remains within its nominal modulation range.

In three-phase power systems, transformers with a Δ -Y configuration are widely employed for stepping voltages up or down. In such a configuration, the primary winding is connected in delta, while the secondary is connected in wye connected. If

$$N = \frac{N_{\Delta}}{N_Y}$$

denotes the turns ratio, where N_{Δ} and N_Y are the number of turns per phase on the delta and wye sides, respectively, the relationships between line currents and line

voltages are given by

$$I_{\text{line},Y} = \frac{N}{\sqrt{3}} I_{\text{line},\Delta}, \quad (6.9)$$

$$V_{\text{line},Y} = \frac{\sqrt{3}}{N} V_{\text{line},\Delta}. \quad (6.10)$$

Therefore, the overall transformation from the Δ side (load converter) to the Y side (CUT) includes both the turns ratio N and the $\sqrt{3}$ factor arising from the different phase-to-line relationships.

Since the two converters are supplied by the same DC-link voltage V_{dc} and use standard three-phase carrier-based PWM, the fundamental line-to-line voltages can be expressed as

$$V_{\text{line},Y} = k M_{\text{CUT}} V_{dc}, \quad V_{\text{line},\Delta} = k M_{\text{Load}} V_{dc}, \quad (6.11)$$

where M_{CUT} and M_{Load} are the modulation indices of the CUT and the load converter, respectively, and k is the PWM gain factor. Combining these expressions with (6.10) yields

$$k M_{\text{CUT}} V_{dc} = \frac{\sqrt{3}}{N} k M_{\text{Load}} V_{dc}, \quad (6.12)$$

so that

$$M_{\text{CUT}} = \frac{\sqrt{3}}{N} M_{\text{Load}}. \quad (6.13)$$

For the case $N = 1$, this relation shows that the CUT can reach a modulation index $\sqrt{3}$ times larger than that of the load converter for the same DC-link voltage, thus extending the usable operating range of the CUT without overstressing the load inverter.

In the experimental prototype, the adopted Δ –Y transformer has a rated 380/220 V rating with an effective turns ratio close to $N = 1$, resulting in an approximately $\sqrt{3} : 1$ line-to-line voltage ratio between the two sides. Hence, (6.13) mainly provides a design guideline for future implementations employing non-unity transformer ratios. It should also be noted that the transformer is a conventional low-frequency device, designed to sustain only the fundamental-frequency component of the CUT output voltage, while high-frequency switching harmonics are filtered by the coupling inductors and AC filters discussed in Section 6.2.

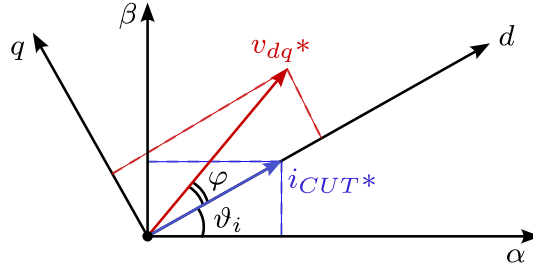


Fig. 6.7 Representation of the rotating d - q vector control scheme.

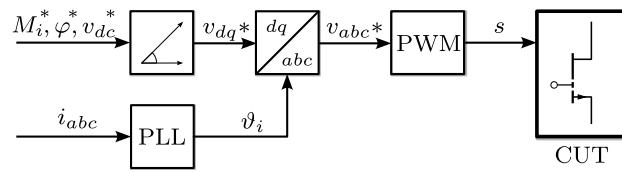


Fig. 6.8 Control structure of the Converter Under Test (CUT).

6.3.1 Control Implementation

As previously discussed, a major advantage of the proposed configuration is that no additional complex common-mode control loop is required, since the Δ -Y transformer inherently suppresses i_{cm} recirculation between the converters. Each converter can therefore operate independently using its own local control strategy, as shown in Fig. 6.8 and Fig. 6.9 for the CUT and load converters, respectively.

The CUT operates under an open-loop voltage control scheme implemented in the synchronous rotating reference frame (d - q axes), as depicted in Fig. 6.8. The converter is modulated at a constant switching frequency f_{sw} (50 kHz in the experimental prototype). Through CAN communication, the CUT receives the desired modulation index and phase angle, which are used to generate the reference voltage vector v_{dq}^* by means of a polar transformation.

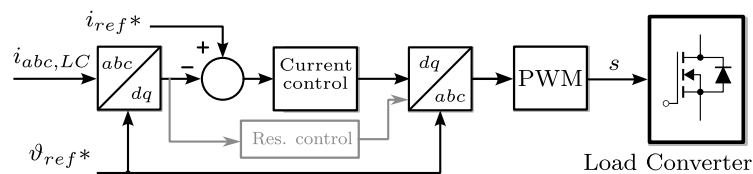


Fig. 6.9 Control structure of the load converter.

A phase-locked loop (PLL) synchronizes the control with the converter current vector by extracting the reference angle ϑ_i from the measured i_{abc} currents. This angle is then used for the inverse Park transformation, which generates the voltage vector reference applied to the PWM block implementing a carrier-based space vector modulation (SVM) technique. The resulting switching pattern defines the fundamental voltage magnitude and phase applied to the transformer primary side.

On the load side, the inverter receives via CAN the reference current magnitude i_{ref}^* and the phase angle ϑ_{ref}^* , corresponding to the same PLL-derived reference used in the CUT control. The reference current is processed within a closed-loop current controller, as shown in Fig. 6.9. The controller is implemented in the same d - q rotating frame used for the CUT, whose geometry is summarized in Fig. 6.7. The d -axis is phase-locked to the rotating current vector imposed by the loading inverter, ensuring synchronization between both converters.

The measured and reference current vectors are compared in the current control loop, enabling the load inverter to accurately inject the desired test currents into the CUT. In summary, the load converter employs a straightforward closed-loop current control scheme, while the CUT operates under open-loop voltage control. This decentralized structure allows independent operation of both converters without requiring shared control hardware, ensuring flexibility and ease of integration into diverse testing environments.

Finally, it is worth noting that, from a practical design standpoint, the CUT switching frequency should be equal to or higher than that of the load converter. Otherwise, the dimensioning of the coupling inductors and filters could be compromised, leading to increased current ripple on the CUT side. The proposed combination of transformer-based common-mode suppression, passive filtering, and simple d - q control loops provides a robust and experimentally practical framework for high-power B2B testing of modern power converters.

6.4 Experimental Validation

In order to validate the proposed testing configuration, two experimental campaigns were carried out on the 30 kW GaN-based inverter prototype:

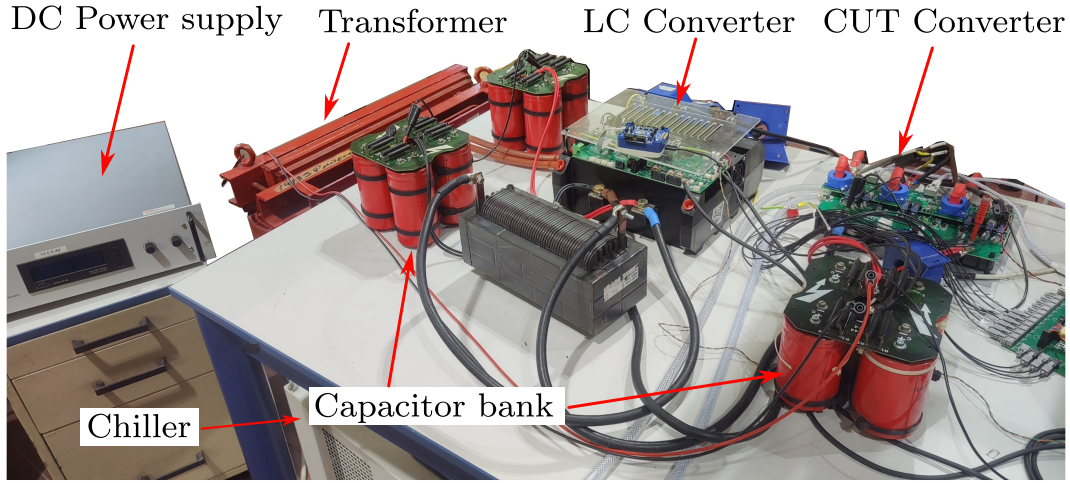


Fig. 6.10 Overview of the experimental setup comprising the Converter Under Test (CUT) and the load inverter.

- Evaluation of the common-mode current suppression strategies introduced in Section 6.2, performed without the isolation transformer.
- Efficiency characterization over the entire operating range of the Converter Under Test (CUT), using the proposed testing configuration with the isolation transformer described in Section 6.3.

Both experimental campaigns were conducted using a dedicated laboratory setup, described in the following subsection, and employed the same CAN-based communication and control infrastructure.

6.4.1 Experimental Setup

A comprehensive test bench was implemented to support both experimental investigations. An overview of the complete laboratory configuration is shown in Fig. 6.10, including the CUT and the Load Inverter. Depending on the experiment, the interconnection and filtering stages were reconfigured, as detailed below. The control schemes presented in Section 6.3—including the PLL for phase synchronization and the d - q control structures in Figs. 6.8 and 6.9—were implemented on both converters during the tests.

In the first test (Section 6.4.2), focused on common-mode current characterization and mitigation, the CUT is connected directly to the load inverter through an

LC/LCL output filter and, optionally, a common-mode choke (CMC). The isolation transformer is omitted in this configuration to allow clearer observation of circulating current phenomena and their attenuation by the passive and active mitigation techniques.

In the second test (Section 6.4.3), dedicated to efficiency mapping, the CUT and load inverter are interconnected through the isolation transformer, as illustrated in Fig. 6.6. This arrangement ensures safe operation and accurate power measurements at higher power levels. The efficiency map is obtained at variable power factors, as the proposed control structure allows current synchronization with the load inverter through a PLL, as shown in Fig. 6.9.

To ensure flexibility at the communication layer, any CAN-compatible device can be used to transmit references and acquire measurements, which is one of the advantages of the proposed architecture. For the experiments, both a dSPACE unit (for the common-mode suppression tests) and a PC running MATLAB equipped with a PEAK USB–CAN interface (for the efficiency mapping) were employed. The use of a standard CAN protocol confirms the portability of the proposed solution across different control and communication hardware.

Table 6.2 summarizes the key components employed in both test campaigns.

6.4.2 Evaluation of Common-Mode Mitigation Techniques

The first experimental campaign focuses on the measurement and mitigation of common-mode currents (i_{cm}) in a B2B configuration *without* the isolation transformer. Several suppression strategies were implemented and compared, namely:

- Baseline operation without any suppression technique, with different switching frequencies for the two converters: $f_{sw,CUT} = 50$ kHz and $f_{sw,LC} = 20$ kHz;
- Baseline operation without suppression, with identical switching frequencies: $f_{sw,CUT} = f_{sw,LC} = 50$ kHz;
- Implementation of a resonant controller for common-mode mitigation, as described in Section 6.2;
- Addition of common-mode chokes on the AC side and on the DC side.

Table 6.2 Main components of the experimental setup for the two test campaigns.

Test 1 – Common-Mode Suppression	
Converter Under Test (CUT)	30 kW GaN-based inverter prototype, $V_{dc} = 400$ V
Load inverter	175 kW SiC-based inverter operating as active load
LC/LCL filter	Three-phase output filter with per-phase inductance L and capacitor C_f
Common-Mode Choke (CMC)	Ferrite-core three-phase choke, optionally installed on the AC or DC side
Acquisition system	HBM high-precision logger for voltage and current measurement
Communication interface	CAN-based control via dSPACE and PEAK USB–CAN interface
Test 2 – Efficiency Mapping	
Converter Under Test (CUT)	30 kW GaN-based inverter prototype
Load inverter	175 kW SiC-based inverter operating as active load
Transformer	50 kVA isolation transformer (nominal 380/220 V, Δ –Y)
Acquisition system	HBM high-precision logger for voltage and current measurement
Communication interface	CAN-based control via MATLAB interface
Control synchronization	PLL-based phase alignment and power factor control

All tests were conducted at an operating point defined by a modulation index $M_i = 0.5$, RMS current $I_{rms} = 15$ A, and fundamental frequency $f_0 = 125$ Hz, corresponding to a typical operating condition of the CUT.

The passive filters employed in the experiments are consistent with the configurations discussed in Section 6.2. When the LCL filter is used, the parameters are $L = 300 \mu\text{H}$ and $C_f = 40 \mu\text{F}$ per phase, resulting in a resonant frequency

$$f_{\text{res,LCL}} = 2054 \text{ Hz},$$

which is well separated from both the fundamental frequency and the converters' switching frequencies. The AC-side common-mode choke used in Fig. 6.11(d) has an inductance of $L_{\text{CM,AC}} = 1.48$ mH, while the DC-side choke in Fig. 6.11(e) provides

Table 6.3 Component values used in the common-mode mitigation experiments.

Component	Value
LCL inductance L	300 μH
LCL capacitor C_f	40 μF
AC CM choke inductance $L_{\text{CM,AC}}$	1.48 mH
DC CM choke inductance $L_{\text{CM,DC}}$	1.48 mH
Resonant gain K_{res}	100

$L_{\text{CM,DC}} = 1.48$ mH. A summary of the relevant component values is reported in Table 6.3.

The resonant controller is implemented with the same ideal structure introduced in Section 6.2. For completeness, the parameters used in the experimental validation are:

- Resonant frequency: $f_{\text{res}} = 3f_0 = 150$ Hz;
- Resonant gain: $K_{\text{res}} = 100$.

These values were tuned to maximize attenuation of the dominant low-frequency component of the circulating common-mode current without compromising the stability of the current control loops of either the CUT or the load converter.

The corresponding experimental results are summarized in Fig. 6.11.

As shown in Fig. 6.11(a), the baseline configuration with different switching frequencies exhibits a substantial circulating common-mode current i_{cm} in the system. When the two converters operate at identical switching frequencies (Fig. 6.11(b)), i_{cm} presents a characteristic pulsating behavior due to the uncontrolled phase shift between the PWM carriers. The introduction of the resonant controller significantly reduces this recirculating current, effectively suppressing its low-frequency harmonics, as illustrated in Fig. 6.11(c). Furthermore, the inclusion of common-mode chokes, either on the AC side or on the DC side, leads to a noticeable attenuation of both common-mode (i_{cm}) and differential-mode (i_{dm}) current ripple components, as shown in Figs. 6.11(d) and 6.11(e). These results confirm the effectiveness of the passive and active mitigation strategies and highlight the practical challenges associated with CM suppression in transformerless B2B configurations, motivating the transformer-based solution adopted in Section 6.3.

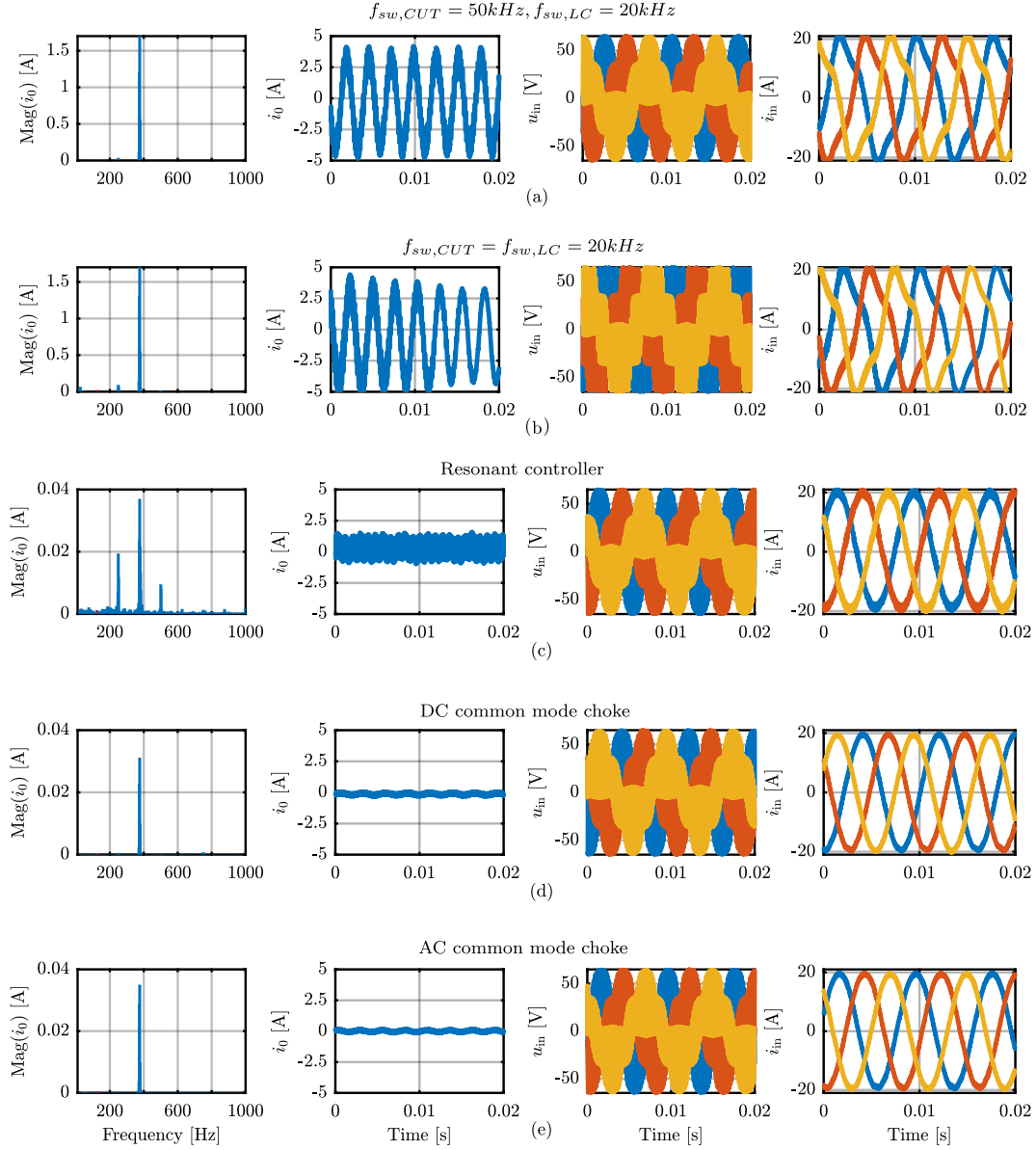


Fig. 6.11 Experimental comparison of different common-mode current mitigation strategies. From left to right: FFT spectra, common-mode current i_{cm} , phase voltages $v_{a,b,c,CUT}$, and phase currents $i_{a,b,c,CUT}$ for: (a) unsynchronized converters with different switching frequencies; (b) unsynchronized converters with identical switching frequencies; (c) resonant common-mode controller; (d) AC-side common-mode choke; (e) DC-side common-mode choke.

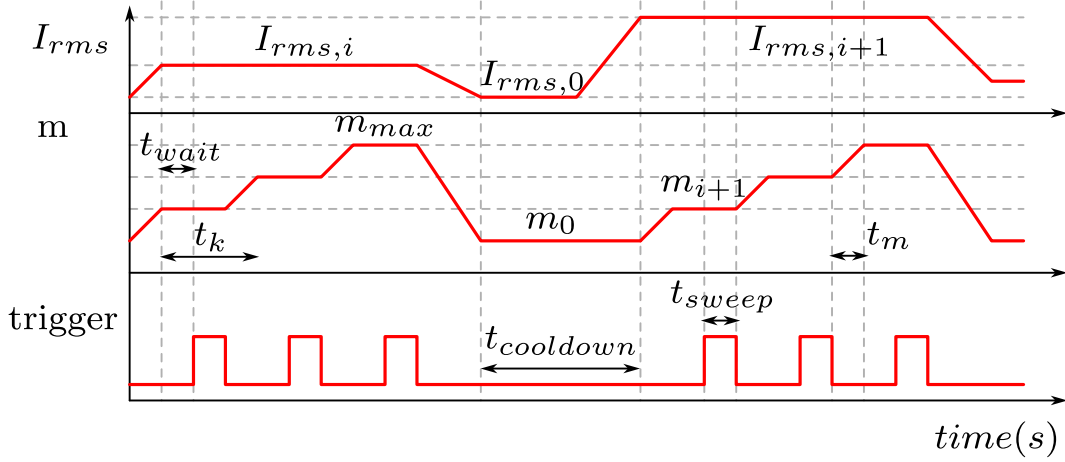


Fig. 6.12 Testing sequence for efficiency mapping, including cool-down periods between operating points.

6.4.3 Efficiency Mapping Technique

The second experimental campaign aims to generate a complete efficiency map of the 30 kW GaN converter prototype using the proposed B2B testing configuration with the isolation transformer. To ensure high precision and repeatability, an automated acquisition routine was developed using an HBM data logger and MATLAB-based reference generation over the CAN interface.

A predefined test pattern, shown in Fig. 6.12, is used to systematically explore the operating envelope of the CUT. For each operating point, the following procedure is executed:

1. The reference values for current and modulation index are generated and transmitted to the converters via CAN.
2. A waiting time of $t_{wait} = 400$ ms is enforced to ensure steady-state conditions.
3. The HBM system is triggered to acquire voltage and current waveforms.
4. A cool-down period is applied before moving to the next operating point, in order to keep the thermal conditions approximately uniform across the map.

This systematic routine improves measurement repeatability and helps maintain approximately uniform thermal conditions across the map. The waiting time is intended to establish electrical steady-state operation, whereas the cool-down interval

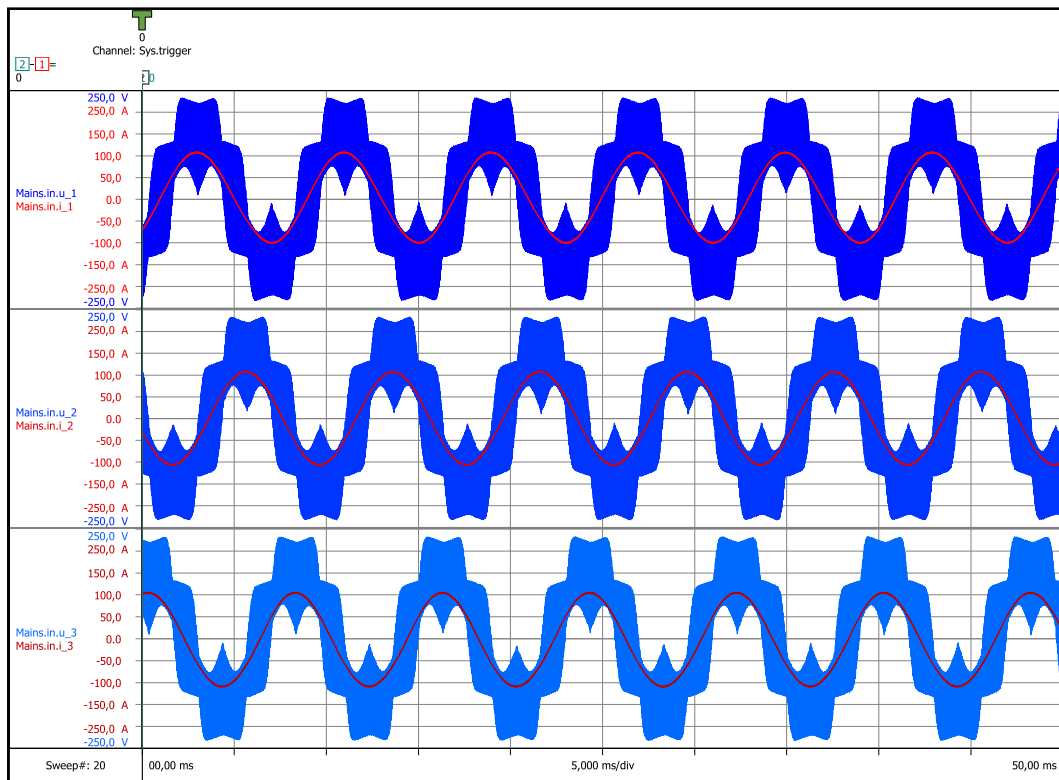
limits, but does not completely eliminate, thermal drift. Figure 6.13 illustrates representative measured line-to-phase voltages and currents from the CUT at two different phase angles. These waveforms confirm that the PLL guarantees stable and accurate synchronization between the CUT and the load converter, and that the phase shift commanded via CAN is correctly tracked across the operating points.

During the efficiency mapping campaign, the CUT was operated up to its full rated power of 30 kW. Under these conditions, thanks to the recirculating-power principle of the B2B configuration, the external DC source supplied only a small amount of power, corresponding to a few percent of the CUT rated power, thus confirming the high energy efficiency of the proposed test setup.

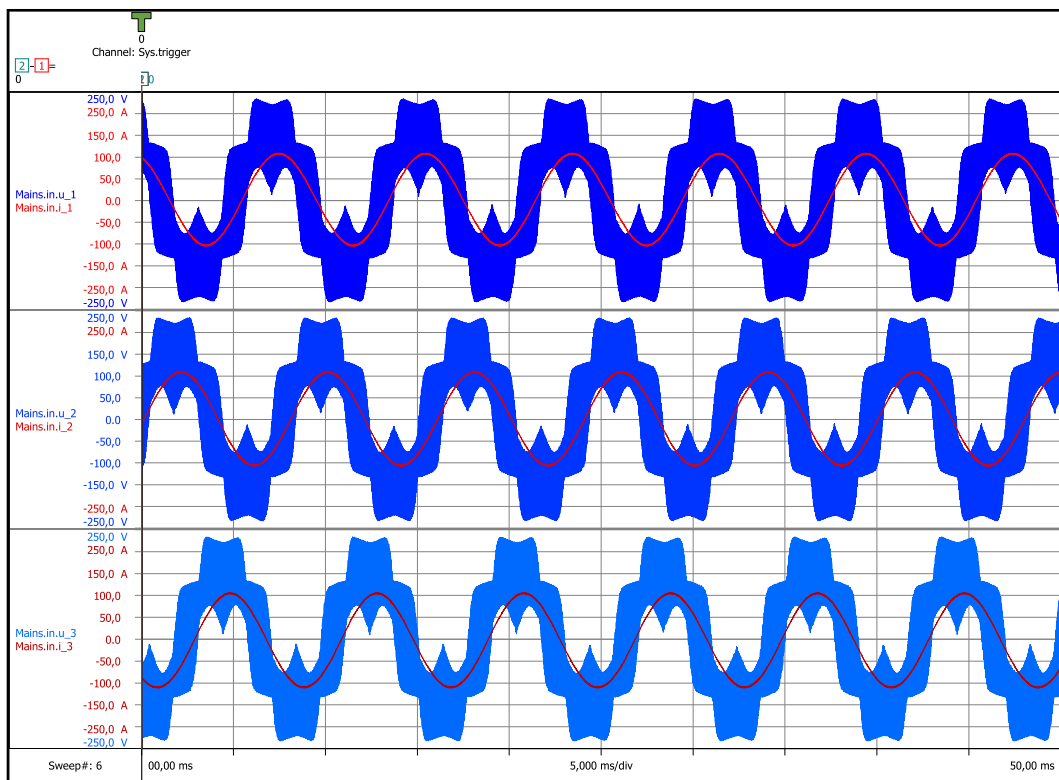
The final efficiency maps are reported in Fig. 6.14, where three estimation cases are presented. In Fig. 6.14(a), the efficiency is computed based on the voltage measured across the LCL filter capacitors C_f , i.e., after the output filter. In Fig. 6.14(b), the same estimation is refined by subtracting the I^2R losses of the filter inductors and output cables, with $R = 13 \text{ m}\Omega$. Finally, Fig. 6.14(c) shows the efficiency directly measured at the CUT output terminals, excluding all test-bench-related elements. The close agreement between Figs. 6.14(b) and 6.14(c) validates the adopted correction approach for loss estimation and confirms that the intrinsic converter performance can be accurately inferred even when measurements are taken downstream of the filter.

6.5 Efficiency mapping of the designed 150 kW DC/AC converter

The efficiency characterization of the 150 kW converter designed in Chapter 5 has been carried out by reusing the very same setup and control infrastructure adopted for the 30 kW prototype (Section 6.4). In particular, the CUT is driven in open-loop voltage mode (carrier-based SVM in the dq frame), while the loading inverter operates as a closed-loop current source synchronized via PLL and commanded through CAN, as in Fig. 6.8 and Fig. 6.9. The interconnection includes the same Δ -Y transformer used for the 30 kW campaign, which guarantees galvanic isolation and effective suppression of circulating common-mode currents. Fig. 6.15 presents the new setup with the 150 kW CUT.



(a)



(b)

Fig. 6.13 Measured voltage and current waveforms from the CUT during the efficiency-mapping procedure at (a) $\varphi = 0^\circ$ and (b) $\varphi = 20^\circ$.

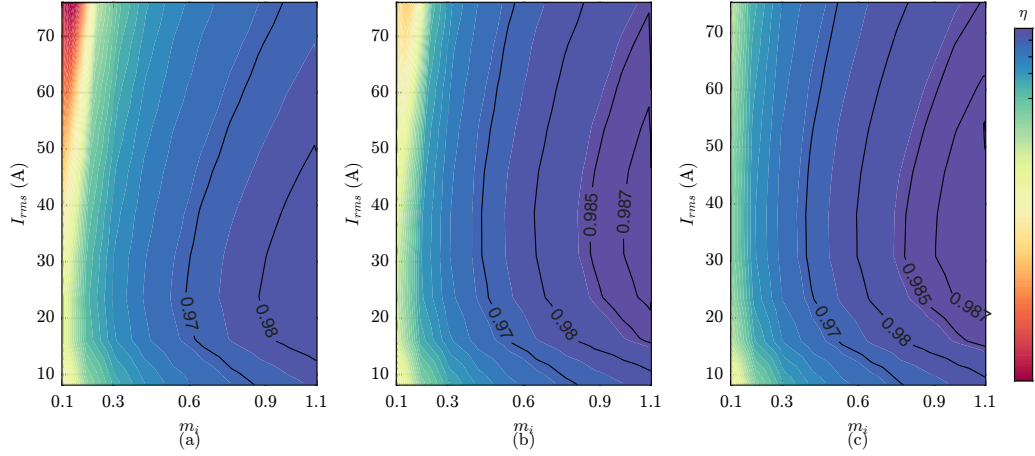


Fig. 6.14 Efficiency mapping of the 30 kW CUT at $V_{in} = 400$ V under varying modulation index and output current. (a) Apparent efficiency including losses of the test-bench LCL filter and connecting cables (voltage measured across filter capacitors). (b) Partially compensated efficiency: same measurement as (a), but with I^2R losses of the filter inductors and cables analytically subtracted. (c) True CUT-only efficiency, measured directly at the converter output terminals, excluding test-bench-related losses.

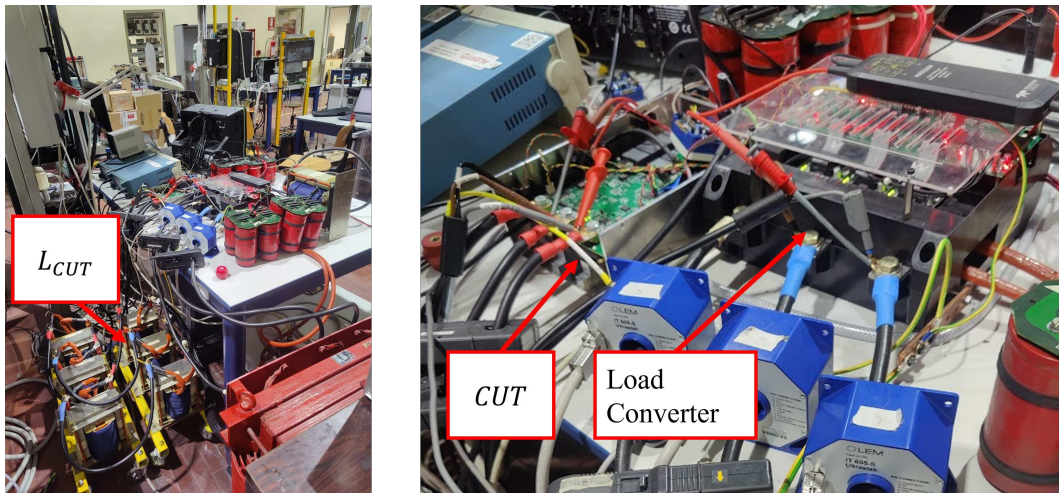


Fig. 6.15 Overview of the experimental setup for the B2B testing of a 150 kW DC/AC converter.

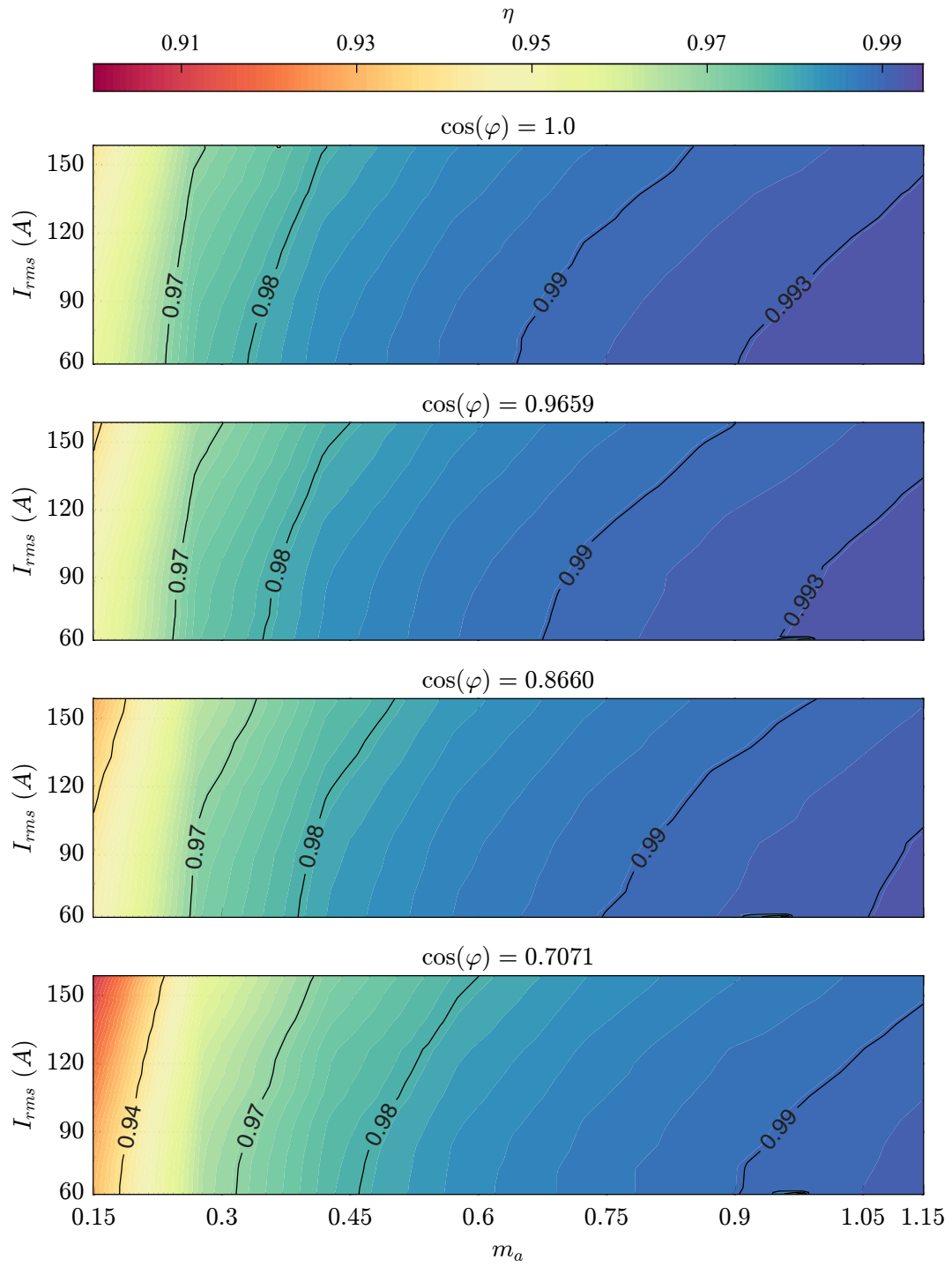


Fig. 6.16 Efficiency mapping of the designed DC/AC 150 kW converter at different power factors.

6.5.1 Efficiency mapping results

Figure 6.16 reports the efficiency maps grouped by $\cos \phi$. The qualitative trends mirror those observed on the 30 kW prototype: efficiency increases with current and M , and gently degrades at light load where switching and auxiliary losses dominate. The dependence on power factor is modest across most of the envelope. No instability or synchronization issues were observed, confirming that the transformer-based common-mode rejection removes the need for carrier synchronization or shared controllers.

6.6 Summary

This chapter presented a novel B2B testing methodology for comprehensive power converter characterization. The key contributions include:

- Development of a B2B configuration with independent control units communicating via CAN bus
- Integration of a Δ/Y transformer for complete common-mode current suppression
- Experimental validation of common-mode mitigation techniques showing effective circulating current reduction
- Automated efficiency mapping procedure enabling systematic characterization across the entire operating region of the converter
- Successful application to both 30 kW GaN and 150 kW SiC converters, demonstrating platform versatility

The proposed approach eliminates the need for shared control hardware or firmware synchronization while enabling full-power testing with minimal external power supply requirements. The efficiency maps obtained provide essential data for powertrain modeling and converter optimization, validating the methodology's effectiveness for comprehensive power converter validation.

Validation of the DC/DC and DC/AC conversion system

Chapter 7

Testing of the integrated DC/DC and DC/AC power conversion system

7.1 Introduction

This chapter details the validation of the integrated control and communication system governing the coordinated operation between the DC/DC converter and the three-phase inverter. The joint operation of these two converters represents the final step of the powertrain implementation, demonstrating the power-flow capabilities and real-time coordination between the converters.

In previous chapters, the two converters (DC/DC and DC/AC) were analyzed and validated as standalone units, operated independently. Here, the focus shifts to their coordinated operation in a multi-converter configuration, where they together realize the complete powertrain. To streamline development and reduce complexity, the validation is carried out on a simplified configuration composed of a single DC/DC converter and a DC/AC inverter, which nonetheless exhibits the same core challenges as the final system with two parallel DC/DC stages.

7.2 System Overview and Control Partitioning

The complete powertrain architecture consists of two DC/DC converters and one DC/AC inverter sharing a common DC-link. In this final configuration, the DC-link

voltage must be regulated by a single outer control loop, while the two DC/DC stages share the required current contribution according to a current-sharing law. For the work presented in this chapter, a simplified configuration with one DC/DC and one DC/AC converter is used for development and experimental validation, preserving all the key control and communication aspects of the final system.

The control architecture is distributed across two independent microcontroller-based platforms, one dedicated to the DC/DC converter and one to the inverter. Each control board executes its own firmware based on interrupt-driven routines, while low-rate coordination tasks and state management are handled through periodic communication events.

The DC/DC controller operates with a control-cycle period of $T_{\text{DCDC}} = 10 \mu\text{s}$ (corresponding to a switching frequency of 100 kHz) and is responsible for:

- differential current-balancing loops for the DC/DC branches,
- DC-link midpoint (capacitor) voltage balancing,
- bidirectional input-current regulation to impose the desired current on the common DC-link,
- local state machine, protection logic, and fault handling.

The inverter controller runs at a lower control frequency, with a control period $T_{\text{AC}} = 50 \mu\text{s}$ (20 kHz switching frequency). Its main tasks are:

- regulation of the DC-link voltage through a PI controller with feed-forward,
- generation of the feed-forward DC current reference i_{dc}^* transmitted to the DC/DC converter,
- control of the three-phase load (e.g. motor or RL load),
- synchronization and communication with the DC/DC unit,
- system-level state management and coordination of protections.

The resulting control structure is a cascaded voltage–current system, where the inverter behaves as the master node regulating the DC-link voltage, while the DC/DC acts as a current-controlled peripheral enforcing the required power flow. A simplified representation of the control partitioning is shown in Fig. 7.1.

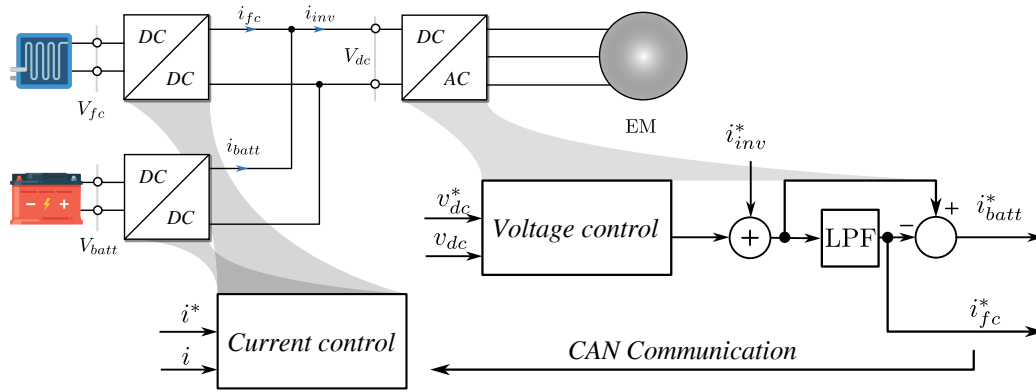


Fig. 7.1 Control partitioning between the inverter (outer DC-link voltage control and load control) and the DC/DC converter (inner current and balancing control).

7.2.1 DC-link Voltage Control and Feed-Forward Term

The DC-link voltage controller is implemented in the inverter microcontroller and operates as the outer loop of the cascaded structure. A PI regulator is used, enhanced with a feed-forward term to improve the dynamic performance, especially during load steps. The control law can be represented as:

$$i_{dc}^* = i_{ff} + i_{PI},$$

where i_{ff} is the feed-forward term derived from the estimated instantaneous power processed by the inverter, and i_{PI} is the corrective term generated by the PI regulator acting on the DC-link voltage error.

The feed-forward contribution is computed from the measured phase currents and the reference phase voltages imposed by the inverter, as sketched in Fig. 7.2. The method is independent of the specific load-control strategy: whether the inverter operates with motor-control algorithms (e.g. FOC, DFVC) or with an open-loop voltage reference for a passive RL load, the necessary quantities (measured currents and average reference voltages) are always available.

In the final configuration with two DC/DC units, a current-sharing law would distribute the total current reference i_{dc}^* between the two converters. In the simplified configuration used here, the full current reference is assigned to the single DC/DC stage. The current reference is then translated to the DC/DC input side by using the input–output voltage ratio and assuming approximate power conservation (ne-

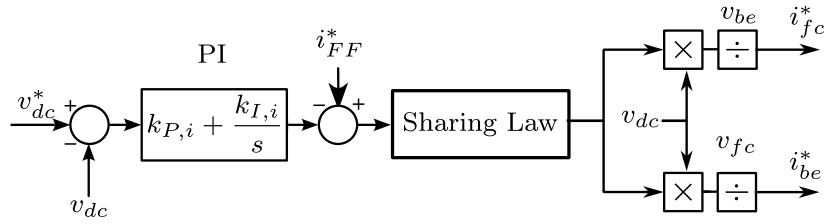


Fig. 7.2 Schematic representation of the DC-link voltage control loop with feed-forward term based on inverter power estimation.

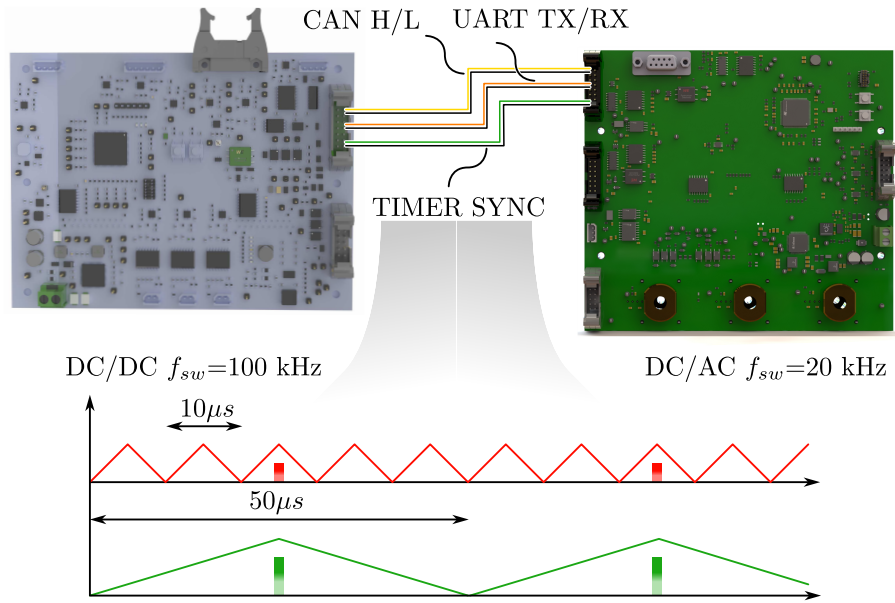


Fig. 7.3 Communication architecture between DC/DC and DC/AC converters: structured links (CAN, UART) and hardware-level synchronization/safety signals.

glecting converter losses). Any residual error introduced by this approximation is compensated by the integral action of the PI controller in the outer loop.

7.3 Communication Architecture

The coordinated operation of the DC/DC and DC/AC converters relies on a multi-layer communication infrastructure, combining structured digital protocols with dedicated hardware-level signals. An overview of the communication links is shown in Fig. 7.3.

Three main layers are employed:

1. **FDCAN bus:** structured, event-based communication for commands, status, and faults.
2. **High-speed UART:** continuous feed-forward link for analog control variables (e.g. i_{dc}^*).
3. **Hardware synchronization and safety signals:** timer/clock synchronization, PWM carrier alignment, and emergency shutdown.

7.3.1 FDCAN Protocol

The FDCAN link operates at 1 kHz, triggered within the TIM6 interrupt of both controllers. It provides asynchronous coordination through a deterministic set of message types:

- **Command frame:** transmitted by the inverter controller (DC/AC) and containing flags such as START, ENABLE, and RESET. These commands drive the state-machine transitions on both converters.
- **Status frame:** transmitted by the DC/DC controller, including state identifiers and selected diagnostic quantities (e.g. measured voltages and currents).
- **Error frame:** transmitted by the DC/DC controller to propagate the fault vector and protective conditions in real time.

Each frame is packed into a fixed 8-byte payload with predefined bitfields, allowing consistent decoding on both boards and straightforward extensibility. Fault-related messages are assigned higher priority and can be transmitted immediately outside the 1 kHz schedule when a critical condition is detected, ensuring rapid reaction of the overall system.

7.3.2 UART/DMA Feed-Forward Link

While the CAN bus handles discrete coordination events at millisecond scale, the instantaneous current reference i_{dc}^* generated by the inverter must be transferred

to the DC/DC converter with much lower latency. For this purpose, a dedicated UART-based link is implemented.

The UART communication operates at a baud rate of 4.5 Mbit/s and is supported by DMA on both sides. On the inverter, the UART DMA buffer is rearmed within the HRTIM interrupt, tightly synchronized with the PWM cycle to minimize latency and jitter. The transmitted data structure includes:

- the DC current reference i_{dc}^* ,
- the measured input/battery voltage v_{in} of the DC/DC converter.

On the DC/DC side, the received data are latched and used at each control cycle to update the current controller reference before duty-cycle computation.

To improve robustness, the standard UART interface is augmented with an additional synchronization line (SYNC), used to realign the communication in case of lost or corrupted frames. All UART-related signals (RX, TX, SYNC) are transmitted over differential lines to enhance immunity to electromagnetic noise in the power electronics environment.

7.3.3 Hardware-Level Synchronization and Safety Signals

In addition to the structured digital links, several low-level hardware signals are used for synchronization and protection:

- **CLK**: a high-frequency clock (8 MHz) generated by the inverter MCU and distributed to the DC/DC control board over a differential line. This clock provides a common time base, ensuring that both MCUs discretize time consistently.
- **PWM_SYNC**: a pulse-type synchronization signal, generated by the inverter MCU, used to align the PWM carrier counters of the DC/DC converter to those of the inverter. At each rising edge of PWM_SYNC, the DC/DC PWM counters are reset to a predefined value, keeping the triangular carriers phase-locked (see Fig. 7.3).
- **EMERGENCY**: a hardware safety loop that must be continuously closed. If the loop is opened—either by one of the converters or by an external safety

device—both MCUs immediately drive their converters to a safe state by disabling the PWM outputs.

- **FAULT:** a dedicated fault line from the DC/DC to the DC/AC converter, indicating that the DC/DC stage has entered a fault or shutdown state. In the full system with two DC/DC converters, this line allows the DC/AC to reconfigure the current-sharing law when one of the converters is unavailable.

Special care is taken to define safe behavior in case of loss of these signals:

- **Loss of CLK:** if the DC/DC controller detects loss of the external clock, it automatically switches to its local oscillator and forces the converter into a safe state, avoiding unsynchronized operation.
- **Loss of PWM_SYNC:**
 - if no synchronization has ever occurred since power-up, the DC/DC remains in its initial state and does not enable the power stage;
 - if at least one valid synchronization event has occurred and both MCUs still share the same clock source, the system may continue operating without a PWM_SYNC pulse every period, as no significant drift is introduced.

These measures, combined with the differential transmission of synchronization and UART signals, ensure high robustness of the data link in a harsh electromagnetic environment.

7.4 Control Timing and Synchronization

Deterministic timing is achieved through the use of the HRTIM peripheral as master scheduler on both MCUs. All critical operations—ADC sampling, control-loop execution, PWM updates, UART buffer refresh, and protection checks—are executed within fixed interrupt windows tied to the PWM carrier.

The typical execution sequence on each converter is:

1. End-of-conversion of the ADC triggers the HRTIM interrupt.

2. Control loops (DC-link voltage, DC/DC current, balancing) are executed using the latest measurements.
3. PWM preload registers are updated with the new duty cycles.
4. UART DMA buffers are rearmed and the new reference/telemetry frame is transmitted (or received) for the next cycle.

Since the DC/DC control loop runs five times faster than the inverter loop, the data exchange mechanism is logically anchored to the slower inverter task. At each inverter control step, the DC/DC sends its latest measured input voltage and receives an updated current reference. This strategy matches the natural hierarchy of the cascaded controls: the DC-link voltage loop is slower and external, while the DC/DC current loop is inner and faster.

7.5 State Machines and Protection Logic

Both control boards implement consistent finite-state machines (FSMs) to manage startup, coordination, and protection. The sequence of states is:

ERROR → OFFSET → READY → PRECHARGE → WAIT → RUN.

- **OFFSET:** ADC offset calibration and basic sensor checks.
- **READY:** power-up completed, communication links verified, and no active faults.
- **PRECHARGE:** controlled charging of the DC-link via the DC/DC converter at reduced duty cycle, up to the target DC-link voltage.
- **WAIT:** synchronization phase, waiting for the inverter START command and PWM synchronization.
- **RUN:** steady-state operation under coordinated voltage–current control.
- **ERROR:** entered upon any critical protection trigger, disabling PWM outputs and notifying the peer controller.

State transitions are primarily driven by FDCAN command and status frames, while safety-critical events (over-current, over-voltage, communication loss) can also trigger immediate transitions to ERROR through hardware shutdown signals or high-priority error frames. Timeouts are monitored on both sides to detect loss of communication; in such cases, both converters immediately transition to ERROR and assert the hardware emergency loop.

7.6 Experimental Validation

To validate the stability and robustness of the integrated system, a series of tests were performed on the simplified DC/DC + DC/AC configuration. The purpose of these experiments is twofold:

- validate the *global* DC-link voltage regulation obtained through the coordinated (distributed) control implemented on two independent MCUs, where the inverter executes the outer voltage loop and the DC/DC converter enforces the inner current regulation;
- verify the correct operation and fault tolerance of the *multi-layer* communication and synchronization platform (UART + FDCAN + hardware-level signals), including behavior under degraded or missing links.

In addition to nominal operation, the validation campaign explicitly includes dynamic load variations, input-voltage transients, and intentionally injected perturbations to stress both the control hierarchy and the data-link infrastructure. The overall objective is to confirm that the two-level controller maintains the DC-link voltage within the specified limits while ensuring stable dynamics and predictable protection behavior.

7.6.1 Experimental Setup

The experimental setup for the integrated tests is illustrated in Figs. 7.4 and 7.5. The DC/DC converter is supplied by a programmable bidirectional DC source, capable of covering the full input-voltage range and imposing the desired input voltage. The inverter is connected to a passive three-phase RL load. The AC-side voltage

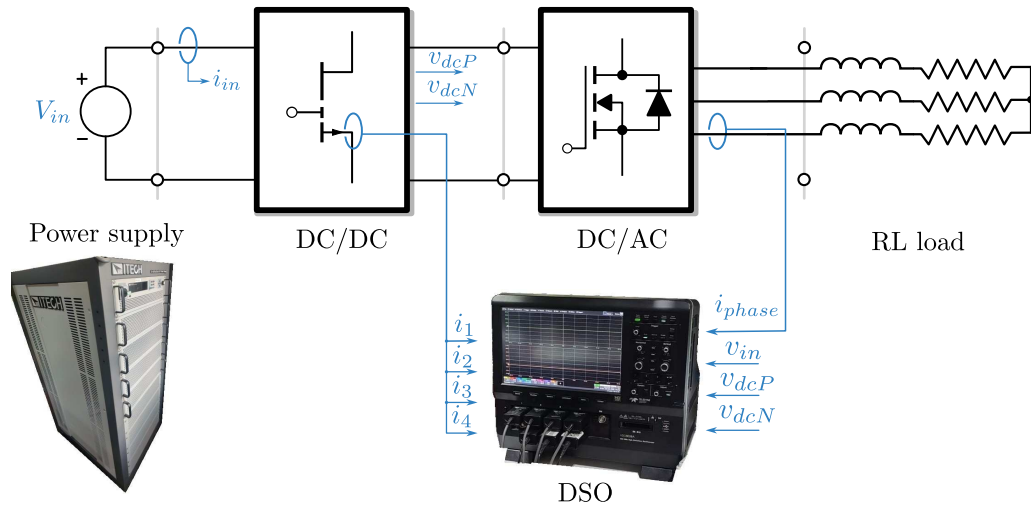


Fig. 7.4 Schematic of the integrated DC/DC + DC/AC experimental setup.

amplitude is varied in open-loop to adjust the operating point and the processed power.

System set-points and start/stop commands are issued via CAN from a supervisory PC. The same PC also hosts two real-time debug environments connected to the MCUs, which are required to verify internal state-machine transitions, control variables, and protection flags during the tests.

Measurement and verification are carried out using an 8-channel oscilloscope to acquire key analog quantities. The monitoring is focused on the DC/DC-side physical variables, namely:

- input voltage v_{in} ,
- upper and lower DC-link voltages $v_{DC,H}$ and $v_{DC,L}$,
- DC/DC branch currents i_1 , i_2 (and, when available, additional branch currents),

together with the phase current of the inverter feeding the RL load (one phase is sufficient to validate synchronization and load steps). The measurement points are indicated in Fig. 7.4. Besides the electrical waveforms, the experimental activity verifies the correct behavior of the four communication layers implemented between the MCUs:

- PWM synchronization between the two converters (carrier alignment),

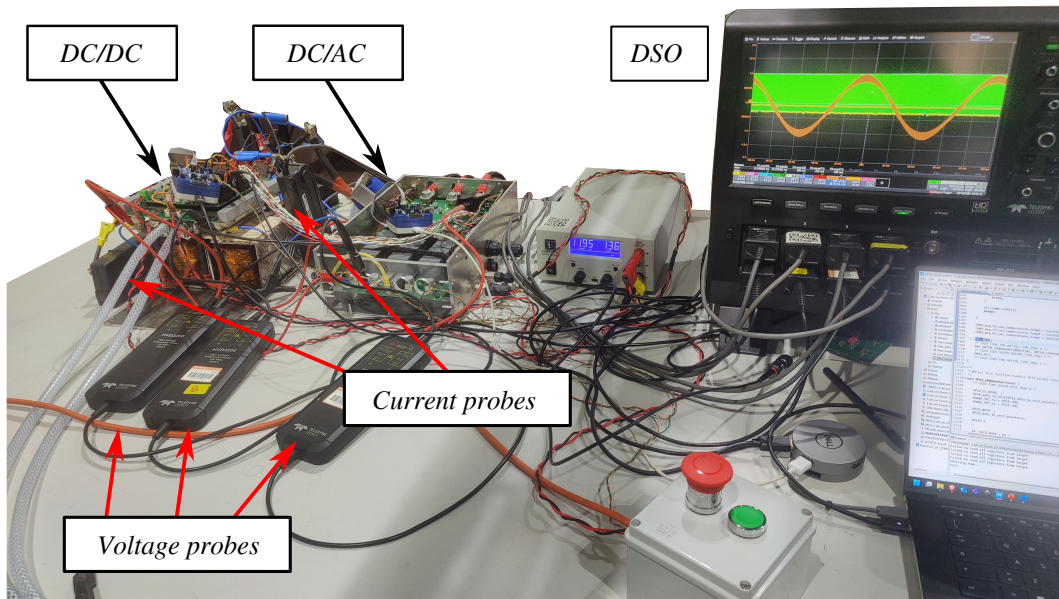


Fig. 7.5 Laboratory implementation of the DC/DC + DC/AC experimental setup.

- high-speed exchange of operational variables (input voltage and current reference),
- asynchronous UART communication robustness (including frame realignment through the additional SYNC signal),
- fault signaling and emergency handling (hardware loop and high-priority fault indications).

These checks are essential because the DC/DC control task runs at a frequency five times higher than the inverter task; therefore, the data exchange must be coherent, deterministic, and anchored to the slower (outer-loop) controller to avoid temporal misalignment and undesired oscillations. In practice, the data-transfer mechanism is synchronized to the inverter control step (20 kHz), which naturally reflects the hierarchy of the cascaded voltage–current regulation.

7.6.2 Dynamic DC-link Voltage Test

Figure 7.6 shows a representative test sequence containing multiple dynamic events, including start-up, DC-link voltage ramping, and load injection/removal. In the upper traces, the following voltages are displayed:

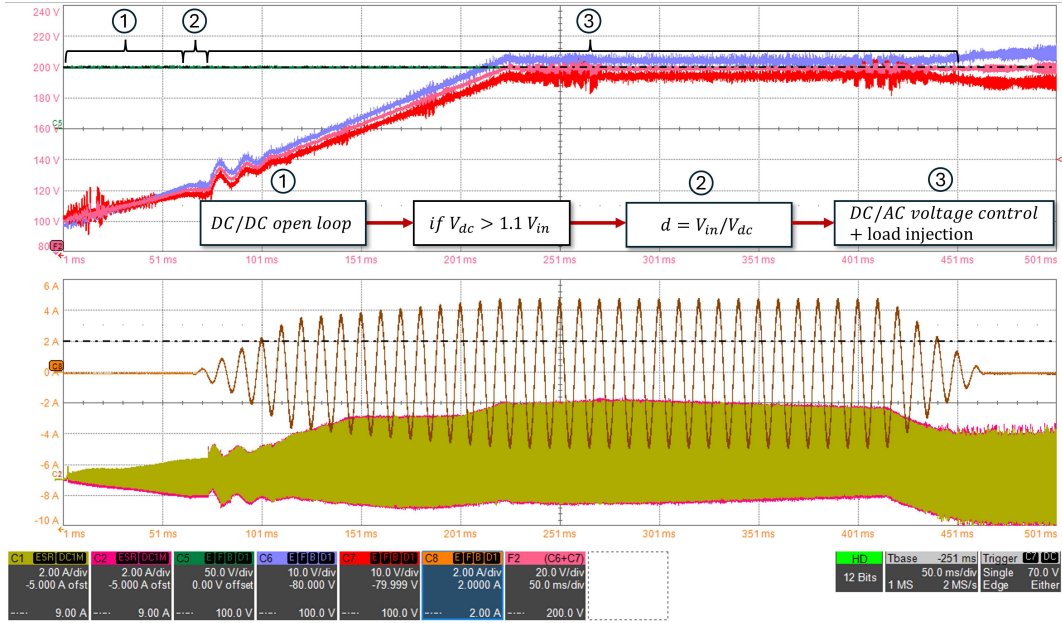


Fig. 7.6 DC-link charging and load injection: dynamic response of the integrated DC/DC + DC/AC system.

- input voltage v_{in} (channel C5),
- upper and lower DC-link voltages $v_{DC,H}$ and $v_{DC,L}$ (channels C6 and C7),
- reconstructed DC-link voltage $v_{DC} = v_{DC,H} + v_{DC,L}$ (math trace).

At the beginning of the plot, the DC/DC converter is started from an input voltage $v_{in} = 100$ V. A ramp is applied to the DC-link voltage reference, bringing v_{DC} from 100 V to 200 V. During the ramp, $v_{DC,H}$ and $v_{DC,L}$ exhibit a slight mismatch, caused by parasitic inductive couplings inside the power stage and by the finite bandwidth of the semi-bus balancing loop. After the ramp ends and current flows through the load, the balancing loop progressively reduces the mismatch. When the load current is removed, the parasitic effects become dominant and a slow divergence of the two semi-bus voltages can be observed again. This behavior is expected: the system's capability to actively rebalance the two capacitor voltages is improved when a sufficient DC-link current is present.

In the bottom traces, the DC/DC branch currents are reported (C1 and C2), while the middle trace shows the inverter phase current feeding the RL load (C8). Although the DC/DC currents may appear noisy at first glance, the observed ripple is the normal triangular switching ripple superimposed on the average current. After

load connection, a small oscillation can be observed on the DC-link voltage ramp. This effect is mainly attributed to dead-time nonlinearity in the DC/DC power stage, i.e., to an effective voltage drop that depends on the current sign. Importantly, the integrated system remains controlled and stable throughout the full transient sequence, demonstrating:

- correct interaction between the outer DC-link voltage loop (inverter) and the inner current loop (DC/DC),
- coherence of the fast feed-forward current reference transmission (UART) during dynamic events,
- stable operation under load steps and during voltage reference ramps.

7.6.3 Steady-State Operation

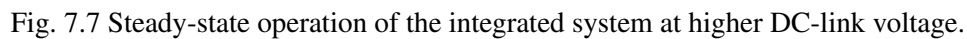
Figure 7.7 reports a steady-state operating point at higher DC-link voltage. The channel assignments are:

- DC/DC branch currents on channels C1 and C2,
- additional DC/DC currents on C3 and C4,
- input voltage v_{in} on C5,
- upper and lower DC-link voltages $v_{DC,top}$ and $v_{DC,bot}$ on C6 and C7,
- inverter phase-C current on C8.

The math traces report:

- DC/DC input current i_{in} reconstructed from branch currents (F1),
- total DC-link voltage $v_{DC} = v_{DC,H} + v_{DC,L}$ (F2),
- difference $v_{DC,H} - v_{DC,L}$ (F3).

The system operates in steady state with stable behavior and no visible oscillations. The DC-link voltage remains constant at its reference value, while the two



This aspect is further evidenced in Fig. 7.8, where the differential currents are explicitly shown as math traces:

- The differential currents oscillate around zero with negligible mean value, confirming the proper operation of the current-balancing loops and the effective mitigation of DC-link imbalance even at increased voltage and load levels.

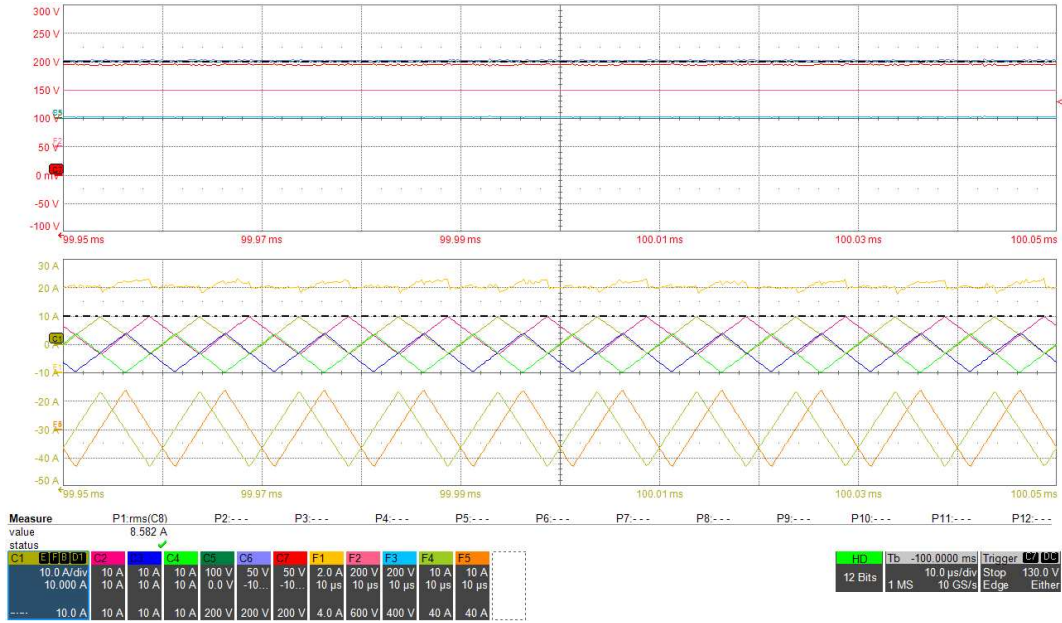


Fig. 7.8 Detail of steady-state operation: differential branch currents of the DC/DC converter (math traces F4 and F5).

7.7 Summary

This chapter presented the integrated control and communication architecture for the coordinated operation of the DC/DC and DC/AC converters. The key contributions include:

- Development of a distributed control architecture in which the inverter regulates the DC-link voltage and the DC/DC converter enforces the corresponding current reference
- Implementation of a multi-layer communication platform combining FDCAN, high-speed UART/DMA, and dedicated hardware synchronization and safety signals
- Definition of deterministic control timing, synchronized PWM operation, and coordinated state-machine and protection logic across two independent microcontrollers
- Experimental validation of the integrated system during DC-link voltage ramps, load transients, and steady-state operation

- Verification of stable DC-link voltage regulation, effective split-capacitor voltage balancing, and accurate differential-current balancing among the DC/DC branches

The experimental results confirm that the proposed distributed architecture enables stable and coordinated operation of the complete power conversion system without requiring a shared control platform. The adopted communication and synchronization strategy provides the deterministic exchange of control variables required by the cascaded voltage–current regulation, while preserving modularity and independent converter control. These results validate the proposed architecture as a suitable basis for the final powertrain configuration with two parallel DC/DC stages and one traction inverter.

Chapter 8

Conclusions and Outlook

This thesis has presented the complete design, modeling, prototyping, and testing of two key power electronic systems for fuel cell electric vehicles: a 75 kW GaN-based DC/DC converter and a 150 kW SiC-based DC/AC traction inverter. The research demonstrated that the integration of wide-bandgap semiconductors enables substantial gains in efficiency, power density, and thermal performance compared to traditional silicon-based solutions.

The GaN-based DC/DC converter was designed to interface the fuel cell stack with the high-voltage bus. Employing a three-level interleaved topology and switching at 100 kHz, the converter leveraged the low switching losses of GaN HEMTs to achieve high efficiency, up to 98% depending on load, and reduced current ripple.

In parallel, a 150 kW SiC traction inverter was developed for the FCEV drive system. The inverter achieved a wide DC input range between 100 V and 800 V, delivering up to 150 A_{rms} per phase and reaching a measured peak efficiency above 98%. With a volumetric power density exceeding 40 kW/L, the inverter fulfilled the compactness and performance objectives required for automotive traction applications. Its modular three-layer architecture—separating the power stage, driver, and control boards—proved highly effective in minimizing parasitic inductances and electromagnetic interference, while improving signal integrity and simplifying assembly. The DC-link capacitor bank was optimized through combined analytical and simulation methods, resulting in a 150 μ F configuration that maintained the voltage ripple below 3% at full load. These results confirmed the robustness of the inverter design and the benefits of SiC technology in high-power vehicle drives.

Both converters were experimentally verified through extensive laboratory testing. The GaN converter exhibited reliable operation and excellent transient response, while the SiC inverter was successfully operated at the full 800 V DC bus and up to 220 A peak output, showing stable behavior and negligible waveform distortion. To characterize efficiency in realistic operating conditions, a novel back-to-back (B2B) testing methodology was implemented, allowing two converters to exchange power through an isolated coupling network. This setup enabled full-power efficiency mapping with minimal grid power draw, providing a practical and cost-effective approach for converter validation at high power levels.

The technological and methodological advances achieved in this work highlight the potential of GaN and SiC devices in enabling more efficient and compact power conversion systems. The three-level interleaved GaN converter demonstrates how digital control can effectively manage phase balancing and current ripple, while the three-layer inverter design offers a blueprint for low-parasitic, high-frequency layouts. Together, these contributions represent a meaningful step forward in the development of high-performance power electronics for FCEVs.

Looking ahead, further research should focus on the full system-level integration of the GaN DC/DC converter and the SiC inverter into a complete fuel cell drivetrain. Such testing will allow validation of coordinated control strategies and the dynamic interaction between converters under realistic power flow conditions. Additionally, scaling the GaN converter to its full 75 kW rating will require refinement of the cooling system and control algorithms to ensure stability and efficiency across the full operating range. Future work should also explore advanced energy management strategies, enhanced diagnostic capabilities, and compliance with automotive reliability standards. As wide-bandgap device technologies continue to evolve, the adoption of next-generation SiC and GaN components with higher voltage ratings and lower losses could further improve system performance, potentially enabling inverter efficiencies approaching 99% and even more compact converter architectures.

In conclusion, this research has advanced the state of the art in high-power converters for fuel cell vehicles by demonstrating that GaN- and SiC-based technologies can deliver superior efficiency, compactness, and reliability. The methodologies and results established in this work form a solid foundation for future development and integration, contributing to the realization of more sustainable and efficient electric propulsion systems.

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