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***Abstract*— As technology scales to advanced FinFET nodes, digital circuits become increasingly susceptible to radiation-induced soft errors, creating a major reliability concern for safety-critical and space applications. Conventional hardening often requires extensive circuit-level vulnerability analysis, leading to substantial design time and effort. This paper presents a radiation-hardened (RH) standard cell library for 7 nm FinFET technology based on the ASAP7 PDK, aiming to improve radiation resilience while limiting both overhead and design time. The library is developed through transistor-level fault injection and 3D layout-aware particle-strike simulation to derive customized hardening strategies for individual cells. Experimental results show that the RH cells achieve significantly higher threshold LET and shorter error duration than standard counterparts. Case studies on a D flip-flop and a C432 benchmark further demonstrate significantly reduced SEE cross-section with modest area, power, and delay overheads, confirming a practical and scalable approach to SEE-resilient design in advanced FinFET circuits.**

***Index Terms*—7 nm FinFET, Radiation-Hardened Standard Cell Library, Single Event Effects**

I. Introduction

FinFET technology has become a key enabler of high-performance digital systems due to its low leakage current, strong electrostatic control, and improved short-channel behavior over planar CMOS. At advanced nodes such as 7 nm, however, aggressive scaling also increases vulnerability to radiation, as supply voltage and node capacitance decrease, the critical charge required to disturb a logic state is also reduced. Consequently, single-event effects (SEEs) remain a major challenge in advanced FinFET technologies, especially for space, avionics, high-energy physics, and other radiation-intensive applications.

The manifestation of SEE-induced soft errors depends on circuit type. In combinational logic, particle strikes typically produce single-event transients (SETs), whereas in sequential elements they may cause single-event upsets (SEUs). These effects are closely coupled: an SET may propagate through logic and be captured by a storage element, while an SEU may be latched by downstream units and continue to propagate. Therefore, not only the occurrence of an error but also its duration is critical. As clock frequencies rise and timing margins shrink, even short transients may be captured, making pulse-width sensitivity increasingly important in deeply scaled technologies.

This work was partially supported by the TIRAMISU project under the EU Grant#101169378 — HORIZON-MSCA-2023-DN-01, and by the PUMA project, under grant agreement No 101189992.

Various radiation-hardening-by-design (RHBD) techniques, such as Triple modular replicatation, guard-ring isolation, and transistor-level optimization, have been reported. Although effective, most prior work focuses on device-level studies or circuit-specific hardening of selected cells and benchmark designs. To avoid excessive overhead, these methods often require repeated vulnerability analysis and manual redesign, which increases design time and limits reusability and scalability in large synthesized systems.

These limitations motivate the development of RH standard cell libraries. By embedding resilience directly into basic logic primitives, an RH library enables radiation tolerance to be integrated into conventional synthesis, placement, routing, and timing sign-off flows without repeated circuit-specific analysis. Compared with conventional hardening approaches, this library-based strategy can significantly shorten design time while maintaining compatibility with existing design flows. While prior studies have demonstrated the feasibility of RH standard cell libraries in bulk CMOS technologies, corresponding library-level work for advanced FinFET nodes remains limited in the open literature.

To address this gap, this paper presents an RH standard cell library developed for the ASAP7 PDK [1]. Through systematic evaluation and hardening of representative cells, a reusable library is established that can directly replace nominal cells in the circuits. To demonstrate its applicability to both combinational and sequential logic, as well as its scalability to different circuit sizes, two case studies are considered: an ISCAS'85 benchmark circuit, C432 [2], and a D flip-flop (DFF). The results show that the RH library reduces both the occurrence and the transient duration, thereby improving resistance to error generation and capture with only modest area, power, and delay overheads.

The rest of this paper is organized as follows. Section II reviews previous work on RH cell libraries. Section III describes the development methodology and representative cells of the proposed 7 nm library. Section IV presents the experimental results, and Section V concludes the paper.

II. State-of-the-Art

Early studies established the feasibility and practical value of RH standard cell libraries, demonstrating that hardened cells could be implemented in commercial bulk CMOS technologies using layout-level techniques without process modifications.

A CERN/LHC-oriented library in a 0.24 μm CMOS process [3] demonstrated the viability of reusable radiation-tolerant cells for demanding applications. Subsequent work advanced this direction by introducing CAD-compatible RHBD methodologies, including ELT- and guard-ring-based design flows that

979-8-3195-1905-4/26/$31.00

preserved compatibility with conventional synthesis and layout processes. These studies also identified the lack of reliable hardened standard cell libraries as a key bottleneck for complex radiation-tolerant systems, and demonstrated hardened-cell generation in 600 nm and 180 nm technologies [4].

At more advanced nodes, the DARE65T platform in 65 nm CMOS provided a more mature example of a reusable hardened library, including both SET-hardened combinational cells and SEU-hardened sequential cells. For FinFET technology, the only related study we found is the 16 nm RH standard cell library reported in [5], which includes a set of RH standard cells but does not report implementation results for larger-scale circuits.

Overall, prior work confirms that library-level RHBD is a practical approach to soft-error mitigation. However, most published RH standard cell libraries target bulk CMOS technologies, while comparable studies for FinFET nodes remain scarce. Moreover, one of the key advantages of RH libraries over conventional hardening approaches—improved design-time efficiency—has not been sufficiently demonstrated in larger-scale circuits. This gap motivates the development of an RH standard cell library for 7 nm FinFET technology and its application to larger-scale circuits.

III. 7-NM RADIATION-HARDENED STANDARD CELL LIBRARY

The development flow of the proposed 7 nm radiation-hardened library consists of two phases: library construction, and circuit implementation and evaluation.

In the first phase, each standard cell undergoes Linear Energy Transfer (LET)-based fault-injection analysis at transistor level to identify sensitive nodes and vulnerable operating conditions by extracting the threshold LET (LET_{th}). Based on these results, customized hardening strategies are applied to construct the hardened cells in the library.

In the second phase, nominal gates in SPICE netlists are directly replaced with their hardened counterparts, eliminating the need for circuit-specific hardening analysis. The resulting unhardened and hardened circuits are then evaluated using HSPICE and a 3D layout-aware, physics-based simulation tool [6], which models ionizing-particle interactions and generates realistic charge-collection pulses. Their effectiveness is quantified through SEE cross-section comparison, confirming the improved radiation resilience of the proposed approach.

A. Radiation hardened library construction

The construction of the RH cell library begins with LET-based fault-injection analysis of logic gates in the ASAP7 PDK to identify sensitive nodes and vulnerable operating conditions. In HSPICE, the injected fault is modeled as a current source based on Messenger's equation (1), where Q_{coll} is the collected charge, $\tau_\alpha\,(1.64 \times 10^{-10}\,\mathrm{s})$ is the charge-collection time constant, $\tau_\beta\,(5 \times 10^{-11}\,\mathrm{s})$ is the ion-track establishment constant, and $L\,(21\,\mathrm{nm})$ is the charge-collection depth. These current sources are injected into every gate node under different input stimuli (e.g., 00, 01, 10, and 11 for a 2-input gate) to cover relevant SEE conditions. For each node, the LET in Eq. (1) is increased in steps of 5 MeV·cm^2/mg to determine the failure threshold, defined as the minimum LET required to generate a transient at the gate output.

$$I(t) = \frac{Q_{\mathrm{coll}}}{\tau_\alpha - \tau_\beta}\left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right) \qquad Q_{\mathrm{coll}} = 10.8 \times L \times LET \tag{1}$$

For each standard cell, hardening was implemented using transistor insertion [7], transistor resizing [8], or a combination of both. In the transistor-insertion approach, a voltage level keeper (VLK), consisting of several transistors connected between sensitive nodes and the power supply or ground, was introduced to reinforce node voltage and suppress radiation-induced perturbations. In the transistor-resizing approach, the dimensions of selected transistors were adjusted to strengthen sensitive nodes and improve their tolerance to collected charge. After evaluating these options for each cell, the final scheme for each cell was selected by considering both the achieved improvement in radiation resilience, as reflected by LET_{th} and error duration, and the overhead introduced by the hardening structures. Once the hardening strategy for a cell was determined, its layout was designed accordingly so that the hardened cells could be integrated into larger circuits and evaluated at the circuit level. Table I compares representative hardened cells with their standard ASAP7 counterparts, reporting the LET_{th} of the most sensitive node and the error duration under an injected fault of $\mathrm{LET} = 77\mathrm{MeV}\cdot\mathrm{cm}^2/\mathrm{mg}$, corresponding to the maximum LET typically encountered at altitudes below 720 km [9]. Representative layouts of the proposed library are shown in Fig. 1.

B. Implementation and evaluation

Once the radiation-hardened library has been developed, circuit implementation can be performed by directly replacing nominal gates with their hardened counterparts. To evaluate radiation resilience under realistic conditions, Rad-Ray is employed as a three-dimensional physics-based Monte Carlo tool. It models ionizing-particle transport through the material stack extracted from the circuit GDSII layout, calculates the deposited energy along each trajectory, and converts it into the corresponding voltage transients. The simulations use an ion spectrum representative of the UCL HIF facility [10], covering species from $^{13}\mathrm{C}^{4+}$ to $^{124}\mathrm{Xe}^{35+}$. For each ion species, 3,000 vertical strikes are simulated at each node, and the resulting transient spectra are injected into the target circuit in HSPICE to evaluate the SEE-induced error rate.

$$\sigma_{\mathrm{SEE}} = \frac{N_{\mathrm{error}}}{N_{\mathrm{strike}}} \cdot A \tag{2}$$

Circuit susceptibility is quantified by the SEE cross-section, defined in (2), where N_{error} is the number of strikes producing observable errors, N_{strike} is the total number of simulated strikes, and A is the effective sensitive area of the circuit, approximated in FinFET designs by the active-layer area. A smaller σ_{SEE} therefore indicates lower soft-error susceptibility. By comparing the σ_{SEE} values of the original and hardened testbenches, the effectiveness of the proposed RH library can be quantitatively verified.

TABLE I: Parameters comparison of standard and hardened cells in the developed library

Cell		Hardening Solution(s)	LET_{th}	Duration of errors (ns)	Number of transistors	Area (μm^2)	Area increase (%)	Power (W)	Delay (ps)
AND2x4	standard cell	VLK	15	0.48	6	0.1458	20.37	6.20E-07	12.36
	hardened cell		30	0.36	8	0.1755		6.36E-07	13.78
AND3x1	standard cell	VLK	15	0.68	8	0.0875	17.26	2.15E-07	9.15
	hardened cell		35	0.52	11	0.1026		2.18E-07	9.94
NOR2x2	standard cell	VLK	20	0.98	4	0.1458	9.26	2.95E-08	4.65
	hardened cell		25	0.56	8	0.1593		1.05E-07	5.39
OR2x2	standard cell	VLK	10	0.44	6	0.0875	29.03	1.58E-07	6.63
	hardened cell		20	0.22	8	0.1129		1.76E-07	7.14
OR4x1	standard cell	VLK & resizing	15	0.36	10	0.1021	39.76	9.79E-08	16.60
	hardened cell		35	0.20	14	0.1427		1.08E-07	20.25
XOR2x1	standard cell	VLK & resizing	10	0.46	10	0.1749	6.23	2.44E-07	10.58
	hardened cell		25	0.30	12	0.1858		2.79E-07	13.02

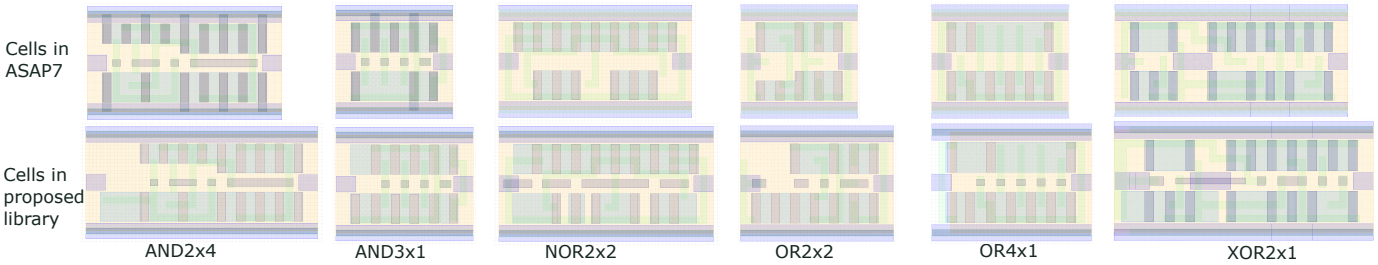


Fig. 1: Representative layouts of the proposed library.

IV. Experimental Results and Analysis

To evaluate the effectiveness of the developed library, testbenches were implemented using the proposed cells and compared with baseline designs. The results show that the library-based implementations exhibit lower σ_{SEE} than designs built with the standard ASAP7 library, while introducing only modest overhead. Two case studies were considered: a D flip-flop (DFF), representing a widely-analyzed sequential logic and enabling comparison with existing RH DFF designs, and the ISCAS'85 benchmark circuit C432, which consists of 160 gates and represents larger-scale combinational logic. The schematic structures of the DFF and C432 are shown in Fig. 2(a) and Fig. 2(b), respectively. In general, the time complexity of modern selective radiation-hardening approaches scales approximately linearly with the number of circuit nodes, making them increasingly time-consuming for larger designs. In a previous circuit-specific hardening study [15], the design process for a 2-input MUX required days of analysis and experiments. In contrast, by using the proposed library, hardened versions of the testbenches were generated within minutes, highlighting the major design-time advantage of the library-based approach for RH circuit design.

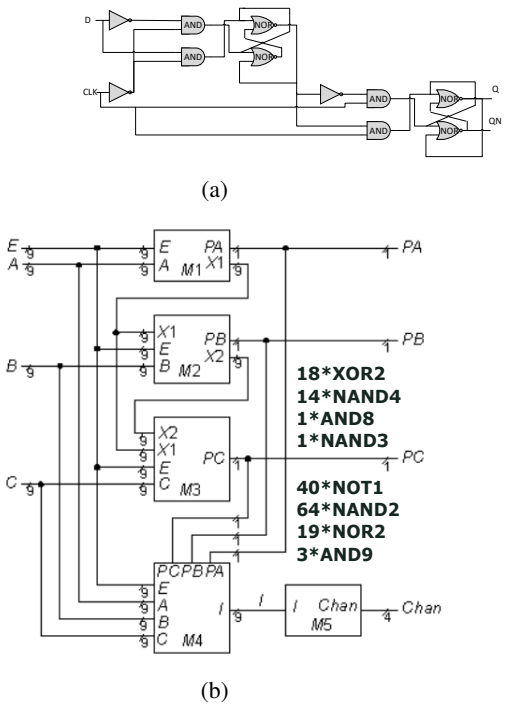


Fig. 2: The gate-level structure of DFF (a) and C432 (b).

To evaluate radiation resilience under particle strikes, a test setup circuit was constructed, as shown in Fig. 3. The testbench was duplicated and driven by identical input stimuli, with one copy serving as the golden reference and the other as the experimental circuit. A Monte Carlo analysis with 3000 particle injections per particle type was performed at each node of the testbench, and the resulting transient pulses were injected into the experimental circuit using HSPICE. A set of XOR gates was used to compare the outputs of the two testbenches; any mismatch indicated that the injected fault had produced a soft error. The resulting SEE cross-sections of the DFF and C432 are shown in Fig. 4(a) and (b), respectively. The hardened implementations significantly reduce the average SEE cross-section compared with the original designs.

To highlight the lightweight nature of the developed library, the overhead of several alternative hardening solutions for the same test circuits was also evaluated. For the DFF, the cost was normalized using the Area–Power–Delay Product (APDP), providing a common basis for comparison because extensive prior work on RH DFFs is available. For the C432 testbench, the area, power, and delay are reported for the ASAP7-based implementation, the design implemented with the proposed library, and the baseline and radiation-hardened

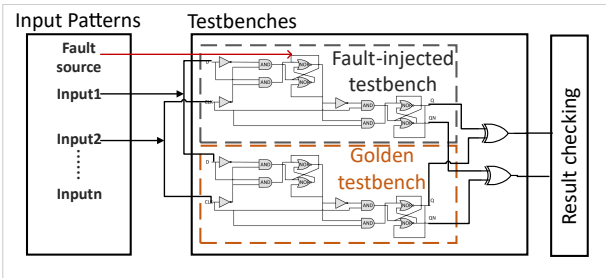
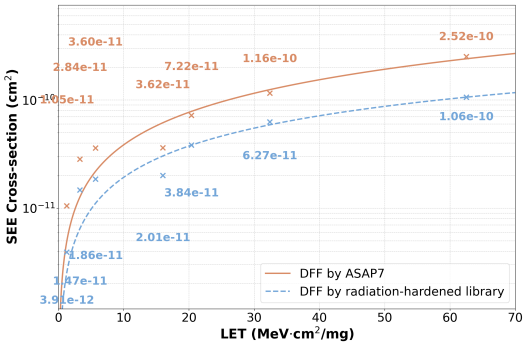
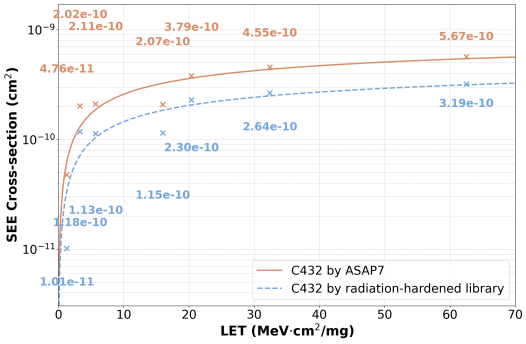


Fig. 3: The developed test setup circuit.



(a)



(b)

Fig. 4: The SEE cross-section comparison of DFF (a) and C432 (b).

versions reported in [14]. Since the results in [14] are given in terms of percentage overhead, only normalized values are presented here. Table II summarizes the normalized overhead comparison for the DFF, while Table III presents the corresponding results for C432.

V. Conclusion

A radiation-hardened standard cell library for 7 nm FinFET technology has been developed and validated through both cell- and circuit-level evaluation. The proposed library improves standard-cell robustness by increasing threshold LET and reducing error duration. Case studies on a D flip-flop and the C432 benchmark show significantly lower SEE cross-section than standard designs with only modest area, power, and delay overhead. In addition, by avoiding repeated circuit-specific hardening analysis, the library can substantially shorten the design time for larger-scale circuits. To the best of our knowledge, this is the first radiation-hardened standard cell library developed for FinFET technology at the 7 nm node.

TABLE II: Comparison of area, power, delay, and APDP normalized to the standard DFF.

Cell	Area	Power	Delay	APDP
Std. DFF	1.00	1.00	1.00	1.00
DAD-FF [11]	2.25	1.69	1.50	6.70
TH-FF [12]	3.45	1.65	1.03	5.86
HPRH-FF [13]	2.33	2.06	0.94	4.53
Proposed DFF	**1.13**	**1.08**	**1.23**	**1.50**

TABLE III: Comparison of area, power, and delay of C432.

Cell	Area (μm^2)	Power (W)	Delay (ps)
C432 by ASAP7	45.79	1.4156E-4	118.58
C432 by proposed library	49.68	1.7132E-4	139.73
Baseline C432 in [14]	100%	100%	100%
Radiation-hardened C432 in [14]	154.8%	170.8%	1.04%

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