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A Novel Node- and Layout-Aware Radiation-Hardened 7 nm D Flip-Flop

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***Abstract*—Technology scaling has increased the vulnerability of sequential logic to radiation-induced single-event upsets (SEUs), motivating radiation-hardened flip-flop designs with low overhead. This paper presents a radiation-hardened D flip-flop (DFF) based on a node- and layout-aware hardening methodology. By selectively reinforcing the most sensitive internal nodes instead of uniformly hardening the entire circuit, the proposed design effectively mitigates SEUs with limited performance penalty. Compared with a standard DFF, the hardened design significantly lifts the SEU resilience while incurs modest cost (area 1.05×, power 1.56×, and delay 1.51×) and achieves a reduced Area–Power–Delay Product (APDP) of 2.47×. When applied in a triple modular redundancy (TMR) system, the proposed DFF reduces the system-level error rate from 0.32% to 0.068% (approximately 21% of the baseline), demonstrating its effectiveness for radiation-tolerant systems.**

***Index Terms*—D-Flip-Flop, SEU, Circuit–layout co-analysis, TMR**

I. Introduction

Modern electronic systems are increasingly deployed in radiation-intensive environments such as outer space, high-altitude avionics, and nuclear instrumentation, where high-energy particles—including heavy ions, protons, and neutrons—can deposit transient charge in semiconductor devices and induce single-event effects (SEEs). Among these effects, single-event transients (SETs) manifest as short-lived voltage or current pulses and may be converted into single-event upsets (SEUs) when captured by clocked storage elements. Technology scaling has further exacerbated SEU susceptibility, as reduced feature sizes, lower supply voltages, and shrinking node capacitances collectively decrease the critical charge Q_{crit} required to upset a storage node. As a result, SEUs have become a critical reliability concern in sequential circuits, since radiation-induced bit flips stored in memory elements or flip-flops can propagate through downstream logic and lead to system-level functional failures.

Within sequential logic, the D flip-flop (DFF) is one of the most basic and vulnerable standard cells, as its internal cross-coupled storage nodes can readily latch incorrect values following a particle strike. Conventional transmission-gate or master–slave DFF architectures offer little intrinsic radiation tolerance, and their resilience further degrades with continued voltage and geometry scaling. To mitigate SEUs, a wide range of radiation-hardened-by-design (RHBD) techniques has been proposed, including spatial redundancy (e.g., Duplication with Comparison (DWC) [1] and Triple Modular Redundancy (TMR) [2], [3]), transistor-level hardening [4], [5], temporal redundancy [6], hardened storage cells such as Dual Interlocked Storage Cells (DICE) [7], [8], and layout-level hardening approaches [9], [10]. Among these, spatial redundancy—particularly TMR—provides strong fault-masking capability and remains widely adopted in safety-critical systems despite its substantial area, power, and delay overheads, owing to its architectural simplicity and robustness.

Although extensive prior work has sought to balance reliability improvement against design overhead, many existing hardened flip-flop designs still incur significant area and power penalties. This inefficiency largely stems from uniform hardening applied at the cell level without fully leveraging node-level sensitivity information, leading to unnecessary protection of relatively robust nodes. Moreover, the correspondence between schematic-level hardening strategies and physical layout attributes is often insufficiently addressed, despite the growing importance of three-dimensional charge collection and particle track effects in nanoscale FinFET technologies. These limitations motivate a more systematic and layout-aware hardening methodology that selectively targets the most vulnerable circuit nodes.

In this paper, we propose a novel radiation-hardened D flip-flop implemented in a 7 nm FinFET technology using

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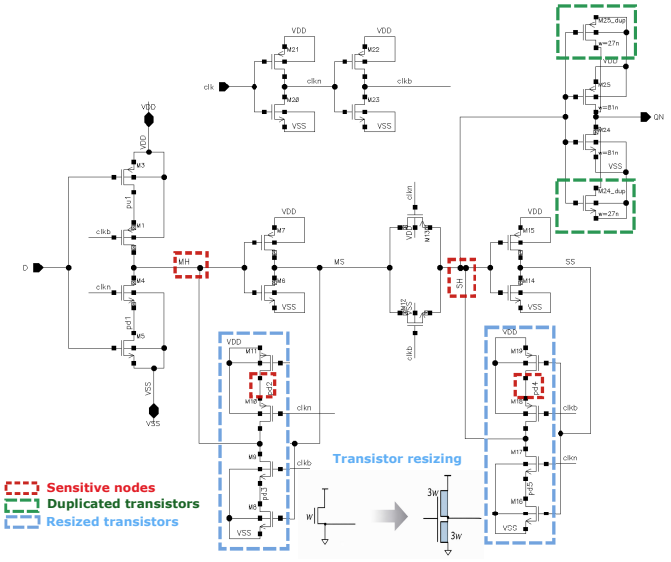


Fig. 1: Schematic structure of the proposed radiation hardened DFF

the ASAP PDK [11]. The proposed methodology systematically evaluates node-level sensitivity through Linear Energy Transfer (LET)-driven fault injection at the schematic level and complements this analysis with three-dimensional, layout-aware particle strike simulations. Based on the extracted upset LET thresholds (LET_{th}), the most vulnerable internal nodes are identified and selectively hardened using targeted techniques, including localized transistor duplication and resizing. By explicitly accounting for both circuit-level sensitivity and physical layout effects, the proposed design enhances radiation resilience while minimizing area, power, and performance penalties.

To validate the effectiveness of the hardened DFF, it is integrated into a triple modular redundancy (TMR) architecture and evaluated under particle fault injection. Simulation results demonstrate that TMR systems constructed with the proposed hardened DFF achieve substantially lower error rates than baseline implementations using unhardened cells, while incurring only modest and acceptable increases in area and delay overhead.

The remainder of this paper is organized as follows. Section II presents the proposed design methodology and hardened DFF structure. Section III discusses experimental results, including fault injection analysis and reliability evaluation in the TMR case study. Section IV concludes the paper.

II. Design of Hardened DFF

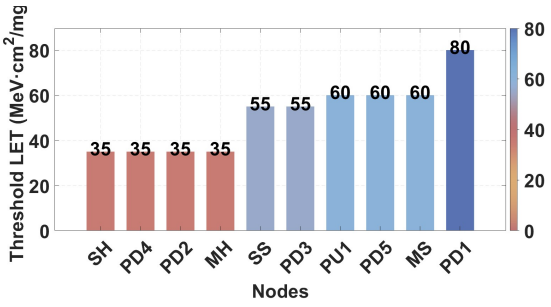
The schematic of the proposed radiation-hardened D flip-flop is shown in Fig. 1. The design flow comprises two complementary and parallel analyses: a static, topology-based node sensitivity assessment and a dynamic, physics-informed evaluation of overall circuit radiation response. The static analysis quantifies the vulnerability of each internal node by determining its LET_{th}, defined as the minimum injected LET required to induce a bit flip at the DFF output. In parallel, the dynamic analysis models the interaction between ionizing particles and the physical layout of the DFF to identify sensitive layout regions and to extract voltage transients generated by particle strikes. These transient waveforms are subsequently used for fault injection to evaluate the SEU error rate of the cell before and after hardening, thereby quantifying the resulting resilience improvement. Guided by the outcomes of both analyses, selective hardening techniques—including targeted transistor duplication and device resizing—are applied to the most vulnerable nodes, with the specific technique chosen based on each node's sensitivity and physical layout location. The effectiveness of the proposed hardening strategy is assessed by comparing SEU error rates before and after hardening.

In static analysis, SETs are modeled by the messenger's equation (1) in HSPICE as current sources injected at each circuit node, where Q_{coll} is the collected charge, τ_α (1.64×10^{-10} s) is the charge-collection time constant, τ_β (5×10^{-11} s) is the ion-track establishment constant, and L (21 nm) is the charge-collection depth. The collected charge Q_{coll} varies with the LET, which ranges from 5 to 80 MeV·cm^2/mg in 5 MeV·cm^2/mg steps, to cover the LET range (less than 77MeV·cm^2/mg) of particles below an altitude of 720 km [12]. The results of the static analysis for the baseline (unhardened) DFF are shown in Fig. 2(a). The distribution of node-level LET_{th} indicates that nodes MH, PD2, PD4, and SH exhibit significantly higher vulnerability than the remaining internal nodes.

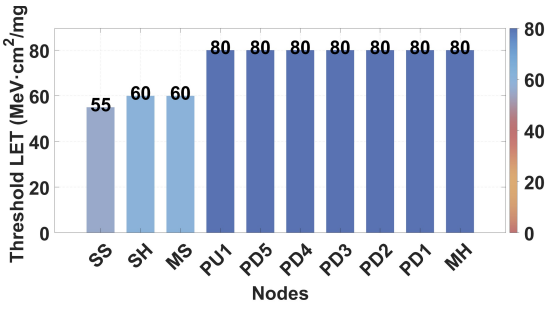
$$I(t) = \frac{Q_{\mathrm{coll}}}{\tau_\alpha - \tau_\beta}\left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right)$$
$$Q_{\mathrm{coll}} = 10.8 \times L \times LET \quad (1)$$

The static analysis assumes a worst-case scenario in which ionizing particles directly strike sensitive regions and deposit their full energy. In contrast, the dynamic analysis provides a more realistic assessment by accounting for the spatial distribution of particle interactions and the fact that not all particle strikes result in significant charge collection at sensitive nodes. The dynamic analysis is performed using a 3-D particle traverse simulation tool [13] and begins with a scan-based simulation in which particle strikes are swept across the DFF layout with a spatial stride of 10 nm. This process generates a radiation-sensitivity heatmap of the cell layout.

Fig. 3 presents the sensitivity heatmap of the baseline DFF under irradiation by $^{124}Xe^{35+}$ ions, selected from the ion spectrum of the UCL Heavy Ion Facility (HIF) [14]. The horizontal and vertical axes represent the physical layout dimensions normalized to the scan resolution, while the color scale encodes the normalized radiation sensitivity. The regions of highest sensitivity in the heatmap spatially correspond to the internal nodes identified as most vulnerable by the static analysis, thereby validating the consistency between schematic-level and layout-aware evaluations.



(a)



(b)

Fig. 2: LET_{th} of internal nodes of (a) the baseline DFF and (b) the proposed radiation hardened DFF.

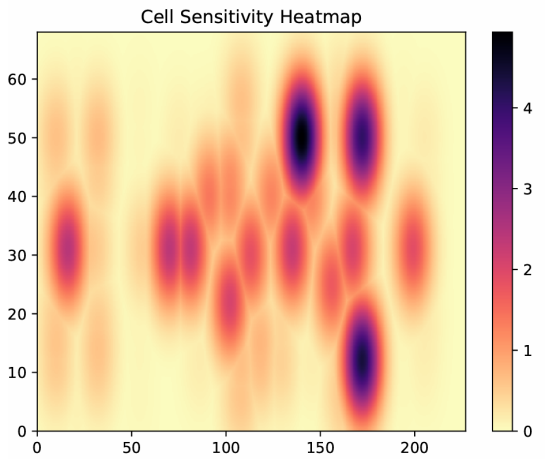
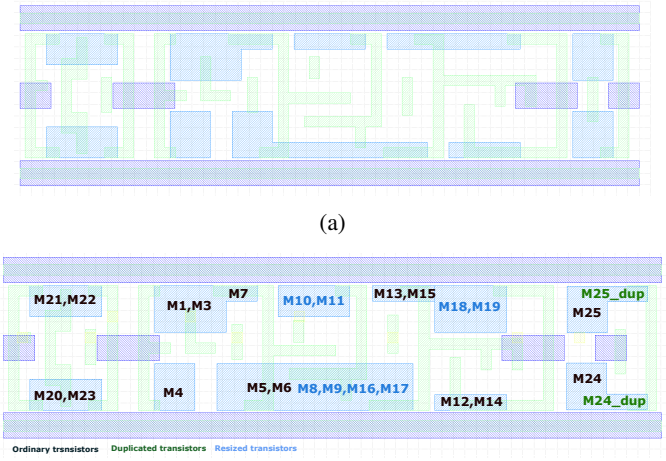


Fig. 3: Sensitivity heatmap of the baseline DFF.

Following the scan-based sensitivity analysis, a Monte Carlo particle interaction simulation was performed using the same 3-D simulation tool. The tool emulates particle traversal through the complete material stack defined by the circuit's GDSII layout, computing the energy deposition along each particle trajectory and converting it into the corresponding voltage transients. For each ion species, 3,000 particle strikes were simulated, generating transient pulses characterized by their amplitude, duration, and waveform shape. Ion species ranging from carbon (C) to xenon (Xe) were analyzed. The resulting transient spectra were subsequently injected into the circuit to evaluate the SEU error rate.



(a)

(b)

Fig. 4: Layout of (a) baseline DFF, and (b) proposed hardened DFF.

Based on the combined static and dynamic analyses, the most sensitive nodes were selectively hardened using different mitigation strategies. Prior work has shown that, in FinFET-based circuits with relatively high drive strength, transistor duplication can achieve radiation hardening comparable to transistor resizing, often with lower layout overhead. This is because, in 7 nm layouts, increasing the number of fins beyond three typically requires additional lateral routing space, resulting in increased area cost. In the proposed 7 nm DFF, however, sufficient internal layout space exists to resize the transistors associated with nodes MH, PD2, and PD4 without increasing the overall cell area. Consequently, transistor resizing was applied to harden these nodes, while transistor duplication was selectively employed to harden node SH, where resizing would incur greater layout overhead.

Through this selective hardening strategy, the proposed design achieves a substantial improvement in SEU resilience while minimizing area overhead. The resulting node-level LET_{th} values of the hardened DFF are shown in Fig. 2(b), where a clear increase in LET_{th} is observed. Fig. 4 compares the layouts of the baseline DFF and the proposed hardened DFF. For clarity, only the Gate Cut, Active, and Metal1 layers are shown. A slight area increase is observed in the hardened design. Table I summarizes the normalized overhead comparison among the proposed DFF, the standard DFF, and other hardened implementations. The results demonstrate that the proposed design not only minimizes area overhead but also achieves a significantly reduced Area–Power–Delay Product (APDP) compare to prior hardened DFFs.

The SEU cross-section of plain and hardened DFF is shown in Fig. 5, with the BRAM bit cross-section extracted from [15] is presented as a reference, where the author irradiated a 7nm FPGA with heavy ions, demonstrating the consistency between the simulated data and the results from the experimental campaign.

TABLE I: Comparison of area, power, delay, and APDP normalized to the standard DFF.

Cell	Area	Power (vs. Std. DFF)	Delay (vs. Std. DFF)	APDP (vs. Std. DFF)
Std. DFF	1.00	1.00	1.00	1.00
BISER [16]	2.33	1.88	2.38	10.43
DAD-FF [17]	2.25	1.69	1.50	6.70
TH-FF [18]	3.45	1.65	1.03	5.86
HPRH-FF [19]	2.33	2.06	0.94	4.53
Proposed DFF	**1.05**	**1.56**	**1.51**	**2.47**

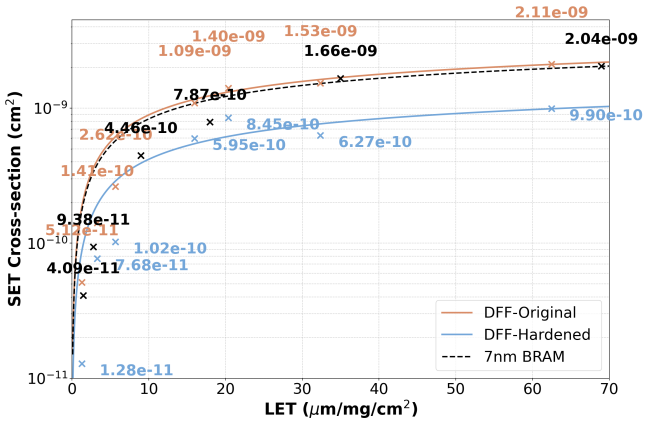


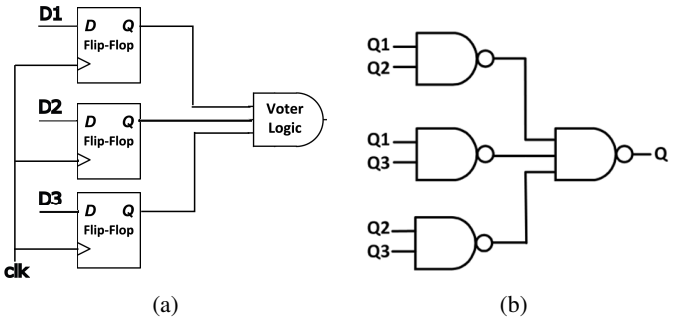
Fig. 5: SEU cross-section comparison.

III. Experimental Results

The proposed radiation-hardened D flip-flop was integrated into a TMR architecture to evaluate its error rate under high-energy radiation conditions. TMR is one of the most widely adopted fault-mitigation techniques in safety-critical systems due to its strong fault-masking capability. The resilience evaluation was conducted using particle-strike-based fault injection. Specifically, 3,000 simulations of $^{124}Xe^{35+}$ ion strikes were performed on the layout of the DFF-based TMR system. The resulting transient pulses were then injected into the corresponding schematic-level circuits using HSPICE.

The register-transfer-level (RTL) structure of the TMR system is shown in Fig. 6(a). The design consists of three replicated DFF instances followed by a majority voter, illustrated in Fig. 6(b). Each DFF receives an independent data input D while sharing a common clock signal, thereby avoiding the introduction of additional temporal redundancy. The voltage transients generated by ionizing particle strikes were randomly injected into individual DFF modules. An error was recorded only when an incorrect value appeared at the output of the majority voter, ensuring that the fault-masking behavior of the TMR architecture was properly evaluated.

Experimental results demonstrate that the TMR system constructed using the proposed hardened DFF exhibits a substantially lower SEU error rate than a baseline TMR implementation composed of standard DFFs, while incurring only minimal additional power consumption and timing overhead.



(a) (b)

Fig. 6: TMR structure (a) and majority voter structure (b) .

TABLE II: Comparison between standard TMR and TMR built with the proposed DFF.

Characteristics	Standard TMR	TMR with Proposed DFF
Error rate	0.32%	0.068%
$T_{d,\text{rise}}$ [ps]	51.8	62.0
$T_{d,\text{fall}}$ [ps]	60.2	62.8
Average power consumption [W]	2.07E-6	2.67E-6

Table II summarizes the quantitative comparison between the standard TMR and the TMR architecture implemented with the proposed hardened DFF. The results show that incorporating the proposed DFF reduces the SEU error rate of the TMR system to approximately 21% of that observed with standard cells. Although delay optimization is not a primary objective of this work, the proposed hardening strategy does not introduce a significant timing penalty when compared with other hardened solutions. Notably, the delay increase is primarily observed on the output rising edge, while the falling edge delay exhibits only a negligible increase. These results indicate that the proposed design achieves a favorable trade-off between radiation resilience and performance overhead.

IV. Conclusion

This work proposed a node- and layout-aware radiation-hardened D flip-flop that targets SEU mitigation with minimal overhead. By identifying and selectively hardening the most vulnerable internal nodes, the design avoids excessive circuit-level redundancy while maintaining robust radiation resilience. The proposed DFF incurs modest cost in terms of area (1.05×), power (1.56×), and delay (1.51×) relative to a standard DFF, while achieving an APDP of 2.47×, the lowest among the researched hardened DFF designs. In a TMR configuration, the use of the proposed DFF reduces the system-level error rate from 0.32% to 0.068%, corresponding to approximately 21% of the baseline error rate. These results demonstrate that selective, node-level hardening guided by layout awareness is an effective approach for designing high-reliability sequential elements in radiation-prone environments.

References

[1] Oliveira, Daniel AG, et al. "Modern GPUs radiation sensitivity evaluation and mitigation through duplication with comparison." IEEE Transactions on Nuclear Science 61.6 (2014): 3115-3122.

[2] Schrape, Oliver, et al. ”Low Overhead Self-Correction in Radiation-Hardening-by-Design Triple Modular Redundancy Flip-Flops for Space Applications.” 2025 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT). IEEE, 2025.

[3] Schrape, Oliver, et al. ”Design concept for radiation-hardening of triple modular redundancy TSPC flip-flops.” 2020 23rd Euromicro Conference on Digital System Design (DSD). IEEE, 2020.

[4] Azimi, Sarah, Corrado De Sio, and Luca Sterpone. ”A radiation-hardened CMOS full-adder based on layout selective transistor duplication.” IEEE Transactions on Very Large Scale Integration (VLSI) Systems 29.8 (2021): 1596-1600.

[5] Yamada, Kodai, et al. ”Radiation-hardened flip-flops with low-delay overhead using pMOS pass-transistors to suppress SET pulses in a 65-nm FDSOI process.” IEEE Transactions on Nuclear Science 65.8 (2018): 1814-1822.

[6] Shambhulingaiah, Sandeep, et al. ”Temporal sequential logic hardening by design with a low power delay element.” 2011 12th European Conference on Radiation and Its Effects on Components and Systems. IEEE, 2011.

[7] Xu, Yaohua, et al. ”A DICE Flip-Flop Design by Resetting Redundancy Hardening for Single Event Upset Tolerance.” IEEE Transactions on Device and Materials Reliability (2025).

[8] Takahashi, Shogo, Donghyun Kwon, and Kazuteru Namba. ”Non-volatile flip-flop with soft error tolerant capability using DICE and C-element.” Nonlinear Theory and Its Applications, IEICE 15.4 (2024): 673-681.

[9] Liang, Bin, et al. ”Layout based radiation hardening techniques against single-event transient.” Microelectronics Reliability 135 (2022): 114572.

[10] Ortega, Carlos Alfredo Pelcastre, and Mónico Linares Aranda. ”An alternative radiation hardened by layout design in a CMOS technology.” 2022 IEEE Latin American Electron Devices Conference (LAEDC). IEEE, 2022.

[11] V. Vashishtha, M. Vangala and L. T. Clark, ”ASAP7 predictive design kit development and cell design technology co-optimization: Invited paper,” 2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Irvine, CA, USA, 2017

[12] Wu, Nelson M-C., et al. ”Designing Radiation-Hardened D Flip-Flop with Reduced Latency and Area Using Filtering Buffer.” 2025 IEEE 43rd VLSI Test Symposium (VTS). IEEE, 2025.

[13] L. Sterpone, F. Luoni, S. Azimi and B. Du, ”A 3-D Simulation-Based Approach to Analyze Heavy Ions-Induced SET on Digital Circuits,” in IEEE Transactions on Nuclear Science, vol. 67, no. 9, pp. 2034-2041, Sept. 2020, doi: 10.1109/TNS.2020.3006997.

[14] L. Standaert, N. Postiau and M. Loiselet, ”UCL irradiation facilities status,” 2017 17th European Conference on Radiation and Its Effects on Components and Systems (RADECS), Geneva, Switzerland, 2017, pp. 13, doi: 10.1109/RADECS.2017.8696227.

[15] M. Aubry et al., ”Study of the heavy-ions sensitivity of last generation high data-rate optical transceivers,” 2024 24th European Conference on Radiation and Its Effects on Components and Systems (RADECS), Maspalomas, Spain, 2024, pp. 1-9, doi: 10.1109/RADECS61970.2024.11298611.

[16] Mitra, Subhasish, et al. ”Built-in soft error resilience for robust system design.” 2007 IEEE International Conference on Integrated Circuit Design and Technology. IEEE, 2007.

[17] Lin, Dave Y-W., and Charles H-P. Wen. ”DAD-FF: Hardening designs by delay-adjustable D-flip-flop for soft-error-rate reduction.” IEEE Transactions on Very Large Scale Integration (VLSI) Systems 28.4 (2020): 1030-1042.

[18] Li, Y-Q., et al. ”A 65 nm temporally hardened flip-flop circuit.” IEEE Transactions on Nuclear Science 63.6 (2016): 2934-2940.

[19] Li, Jie, Xiaoming Teng, and Yufeng Zhang. ”High-Performance Radiation-Hardened Flip-flop for Reliable Systems.” 2025 IEEE 16th International Conference on ASIC (ASICON). IEEE, 2025.