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A Cauer-Foster Integrated Thermal Network Model for Multi-Chip SiC Power Modules Considering Temperature-Dependent Material Properties

SHUOYU YE [1] (Student Member, IEEE), JINGYANG HU[1], GUOFU CHEN[1], CHUSHAN LI [1,2] (Member, IEEE), HAOZE LUO [1] (Senior Member, IEEE), WUHUA LI [1] (Senior Member, IEEE), XIANGNING HE [1] (Fellow, IEEE), AND FRANCESCO IANNUZZO [3] (Fellow, IEEE)

[1]College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China
[2]Zhejiang University—University of Illinois at Urbana Champaign Institute, Haining 314400, China
[3]Department of Energy, Politecnico di Torino, 10129 Turin, Italy

CORRESPONDING AUTHOR: HAOZE LUO (e-mail: haozeluo@zju.edu.cn)

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ABSTRACT This paper proposes a thermal network model (TNM) for multi-chip silicon carbide (SiC) power modules, which effectively incorporates temperature-dependent material properties and thermal cross-coupling (TCC) effects among parallel chips. The model adopts a hybrid three-dimensional (3-D) structure, combining a Cauer network for internal layer-wise heat conduction with a Foster network for external dissipation paths, enabling accurate and efficient electro-thermal simulations. A systematic parameter identification method is developed, leveraging finite element method (FEM) simulations to extract thermal conductance and thermal capacitance parameters through non-negative least-squares optimization and transient response fitting, with the temperature dependence of material properties fully considered. Steady-state and transient validations against FEM results show excellent consistency under different power loss levels and boundary conditions. For experimental validation, a dedicated test bench for SiC module junction temperature measurement is built, combining fiber-optic temperature sensing and thermal imaging techniques. The slight experimental deviations with a maximum error of less than 2.5 °C demonstrate that the model can accurately track the measured transient junction temperature of the module.

INDEX TERMS 3-D cauer model, silicon carbide (SiC) power module, temperature-dependent, thermal coupling.

I. INTRODUCTION

The fluctuation of junction temperature (T_j) is a critical factor leading to the failure of power modules, with its accurate estimation fundamental to ensuring system reliability, enabling condition monitoring, and fault warning. Currently, methods based on temperature sensitive electrical parameter (TSEP) and thermal models are most widely used in practice [1], [2], [3]. The TSEP method utilizes the chip itself as a sensor, inferring the T_j by measuring external electrical parameters sensitive to temperature, such as the on-state voltage and resistance [4], [5], [6]. While this method offers fast response, it provides only the average junction temperature of chips. This leads to significant measurement errors in multi-chip parallel power modules with severe thermal imbalance. Moreover, it cannot acquire temperatures of other critical internal layers, such as the solder layer. On the other hand, numerical simulation methods, primarily the finite element method (FEM), finite volume method (FVM), and finite difference method (FDM), have been extensively applied to analyze the thermal characteristics of power modules [7], [8],

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[9]. Although these methods achieve high accuracy, they are computationally intensive and demand substantial resources, resulting in low efficiency for long-term mission profile temperature predictions. In contrast, lumped thermal networks have consistently garnered attention from both academia and industry due to their high accuracy and ease of integration into circuit simulators for electro-thermal co-simulation.

The lumped thermal network model (TNM) primarily consists of two basic forms: Foster and Cauer models [10], [11]. The RC parameters of Foster models are obtained by mathematically fitting the module's transient thermal impedance curve, whose nodes do not correspond to the actual physical structure, making it suitable primarily for describing the thermal response between junction and reference point. One-dimensional (1-D) Cauer model, however, is constructed based on material properties and geometrical structure of each layer within the power module. Its RC parameters correspond to actual physical layers, enabling a more realistic representation of heat conduction through the multilayer structure. It is noteworthy that heat does not transfer entirely vertically downward but also undergoes lateral thermal diffusion during the transfer process inside the module. Consequently, the effective heat transfer area increases with the number of layers [12]. Furthermore, in multi-chip power modules, the close proximity of chips leads to thermal cross-coupling (TCC) effect caused by lateral heat diffusion. The thermal diffusion angle refers to the angle between the 3-D heat flux vector and the vertical direction and overlapping heat fluxes from adjacent chips make this angle hard to measure accurately [13].

To characterize TCC effect between chips accurately, researchers have introduced the thermal impedance matrix [14], [15], [16] and three-dimensional thermal network models (3-D TNM) [17], [18], [19], [20]. The thermal impedance matrix treats the system as a "opaque system", whose elements quantitatively describe the contribution of each chip's heating to the junction temperature of itself and other chips. However, for a system containing n chips, the matrix dimension is n^2, leading to a significant computational burden. Some early 3-D Foster-based models still used the thermal impedance matrix to describe inter-chip thermal interactions [17], [18]. Subsequently developed 3-D Cauer models addressed this issue by incorporating lateral thermal resistances between adjacent chips to characterize TCC effect. These models eliminate the dependency on the thermal impedance matrix, substantially reducing computational complexity [19], [20].

The temperature dependence of materials is also a non-negligible factor in thermal modeling. The RC parameters of Cauer models are directly related to the thermal conductivity and specific heat capacity of materials, both of which vary with temperature, particularly under high-temperature conditions. Existing studies have attempted to incorporate temperature-dependent effects into thermal models, such as those for insulated gate bipolar transistor (IGBT) modules [21], [22] and silicon carbide (SiC) modules [23]. However, these models fail to consider TCC effect between chips and are thus unsuitable for the heat transfer characteristics of multi-chip parallel modules. Although [24] established a 3-D thermal model considering temperature-dependent effect of materials, it simplified the packaging structure to only three layers, which cannot accurately reflect the actual heat transfer behavior. The model in [25] used a realistic layer count. However, its parameter extraction relied on adaptive particle swarm optimization with FEM data, leading to high complexity and poor engineering practicability. For a clear overview of the characteristics of these typical thermal models, Table 1 outlines their key advantages and limitations.

TABLE 1. Comparisons of Typical Thermal Models

Type	Pros	Cons	Ref.
FDM	High computational accuracy	Computationally complex	[8], [9]
1-D Foster	Including TCC effect through thermal impedance matrix	Without physical meaning	[10]
1-D Cauer	Considering temperature effect of materials	Omit TCC effect	[11]
3-D Foster	Considering TCC effect through layers	Time-consuming	[17]
3-D Cauer	Convenient for parameter extraction	Ignore temperature effect of materials	[20]

To address the shortcomings of the above existing studies, this paper develops a hybrid thermal network modeling scheme for multi-chip SiC power modules. The proposed approach integrates temperature-dependent material properties and inter-chip thermal coupling, and uses a Cauer-Foster hybrid structure to balance modeling accuracy and computational efficiency for both internal heat conduction and external heat dissipation. The main contributions of this work can be summarized as follows:

1) A hybrid 3-D Cauer-Foster topology is proposed, which combines the physical interpretability of the Cauer network for multi-layer internal heat conduction and the dynamic fitting efficiency of the Foster network for the heatsink-ambient path, overcoming the limitations of using a single network structure.
2) The model simultaneously incorporates temperature-dependent material characteristics and inter-chip thermal cross-coupling, two key factors that are often separately considered or neglected in traditional thermal models.
3) A complete FEM-based parameter identification framework using non-negative least-squares optimization is established, which ensures the physical rationality of extracted parameters and enables efficient and accurate electro-thermal simulation.

II. TEMPERATURE-DEPENDENT MATERIAL PROPERTIES AND FINITE ELEMENT SIMULATION MODELING

A. BASIC LAW OF HEAT CONDUCTION

The heat transfer process inside a multi-chip SiC power module is a typical three-dimensional unsteady solid heat transfer process involving both vertical heat dissipation and lateral

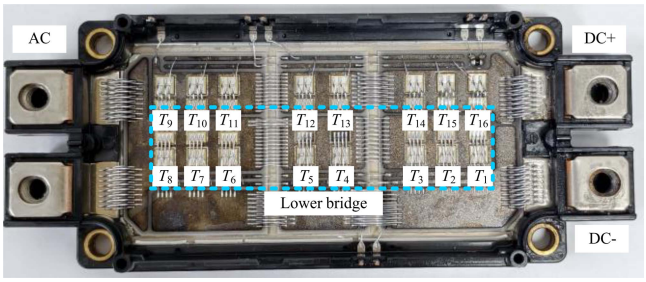

FIGURE 1. Structure of Rohm BSM300D12P2E001.

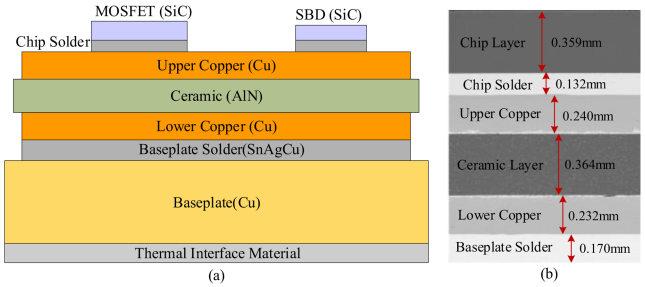

FIGURE 2. Cross-sectional structure of the power module. (a) Notional diagram of the multi-layer layout. (b) Microscopic image.

heat diffusion. Its complex heat transfer behavior can be quantitatively described by Fourier's Law of Heat Conduction. This law defines the quantitative relationship between heat flux density and temperature gradient, and its three-dimensional vector form is expressed as:

$$\boldsymbol{q} = -k \cdot \nabla T = -k\left(\frac{\partial T}{\partial x}\boldsymbol{i} + \frac{\partial T}{\partial y}\boldsymbol{j} + \frac{\partial T}{\partial z}\boldsymbol{k}\right) \tag{1}$$

where $\boldsymbol{q}$ is the 3-D heat flux vector (W/m^2), k is the thermal conductivity of the material (W/(m·K)), and ∇T is the 3-D temperature gradient. $\partial T/\partial x$ and $\partial T/\partial y$ are the horizontal temperature gradients in the x and y directions, respectively, which are the physical origin of the thermal cross-coupling effect between adjacent chips. $\partial T/\partial z$ is the vertical temperature gradient in the z direction, which dominates the vertical heat conduction from the chip to the heatsink.

B. TEMPERATURE-DEPENDENT CHARACTERISTICS OF KEY MATERIALS

The SiC power module investigated is the Rohm BSM300D12P2E001, a half-bridge topology module rated at 1200 V and 300 A, whose overall structure is illustrated in Fig. 1. Each bridge arm of the module integrates eight paralleled MOSFET chips. To enhance switching performance, the body diode of each MOSFET is paralleled with a Schottky barrier diode (SBD). This work focuses on the lower bridge arm, which comprises eight MOSFET chips T_1–T_8 and eight corresponding SBD chips T_9–T_{16}. To facilitate the installation and positioning of fiber-optic temperature probes on the chip top surfaces for accurate thermal monitoring, the silicone gel encapsulation layer of the module was removed prior to the experiments. This removal has a negligible impact on the thermal behavior of the module since silicone gel has a very low thermal conductivity and only wraps the non-functional side and top regions, contributing minimally to the dominant vertical heat dissipation path. The main heat flow path and boundary conditions of the module remain unchanged, ensuring the consistency between experimental measurements and simulation results.

Fig. 2 presents the cross-sectional structure of the power module. Fig. 2(a) shows a notional multi-layer packaging layout, which consists of the following core layers from top

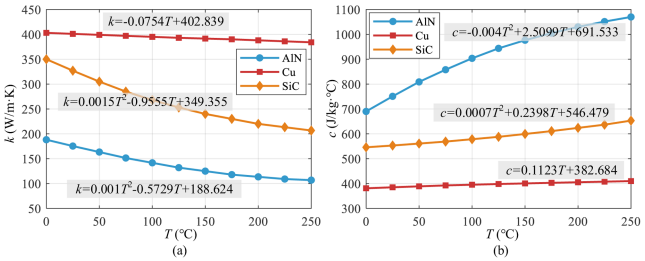

FIGURE 3. Temperature-dependent material properties of the SiC power module. (a) Thermal conductivity. (b) Specific heat capacity.

to bottom: the chip layer, solder layer, upper copper layer, ceramic insulating layer, lower copper layer, baseplate solder layer, and metal baseplate. To reduce the interfacial contact thermal resistance and ensure reliable heat dissipation of the power module, thermal interface material (TIM) is filled between the surface of substrate and liquid-cooled heatsink. Fig. 2(b) shows a microscopic detail of the module cross-section. High-precision sample cutting and preparation were performed to directly verify the actual material layer distribution and interface characteristics of the module.

The thermophysical properties of the internal materials in a SiC power module vary with the operating temperature, which results in a nonlinear distribution of the module junction temperature. An increase in temperature enlarges the amplitude of thermal vibration of the crystal lattice, raises the collision probability between phonons, and shortens the phonon mean free path. Consequently, the heat conduction efficiency of materials dominated by lattice heat conduction is significantly reduced. Therefore, incorporating the temperature-dependent characteristics of materials into the model construction is critical to ensuring the calculation accuracy of the module temperature field.

Fig. 3 is a plot of the thermal conductivity and specific heat capacity of key materials as functions of temperature, along with their fitted expressions [26]. The data show that the thermal properties of copper (Cu) exhibit minimal variation with temperature. In contrast, materials such as aluminum nitride (AlN) and SiC demonstrate significant temperature dependence, which can be well captured by second-order polynomial fits over the range of 0 °C to 250 °C. Therefore, to

TABLE 2. Dimension of Structure Layers

Layers	Dimension (mm^2)	Thickness (mm)	Density (g/cm^3)
MOSFET Chip	5.00×5.00	0.35	3.21
SBD Chip	5.00×3.00	0.25	3.21
MOSFET Solder	5.00×5.00	0.13	7.46
SBD Solder	5.00×3.00	0.13	7.46
Upper Copper	33.80×44.84	0.24	8.96
Ceramic	35.80×46.84	0.37	3.23
Lower Copper	33.80×44.84	0.24	8.96
Baseplate Solder	33.80×44.84	0.17	7.46
Baseplate	57.40×117.40	4.00	8.96
TIM	57.40×117.40	1.00	3.50
Heatsink	190.15×220.00	41.00	2.70

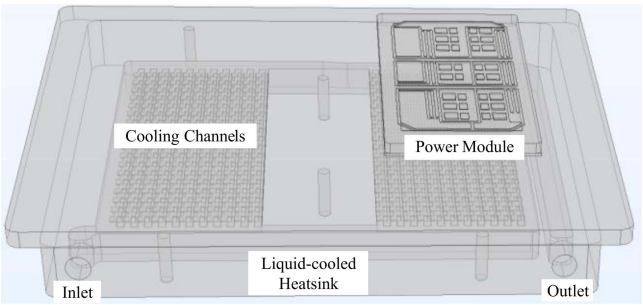

FIGURE 4. COMSOL 3-D model of the module and heatsink.

balance model accuracy and complexity, only the properties of AlN and SiC are defined as temperature-dependent in this paper.

C. COMSOL FINITE-ELEMENT SIMULATION AND MODEL VALIDATION

To obtain the detailed temperature field and heat flux distribution within the SiC power module, a 3-D finite-element simulation model integrating the module and liquid-cooled heatsink was developed based on COMSOL Multiphysics. The simulation results of this model provide a key data foundation for subsequent extraction of thermal network RC parameters. To ensure geometric accuracy, precise dimensions of internal material layers of the module were obtained through precision sectioning and microscopic measurement, as well as key dimensions of liquid-cooled heatsink.The relevant parameters are listed in Table 2.

Based on measured data, a simulation model was constructed in Fig. 4. A key improvement of this model is the detailed geometric construction of the internal cooling channels within the heatsink, rather than applying a simplified and potentially inaccurate equivalent heat transfer coefficient (HTC) to the baseplate surface, in order to accurately reproduce the actual thermal boundary conditions. In this model, the coolant was set as a 50% ethylene glycol aqueous solution, and temperature-dependent material properties were imported. Heating characteristics of chips were simulated by applying a volumetric heat source matching the power loss

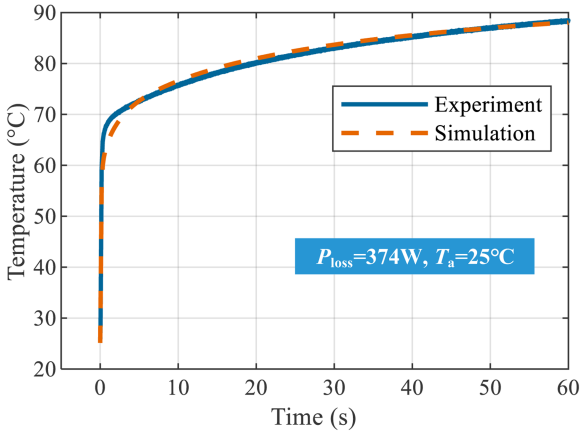

FIGURE 5. Comparison of transient temperature curves between experiment and simulation (max error 2.1%).

within chip regions and refined meshing was employed to ensure mesh-independent results.

In practical cooling systems, the TIM layer deforms under compression when the module is mounted on the heatsink. To take this factor into account on the simulation results, targeted corrections were applied to the thickness and material properties of this layer in the FEM model to reflect the actual contact condition. To verify the accuracy of the finite-element model, optical fiber temperature measurement was employed to obtain the transient thermal responses. Transient temperatures were measured at the geometric center of the top surface for all eight MOSFET chips on the lower bridge arm, and the FEM model was equipped with domain point probes at identical positions for synchronous comparison. The test was conducted on an established test bench with the coolant maintained at constant temperature of 25 °C, and a total constant power loss of 374 W was applied to all chips to record the 60 s transient temperature. The FEM model adopted the same boundary conditions and heat source power as the experimental setup. All measured curves agreed well with the FEM results, and the maximum deviation of 2.1% appeared at the first MOSFET chip. For brevity, only the transient curve of the first chip is presented in Fig. 5. The high consistency between measurement and simulation confirms the accuracy of the developed FEM model.

III. HYBRID 3-D TEMPERATURE-DEPENDENT THERMAL NETWORK MODEL

A. STRUCTURE OF THE 3-D TNM

Fig. 6 illustrates the proposed hybrid 3-D TNM schematic, where each layer contains 16 chip nodes. Nodes 1 to 16 are located at the geometric centers of top surface of each MOSFET and diode chip, while remaining nodes positioned along their vertical projection lines. Since solder layer temperature is not the focus of this study, nodes corresponding to chip solder layer and substrate solder layer are omitted from the model to reduce unnecessary complexity. Furthermore, the upper and

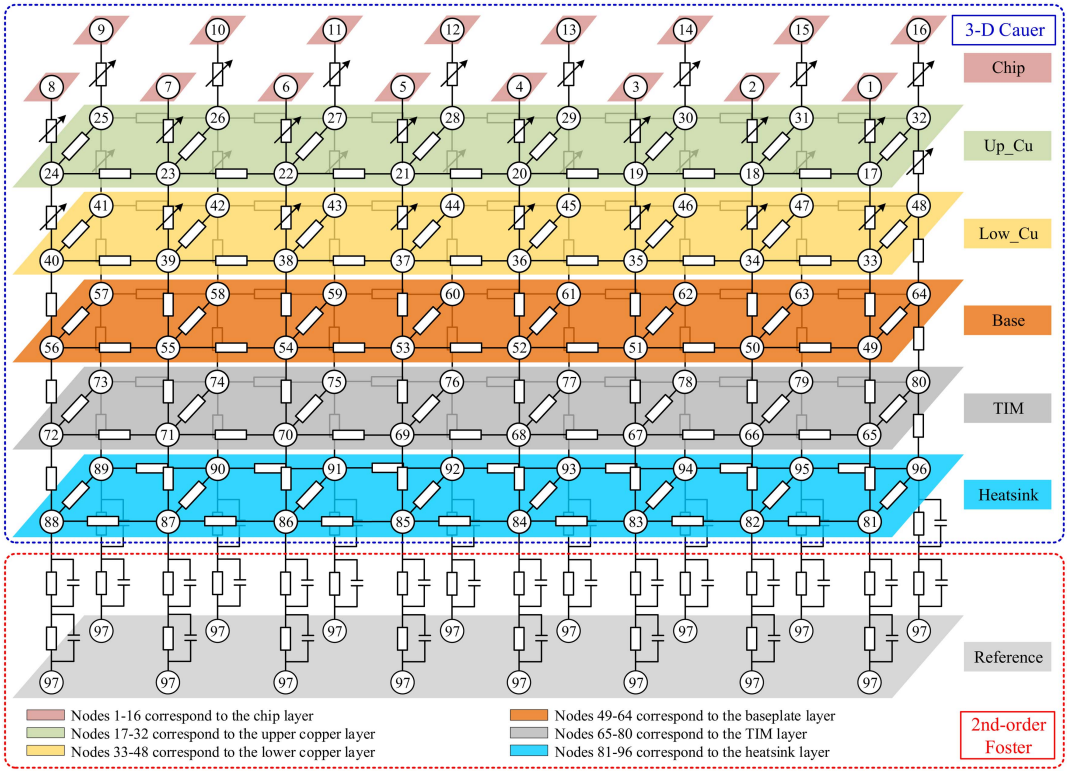

FIGURE 6. Structure of hybrid 3-D temperature-dependent TNM.

lower copper layers have extremely high thermal conductivity (∼400 W/m·K), leading to negligible through-plane temperature gradients across their thickness under rated operating conditions. Thus, each copper layer is represented by a single mid-plane node, eliminating the need for separate nodes for their top and bottom surfaces. Notably, the intermediate ceramic layer is not modeled as an independent layer and its thermal conductance is directly represented by the vertical thermal conductance between the upper and lower copper nodes, as its top and bottom surfaces are directly bonded to the copper layers. Accordingly, the model is simplified to six layers, with an additional ambient reference temperature layer. It should be clarified that only one node 97 is employed as the global ambient reference temperature. In the FEM simulation, domain point probes have been placed at corresponding locations of all nodes to monitor these temperatures. Vertical and lateral thermal conductances are respectively arranged between adjacent layers and among intra-layer nodes for characterizing TCC effect. All nodes are numbered counterclockwise to facilitate the rapid identification of thermal conductances.

Considering that thermal dissipation path from heatsink to ambient involves complex fluid flow and three-dimensional thermal diffusion processes, Cauer network is not enough to fully characterize its dynamic thermal behavior. In contrast, Foster network enables flexible and efficient equivalent modeling via parameter fitting. The proposed model adopts a hybrid topology: the region above the heatsink upper surface is modeled using a 3-D Cauer structure, while the path from heatsink to ambient reference temperature is described by a 2-nd order Foster network.

Given the temperature-dependent material properties of chip and ceramic layers, thermal resistances beneath the first and second layer nodes are modeled as temperature-sensitive parameters, as marked by slanted arrows in Fig. 6. Although heat capacity also exhibits temperature dependence, its variation is not considered, as incorporating temperature dependent heat capacity would significantly increase the computational burden by affecting the transient simulation at every time step. For the sake of clarity, the heat capacitances of nodes 1 to 80 are omitted, while those of nodes 81 to 96 are shown.

B. IDENTIFICATION OF THERMAL CONDUCTANCE PARAMETERS

Derived from the step-by-step extraction strategy of conventional 3-D Cauer model [20], systematic thermal conductance extraction method for proposed 3-D TNM has been modified and enhanced to fit hybrid topological structure.

First, the thermal path from heatsink to ambient reference point is treated as an overall thermal resistance for preliminary identification, without separating the Foster network part at this stage.

Therefore, the 3-D thermal network part to be identified includes 97 temperature nodes and 206 thermal conductance parameters. Based on Kirchhoff's current law, the thermal

balance equation for node i can be expressed as:

$$C_{\mathrm{i}}\frac{dT_{\mathrm{i}}}{dt}+\sum_{j\in M_{\mathrm{i}}}G_{\mathrm{i_j}}(T_{\mathrm{i}}-T_{\mathrm{j}})=P_{\mathrm{i}} \tag{2}$$

In the equation, C_{i} represents the thermal capacitance at node i, $G_{\mathrm{i_j}}$ denotes the thermal conductance between node i and j, T_{i} is the temperature of node i, M_{i} indicates the set of nodes connected to node i, and P_{i} signifies the power loss injected into node i, where P_{i} is non-zero only for chip nodes 1–16.

To construct a solvable matrix equation, thermal conductances in the network must be systematically numbered. The numbering rule is as follows: starting from node $i = 1$, all $G_{\mathrm{i_j}}$ are numbered sequentially in the order of increasing j. For example, G_{1_17} is numbered as G_1, G_{17_18} as G_{17}, and so on, until all 206 thermal conductances are covered. This rule ensures that each thermal conductance parameter G_{k} uniquely corresponds to the thermal connection between two specific nodes.

The network topology differs by node type in Fig. 6. Top chip nodes have one downward connection, edge nodes have four while internal nodes have five. Thus, the number of summation terms in the equation changes accordingly.

Taking the 97 nodes in this work as an example, (2) is rewritten in matrix form as follows:

$$\boldsymbol{C}_{97\times97}\frac{d\boldsymbol{T}_{97\times1}}{dt}+\boldsymbol{G}_{97\times97}\boldsymbol{T}_{97\times1}=\boldsymbol{P}_{97\times1} \tag{3}$$

Here, $\boldsymbol{C}$ represents diagonal thermal capacitance matrix, $\boldsymbol{T}$ is temperature vector, $\boldsymbol{G}$ denotes thermal conductance matrix, and $\boldsymbol{P}$ is power loss vector. Their expressions are given below:

$$\boldsymbol{C}_{97\times97}=\begin{bmatrix}C_1&0&0&\cdots&0\\0&C_2&0&\cdots&0\\\vdots&\vdots&\ddots&\vdots&\vdots\\0&0&0&C_{96}&0\\0&0&0&0&1\end{bmatrix},\boldsymbol{T}_{97\times1}=\begin{bmatrix}T_1\\T_2\\\vdots\\T_{96}\\T_{97}\end{bmatrix},$$

$$\boldsymbol{P}_{97\times1}=\begin{bmatrix}P_1\\\vdots\\P_{16}\\\vdots\\0\end{bmatrix} \tag{4}$$

$$\boldsymbol{G}_{97\times97}=\begin{bmatrix}G_{1_17}&0&\cdots&0&0\\0&G_{2_18}&\cdots&0&0\\\vdots&\vdots&\ddots&\vdots&\vdots\\0&0&\cdots&\sum\limits_{j\in M_{96}}G_{96_\mathrm{j}}&-G_{96_97}\\0&0&\cdots&0&0\end{bmatrix} \tag{5}$$

TABLE 3. Finite Element Simulation Parameter Setting

Number	Power loss	Notes
1	$P_{1,3,5,7}=60$W	Training set
2	$P_{2,4,6,8}=60$W	Training set
3	$P_{9,11,13,15}=60$W,	Training set
4	$P_{10,12,14,16}=60$W	Training set
5	$P_{1,2,3,4,5,6,7,8}=60$W	Validation set
6	$P_{1,2,3,4,5,6,7,8}=80$W	Validation set
7	$P_{1,2,3,4,5,6,7,8}=100$W	Validation set

Given the sparsity of $\boldsymbol{G}$ matrix, it can be further reconstructed through derivation as follows:

$$\boldsymbol{C}_{97\times97}\frac{d\boldsymbol{T}_{97\times1}}{dt}+\boldsymbol{T}^{*}{}_{97\times206}\boldsymbol{G}^{*}{}_{206\times1}=\boldsymbol{P}_{97\times1} \tag{6}$$

where:

$$\boldsymbol{G}^{*}{}_{206\times1}=\begin{bmatrix}G_1&G_2&\cdots&G_{205}&G_{206}\end{bmatrix}^{T} \tag{7}$$

$$\boldsymbol{T}^{*}{}_{97\times206}=\begin{bmatrix}T_1-T_{17}&0&\cdots&0&0&0\\0&T_2-T_{18}&\cdots&0&0&0\\\vdots&\vdots&\ddots&\vdots&\vdots&\vdots\\T_{17}-T_1&0&\cdots&0&0&0\\0&T_{18}-T_2&\cdots&0&0&0\\\vdots&0&\cdots&\vdots&\vdots&\vdots\\\vdots&\vdots&\cdots&T_{95}-T_{96}&T_{95}-T_{97}&0\\\vdots&\vdots&\cdots&T_{96}-T_{95}&0&T_{96}-T_{97}\\0&0&\cdots&0&0&0\end{bmatrix} \tag{8}$$

In the above expressions, $\boldsymbol{G}^{*}$ is a column vector composed of all 206 thermal conductances, and $\boldsymbol{T}^{*}$ is the corresponding nodal temperature difference matrix. Except for node 97, each thermal conductance in the network is connected between two specific nodes (node i and node j). Therefore, in the $\boldsymbol{T}^{*}$ matrix, the column vector corresponding to $\boldsymbol{G}_{\mathrm{i_j}}$ contains the element (T_{i} - T_{j}) in row i and its opposite value (T_{j} - T_{i}) in row j. This pattern ensures that the heat flow direction across each thermal conductance complies with Kirchhoff's law, which is a core feature of constructing this matrix equation. Since node 97 serves as the reference ambient temperature, all elements in its corresponding row are zero.

Under steady-state conditions, the temperature time derivative term in (6) becomes zero, and the equation simplifies to:

$$\boldsymbol{T}^{*}{}_{97\times206}\boldsymbol{G}^{*}{}_{206\times1}=\boldsymbol{P}_{97\times1} \tag{9}$$

This form eliminates the influence of thermal capacitance. Since the rank of $\boldsymbol{T}^{*}$ is 96, while the number of thermal conductance parameters to be identified is 206, (9) is an underdetermined system that cannot yield a unique solution. As listed in Table 3, four sets of DC power loading patterns serve as the training set for steady finite-element simulations, and

the remaining three groups are used as the validation set to check identification accuracy. Power loss is applied to different chip combinations to amplify the temperature differences between nodes, thereby fully exciting vertical heat conduction paths and lateral inter-chip thermal coupling effects, and enhancing parameter identifiability. By superimposing the steady-state temperature data from the four simulation cases, the expanded overdetermined matrix equation is obtained:

$$\boldsymbol{T}^*_{388\times206}\boldsymbol{G}^*_{206\times1} = \boldsymbol{P}_{388\times1} \tag{10}$$

The stacked matrix $\boldsymbol{T}^*$ has a dimension of 388 × 206 with full column rank of 206, which ensures that the equation system is solvable and all 206 thermal conductance parameters can be uniquely identified. The four loading patterns provide sufficient independent equations for reliable parameter extraction without redundant computation. The quantity of training data and power distribution mode both affect identification performance. Insufficient loading cases cannot provide enough independent equations for complete parameter solving, whereas excessive working conditions merely increase computational burden with limited accuracy improvement. Reasonably designed loading quantity and staggered chip power distribution can well capture actual multi-dimensional heat transfer features and achieve stable parameter extraction.

Thermal conductance characterizes the heat conduction capability of materials and structures, which must be non-negative in line with the fundamental law of heat conduction. The non-negative least squares (NNLS) algorithm imposes non-negativity constraints on the identified parameters to exclude physically unreasonable values. Considering such physical rationality of thermal parameters, the NNLS method embedded in MATLAB is adopted to solve $\boldsymbol{G}^*$:

$$\boldsymbol{G}^*_{206\times1} = \text{lsqnonneg}(\boldsymbol{T}^*_{388\times206}, \boldsymbol{P}_{388\times1}) \tag{11}$$

To characterize the temperature-dependent characteristics of SiC and AlN materials, the aforementioned four sets of steady-state simulations are performed at intervals of 25 °C within the temperature range of 25 °C to 175 °C, followed by the parameter identification procedure. Finally, the identified temperature-dependent thermal conductances are converted into thermal resistances, and curve fitting is applied accordingly. Specifically, the thermal resistances R_1–R_8 and R_9–R_{16}, corresponding to SiC material, are fitted using second-order polynomial, while the thermal resistances R_{19}–R_{39} and R_{41}–R_{54}, corresponding to AlN material, are fitted using first-order linear fit. As shown in Fig. 7, the fitting results align with the trend of the reciprocal of material thermal conductivity versus temperature, validating the physical rationality of the method. Representative parameters of the identified thermal conductances at 25 °C are detailed in Table 4. Given the large number of parameters, the table systematically presents a series of vertical thermal conductances along the projection path of node 1, as well as selected lateral thermal conductances, to clearly illustrate the parameter distribution and thermal path relationships.

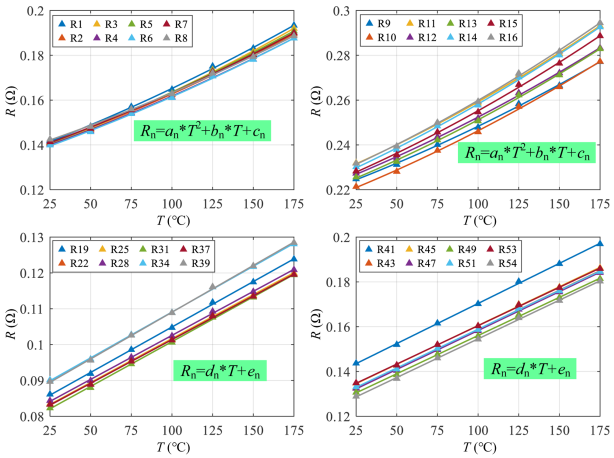

FIGURE 7. Temperature-related thermal resistance fitting results.

TABLE 4. Selected Representative Thermal Conductance Parameters

Category	Parameter	Value (W/K)	Position
Vertical thermal conducance	G_{1_17}	7.05	Chip and Up_Cu
	G_{17_33}	11.61	Up_Cu and Low_Cu
	G_{33_49}	7.80	Low_Cu and Base
	G_{49_65}	9.98	Base and TIM
	G_{65_81}	1.30	TIM and Heatsink
Lateral thermal conducance	G_{18_19}	0	Adjacent on Up_Cu
	G_{19_20}	0.038	Adjacent on Up_Cu
	G_{33_34}	0.077	Adjacent on Low_Cu
	G_{51_52}	0.172	Adjacent on Base
	G_{65_66}	3.21	Adjacent on TIM
	G_{81_82}	1.05	Adjacent on Heatsink

C. IDENTIFICATION OF THERMAL CAPACITANCE PARAMETERS

Thermal capacitance parameters in the model are identified through transient finite element simulation. A power dissipation of 60 W is applied to all chips in COMSOL, and the transient temperature response data of each node are recorded as the benchmark. Subsequently, the "Parameter Estimation" toolbox in MATLAB/Simulink is utilized for parameter optimization. This module iteratively adjusts parameter values so that the thermal network simulation results continuously approach the finite element benchmark. The specific optimization process is based on the local thermal network structure shown in Fig. 8. This figure illustrates the topology using node 49 as an example, which includes its connected nodes (33, 50, 64, 65), thermal resistances and target thermal capacitance. By inputting transient temperature time vectors obtained from FEM simulation into these nodes and setting the target thermal capacitance of node 49 as the parameter to be optimized, the temperature response of this node from the thermal network simulation can achieve high agreement with the finite element results. Through script-based batch processing, this method can be extended to all nodes, ensuring the efficiency and consistency of thermal capacitance parameter extraction.

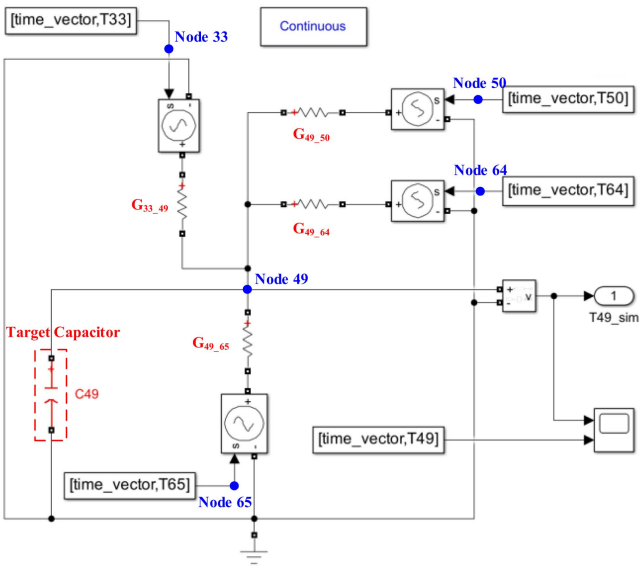

FIGURE 8. Thermal capacitance extraction through local thermal network.

TABLE 5. Selected Representative Thermal Capacitance Parameters

Category	Parameter	Value (J/K)	Position
Cauer	C_1	0.0125	Chip
	C_{17}	0.0533	Up_Cu
	C_{33}	0.0848	Low_Cu
	C_{49}	0.1803	Base
	C_{65}	2.397	TIM
Foster	C_{81_1}	29.54	Heatsink
	C_{81_2}	0.1648	

Meanwhile, to extract thermal resistance and thermal capacitance parameters of Foster network part in the proposed hybrid structure, the following steps are adopted:

First, based on the thermal conductance identification results in Table 4, the 16 thermal conductance parameters connected to node 97 are extracted and converted into thermal resistances. According to Kirchhoff's law, the total resistance of series-connected thermal resistances equals the sum of the individual resistances. Then, one of the thermal resistances is set as an unknown variable, while the other is constrained by the sum. Additionally, two thermal capacitances are introduced as parameters to be determined, resulting in a total of three unknowns. These parameters are simultaneously optimized using the "Parameter Estimation" module, ultimately obtaining thermal resistance and thermal capacitance values. Due to the large number of thermal capacitance parameters, Table 5 shows a selection of the thermal capacitances along the vertical projection path of node 1 as a typical example for clear presentation of the parameter distribution pattern. The thermal capacitance distribution along this path effectively reflects the thermal dynamic characteristics from the chips to the heatsink, and the results are representative for other symmetric paths.

Fig. 9 summarizes the overall modeling workflow proposed in this study, which is divided into four core stages: COMSOL FEM model preparation, steady-state thermal conductance extraction, transient thermal capacitance extraction and Simulink thermal network validation. The structured framework explicitly visualizes the complete technical pathway, starting from FEM model setup and thermal network parameter identification, progressing through steady-state and transient characterization, and concluding with Simulink-based TNM validation.

IV. VALIDATION AND DISCUSSION OF THERMAL NETWORK MODEL

A. ANALYSIS AND DISCUSSION OF MODEL CHARACTERISTICS

1) PHYSICAL MEANING OF THERMAL NETWORK TOPOLOGY AND PARAMETER DISTRIBUTION

Previous calculation results indicate that some lateral thermal conductances were identified as zero values, such as G_{18_19} in Table 4. In fact, 12 out of the total 206 thermal conductances were identified as zero. This phenomenon is not wrong and has clear physical interpretation. Taking G_{18_19} as an example, a temperature difference exists between its corresponding nodes 18 and 19, yet the direct thermal conductance is zero. This indicates that the thermal coupling between them does not occur through a direct path but rather via an indirect path across node 31 and 30. This result aligns with the physical expectation of multi-dimensional heat diffusion in 3-D package structures, verifying that the proposed thermal network topology can accurately reflect complex internal thermal coupling effects. Furthermore, benefiting from the symmetry of the chip layout, the vertical thermal conductances corresponding to chips in the same layer (e.g., R_1–R_8) exhibit relatively close numerical values, showing a regular distribution pattern. In contrast, the distribution of lateral thermal conductances is more complex due to the combined influence of thermal coupling with adjacent chips and their respective heat dissipation paths, making precise extraction through finite element simulation and parameter identification necessary.

2) IMPLEMENTATION OF THE SIMULATION MODEL AND SOLUTION STABILITY

In Simulink, all constant thermal resistances and capacitances are connected according to the topology structure shown in Fig. 6. For temperature-dependent thermal resistances, taking the thermal resistance R_1 between node 1 and 17 as an example, its modeling approach is illustrated in Fig. 10. This structure simulates the thermal resistance as a controlled variable resistor: terminals 1 and 3 represent the two ends of the thermal resistance, terminals 1 and 2 input the temperatures at these ends, which is equivalent to voltages, and the fitting polynomial result shown in Fig. 7 is calculated in real-time using mathematical blocks such as Sum, Gain, and Square. A large resistor R_o is connected in parallel with the variable resistor to avoid convergence problems. This structure was

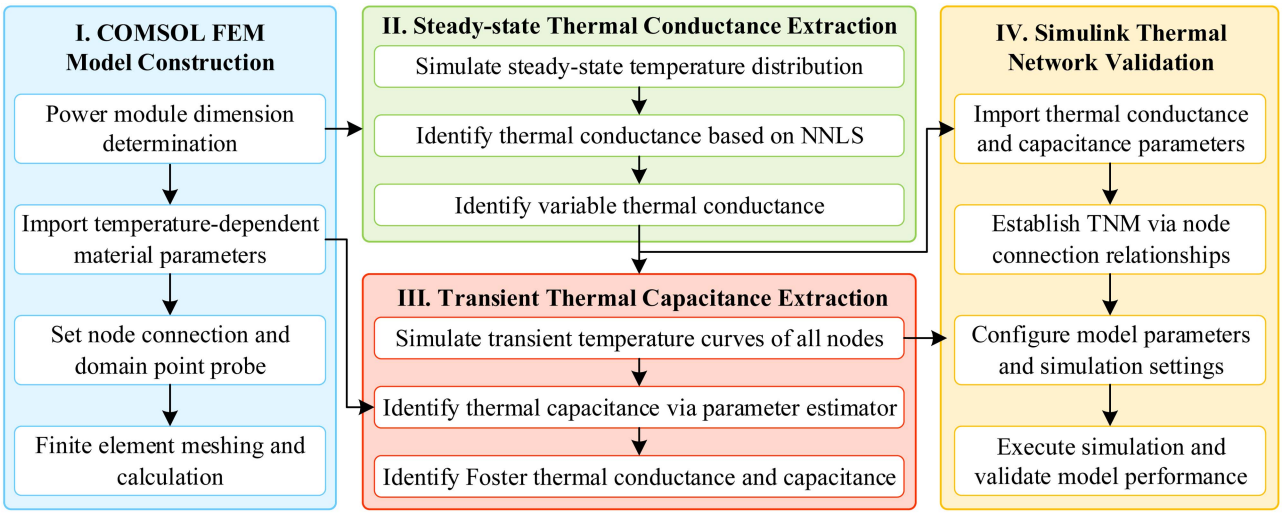

FIGURE 9. Overall TNM modeling process.

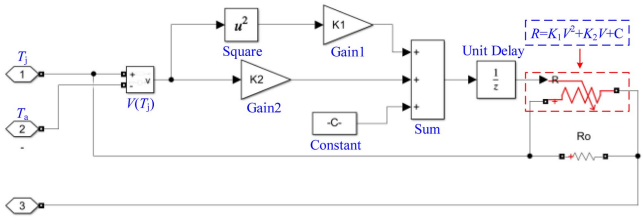

FIGURE 10. Implementation method of variable thermal resistance.

encapsulated into a reusable subsystem. To avoid "algebraic loop" errors during simulation, a "Unit Delay" block was inserted into the feedback loop to introduce a 0.1 ms one-sample period delay, which is far smaller than the thermal time constants of the chip layer (around 1.8 ms). This small delay guarantees numerical stability without distorting the transient thermal dynamic characteristics of the model.

3) MODEL PARAMETERIZATION AND MODULARIZATION

The model implemented in this study features a high degree of parameterization and modularization. All identified thermal conductances, thermal capacitances, and temperature-dependent coefficients are stored in the MATLAB workspace and automatically imported into Simulink via scripts, facilitating batch simulation and parameter studies. Encapsulating the temperature-dependent thermal resistances into subsystems not only significantly improves the maintainability of the model but also provides convenience for subsequent expansion of the topology structure.

B. VALIDATION OF SIMULATION MODEL ACCURACY

The accuracy of the established thermal network model was comprehensively evaluated by comparing the chip temperatures from Simulink simulations with FEM results under the validation conditions listed in Groups 5-7 of Table 3. This comparison encompasses both steady-state and transient operational dimensions.

1) STEADY-STATE ACCURACY VALIDATION

As shown in Fig. 11, the steady-state temperature profiles of chips T_1–T_4 are presented for three distinct power levels: (a) 560 W, (b) 720 W, and (c) 880 W, where the blue, green, and red bars denote the FEM reference, the proposed TNM (accounting for temperature-dependent material properties), and the TNM0 model (neglecting temperature effects), respectively. A key observation is that the discrepancy of the TNM0 model increases progressively with applied power: the maximum error rises from 3.2 °C at 560 W to 6.4 °C at 720 W and further to 11.3 °C at 880 W. This trend is directly attributable to the more pronounced reduction in thermal conductivity at elevated operating temperatures, which the TNM0 model fails to capture. In contrast, the TNM model maintains high accuracy across all conditions, with maximum errors of 1.0 °C at 560 W, 1.1 °C at 720 W, and 0.9 °C at 880 W. The strong consistency between TNM and FEM results at all power levels verifies the high steady-state accuracy of proposed model, which arises directly from proper inclusion of temperature-dependent material properties that are neglected in conventional thermal models.

2) TRANSIENT ACCURACY VALIDATION

To validate the transient accuracy of the model, this study selected Chips 1, 33, and 65 as representative cases. The transient comparison of their temperature response curves is shown in Fig. 12. The figure simultaneously displays the transient curves of the proposed hybrid 3-D TNM, the conventional 3-D Cauer model, and the FEM results, from which the following conclusions can be drawn:

Throughout the entire dynamic process, the prediction curves of the proposed hybrid 3-D TNM show excellent agreement with the FEM benchmark, with a maximum error of

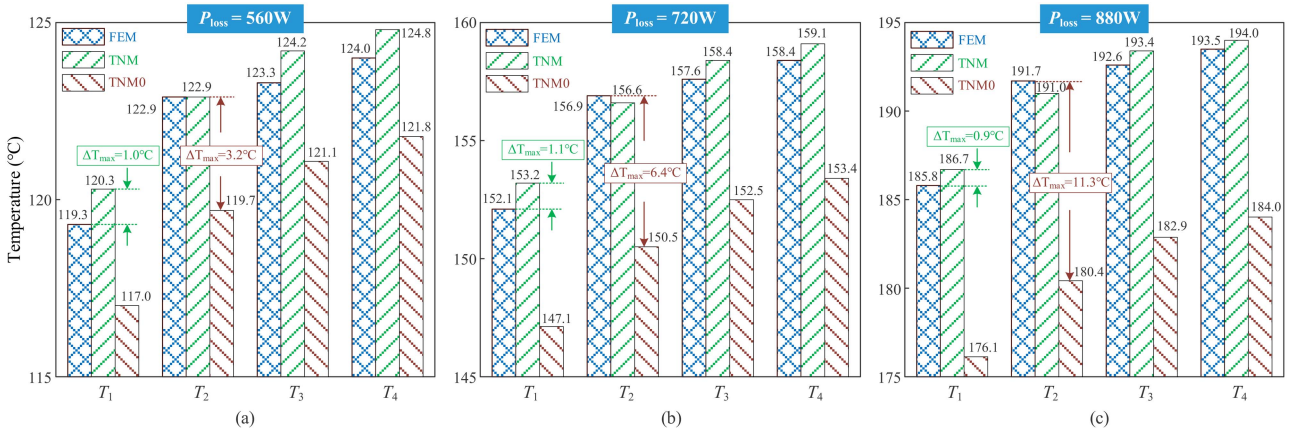

FIGURE 11. Steady-state accuracy validation. (a) 560 W Condition. (b) 720 W Condition. (c) 880 W Condition.

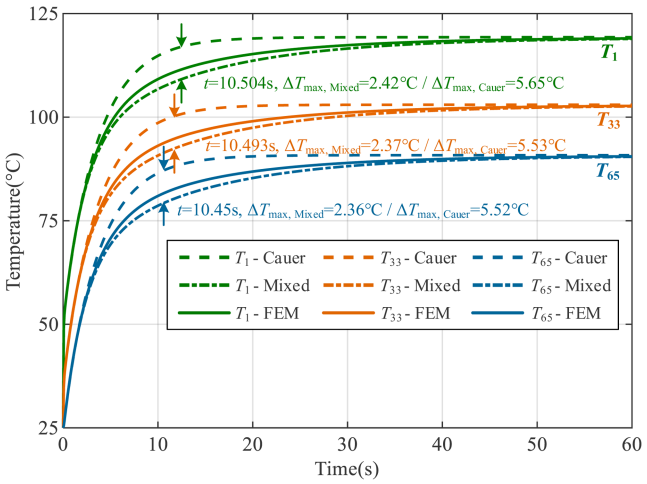

FIGURE 12. Comparison of the proposed model, conventional model, and finite element simulation.

2.42 °C, verifying that the model also exhibits high accuracy under transient conditions. In contrast, the conventional 3-D Cauer model exhibits a faster convergence to steady-state temperature, leading to more pronounced deviations from the FEM results across all representative nodes, including node 1, node 33, and node 65, with a maximum error of 5.65 °C.

This discrepancy indicates that the thermal capacitance of the heatsink is not accurately captured in the conventional model. The results directly verify the necessity and superiority of the hybrid structure, which improves modeling accuracy by separately characterizing the internal Cauer network of the package and the external Foster network for the heat-dissipation path. By more accurately characterizing the dynamic thermal response from the heatsink to the environment using the Foster network, the hybrid model achieves significantly better consistency with the finite element results in transient simulations.

Table 6 presents a comprehensive performance comparison of transient simulations among the proposed hybrid model,

TABLE 6. Comparison of Computational Efficiency

Method	Solving time/s	Time Percentage	Error
Proposed method	27.32	0.203%	0.83%
Traditional method	9.36	0.070%	5.71%
COMSOL FEM	13440	1	/

the conventional 3-D Cauer model, and COMSOL FEM. Under identical conditions (60 s duration, 1 ms time step), the proposed model requires only 0.203% of the computational time needed by COMSOL FEM, while exhibiting a relative error of merely 0.83% against the FEM benchmark solution. Compared with the traditional 3-D Cauer model, the proposed method only incurs a moderate increase in computational time (from 9.36 s to 27.32 s, still far below the FEM cost) but reduces the prediction error from 5.71% to 0.83%. These results validate that the proposed model achieves a superior balance between high simulation accuracy and reduced computational cost, significantly outperforming both the conventional thermal network model and the FEM benchmark in practical applicability.

3) STUDY ON INFLUENCE OF BOUNDARY CONDITIONS

To validate the applicability of the developed model under different boundary conditions, simulations were conducted at three distinct reference ambient temperatures: 25 °C, 50 °C, and 75 °C. First, to determine whether the model parameters vary with ambient temperature, finite element simulations were performed under each temperature condition, and the thermal resistances and capacitances were identified following the step-by-step parameter extraction procedure described before. The results show that the extracted parameter values remain largely consistent across different ambient temperatures, with an average deviation not exceeding 1%, demonstrating that the model parameters are independent of ambient temperature.

Furthermore, since the model already accounts for the temperature dependence of material properties, variations in

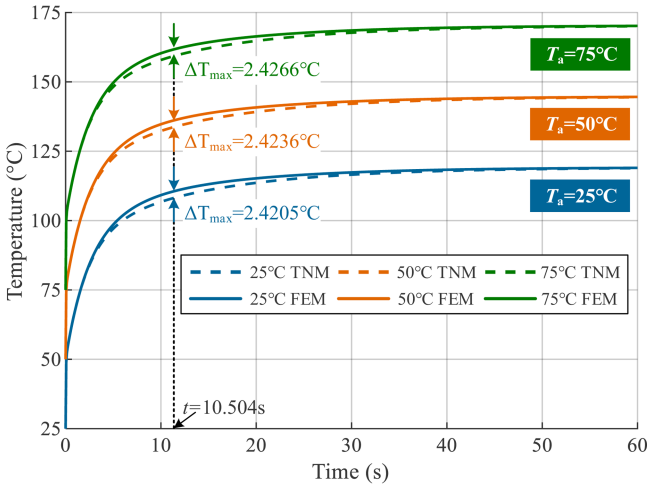

FIGURE 13. Comparison of FEM and TNM under different boundary conditions.

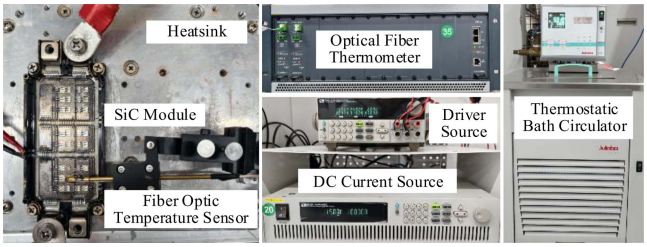

FIGURE 14. Junction temperature test bench for SiC power modules.

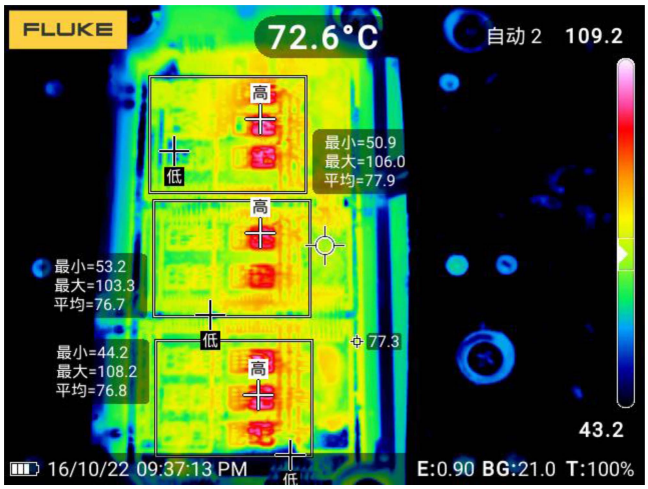

FIGURE 15. Steady state infrared temperature distribution.

power loss primarily influence material parameters indirectly by affecting the device temperature, without altering the model structure or the extracted R and C parameters themselves. This indicates that the proposed TNM also exhibits stable parametric representation under different power levels.

Fig. 13 further compares the transient temperature response of node 1 under the three ambient temperatures, where the solid lines represent the finite element simulation results and the dashed lines correspond to the predictions from the proposed thermal network model. It can be observed that the curves from both methods show excellent agreement under all temperature conditions, with the maximum transient error of around 2.42 °C at 10.504 s. This fully verifies that the model maintains high predictive accuracy under different ambient temperatures, demonstrating good temperature adaptability and boundary condition robustness.

V. EXPERIMENTAL VALIDATION

To validate the accuracy of the proposed TNM, a junction temperature test experimental platform for SiC power modules was built as shown in Fig. 14. In the experiment, the research object was fixed to an oil-heated, thermostatically controlled water-cooled plate, and was controlled via gate drive signals. An Opsens fiber optic thermometer equipped with an OTG-F-10 fiber optic temperature probe was adopted to collect temperature at target measuring points, with a maximum sampling frequency of 1 kHz. This fiber optic probe features a response time of 5 ms and a measurement accuracy of better than 0.8 °C, which can fully meet the requirements for high-precision measurement of the transient junction temperature of power modules. A DC current source was capable of outputting an adjustable current with a maximum value of 220 A, which was used to apply different levels of conduction losses to the module and simulate the power heating characteristics under practical operating conditions.

Two boundary conditions with coolant temperatures of 25 °C and 50 °C were set in the experiment. By applying currents of different magnitudes and calculating the module power loss based on the on-state voltage drop, loading tests under different power levels were implemented.

Steady-state temperature distribution validation was carried out using a Fluke Ti450 infrared thermal imager. Under the operating condition of a coolant temperature of 25 °C and an applied current of 374 W, the steady-state temperature distribution of the module is shown in Fig. 15. Three measurement boxes set in the experiment fully cover the temperature monitoring regions of the 8 chips Table 7 presents a comparison of errors between the simulation results of the proposed model and the traditional model against experimental measurements under another two operating conditions. The steady-state error of the proposed model remains within 1.5%, while the error of the traditional model that neglects temperature-dependent material properties reaches as high as 5%, fully reflecting the significant accuracy advantage of the proposed model.

In addition, since the proposed complex thermal network is purposely designed for accurate transient thermal analysis, a cyclic mode of heating for 30 s followed by cooling for 30 s was adopted to carry out the temperature response tests for 2 cycles. A comparison of the experimental and simulation

TABLE 7. Steady Simulation and Measurement Comparison Under Different Boundary Conditions and Power Losses

Method	Case	P=573W, T_a=25°C	P=252W, T_a=50°C
	Node	Temperature/Error	Temperature /Error
Proposed Method	1	123.3°C/1.20%	93.3°C/1.17%
	2	123.0°C/1.19%	93.0°C/1.28%
	3	122.8°C/1.29%	92.7°C/1.49%
	4	122.3°C/1.13%	92.3°C/1.39%
	5	119.8°C/1.07%	90.5°C/1.42%
Traditional Method	1	118.8°C/4.81%	91.4°C/3.18%
	2	118.5°C/4.82%	91.3°C/3.08%
	3	118.3°C/4.90%	91.2°C/3.08%
	4	117.9°C/4.69%	90.7°C/3.10%
	5	115.4°C/4.71%	89.0°C/3.05%

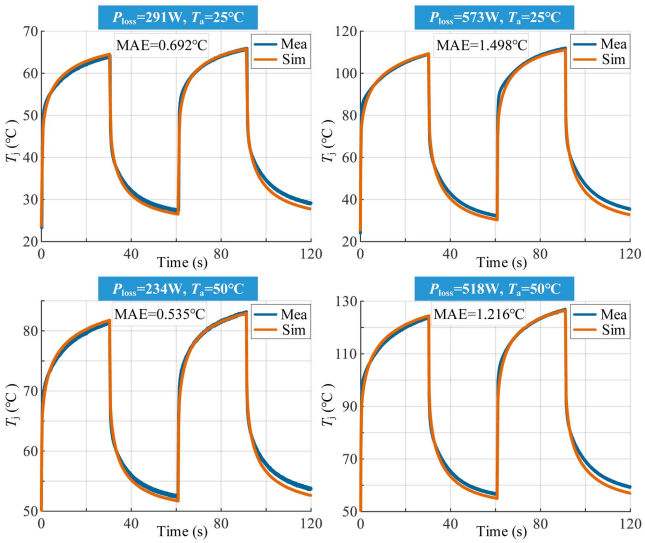

FIGURE 16. Transient simulation and measurement comparison under different boundary conditions and power losses.

results is presented in Fig. 16. Under the above four different operating conditions, the simulated orange curves (Sim) of the proposed TNM can accurately track the measured blue curves (Mea), with an average error of less than 1.5 °C. These sets of curves are highly consistent in their variation trends, verifying the transient temperature tracking capability of the model.

VI. CONCLUSION

This work developed a hybrid 3-D thermal network model for multi-chip SiC power modules, addressing the deficiency of conventional models in simultaneously accounting for temperature-dependent material properties and inter-chip thermal cross-coupling effects. The hybrid 3-D topology, integrating Cauer and Foster networks, provides a physically meaningful representation of heat transfer processes, from chip-level generation to ambient dissipation. Notably, the proposed hybrid Cauer-Foster topology accurately captures the thermal capacitance of the heatsink that conventional 3-D Cauer models neglect, which is the primary reason for its superior transient accuracy. A systematic FEM-based parameter identification method is adopted for thermal conductance and capacitance extraction with full consideration of material temperature dependence. FEM validations confirm excellent steady and transient consistency of the model, with a maximum steady-state error below 1.1 °C and transient deviation below 2.5 °C. Experimental tests via fiber-optic sensing and thermal imaging verify the model's reliability, with the maximum error within 1.5%. Benefiting from the compact hybrid topology and systematic parameter identification, the proposed model achieves outstanding computational efficiency while preserving high accuracy, making it well-suited for fast electro-thermal co-simulation and long-term mission profile analysis.

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