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Sensor Applications

A 0.0025 mm² CMOS Neural Front-End With VCO-Based Frequency Encoding for Body-Coupled Communication

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Abstract—This letter presents the first neural front-end specifically targeting intravascular recording with direct frequency-domain encoding for body-coupled communication. It employs a differential amplifier and voltage-controlled oscillator (VCO)-based amplitude-to-frequency encoding. Fabricated in TSMC 180 nm CMOS technology, the proposed architecture integrates a fully differential capacitive-feedback low-noise amplifier with a current-starved ring VCO to directly translate microvolt-level neural signals into frequency variations. The design occupies 0.0025 mm^2 and operates from externally supplied ±0.6 V DC rails, intended to be delivered through the catheter in the target application, without any on-chip negative-voltage generator. Measured results demonstrate linear amplitude-to-frequency conversion up to 2 mV$_{pp}$ input with a minimum detectable signal of 20 µV$_{pp}$. The measured bandwidth is 6 Hz–6.7 kHz. The total power consumption is 11 µW under PCB loading conditions. The integrated equivalent input-referred noise is 5.55 µV$_{rms}$ over the spike band (300 Hz–6 kHz). By prioritizing extreme miniaturization and frequency-domain robustness, the proposed design enables neural interfaces compatible with catheter-based deployment and body-coupled transmission.

Index Terms—Neural Interfaces, Low-Noise Amplifier, Amplitude-to-Frequency Conversion, Ultra-Miniaturized, Biomedical Implants

I. INTRODUCTION

Extracellular neural recording requires front-end circuits capable of recording microvolt-level signals within a limited spectral band while operating under strict power and area constraints. Extracellular action potentials typically exhibit amplitudes between 40–500 µV and dominant spectral content in the 300 Hz–6 kHz range [1], [2]. These characteristics impose stringent requirements on input-referred noise, dynamic range, and common-mode rejection. In miniaturized implantable systems, the challenge is compounded by low supply voltages, large electrode–tissue interface impedances, and susceptibility to interference.

Conventional neural recording architectures rely on voltage-domain amplification followed by analog-to-digital conversion [3]. While effective, this approach becomes inefficient in ultra-compact implants where routing complexity, robustness to loading, and transmission through biological media are limiting factors [4]. Frequency-domain encoding provides an alternative strategy in which neural amplitude information is converted into frequency variations prior to transmission. Such encoding improves resilience to amplitude attenuation and is particularly attractive for body-coupled communication (BCC) links [5].

Recent neural front-ends have achieved significant improvements in noise efficiency and power consumption; however, many implementations prioritize multi-channel scalability or high-resolution digitization rather than extreme miniaturization and direct frequency encoding. For catheter-delivered or minimally invasive platforms, a compact architecture combining low-noise differential amplification with amplitude-to-frequency conversion is desirable.

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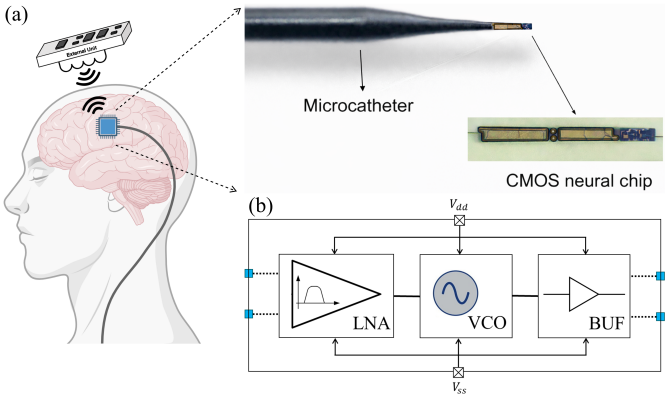

Fig. 1: a) Conceptual illustration of the intravascular probe, where a CMOS neural chip is mounted at the tip of a microcatheter. The inset shows a zoomed view of the chip. b) System-level block diagram of the proposed neural recorder based on frequency-domain encoding and body-coupled communication.

This work presents a CMOS neural front-end integrating a fully differential capacitive-feedback low-noise amplifier (LNA) with a current-starved ring voltage-controlled oscillator (VCO) to perform direct amplitude-to-frequency translation. The design targets ultra-miniaturized neural interfaces compatible with low-voltage operation and electrode impedance variability, with a configuration that is particularly well-suited for intravascular neural recording, where reduced invasiveness and substantial geometric constraints must be addressed together.

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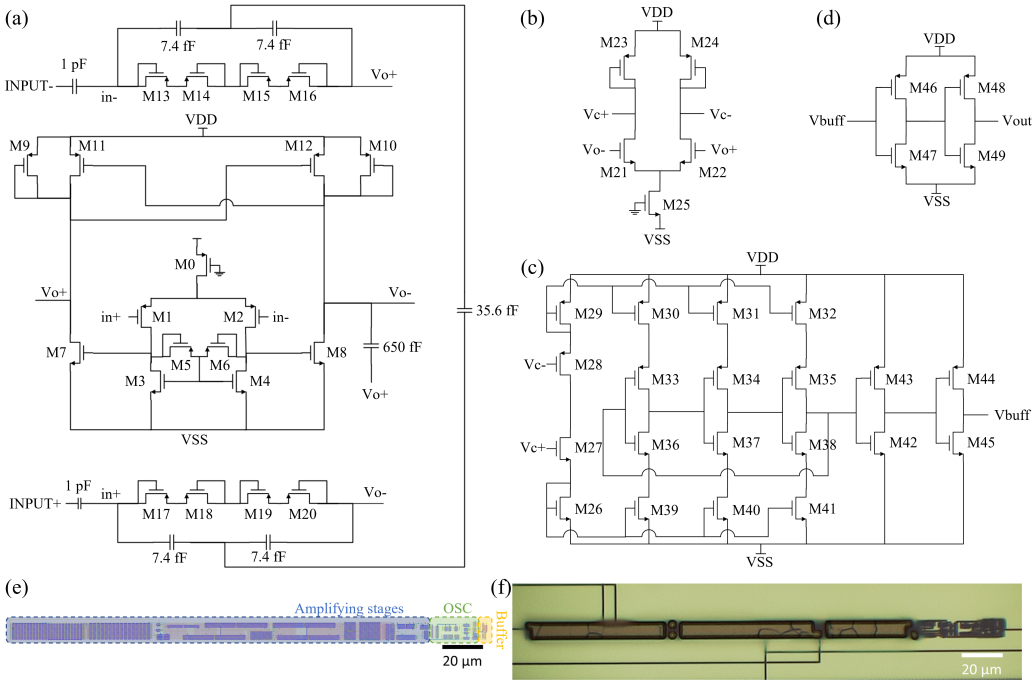

Fig. 2: Schematic of the a) LNA, b) diode-based amplifier for balancing the load of LNA, c) voltage-controlled oscillator and d) buffer to drive the system's load. e) System layout, and f) microphotograph of the fabricated circuit. Supply rails (V_{DD} = +0.6 V, GND = 0 V, V_{SS} = −0.6 V) are externally supplied DC biases, intended to be delivered through the catheter in the target application.

II. INTRAVASCULAR NEURAL RECORDING

Scalp EEG suffers from bio-electric shielding and poor spatial resolution, particularly for deep sources [6]; intracranial EEG offers higher fidelity but requires skull trepanation and its attendant risk. Because the cerebrovascular tree penetrates the whole brain and runs close to active neurons, intravascular recording provides an intermediate route, approaching deep sources with minimal invasiveness and no trepanation. Oxley et al. [7] demonstrated this with a stent-electrode array achieving stable, long-term recordings comparable to epidural ones, validating the vascular compartment for chronic interfacing while underscoring the need for further miniaturization and reduced catheter dependence.

The proposed architecture addresses these needs: by encoding neural signals in the frequency domain before transmission, it eliminates the dedicated analog signal wire, one of the two functional dependencies on the catheter, simplifying the system, improving robustness to the amplitude attenuation of body-coupled links, and advancing toward a fully wire-free intravascular interface.

III. SYSTEM ARCHITECTURE

Fig. 1 illustrates the proposed intravascular neural recording system. The CMOS neural chip is mounted at the tip of a microcatheter to enable intravascular acquisition of neural signals, as conceptually illustrated in Fig. 1(a). The circuit block diagram is shown in Fig. 1(b). Neural signals are sensed differentially using a pair of microelectrodes and amplified by the LNA. The amplified signal modulates a current-starved ring VCO, translating amplitude variations into frequency deviations. The VCO output is buffered through a tapered inverter chain to drive the electrode–tissue load and enable body-coupled transmission.

In the final application of the device, the power is delivered via a catheter, allowing the design to focus specifically on the neural front-end and body-coupled transmission path rather than wireless power delivery. An electrical microelectrode model derived from [8] was incorporated during circuit simulation to evaluate the impact of electrode impedance at both the input and output nodes. Electrical measurements were performed on the packaged chip using PCB-level loading conditions. In the intended application, physical microelectrodes will be directly connected to these nodes.

IV. CIRCUIT IMPLEMENTATION

A. Low-Noise Amplifier

The LNA is implemented as a fully differential capacitive-feedback amplifier. Fig. 2(a) shows the schematic of the LNA. The input capacitor provides AC coupling with a cutoff frequency in the 6 Hz range, while the LNA capacitive loading defines the low-pass cutoff. A T-capacitor network is employed because a similar gain can be achieved with smaller input capacitance [3]. The total output capacitance is 650 fF in parallel with the feedback capacitance, which is much smaller (approximately 7 fF) and therefore negligible.

To avoid loading asymmetry, a diode-based differential amplifier (Fig. 2(b)) with low gain is introduced to provide balanced loading for the LNA. The amplifier is designed with a band-pass response from 10 Hz to 10 kHz to suppress DC drift, reduce low-frequency 1/f noise, and limit high-frequency noise.

The front-end is powered by three externally supplied DC bias levels, V_{DD} = +0.6 V, GND = 0 V, and V_{SS} = -0.6 V. In the intended application, these rails are generated by the proximal external unit and delivered through the microcatheter; equivalently, they form a 1.2-V supply span referenced to its 0 V midpoint. No

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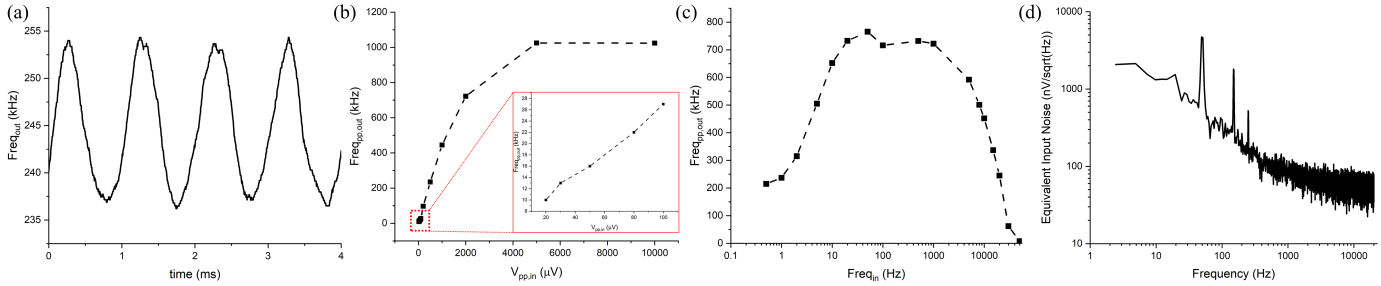

Fig. 3: Measured system performance: (a) instantaneous output frequency for a 50 μV_{pp}, 1 kHz sinusoidal input; peak-to-peak frequency deviation versus (b) input amplitude and (c) input frequency; and (d) equivalent input-referred noise spectral density of the complete frequency-encoding front end.

Table 1: Transistor sizes used in the proposed design.

Transistor	W/L (μm/μm)	Transistor	W/L (μm/μm)
M0	8/0.25	M23, M24, M27	2/4
M1, M2	96/1	M25	2/10
M3, M4	64/1.5	M26	4/2
M5, M6	1/8	M28	6/0.4
M7, M8, M33–M35	1/2	M29	6/1
M9–M12, M36–M38	1/3	M30–M32	2/1.3
M13–M20	2/16	M39–M41	2/2
M21, M22	8/2	M42–M45	2/0.18

negative-voltage generator is integrated on-chip. The fully differential topology improves common-mode rejection and enhances immunity to interference while maintaining the common-mode level within the linear operating range.

B. Voltage-Controlled Oscillator

A current-starved ring VCO (Fig. 2(c)) is employed to enable amplitude-to-frequency conversion. The oscillation frequency is directly set by a bias current modulated by the LNA output voltage, enabling linear voltage-to-frequency tuning with controlled amplitude and reduced power consumption [9].

C. Output Buffer

A cascaded driver consisting of two cascaded inverter stages is designed to drive the output microelectrodes with an area of 100 μm^2. The microelectrode electrical model was derived from our previous work [8]. The schematic of the output buffer is shown in Fig. 2(d). Medium-threshold-voltage transistors M46-M49 were used for better driving strength.

V. ELECTRICAL CHARACTERIZATION

A. CMOS Fabrication and Measurement Setup

Table 1 reports the transistor sizes for the entire circuit. The circuit was fabricated in TSMC 180-nm MS/RF/G technology. The layout and microphotograph of the whole system are shown in Fig. 2(e) and (f), respectively. The total active area is 9.92×252.25 μm^2 (2502 μm^2). The active-core width was kept below 10 μm to facilitate catheter-based deployment. Metal-Insulator-Metal capacitors are used for input capacitors, while Metal-Oxide-Metal capacitors are used in the T-capacitor network to further reduce area.

All measurements were performed on a PCB test platform. A dual-output DC power supply provides the supply voltages of ±600 mV. An oscilloscope was used to evaluate time-domain and frequency-domain responses. Power consumption was measured using a source meter. The output signal was recorded with the oscilloscope and post-processed in MATLAB to extract instantaneous frequency and perform noise analysis.

B. Frequency Translation and Linearity

The results of the full system evaluation are shown in Fig. 3. Fig. 3(a) shows the frequency translation obtained when a 50 μV_{pp}, 1 kHz sinusoidal signal was applied to the LNA input. The output frequency varies between 237 and 254 kHz with a 1 ms modulation period, confirming voltage-to-frequency translation.

Peak-to-peak frequency swing was measured for different input amplitudes and shown in Fig. 3(b). The system remains linear up to $V_{pp,in}$ = 2 mV. For higher amplitudes, saturation occurs due to LNA nonlinearity. The minimum detectable input signal is 20 μV_{pp}. The measured conversion sensitivity is K_{vf} = 347 Hz/μV.

C. Bandwidth and Power Consumption

To determine bandwidth, a sinusoidal signal with $V_{pp,in}$ = 2 mV was applied while sweeping frequency. Fig. 3(c) shows peak-to-peak output frequency swing with respect to input frequency. The −3 dB bandwidth is defined as the input frequency range over which the peak-to-peak frequency deviation drops to 0.707× its maximum value. Using this definition, the measured bandwidth is 6 Hz to 6.7 kHz.

The total measured power consumption of the complete frequency-encoding chain, including the LNA, VCO, and output buffer stages, is 11 μW under PCB loading conditions.

D. Noise Performance

Noise performance of the complete frequency-encoding chain was evaluated by shorting the differential LNA inputs and biasing them at the nominal common-mode voltage. The instantaneous VCO frequency was extracted from the output waveform, converted into a uniformly sampled frequency-versus-time sequence, and processed using Welch power spectral density estimation in MATLAB.

The resulting frequency-noise spectral density was converted to equivalent input-referred noise using the measured sensitivity K_{vf}. The equivalent input-referred noise spectral density is shown in Fig. 3(d). The integrated equivalent input-referred noise is 15.5 μV_{rms} over 6 Hz–6.7 kHz and 5.55 μV_{rms} over the spike band (300 Hz–6 kHz). These values include contributions from the LNA noise, VCO phase noise, and frequency-extraction quantization.

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Table 2: Comparison with state-of-the-art neural-recording architectures.

Work	Year	Tech (nm)	Supply (V)	BW (kHz)	IRN (μV_{rms}, band)	#Channels	Power/Ch (µW)	Area/Ch (mm^2)	Topology
[10]	2021	55	1.2	10.9	5.53 (300–10kHz)	16	48.7	0.0077	2nd-order Δ-ΔΣ
[11]	2022	55	1.2	10	6.26 (AP band)	22	13.75	0.00426	1st-order VCO-based continuous-time Δ-Σ
[12]	2023	180	1.8	10	4.46 (300–10kHz)	8	14.62	0.00462	continuous-time two-step incremental Δ-Σ
[13]	2023	180	1.8	5	5.7 (300–5kHz)	20	40	0.0056	VCO-Timestamping
[14]	2023	22	0.8	10	7.71 (300–10kHz)	128	12.6	0.0050	AC-coupled 1st-order Δ-ΔΣ
[15]	2025	180	0.9	10	6 (1.25–10kHz)	8	11.7	0.09	continuous-time Δ-Σ
[16]	2025	180	1.2	10	11.22 (300–10kHz)	192	9.62	0.00175	TDM OTA-C two-step IΔΣ
This work	**2026**	**180**	**±0.6**	**6.7**	**5.55 (300–6kHz)**	**1**	**11**	**0.0025**	Cap-feedback LNA + open-loop VCO (V–F)

Functional scope: Per-channel area and power in multi-channel designs may benefit from shared circuitry. This work is a complete single-channel AFE–frequency-encoder–driver node without an on-chip ADC or digital backend.

E. Comparison and Discussion

Let $\alpha < 1$ denote the body-channel voltage gain. For amplitude-domain transmission, $v_{RX} = \alpha A_v v_{in} + n_{RX}$; thus, a 20-dB channel loss reduces the received amplitude by 10× and, under receiver-noise-limited conditions, the SNR by 20 dB. In the proposed architecture, $f_{out} = f_0 + K_{vf} v_{in}$. Linear attenuation scales the carrier amplitude but not the encoded frequency deviation; therefore, channel-gain variation does not directly scale the recovered neural signal, provided that the carrier remains detectable. Attenuation nevertheless reduces the carrier-to-noise ratio and may increase frequency-estimation error. From the measured 2 mV_{pp} linear range and 5.55 μV_{rms} spike-band noise,

$$\mathrm{DR} = 20\log_{10}\left[\frac{2\ \mathrm{mV}}{2\sqrt{2}(5.55\ \mu\mathrm{V})}\right] = 42.1\ \mathrm{dB}, \tag{1}$$

corresponding to 6.7 equivalent noise-limited bits. Direct frequency encoding also avoids an on-chip ADC and a dedicated analog signal wire.

Comprehensive PVT characterization was not performed for this first-silicon demonstrator. In the linear region, $f_{out}=f_0(P,V,T)+K_{vf}(P,V,T)v_{in}$. Slow variations of f_0 can be rejected by recovering the frequency deviation relative to the carrier mean, whereas variations of K_{vf} appear as a scalar gain error that could be compensated by per-device calibration. The LNA gain is mainly set by C_{in}/C_{fb}, while the more PVT-sensitive VCO gain is included in the measured conversion sensitivity. The intended regulated supply and narrow intravascular temperature range further limit these variations; complete multi-sample PVT characterization remains future work.

Table 2 compares the proposed design with recent neural front ends. Most prior works are multi-channel ICs whose reported area and power per channel may benefit from shared conversion, biasing, and digital circuitry. These normalized values do not necessarily represent the footprint of an independently deployable single-channel node. The proposed circuit implements the complete AFE–frequency-encoder–driver path in 0.0025 mm^2 with a 9.92 µm active-core width.

VI. CONCLUSION

A compact CMOS neural front-end employing differential amplification and VCO-based amplitude-to-frequency translation has been demonstrated. Fabricated in 180 nm CMOS, the design occupies 0.0025 mm^2 and consumes 11 µW while achieving a 6 Hz–6.7 kHz bandwidth and 5.55 μV_{rms} input-referred noise over the spike band. The architecture enables us to develop an ultra-miniaturized neural interface suitable for catheter-based neural recording deployment in the brain's arteries and veins.

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