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RESEARCH ARTICLE

Robust Vertical Interface Design for Battery Management Systems: EMI Failure Analysis and Countermeasures

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ABSTRACT The rapid electrification of the automotive industry has made the electromagnetic compatibility (EMC) of battery management systems (BMS) a crucial factor in ensuring vehicle safety and reliability. In this paper, the susceptibility of a vertical interface (VIF) to electromagnetic interference (EMI) for digital data transfer between galvanically isolated IC modules is addressed at the IC level. The study begins with a system-level preliminary experimental susceptibility assessment using direct power injection (DPI) tests in compliance with ISO 11452-7. Leveraging transistor-level simulations and fundamental circuit analysis, the primary failure mechanisms and their root causes are identified and mitigated through targeted IC-level countermeasures. The efficacy of these countermeasures is verified via accurate transistor-level simulations and experimental measurements on a test chip fabricated in 110 nm BCD technology. A dual-transceiver peer-to-peer communication setup is employed to rigorously assess the robustness of the bidirectional link under EMI excitation. Experimental results demonstrate a robustness enhancement exceeding 15 dB within the critical 1–10 MHz frequency range, significantly improving the interface's most vulnerable band. This enhancement ensures full compliance with the stringent requirements of automotive BMS applications.

INDEX TERMS Battery management systems (BMS), vertical interface (VIF), electromagnetic interference (EMI), electromagnetic compatibility (EMC), direct power injection (DPI).

I. INTRODUCTION

The widespread adoption of lithium-ion (Li-ion) technology in electric and hybrid electric vehicles (EVs/HEVs) necessitates the development of robust battery management systems (BMS) to ensure their safe and reliable operation [1]. The fundamental role of a BMS is to protect individual battery cells, extend their service life, and enhance cycle efficiency. This functionality is particularly critical in lithium-ion battery technology, where protection against overcharging and thermal excursions is essential to prevent cell degradation or catastrophic failure. To ensure safe operation, continuous monitoring of battery parameters, including cell voltage, temperature, and communication integrity, is performed. Detected anomalies are subsequently communicated to the central control unit.

In this context, electromagnetic interference (EMI) poses a significant threat to BMS operation, particularly in the harsh automotive environments, where high switching currents, long wiring harnesses, and compact module integration create strong sources and coupling paths for interference. Such disturbances can impair analog signal acquisition and digital signal transmission, leading to potential system-level malfunctions [1].

Due to these risks, several studies have investigated the susceptibility of BMS circuits to EMI, consistently demonstrating that digital communication interfaces for inter-module data transfer are significantly more vulnerable than their internal analog sensing circuitry [2], [3]. Initial investigations revealed that communication errors appeared at specific EMI

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frequencies, identifying inter-module links as the dominant failure point [4]. Subsequent studies reinforced this result through standard electromagnetic compatibility (EMC) tests, including direct power injection (DPI) and bulk current injection (BCI) [5], [6]. These tests experimentally confirmed communication failures, their frequency-dependent behavior, and the underlying coupling mechanisms [7], [8], [9], [10].

In response, several countermeasures have been proposed to improve the robustness of communication [11]. Some approaches introduce digital-domain solutions, such as proportional-integral-derivative (PID) based clock-data-recovery (CDR) schemes, to mitigate EMI-induced timing distortions [12]. Others focus on system-level mitigation, including optimized shielding or cable routing to reduce EMI coupling onto data lines [13] and under standardized tests [14], [15]. A further system-level approach is to coordinate the timing of communication with respect to switching noise, thereby reducing the probability that noise and sampling instants coincide [16]. Other works have addressed mitigation mainly through external means, such as filtering, shielding, or link-level architectural choices [17], [18], [19].

In parallel, other sources show that EMI mitigation is often associated with measurable implementation trade-offs. Hybrid active/passive filters can improve attenuation and reduce the required common-mode-choke inductance, but at the cost of increased component count, weight, volume, and cost [20]. Vehicle-level differential-mode filtering and complete traction-voltage-system simulations have also been shown to reduce resonance-related conducted EMI. However, they require subsystem-level impedance information and operate at the vehicle-integration level [21]. Package-level optimization of SiC power modules has demonstrated that reducing parasitic capacitance can lower common-mode EMI and switching losses, but this requires dedicated package and layout co-design [22]. Algorithmic or redundancy-based methods can improve decision robustness under EMI-induced communication errors, but they do not directly suppress the physical coupling or circuit-level failure mechanisms [23]. In addition, studies on analog ICs have shown that conducted EMI can induce large DC offsets in operational amplifiers through nonlinear mechanisms and capacitive coupling to IC terminals, further motivating circuit-level EMI analysis [24].

Despite these advances, the IC-level origin of EMI-induced failures within the transceiver has remained relatively unexplored, particularly regarding nonlinear device behavior, temporary symmetry breaking in the signal path, and the propagation of common-mode disturbances into sensitive internal nodes. This work addresses that gap by providing an IC-level analysis of EMI susceptibility in a capacitive VIF for automotive BMS applications, identifying the dominant failure mechanisms, and validating targeted integrated countermeasures through simulations and measurements.

To place the proposed solution in this context, Table 1 benchmarks representative EMI-robustness approaches using the main EMI-related result reported in each source, together with compact indicators of implementation overhead and power impact. In contrast to approaches acting mainly at the board, package, converter, or system level, the method proposed here directly targets the dominant internal failure mechanisms of the transceiver. This enables a measured DPI immunity improvement without requiring additional off-chip EMC hardware or changes to the overall communication architecture.

The rest of the paper is organized as follows. Section II provides an in-depth discussion of the VIF architecture considered in this work, detailing its data transmission mechanism and key circuit components. Section III introduces the DPI test setup and procedure used to assess the VIF's immunity through experiments, as well as a simulation-oriented model of this setup. Section IV analyzes the EMI-induced failure mechanisms and proposes targeted circuit-level solutions. Section V validates the effectiveness of the proposed approaches through detailed simulations and measurements. Finally, Section VI draws some conclusions.

II. VIF ARCHITECTURE

A typical BMS architecture incorporating a VIF is illustrated in Fig. 1. It comprises multiple front-end integrated circuits (FEICs), each monitoring a subset of the series-connected cells. The number of cells that a single FEIC can handle is limited by the maximum voltage that its semiconductor technology can withstand. Since different FEICs operate at different reference potentials within the battery stack, they must be galvanically isolated from one another; consequently, capacitive [29], [30], or transformer-based coupling [31] is required in differential data lines connecting the different FEICs.

In this work, the capacitively coupled VIF of a BMS IC integrated in 110 nm bipolar-CMOS-DMOS (BCD) technology is analyzed, and its susceptibility to EMI is investigated at the IC level. A functional diagram of the VIF is depicted in Fig. 2. The off-chip network is connected to the transceiver's differential input/output pins (ISO+ and ISO–). It consists of two series resistors (R_{SER}) for ESD current limiting, two filtering capacitors (C_{FIL}) for high-frequency noise suppression, two high-voltage AC-coupling capacitors (C_{CPL}), and an unshielded twisted-pair cable acting as the communication bus. The on-chip part, represented by the blocks within the dashed lines in Fig. 2, includes two internal series resistors (R_{DEV}), the VIF transmitter and receiver, a low-dropout (LDO) regulator, a common-mode voltage source, and an internal switched termination resistor (R_{TER}). These resistive elements are sized to achieve a total series impedance of 120 Ω, matching the characteristic impedance of the twisted-pair cable. The specific values for the passive components in the VIF network are summarized in Table 2.

TABLE 1. Representative semi-quantitative benchmarking of EMI-robustness approaches and comparison with the proposed IC-Level countermeasure strategy.

Reference	Approach / Mitigation Point	Reported Benchmark	Test / Frequency Range	Implementation Overhead	Power Overhead	Limitation vs. This Work
Aiello and Crovetti [8], Aiello [7]	BMS IC susceptibility benchmark	DPI immunity: $<$ 10–13 dB BCI failure: 20 mA	DPI: 1 MHz–2 GHz; BCI: ISO 11452-4	External RC filters	Passive only	Characterization study; no IC-level hardening
Allioua *et al.* [20]	External hybrid EMI filter	CM attenuation: 23.2 dBμA at 1 MHz	Conducted EMI; 1 MHz switching	+37% mass; +26% volume; +135% cost	Active filter	Power-converter emission filtering
Jia *et al.* [25]	In-package common-mode filter	EMI reduction: up to 50 dBμV	10–100 MHz	Package-integrated filter	Passive only	Power-module emission reduction
Qu *et al.* [26]	EV converter EMI mitigation	Resonance reduction: 6.02 dB	16.32 MHz resonance	Capacitor / winding redesign	Passive only	Converter-level mitigation
McGrew *et al.* [27]	Layout / shielding optimization	CM-noise reduction: up to 35 dB	150 kHz–30 MHz	Shielding / filter spacing	Passive only	Layout-dependent solution
Xu *et al.* [28]	Alternative isolated interface	CMTI*: 200 kV/μs	100 Mbps data link	New isolator architecture	2.6 mA at 1 Mbps	Requires interface replacement
This work	VIF IC front-end hardening	DPI improvement: $>$15 dB	DPI: 1 MHz–1 GHz	Local devices; 42.4×10^3 μm^2	$\approx$0 static	VIF-specific implementation

*CMTI: common-mode transient immunity.

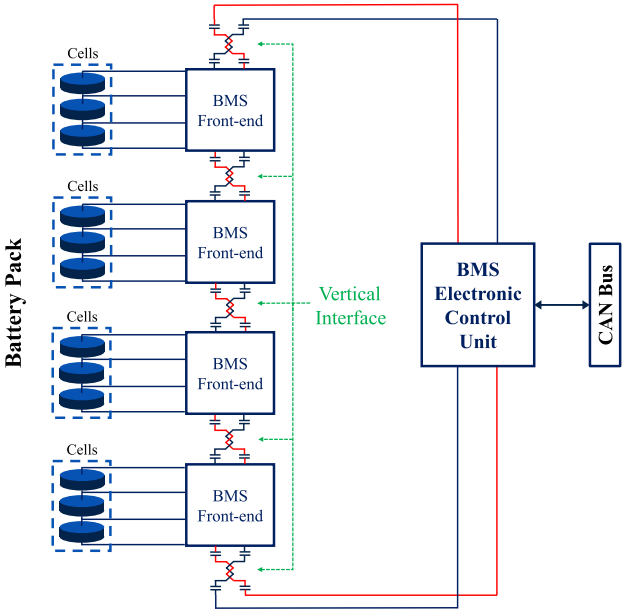


FIGURE 1. A typical BMS structure.

TABLE 2. VIF passive component values and parameters.

Component	Symbol	Value	Location
Filtering Capacitor	C_{FIL}	100 pF	Off-Chip
AC-Coupling Capacitor	C_{CPL}	8.8 nF	Off-Chip
Series Resistance	R_{SER}	40 Ω	Off-Chip
Series Resistor	R_{DEV}	12 Ω	On-Chip
Termination Resistor	R_{TER}	13 Ω	On-Chip
Common-Mode Resistor	R_{CM}	5 kΩ	On-Chip

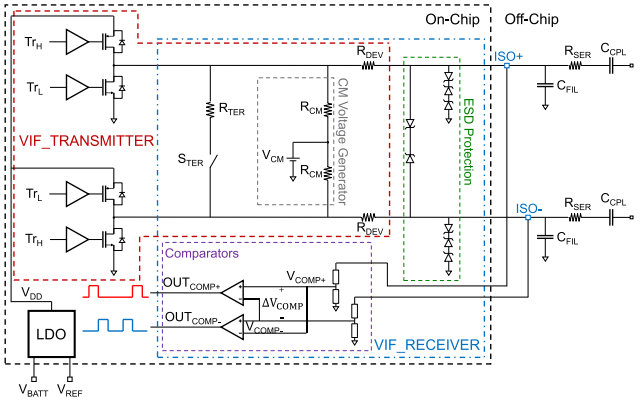


FIGURE 2. Schematic view of the VIF considered in this work.

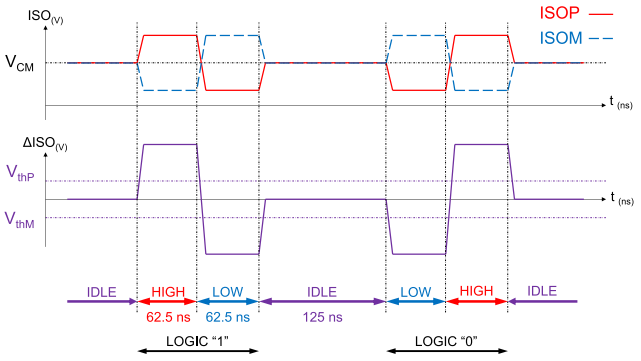


FIGURE 3. VIF protocol waveforms.

The VIF transceiver employs a proprietary differential signaling protocol operating at 4 Mbit/s, as illustrated in Fig. 3. In detail, the communication protocol encodes data bits into differential pulses: a logic "1" is encoded as a positive differential (high) pulse of 62.5 ns followed by a negative (low) pulse of 62.5 ns; conversely, a logic "0" is encoded as a low pulse followed by a high pulse. A mandatory idle phase of 125 ns separates each bit.

Electrically, each differential pulse is generated by driving the complementary switches S_H and S_L in the transmitter. To create a positive differential pulse, the S_H switches connect the upper branch to the supply voltage (VDD =

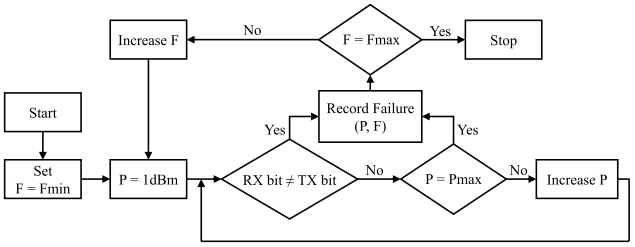


FIGURE 4. Flowchart of the DPI test procedure.

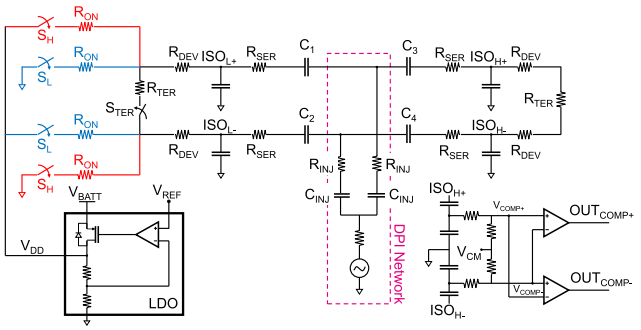


FIGURE 5. DPI test structure for the proposed VIF.

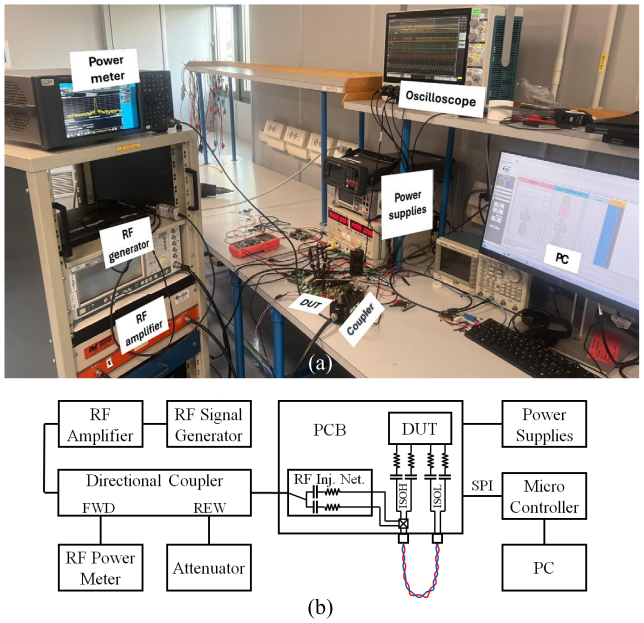


FIGURE 6. Experimental DPI test setup: (a) photograph of the laboratory bench and (b) functional block diagram of the measurement.

5 V) and the lower branch to ground. Conversely, a negative pulse is obtained by closing S_L and opening S_H. Initially, the transmitter's internal termination resistor (R_{TER} in Fig. 2) is connected across the lines to provide source termination; it is subsequently disconnected for the remainder of the idle phase to minimize quiescent power consumption. This two-step process ensures that the line remains stable during idle periods, reducing power consumption and preparing the system for the next data transmission.

At the receiver side, the VIF differential signals are processed by two voltage comparators, which detect when the differential input signal crosses predefined threshold voltages (V_{thP} and V_{thM} in Fig. 3), set to ± 20 mV to ensure reliable signal recovery. The comparators' output triggers internal digital logic that reconstructs the transmitted bits.

To assess the EMI susceptibility of this architecture, Section III describes the results of Direct Power Injection (DPI) testing [32]. The analysis of the failure mechanisms uncovered by these tests is then presented in Section IV.

III. DPI TEST SETUP

This section describes the DPI test method, performed in compliance with IEC 62132-4 [32] to assess the EMI susceptibility of the initial VIF prototype. Simulations were then used to replicate this test and gain insight into the observed failure mechanisms. The overall automated test procedure is summarized in Fig. 4.

A. EXPERIMENTAL TEST SETUP

In DPI tests performed in compliance with IEC 62132-4, a controlled RF disturbance is injected into the device under test (DUT) through a capacitive coupling network, as shown in Fig. 5.

The experimental arrangement used for these measurements is illustrated in Fig. 6, comprising a photograph of the laboratory bench (Fig. 6 (a)) and a corresponding functional block diagram (Fig. 6 (b)). While official compliance trials were conducted in a shielded chamber, the bench setup in Fig. 6 (a) was specifically developed to replicate the chamber environment for thorough debugging and correlation. The setup includes an RF generator, an amplifier, and a power meter. An oscilloscope is also used for signal monitoring. The DUT is mounted on a dedicated test board and connected to power supplies and a PC for control and data logging.

A microcontroller serves as the communication leader, coordinating data transfer between the two identical VIF transceivers integrated on the same DUT. Digital data from the computer is transferred via the microcontroller to one VIF interface, which acts as the transmitter. This VIF transmits the differential signal through the off-chip network and the unshielded twisted-pair cable to the receiving interface on the die. The second VIF acts as the receiver, reconstructing the digital data and sending it back to the computer via the microcontroller for final comparison.

In the ISOH-TX mode, the DUT transmits data from the ISOH port to the ISOL port. Conversely, in the ISOH-RX mode, the data path is reversed: the DUT transmits from the ISOL port and receives the signal at the ISOH port. This loopback structure, featuring independent transmitter and receiver roles for each interface, enables a comprehensive assessment of bidirectional link robustness on a single chip.

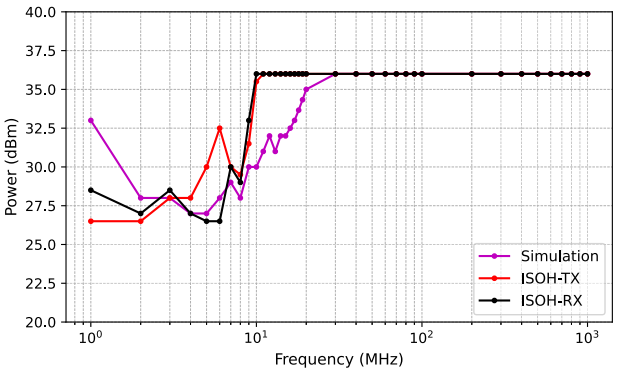


FIGURE 7. Comparison between the measured susceptibility levels of the VIF in transmitter (ISOH-TX) and receiver (ISOH-RX) modes, and the susceptibility level obtained from simulation.

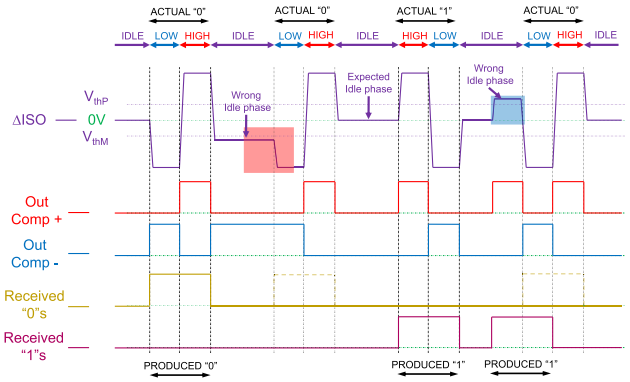


FIGURE 8. Different communication errors observed due to idle phase misbehavior.

The direction of differential data transfer is selected through the graphical user interface (GUI) control. Regardless of the data flow direction, the RF disturbance is consistently injected into the ISOH pin to establish a uniform interference reference. After each transmission cycle, the microcontroller retrieves the reconstructed data, compares it with the original sequence, and logs any mismatch as a communication failure.

B. MEASUREMENT RESULTS

The susceptibility levels for the two operating modes were measured and are plotted in Fig. 7 (see the ISOH-TX and ISOH-RX curves).

A key observation from these results is that the VIF's EMI susceptibility is worse at low frequencies, with all communication failures occurring between 1 MHz and 10 MHz. Above 10 MHz, the device showed no failures even at the maximum injected power of 36 dBm.

An analysis of the communication failures revealed two primary failure mechanisms. The first is data loss, which occurs when the differential voltage at the comparator inputs $\Delta V_{COMP} = V_{COMP+} - V_{COMP-}$ fails to cross the required threshold voltage V_{th} (see Fig. 5). The second, more complex mechanism involves the generation of unintended pulses during the idle phase, leading to errors in two distinct ways, as illustrated in Fig. 8 and described hereafter.

1) COMPLETE IDLE-PHASE PULSE DISTORTION

An unintended pulse persists through the entire idle phase and merges with the subsequent data pulse, rendering the bit unrecognizable (red-shaded region in Fig. 8). This type of failure occurs when the idle phase and the following data pulse activate the same comparator.

2) PARTIAL IDLE-PHASE PULSE DISTORTION

An unintended pulse appears in the second half of the idle phase. It disrupts the encoding process, leading to erroneous interpretation of data bits. Specifically, if a negative (or positive) pulse is generated during the idle phase just before a logic "1" (or "0"), the receiver mistakenly decodes it as a logic "0" (or "1"). This behavior is highlighted in blue in Fig. 8. Such errors occur when the idle-phase pulse and the first pulse of the subsequent data bit activate opposite comparators.

C. SIMULATION SETUP AND MODELING

To investigate the root causes of failures at the IC level, a model of the DPI test-bench has been implemented in the Cadence Virtuoso environment and analyzed in the time domain using Spectre. The on-chip circuitry was modeled using MOSFET and passive device models from the STMicroelectronics BCD Process Design Kit (PDK). In contrast, off-chip passive components are modeled as ideal elements. At the relatively low frequencies of interest (below 10 MHz), high-frequency parasitics such as equivalent series resistance (ESR) and cable resonance effects are negligible and therefore have been omitted. The twisted-pair cable is modeled as a simple lumped connection for the same reason: its length (less than 2 m) is electrically short at low frequencies. Therefore, detailed transmission-line modeling [33], [34] is unnecessary.

D. SIMULATION VS. MEASUREMENT COMPARISON

The DPI simulation results are plotted in Fig. 7 and compared with measurement results, revealing good overall agreement, especially in the 1-10 MHz frequency range where the VIF is most vulnerable. The largest deviation is observed around 1 MHz, i.e., near the onset of the critical susceptibility region.

In this condition, the measured susceptibility is determined by the first occurrence of a communication failure, so even a small difference in the internally disturbed waveform may translate into an appreciable shift in the failure threshold expressed in dBm. This sensitivity is particularly relevant at low frequencies, where the RF period is comparable with several VIF transmission intervals, and the relative phase between the injected disturbance and the transmitted bit sequence strongly affects the voltage margin at the comparator input. This behavior was discussed in the preliminary simulation study in [35], where low-frequency

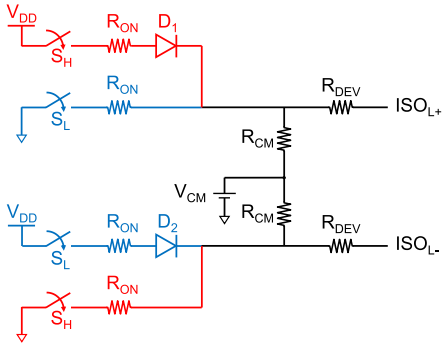


FIGURE 9. VIF structure with protective diodes.

failures were correlated with degradation of the comparator input signal-integrity parameters. Moreover, the transfer path between the RF injection point and the internal TX/RX nodes includes filtering effects due to extrinsic elements and parasitic components. Near the onset of the susceptible region, small differences in this low-pass coupling path may cause a notable shift in the measured threshold relative to the simplified simulation model. Consequently, although the exact threshold at 1 MHz may differ, the simulation correctly reproduces the vulnerable low-frequency region and the dominant physical mechanisms responsible for the observed susceptibility.

IV. FAILURE MECHANISMS ANALYSIS AND DISCUSSION

This section provides an in-depth investigation of EMI-induced failure mechanisms at the IC level, aiming to identify their root causes and propose effective mitigation strategies.

A. EMI-INDUCED LDO VOLTAGE REGULATOR FAILURES

In the proposed VIF architecture, an on-chip LDO regulator is essential to provide a stable low-voltage supply to the transceiver's sensitive analog and digital blocks.

One specific failure mechanism identified through DPI simulations concerns EMI-induced failures in the LDO regulator [36], [37], [38]. In detail, during the positive half-cycles of the DPI RF excitation, the voltage across the ISO lines may temporarily exceed the VIF transmitter's LDO-regulated supply voltage. Consequently, if one of the pull-up switches in the transmitter is ON, the LDO regulator output is directly driven by the ISO line at a high voltage through a low impedance. This condition induces a large reverse current into the regulator's output, resulting in a sharp transient. The resulting current spikes charge the regulator's output capacitor, potentially causing circuit stress or triggering internal protections, which can damage the LDO regulator.

To mitigate this issue, two protective diodes D_1 and D_2 are introduced in series to the pull-up MOSFETs of the transmitter, as illustrated in Fig. 9.

When the ISO lines are driven by EMI above the LDO supply voltage, the diodes turn off, disconnecting the ISO lines from the LDO output. Consequently, the amplitude

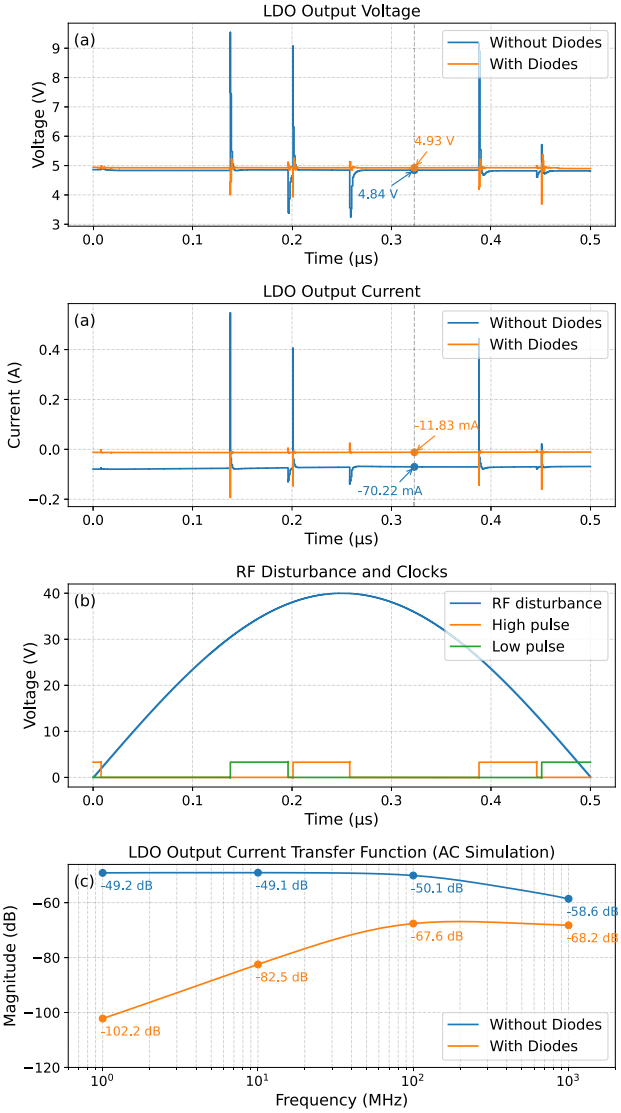


FIGURE 10. LDO regulator output simulations with and without diodes: a) the LDO regulator output current and voltage, b) 1 MHz RF signal along with clocks for a half positive period of the RF signal, c) Transfer function amplitude from EMI source to LDO regulator output current.

of the reverse current injected into the LDO via capacitive coupling is significantly attenuated, thereby preserving regulator functionality. This is illustrated in Fig. 10 (a), which presents simulation results comparing transient responses of both the current and voltage at the LDO regulator output before and after the introduction of the diodes. Concurrently, Fig. 10 (b) illustrates the corresponding RF disturbance and pulse timing on the same time axis. Without the diodes, positive EMI-induced disturbances result in current spikes up to approximately 830 mA and voltage peaks around 9 V. With the diode, current spikes are reduced to less than 50 mA, and voltage peaks are suppressed to approximately 5.5 V.

To further support the transient results, the small-signal coupling from the RF injection node to the LDO supply path was also evaluated through AC simulation. For this

purpose, the RF disturbance was modeled as a small-signal AC voltage source $V_{RF,ac}$ with an internal resistance of 50 Ω, applied at the same injection node used in the transient setup. The original LDO block was replaced by an ideal 5 V source preserving the output connection. The quantity reported in Fig. 10 (c) is the magnitude of the current flowing through this source, i.e., the transfer function from the injected RF voltage to the LDO supply current. The results confirm that the insertion of diodes D_1 and D_2 strongly attenuates the coupling from the injected disturbance to the LDO supply path, especially in the low-frequency region where this failure mechanism is most critical. Specifically, at 1 MHz, the transfer function magnitude decreases from approximately −49 dB without the diode to −102.2 dB with the diode. Similarly, at 10 MHz, it decreases from −49 dB to −82.5 dB. The observed difference between the AC and transient simulation results, which is larger in AC than in transient, is due to the circuit's inherent nonlinearities, which are not fully captured by the linear AC simulation.

Finally, the LDO output voltage and current waveforms exhibit a DC offset under EMI excitation. This offset is due to the nonlinear behavior of the operational amplifier's differential input stage within the LDO under high-frequency EMI. Such EMI can cause rectification effects within the amplifier, leading to a shift in the mean output level. This phenomenon has been documented in literature [37], [39], [40], where EMI-induced distortion in differential stages results in output offset voltages due to nonlinear demodulation of high-frequency interference signals. This DC value shift can be seen in Fig. 10 (a), where the presence of the diode reduces the DC offset in voltage and current by approximately 10 mV.

More generally, this mechanism illustrates how externally disturbed I/O nodes can inject unwanted current into internal supply-regulation paths whenever low-impedance conduction paths are present during switching operation.

It is worth noting that the diodes D_1 and D_2 were already included in the prototype used for the measurements presented in Fig. 7. Nevertheless, this failure mechanism is detailed here to provide a more comprehensive assessment of the device's susceptibility profile and to rigorously justify the inclusion of such protective components in the final design.

B. CM-TO-DM CONVERSION IN TRANSMITTER AND IDLE PHASE FAILURES

While diodes D_1 and D_2 effectively protect the LDO against EMI-induced failures when the transmitter is active, their introduction leads to failures observed during the idle phase.

Ideally, in the absence of EMI, the common-mode excitation does not generate any differential disturbance because the two ISO branches are electrically symmetric. As shown in Fig. 11 (a), the current injected into the coupling capacitors during the high pulse is balanced by the current flowing during the subsequent low pulse ($I_H \approx I_L$), so that the net stored differential charge is nearly zero, and the

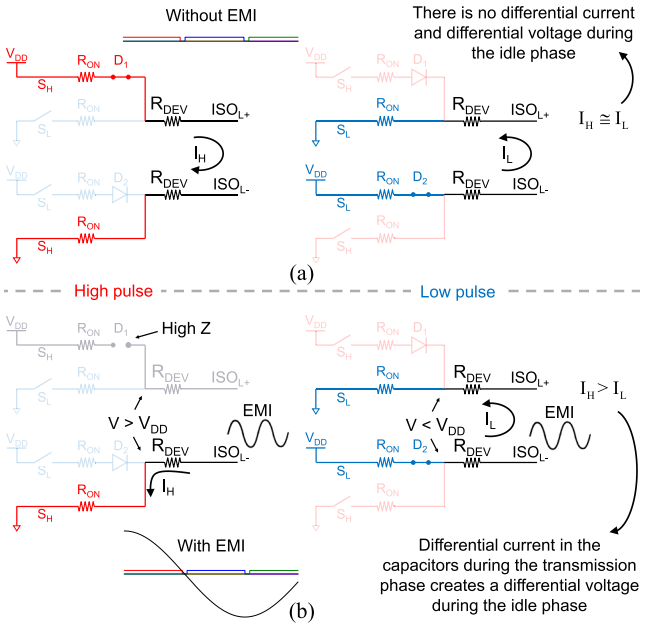


FIGURE 11. Pictorial representation of the failure mechanism: (a) Balanced currents during high and low pulses without EMI, leading to zero differential voltage; (b) when a sufficiently large common-mode EMI temporarily turns off one diode, the branch symmetry is broken, the capacitor currents become unequal, and the resulting unbalanced stored charge appears as a differential disturbance during the idle phase.

differential voltage settles back to zero during the idle phase.

In the presence of sufficiently large common-mode EMI, this symmetry is no longer preserved. As illustrated in Fig. 11 (b), when the EMI-driven common-mode voltage exceeds V_{DD} during part of a transmission pulse, one of the protection diodes becomes reverse-biased and temporarily disconnects that branch from the supply, creating a high-impedance condition. At that point, the two branches no longer experience the same boundary conditions: the branch that remains connected is still referenced to the supply, while the injected EMI mainly drives the disconnected branch. As a result, the common-mode excitation produces unequal branch currents during the high- and low-pulse phases.

This current imbalance causes unequal charge accumulation on the AC-coupling capacitors C_1, C_2, C_3, and C_4. Therefore, even though the external disturbance is applied as a common-mode signal, it is converted into a residual differential voltage because the capacitor charges stored in the two high- and low-pulse phases are no longer equal. This residual voltage appears at the beginning of the idle phase as an unintended differential pulse and, if it exceeds the comparator threshold V_{th}, it leads to erroneous pulse detection.

In other words, the CM-to-DM conversion is not caused by the common-mode excitation alone, but by the temporary loss of symmetry introduced by the diode cutoff during the transmission phase.

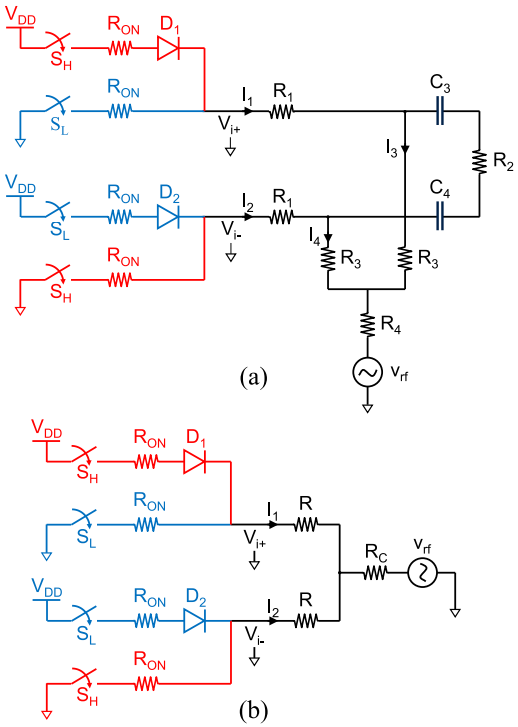


FIGURE 12. Simplified equivalent circuits used for analytical evaluation: a) initial model including C_3 and C_4; b) resistive model after simplification.

This behavior is not unique to the present VIF but is representative of a broader class of EMI-induced failures in differential links whenever nonlinear device behavior temporarily breaks branch symmetry.

To further analyze this behavior, the simplified equivalent circuit shown in Fig. 12 is employed. As detailed in Appendix, this model retains only the coupling capacitors C_3 and C_4 and capacitors C_1, C_2, and C_{INJ} are neglected, while the switches (S_H, S_L) and on-resistances (R_{ON}) model the transmitter state.

For further simplification, capacitor voltages during each sub-period (high pulse, low pulse, and idle phase) are approximated as nearly constant. Under this assumption, the capacitors C_3 and C_4 in Fig. 12 (a) can be temporarily modeled as ideal voltage sources corresponding to their initial condition. The resistances R and R_C represent the simplified resistor network obtained through star-to-delta and delta-to-star transformations, as described in Appendix.

At the end of each transmission sub-period, the resulting voltage variation (ΔV_C) across each capacitor is evaluated as:

$$\Delta V_C = \int_t^{t+\Delta t} \frac{i_C(t)}{C}\, dt \tag{1}$$

where $i_C(t)$ is the capacitor current during the considered sub-period, C is the capacitance, and Δt represents the duration of the sub-period. By evaluating this integral, the differential voltage induced at the comparator input can be estimated.

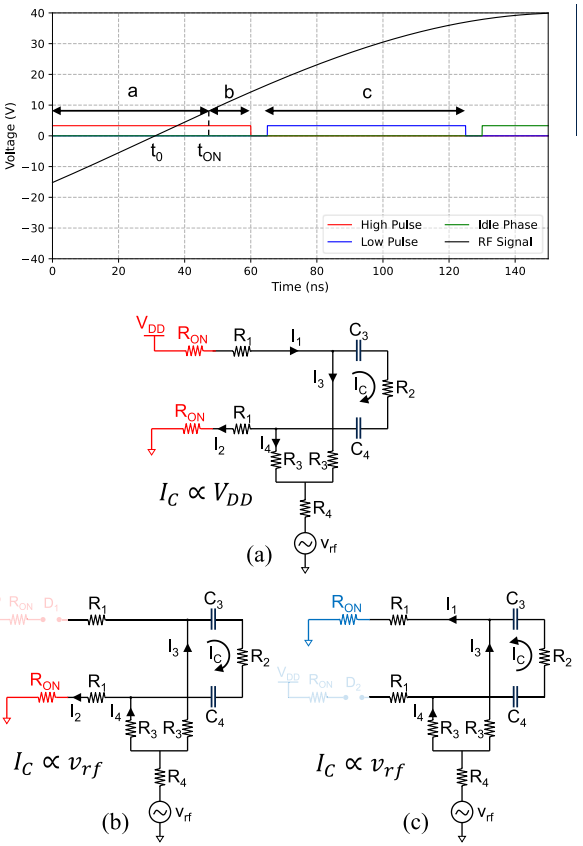


FIGURE 13. Time intervals and corresponding equivalent circuits for the worst-case failure scenario under EMI. The top plot shows the different time intervals (a, b, and c) created by a 2 MHz RF disturbance. The bottom diagrams show the equivalent circuit for each respective interval.

The worst-case scenario for generating a large differential voltage arises from the interplay between the high-pulse and low-pulse phases of data transmission. During the high pulse, the EMI-induced current flows in one direction, while during the low pulse, it flows in the opposite direction. This behavior causes the differential voltages across the capacitors in these two periods to cancel each other partially. It follows that the most severe condition arises when this cancellation is minimized, yielding the largest possible net differential voltage at the start of the idle phase. One example of this scenario is depicted in Fig. 13, showing an RF disturbance at 2 MHz.

The circuits are shown in Fig. 13 (a) to (c) for the different states of the diodes at their corresponding time intervals. It can be seen that the capacitors' current (I_C) varies in magnitude and direction depending on the diode states. In state (a), the circuit is symmetric, so the common-mode EMI does not generate a differential current (the current from V_{DD} is not considered in this analysis). Accordingly, the net differential voltage is the sum of the contributions from the high and low pulse periods (intervals b and c), as shown in the initial integral form:

$$\Delta V_C = \int_{t_0+t_{ON}}^{t_H} -\frac{2i_C}{C} dt + \int_{t_H}^{2t_H} \frac{2i_C}{C} dt \tag{2}$$

The terms in (2) are defined as follows. The variable t_H is the high pulse duration (62.5 ns), and t_0 is the RF signal starting time, representing the phase shift between the data bit and the sinusoidal RF signal. The term t_{ON} represents the time elapsed from t_0 until the RF signal reaches the voltage required to disconnect one of the transmitter diodes; this period can be calculated and is frequency-dependent.

The calculation of t_{ON} relies on the simplified resistive network depicted in Fig. 12 (b). This network acts as a voltage divider, attenuating the injected RF source voltage (v_{rf}) before it appears at the common-mode node. The diode disconnects only when this attenuated common-mode voltage reaches a specific fixed threshold. Since the RF excitation is sinusoidal ($V_{RF}\sin(\omega t)$), the time required for the signal to rise from zero to this specific disconnection threshold depends directly on the EMI angular frequency (ω).

The capacitance $C/2$ is the equivalent of the two series capacitors (C). Finally, i_C is the current through these capacitors. During the asymmetric conduction phases, when either the current i_1 or i_2 is zero, i_C is approximately equal to $i_2/3$ or $i_1/3$, respectively.

Considering that the EMI-induced current is sinusoidal, $i_{1,2} = V_{RF}\sin(\omega(t-t_0))/R_T$, and defining a constant $K = 2V_{RF}/3CR_T$, where $R_T = R_{ON} + R + R_C$ according to Fig. 12 (b), solving the integrals yields ΔV_C as a function of the initial phase, t_0:

$$\Delta V_C = \frac{K}{\omega}[2\cos(\omega(t_H - t_0)) - \cos(\omega(2t_H - t_0)) - \cos(\omega t_{ON})] \tag{3}$$

To identify the worst-case failure condition, the expression for ΔV_C in (3) is maximized with respect to the initial phase t_0, which gives the maximum ΔV_C for a given frequency and EMI amplitude (V_{RF}).

The resulting maximum capacitor voltage translates to a differential voltage at the comparator input, ΔV_{COMP}:

$$\Delta V_C = \alpha \cdot \Delta V_{COMP} \tag{4}$$

The factor α is determined by the circuit element values found to be 47.5 in the proposed VIF. However, a communication failure depends on the cumulative ΔV_C over multiple bits, as the voltage from a preceding bit does not fully decay before the subsequent bit arrives. This accumulation is governed by the idle-phase RC time constant (τ).

To model this, a worst-case scenario is assumed in which each transmitted bit generates the same ΔV_C, multiplied by a decay factor. The total differential voltage, ΔV_{C_T}, is defined by the infinite geometric series, where each term is the contribution from a next bit decayed over one or more bit periods ($T_{bit} = 1\,\mu$s):

$$\Delta V_{C_T} = \Delta V_C \sum_{n=0}^{\infty} e^{-nT_{bit}/\tau} \simeq 2.1 \cdot \Delta V_C \tag{5}$$

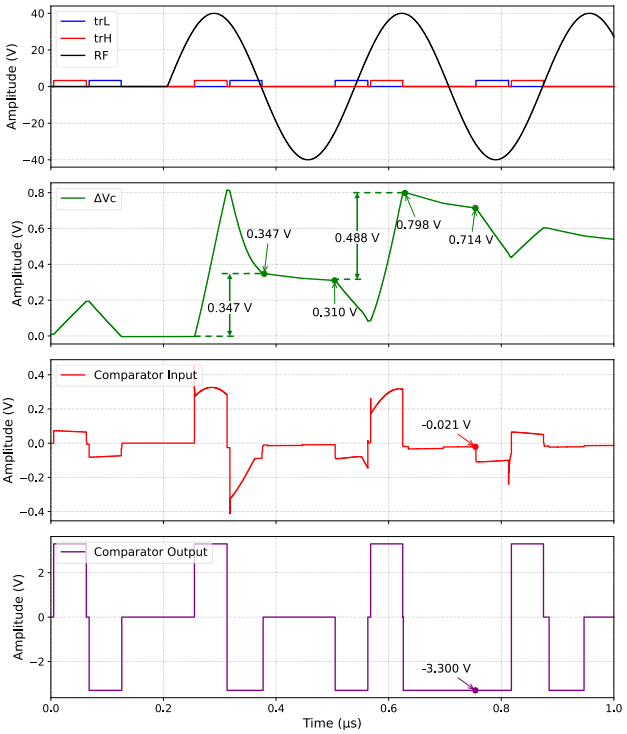


FIGURE 14. Example of constructive accumulation of ΔV_C over multiple bit periods, showing the comparator input voltage eventually crossing the threshold and causing an error before the fourth bit.

A communication failure occurs when this cumulative voltage ΔV_{C_T} exceeds the effective comparator threshold $\Delta V_{C_{th}} = \alpha \cdot V_{th}$, which implies that the ΔV_C generated by a single bit must be greater than $\Delta V_{C_{th}}/2.1$. This constructive accumulation, visualized in Fig. 14 , demonstrates how residual voltages from successive bits cumulatively exceed the threshold, triggering failure at lower RF amplitudes than a single-bit analysis would predict. By substituting the threshold condition into the inverse of (3), the critical RF voltage (V_{RF}) for failure is determined:

$$V_{RF} = \frac{\frac{\Delta V_{C_{\text{th}}}}{2.1} \cdot \frac{3\omega CR_T}{2}}{2\cos\big(\omega(t_H - t_0)\big) - \cos\big(\omega(2t_H - t_0)\big) - \cos\big(\omega t_{ON}\big)} \tag{6}$$

The EMI susceptibility versus frequencies based on the approximate analysis proposed above is plotted in Fig. 15 and compared with simulations and measurement results.

As shown, the analytical model is in reasonable agreement with both the simulation and measurement results. The deviation between the analytical curve and the experimental data can be attributed to several factors. For instance, the model is inherently simplified and does not account for all circuit parasitics. Furthermore, the model accounts only for the idle-phase failure mechanism, while other causes, such as the signal suppression discussed in Section III-B, also

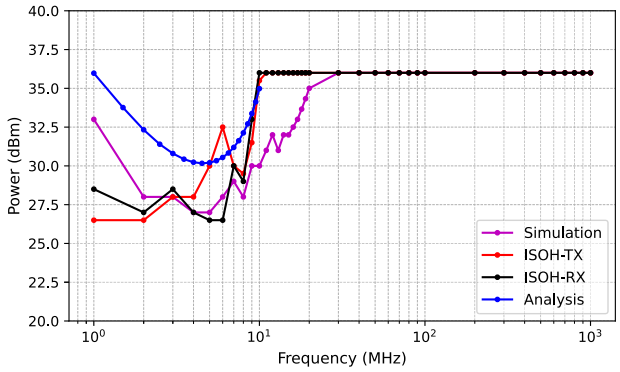


FIGURE 15. Susceptibility level of the VIF for analytical model, simulation, and measurement results.

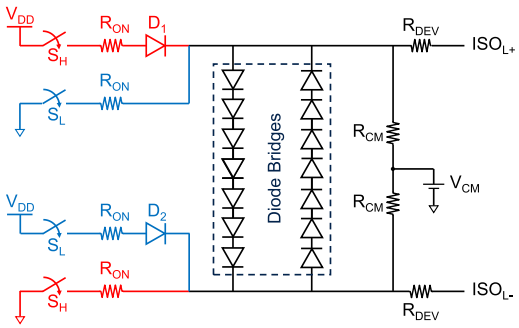


FIGURE 16. Schematic view of the diode strings to clamp the differential voltage.

contribute to overall susceptibility. Finally, the model was simplified by considering only capacitors C_3 and C_4 and did not account for certain practical conditions, such as the brief period ($\sim$ 5 ns) between high and low pulses.

C. COUNTERMEASURE

To prevent such distortions, two anti-parallel diode strings are connected across the differential signal lines, as shown in Fig. 16. In standard data transmission, the differential pulse amplitude remains below the forward-bias threshold of these diodes, ensuring they remain off without affecting the circuit operation. However, when EMI induces a large differential voltage during an idle period, the diodes become forward-biased, creating a low-impedance path that effectively clamps the DM voltage to the diodes' forward drop. This clamping action prevents the differential line voltage from significantly exceeding its nominal value, thereby avoiding failures related to incorrect pulse detection in the idle phase, as highlighted in Fig. 8.

The effectiveness of this approach is validated through simulations, in which the differential voltage between the input and output of the comparators is shown in Fig. 17. As shown in the results, the solution maintains a stable, near-zero differential voltage, preventing communication errors that would otherwise occur.

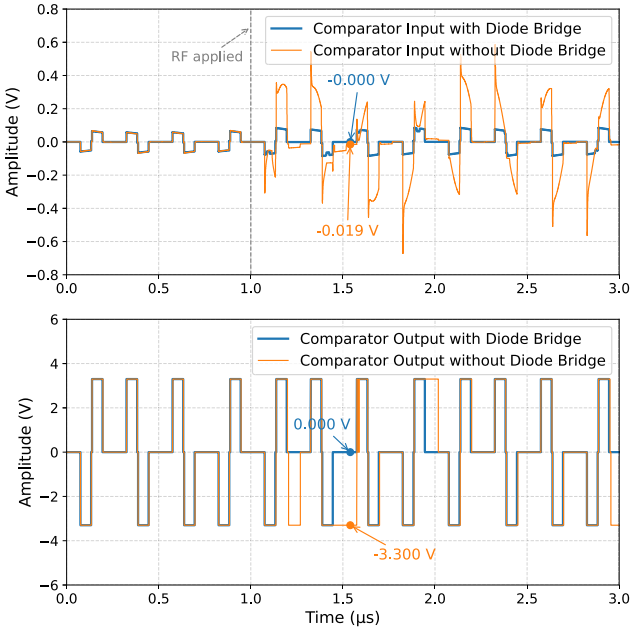


FIGURE 17. Comparison of comparator input and output waveforms with and without the diode bridge countermeasure under EMI excitation.

D. COMMON MODE VOLTAGE PROPAGATION TO COMPARATOR INPUT

EMI coupled onto the ISO lines propagates to the inputs of the receiver comparators. Under ideal conditions, it results in common-mode (CM) interference and does not affect the comparators' operation as long as it stays within their CM input range (CMIR). However, if the amplitude of the common-mode voltage

$$V_{\mathrm{CM}} = \frac{V_{\mathrm{COMP+}} + V_{\mathrm{COMP-}}}{2} \tag{7}$$

exceeds the CMIR, the comparators' operation is impaired, causing erroneous bit decisions.

More generally, receiver susceptibility can arise whenever RF common-mode propagation drives internal sensing nodes beyond the functional input range of the front-end comparator or receiver stage.

To predict CM fluctuations at the voltage comparator inputs, an AC simulation was performed to estimate the transfer function magnitude $|H(f)|$ from the EMI source to the comparator's CM input under a fixed transmitter state: the high pulse, the low pulse, and the idle phase. Since the circuit is symmetric, the results for the high- and low-pulse transmission phases are identical. Fig. 18 shows that the circuit in the idle phase has a higher $|H(f)|$ than the circuit in the transmission phase. It also shows that $|H(f)|$ remains relatively constant at lower frequencies (up to approximately 10 MHz), which is particularly relevant as failures predominantly appear within this range.

To quantify how the transfer function influences the EMI amplitude leading to comparator failure, the following analysis was conducted:

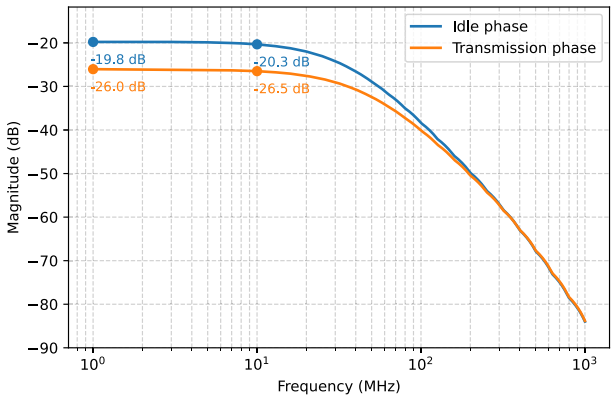


FIGURE 18. EMI to comparators' CM transfer function.

The V_{CM} seen at the input of the comparators and influenced by the EMI is defined as:

$$V_{\mathrm{CM}} = V_{\mathrm{CM}_{DC}} \pm V_{\mathrm{EMI}} \cdot |H(f)| \tag{8}$$

where $V_{CM_{DC}}$ is the DC bias of the comparators (0.83 V). This voltage must remain within the CMIR, defined by $V_{CM_{MIN}}$ and $V_{CM_{MAX}}$. The maximum EMI amplitude ($V_{\mathrm{EMI}_{\mathrm{MAX}}}$) compatible with the operation of the comparators within their CMIR is therefore:

$$V_{\mathrm{EMI}_{\mathrm{MAX}}} = \min\left(\frac{|V_{\mathrm{CM}_{\mathrm{MAX}}} - V_{\mathrm{CM}_{\mathrm{DC}}}|}{|H(f)|}, \frac{|V_{\mathrm{CM}_{\mathrm{MIN}}} - V_{\mathrm{CM}_{\mathrm{DC}}}|}{|H(f)|}\right) \tag{9}$$

For the specific VIF IC considered in the paper, the critical threshold for $|H(f)|$ is approximately 0.045 at an EMI amplitude of 40 V. Consequently, when $|H(f)| > 0.045$, the EMI amplitude causing CM input range violations is lower than 40 V, indicating potential susceptibility.

To mitigate this failure mechanism, the amplitude of CM EMI at the comparator input must be attenuated, but off-chip CM chokes would increase the component count and the cost, and on-chip RC filters on the ISO lines would be area-intensive and attenuate both the CM EMI and the higher frequency components of the nominal signal, resulting in signal degradation. Aiming to overcome such limitations of filtering-based approaches, an active clamp circuit is introduced. As illustrated in Fig. 19, this clamp consists of complementary diode pairs (D_5–D_8) configured to limit positive and negative CM voltage excursions to predefined safe thresholds defined by the voltages V_{POS} and V_{NEG}.

In detail, for the positive clamp, the CM voltage of the ISO lines is extracted by a resistive voltage divider, comprising matched resistors and the high-impedance M_{n3}–M_{n4} (M_{p3}–M_{p4}) MOS pairs. This extracted voltage is applied to the gates of two identical, well-matched NMOS devices M_{n1}–M_{n2}, level-shifted by an offset voltage source V_{POS}, resulting in a gate-source voltage of:

$$V_{GS,n} = V_{CM} - V_{POS} \tag{10}$$

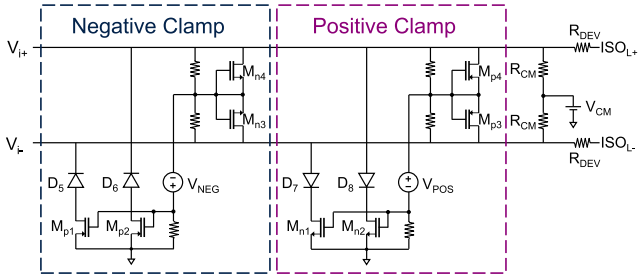


FIGURE 19. Simplified schematic of the clamp circuit.

As such, when

$$V_{GS,n} = V_{CM} - V_{POS} > V_{TH,n} \Rightarrow V_{CM} > V_{POS} + V_{TH,n} \tag{11}$$

i.e., when the CM voltage exceeds the maximum limit $V_{POS} + V_{TH,n}$, the NMOS transistors are turned ON and operate in the saturation region. In this state, they act as active current sources drawing identical currents from both ISO lines, which effectively suppresses the CM voltage within the functional window without degrading the differential-mode impedance.

Similarly, for the negative clamp, two well-matched PMOS devices M_{p1}–M_{p2} are used. Their operation is governed by:

$$V_{SG,p} = -V_{CM} - V_{NEG} > V_{TH,p} \Rightarrow V_{CM} < -V_{NEG} - V_{TH,p} \tag{12}$$

When the CM voltage falls below this minimum, the PMOS transistors turn ON to sink identical currents from the ISO lines, thereby raising the CM voltage back into the functional range.

To prevent the drain-body junctions of the NMOS (PMOS) clamp devices from becoming forward-biased during opposite voltage swings (e.g., when ISO lines are negative but the positive clamp is inactive), the diodes D_7–D_8 (D_5–D_6) are connected in series with the drains, as illustrated in Fig. 12. Under normal operation, where:

$$-V_{NEG} - V_{TH,p} < V_{CM} < V_{POS} + V_{TH,n} \tag{13}$$

All MOS transistors and series diodes remain OFF, presenting a high-impedance state that does not load the transceiver.

Given that the AC simulations do not capture the clamps' activation when the CM threshold is exceeded, it is not possible to compare the transfer function with and without the clamp circuits. Subsequently, transient simulations were conducted at 1 MHz under three transmitter conditions (high pulse, low pulse, and idle phase) with varying EMI amplitudes, both with and without the clamp circuits. The comparison between the AC transfer function magnitude and the transient transfer ratio from the EMI source to the comparator's CM input, summarized in Table 3, confirms good alignment between the simulations, particularly in the absence of the clamp.

TABLE 3. AC Transfer function and transient transfer ratio from the EMI source to the comparator's CM input at 1 MHz.

EMI Frequency	1 MHz		
EMI Amplitude	1 V	10 V	40 V
AC TF during Data transmission (0 or 1)	$-26\,\text{dB} = 0.0501$		
Transient transfer ratio during Data transmission (0 or 1)	0.0495	0.0495	0.0492
Transient transfer ratio during Data transmission (0 or 1) including clamps	0.0261	0.0259	0.0214
AC TF during Idle phase	$-19.78\,\text{dB} = 0.102$		
Transient transfer ratio during Idle phase	0.1065	0.1065	0.071
Transient transfer ratio during Idle phase including clamps	0.1154	0.0822	0.0256

Based on the AC and transient simulation results, the data transmission phase exhibits a transfer function magnitude $|H(f)|$ of approximately 0.05 in the 1 to 10 MHz range, which exceeds the critical threshold of 0.045. This value is sufficient to trigger failures when the EMI amplitude approaches 40 V, indicating that the system is susceptible to common-mode disturbances during data transmission.

For the idle phase, the AC simulation shows the highest transfer function magnitude ($|H(f)| = 0.102$). Although the transient simulation at higher EMI amplitudes slightly reduces $|H(f)|$ to 0.071, this magnitude remains significantly high, indicating a primary susceptibility concern.

During the idle phase, the differential signal is ideally zero, and the comparators should not be triggered. However, the transmitter side is in an open-circuit condition, which increases the sensitivity to CM signal propagation. This amplified CM voltage can lead to a malfunction in two ways:

1) It can be converted into a differential voltage large enough to exceed the comparator's threshold (V_{th}) (as discussed in subsection IV-B).
2) The CM voltage itself can exceed the comparator's CMIR.

To illustrate this latter effect, Fig. 20 presents the Fast Fourier Transform (FFT) of the CM signal measured at the comparator input for both the unmitigated and clamped circuits. This specific transient simulation was conducted with the VIF in the idle phase condition, subjected to a 1 MHz RF signal with an amplitude of 40 V.

The FFT plot without the clamp (the blue line) shows a prominent peak at 1 MHz RF with an amplitude of 2.84 V. This peak value represents the maximum amplitude of the common-mode noise voltage coupled to the comparator inputs. This CM peak magnitude of 2.84 V is above the upper CMIR limit, directly causing a comparator malfunction. Once the CMIR is violated, the comparator's input stage becomes improperly biased, causing the output to switch erroneously and ultimately leading to communication errors.

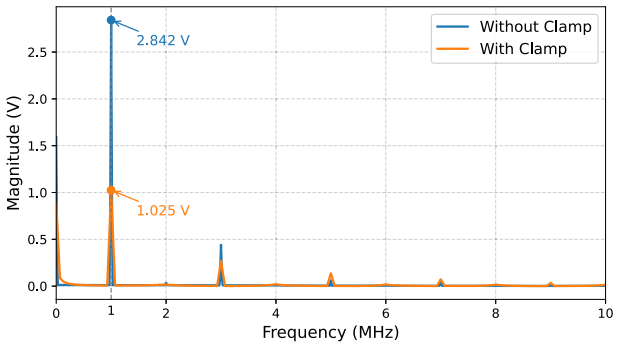


FIGURE 20. Common-mode FFT magnitude at comparator input with and without clamp circuits at 1 MHz RF disturbance.

The proposed clamp circuit effectively addresses this vulnerability. As shown by the orange line in Fig. 20, the clamp drastically reduces the CM magnitude. The 1 MHz peak drops sharply from 2.84 V (without the clamp) to only 1.02 V (with the clamp). This reduction corresponds to a CM transfer function magnitude of 0.025 (1.02 V at 40 V EMI amplitude), which is well below the critical failure threshold of 0.045. By limiting CM voltage excursions, the clamp maintains the CM signal within the CMIR, thereby preserving the integrity of the comparator inputs and the reliability of the communication link.

In summary, both the data transmission and idle phases are susceptible to EMI-induced common-mode excursions, with the idle phase being particularly vulnerable. The clamp circuit plays a crucial role in maintaining the integrity of the comparator inputs and the reliability of the communication link by effectively limiting these excursions.

V. FINAL SUSCEPTIBILITY ASSESSMENT

To validate the combined efficacy of the proposed countermeasures, a comprehensive assessment was conducted via both transistor-level simulations and laboratory measurements. The proposed VIF design integrates all three solutions detailed in Section IV: protective diodes for the LDO regulator, diode bridges for idle-phase stability, and a clamp circuit to protect the comparator's common-mode input range.

The proposed countermeasures also illustrate a general IC-level design approach in which each dominant EMI failure path is mitigated locally.

A. SIMULATION RESULTS AND COUNTERMEASURE ANALYSIS

First, the effectiveness of the proposed countermeasures was evaluated through simulations. In this analysis, the diodes D_1 and D_2 in Fig. 9, which are always included, and the improvement in terms of immunity resulting from the two countermeasures described in this paper, namely: diode bridges and active clamps, are investigated by DPI immunity simulations, incorporating each of these countermeasures

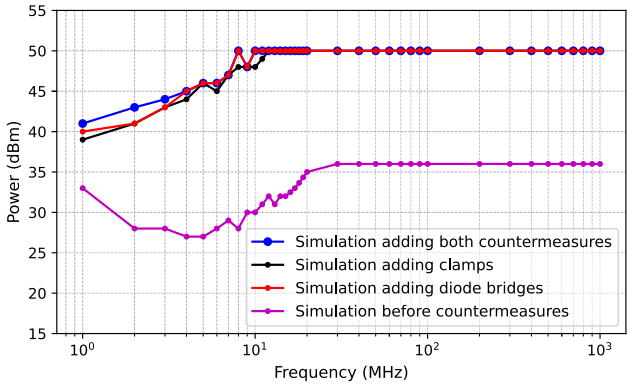


FIGURE 21. Simulation susceptibility comparison showing the individual effectiveness of the diode bridges and clamp circuits, compared to the complete solution and the circuit without countermeasures. The circuit shows no failures up to the maximum injected power of 36 dBm for all the simulation configurations with countermeasures.

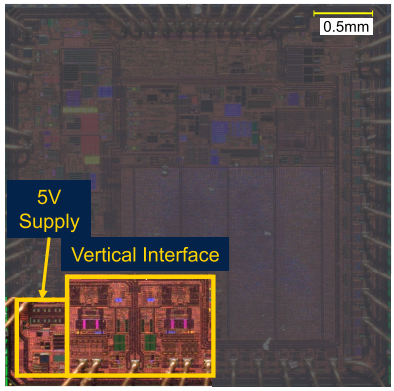


FIGURE 22. Die micrograph showing the VIF and 5V LDO supply area.

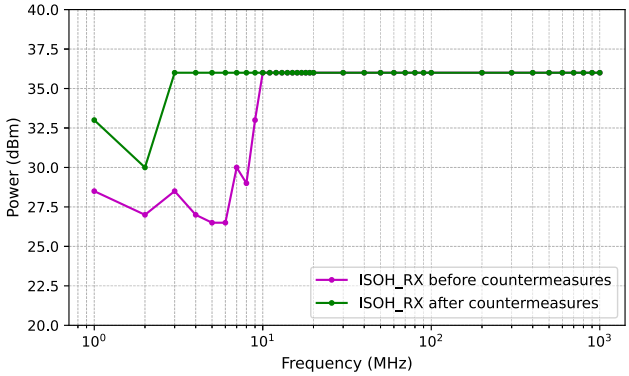


FIGURE 23. Measured susceptibility level of the VIF receiver (ISOH-RX) before and after implementing the proposed countermeasures.

individually and then simultaneously. The results are compared in Fig. 21.

The simulation results indicate that applying either the diode bridges or the clamp circuits individually significantly increases immunity, pushing it above the 36 dBm requirement across the entire tested frequency range from 1 MHz to 1 GHz. To assess the susceptibility of the proposed VIF, the power level was increased to 50 dBm. The results demonstrate that the susceptibility level exceeds 40 dBm across all frequencies. Specifically, the diode bridges effectively mitigate differential-voltage buildup during the idle phase, while the clamps constrain the common-mode voltage within the comparator's CMIR.

To complement the broader benchmarking discussion, Table 4 presents an internal comparison of the identified failure mechanisms and the corresponding IC-level mitigation strategies proposed in this work, summarizing their immunity benefits, implementation overheads, and expected impacts on nominal operation.

From a design perspective, the proposed countermeasures were selected to maximize EMI robustness while minimizing implementation overhead. The diode-based solutions introduce only localized device additions and do not require external filtering components, shielding, or protocol-level modifications. Their main design trade-off is the introduction of additional parasitic junction capacitance and silicon area. At the same time, the clamp-based solution also requires careful sizing to avoid undue loading of the receiver input. However, no degradation of the nominal communication functionality was observed in simulation or in the experimental validation of the redesigned chip. Compared with system-level mitigation techniques, the proposed IC-level approach offers a more compact, implementation-oriented route to improving robustness.

A final remark concerns the sensitivity of the proposed countermeasures to circuit parameters. Some of the adopted solutions, such as the diode bridge and the protective diodes, act mainly by suppressing the corresponding failure mechanism at the topological level and are therefore not critically dependent on fine parameter tuning from a qualitative standpoint. Moreover, the selected component values were chosen under the relevant design constraints and, for the most critical parameters, through simulation-based design exploration. Nevertheless, the exact immunity margin remains dependent on circuit and parasitic parameters, and a formal sensitivity analysis across variations and corners was not included in the present work and is therefore left for future investigation.

B. EXPERIMENTAL VALIDATION

To validate these simulation findings in a physical environment, the full set of countermeasures was implemented on a new revision of the test chip. A micrograph of the fabricated die is shown in Fig. 22, illustrating the placement of the VIF transceiver and the 5V LDO supply regulator within the chip. This new release was mounted in the same package and on the same test PCB as the initial prototype; its EMI susceptibility was then experimentally evaluated via DPI as described in Section III. The measured susceptibility, comparing the VIF performance before and after the application of countermeasures, is presented in Fig. 23.

TABLE 4. Summary of identified EMI failure mechanisms and proposed countermeasures.

Failure Mechanism	Proposed Countermeasure	Main Immunity Benefit	Implementation Overhead / Trade-Off	Impact on Nominal Operation
EMI-induced reverse current into the LDO regulator during transmission	Series protection diodes D_1 and D_2 in the transmitter pull-up path	Suppresses the reverse-current path from the ISO lines to the LDO output and protects the regulator from EMI-induced stress	Small additional on-chip area and added series junction parasitics	Negligible effect in normal operation; active only when the ISO-line voltage exceeds the LDO supply
CM-to-DM conversion during transmission, leading to idle-phase false differential pulses	Diode bridges at the VIF receiver input	Restores symmetry under large CM excursions and prevents differential-voltage buildup across the coupling capacitors	Additional on-chip area and junction parasitic capacitance	Limited impact on nominal differential signaling when properly sized; prevents erroneous idle-phase pulse detection under EMI
Excessive common-mode voltage at comparator inputs exceeding the CMIR	Clamp circuit at the comparator inputs	Limits CM voltage excursions at the receiver input and preserves comparator functionality under EMI	Additional area and input loading; requires sizing to avoid overloading the signal path	Designed to preserve normal communication operation while constraining EMI-induced CM peaks
Combined susceptibility of the complete VIF front-end	Integration of all the above countermeasures	More than 15 dB measured immunity improvement in the critical 1–10 MHz range	Aggregate silicon overhead and added circuit complexity	No functional degradation observed in simulations or measurements of the revised design

The experimental results demonstrate a significant improvement in EMI robustness. The deep susceptibility notch observed in the original design between 1 MHz and 10 MHz was effectively mitigated. As seen in Fig. 23, the immunity level has improved by over 15 dB within the critical low-frequency band.

It is worth noting that while the simulation predicted immunity levels exceeding 50 dBm, experimental measurements reveal a susceptibility threshold slightly below 36 dBm in the 1-2 MHz range. This discrepancy highlights the impact of real-world parasitics and second-order coupling effects, which are not fully captured in the simulation model. This result validates the design choice discussed in Section V-A: relying on a single countermeasure would likely have resulted in a non-compliant silicon device. By integrating targeted solutions for the LDO, the idle phase, and the CMIR, the final design achieves robustness that approaches the stringent automotive limits, ensuring reliable operation in harsh electromagnetic environments.

VI. CONCLUSION

The EMI susceptibility of the VIF in a BMS IC for EVs has been investigated at the IC level using DPI measurements and transistor-level simulations. Three distinct failure mechanisms were identified: EMI-induced failures in the LDO voltage regulator; CM-to-DM conversion during transmissions leading to failures in the transmitter idle phase; and CM EMI at the receiver exceeding the comparators' CMIR.

The failure mechanisms were characterized qualitatively and using simplified analytical models, and then mitigated through targeted countermeasures integrated into the VIF IC design. The effectiveness of countermeasures was validated through both transistor-level simulations and DPI measurements on a new version of the BMS IC.

Although the quantitative results reported in this work are specific to the investigated VIF architecture, technology implementation, and test vehicle, the identified classes of EMI failure mechanisms are more general. In particular, reverse-current corruption of supply-regulation blocks, CM-to-DM conversion caused by temporary symmetry breaking in capacitively coupled differential links, and receiver failure due to common-mode input-range violation can potentially arise in other isolated communication interfaces subjected to strong RF common-mode disturbances. Therefore, the proposed analysis methodology is generalizable, even though the exact susceptibility levels, critical frequencies, and optimal countermeasure sizing remain implementation-dependent.

APPENDIX
DERIVATION OF THE EQUIVALENT CIRCUIT FOR IDLE PHASE ANALYSIS

To analytically evaluate the differential voltage at the comparator input during the idle phase under EMI conditions, a simplified equivalent circuit is derived from the original VIF structure, as depicted in Fig. 5. The goal is to reduce the circuit's complexity while retaining the essential behavior governing the asymmetric charging and discharging of the differential capacitors. The derivation proceeds as follows:

1) Capacitor Approximation: For this analysis, all capacitors not directly responsible for the observed voltage variation (C_1, C_2, and C_{INJ}) are neglected. Series capacitors are modeled as short circuits, and parallel capacitors are treated as open circuits. Only C_3 and C_4 are retained since they directly influence the differential voltage at the comparator inputs.
2) Initial Resistive Network Simplification: With the capacitors removed, the remaining circuit consists of resistive elements and sources. The EMI injection network appears as a star (Y) configuration centered at the injection node.

3) Star-to-Delta Conversion: The Y-network is transformed into an equivalent delta (Δ) configuration using standard conversion formulas, allowing for easier current path analysis.
4) Series and Parallel Combination: Resistors in series and parallel are combined to reduce the network complexity further.
5) Delta-to-Star Transformation: A final transformation is applied to obtain a simplified resistive structure suitable for analytical evaluation of current flow through C_3 and C_4.

It should be noted that in the 1–10 MHz range, the cable is treated as an electrically short interconnect, so a lumped representation is adopted. The simplification from the complete passive network to the reduced model relies on the fact that, in the frequency range of interest, the neglected parasitic branches have impedance values either much larger than those of the dominant current path or much smaller than those of the storage-related nodes governing the CM-to-DM conversion mechanism. Likewise, passive-component self-resonances are neglected because the mechanism under study is dominated by low-frequency asymmetric capacitor charging/discharging rather than by high-frequency resonant effects. The resulting simplified equivalent circuit is shown in Fig. 12 (b), with an intermediate stage shown in Fig. 12 (a). These circuits provide the analytical foundation for Subsection IV-B.

REFERENCES

[1] K. Ramya, J. Gopalakrishnan, B. Chokkalingam, R. Verma, and L. Mihet-Popa, "A complete review of electromagnetic interference in electric vehicle," *IEEE Access*, vol. 13, pp. 40520–40560, 2025.
[2] S. Saxena, "Wireline communication: The backbone of data transfer," *CSI Trans. ICT*, vol. 8, no. 2, pp. 147–156, 2020.
[3] O. Çiloğlu, İ. G. Önel, and Ö. Korçak, "Leveraging SPI-DMA for PROFINET isochronous IRT cyclic communication," *IEEE Access*, vol. 13, pp. 122960–122971, 2025.
[4] O. Aiello, P. S. Crovetti, and F. Fiori, "Susceptibility to EMI of a battery management system IC for electric vehicles," in *Proc. IEEE Int. Symp. Electromagn. Compat. (EMC)*, Aug. 2015, pp. 749–754.
[5] S. Mosleh, J. B. Coder, J. M. Ladbury, M. O. A. Kalaa, J. L. Silberberg, Y. Ardeshirpour, J. Guag, Y. Liu, and S. J. Seidman, "A metrology-driven approach to distilling live wireless signals into immunity test signals," *IEEE Access*, vol. 13, pp. 28711–28732, 2025.
[6] Y. Meng, Y. Peng, H. Zhang, L. Li, and D. Su, "A novel approach of electromagnetic compatibility conducted susceptibility analysis based on Gaussian even pulse signal," *Chin. J. Electron.*, vol. 33, no. 2, pp. 472–478, Mar. 2024.
[7] O. Aiello, "Electromagnetic susceptibility of battery management systems' ICs for electric vehicles: Experimental study," *Electronics*, vol. 9, no. 3, p. 510, Mar. 2020.
[8] O. Aiello and P. Crovetti, "Characterization of the susceptibility to EMI of a BMS IC for electric vehicles by direct power and bulk current injection," *IEEE Lett. Electromagn. Compat. Pract. Appl.*, vol. 3, no. 3, pp. 101–107, Sep. 2021.
[9] X. Siyi, Y. Zhaowen, G. Tengfei, C. Ying, L. Xingyu, and F. Changshun, "Digital chip susceptibility assessment and level classification via the DPI approach," in *Proc. IEEE 10th Int. Symp. Microw., Antenna, Propag. EMC Technol. Wireless Commun. (MAPE)*, Nov. 2024, pp. 1–4.
[10] Q. M. Khan, L. Devaraj, R. Perdriau, A. R. Ruddle, T. Claeys, M. Ramdani, and M. Koohestani, "Experimental characterization of multitone EM immunity of integrated oscillators under thermal stress," *IEEE Access*, vol. 10, pp. 83898–83915, 2022.
[11] M. S. Choudhary, J. Redouté, and M. S. Baghini, "Comprehensive study of EMI effects on wireline transceiver systems: A review of silicon-proven techniques," in *Proc. 14th Int. Workshop Electromagn. Compat. Integr. Circuits (EMC Compo)*, Oct. 2024, pp. 100–105.
[12] Z. Zheng, Y. Chen, D. Jie, X. Xu, K. Deng, Y. Xiang, W. Li, and J. Wu, "Design and implementation of an EMI-immune daisy chain interface with a PID-based CDR algorithm for battery management system communication," *IEEE Access*, vol. 12, pp. 126438–126445, 2024.
[13] M. Lelie, T. Braun, M. Knips, H. Nordmann, F. Ringbeck, H. Zappen, and D. U. Sauer, "Battery management system hardware concepts: An overview," *Appl. Sci.*, vol. 8, no. 4, p. 534, Mar. 2018.
[14] L. Devaraj, A. R. Ruddle, and A. P. Duffy, "System level risk analysis for immunity in automotive functional safety analyses," in *Proc. Int. Symp. Electromagn. Compat.-EMC Eur.*, Sep. 2020, pp. 1–6.
[15] S. Murlidharan, V. Ravulakole, J. Karnati, and H. Malik, "Battery management system: Threat modeling, vulnerability analysis, and cybersecurity strategy," *IEEE Access*, vol. 13, pp. 37198–37220, 2025.
[16] R. Shirai, K. Wada, and T. Shimizu, "Failure protection method for CAN communication against EMI noise generated by switched-mode power supplies," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 6152–6160, Oct. 2021.
[17] A. Camarda, M. Balbarani, F. Calvano, S. Righi, L. Dossi, and A. Tacchini, "Characterization of high voltage EMC filters for electric vehicles charging applications," in *Proc. Int. Symp. Electromagn. Compat.-EMC Eur.*, Sep. 2023, pp. 1–6.
[18] P. González-Vizuete, J. Bernal-Méndez, M. J. Freire, and M. A. Martín-Prats, "Improving performance of compact EMI filters by using metallic and ferrite sheets," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9057–9068, Aug. 2021.
[19] T. Tamoor, F. Ahmed, S. M. Qasim Ali Shah, T. Hassan, and N. Shoaib, "An FSS based stop band filter for EM shielding application," in *Proc. Int. Symp. Electromagn. Compat.-EMC Eur.*, Sep. 2020, pp. 1–3.
[20] A. Allioua, D. Großmann, and G. Griepentrog, "Enhanced EMI mitigation in high-frequency DC–DC converters through hybrid filtering approaches," in *Proc. IEEE 9th Southern Power Electron. Conf. (SPEC)*, Dec. 2024, pp. 1–6.
[21] P. Widek and M. Alaküla, "Methods for the investigation and mitigation of conducted differential-mode electromagnetic interference in commercial electrical vehicles," *Energies*, vol. 18, no. 4, p. 859, Feb. 2025.
[22] Y. Zhang, Y. Xie, C. Chen, X. Guo, Y. Yan, L. Yang, and Y. Kang, "Comprehensive analysis and optimization of parasitic capacitance on conducted EMI and switching losses in hybrid-packaged SiC power modules," *IEEE Trans. Power Electron.*, vol. 38, no. 11, pp. 13988–14003, Nov. 2023.
[23] M. Gonzalez-Atienza, D. Vanoost, M. Verbeke, and D. Pissoort, "An optimized adaptive Bayesian algorithm for mitigating EMI-induced errors in dynamic electromagnetic environments," *IEEE Trans. Electromagn. Compat.*, vol. 66, no. 6, pp. 2085–2094, Dec. 2024.
[24] A. Richelli, G. Delaini, M. Grassi, and J.-M. Redoute, "Susceptibility of operational amplifiers to conducted EMI injected through the ground plane into their output terminal," *IEEE Trans. Rel.*, vol. 65, no. 3, pp. 1369–1379, Sep. 2016.
[25] N. Jia, X. Tian, L. Xue, H. Bai, L. M. Tolbert, and H. Cui, "Integrated common-mode filter for GaN power module with improved high-frequency EMI performance," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 6897–6901, Jun. 2023.
[26] J. Qu, Q. Zhang, Y. Wang, and S. Cui, "Conducted EMI investigation of a SiC-based multiplexing converter for EV/PHEV," *IEEE Access*, vol. 9, pp. 58807–58823, 2021.
[27] T. McGrew, S. Wang, and Q. Li, "Reduction of CM noise by minimizing near-field effects in a DC/DC converter," *IEEE Trans. Power Electron.*, vol. 1, pp. 1761–1768, Dec. 2023.
[28] H. Xu, W. Ma, Y. Yin, and X. Huang, "A 200kV/μs common-mode transient immunity capacitively coupled digital isolator," in *Proc. Int. Conf. New Power Syst. Technol. (PowerCon)*, Sep. 2025, pp. 1–6.
[29] M. M. Wenger, R. Filimon, V. R. H. Lorentz, and M. März, "A robust contactless capacitive communication link for high power battery systems," in *Proc. IEEE 23rd Int. Symp. Ind. Electron. (ISIE)*, Jun. 2014, pp. 1766–1772.
[30] J. F. Justo, W. Beccaro, A. M. D. O. Neto, and A. M. D. Oliveira, "A fully capacitive transformer device for galvanic isolation applications," *IEEE Access*, vol. 13, pp. 153764–153772, 2025.

[31] C. Chen, P. Pan, J. Gu, and X. Li, "A high-voltage-isolated MEMS quad–solenoid transformer with specific insulation barriers for miniaturized galvanically isolated power applications," *Micromachines*, vol. 15, no. 2, p. 228, 2024.
[32] *Integrated Circuits—Measurement of Electromagnetic Immunity 150 KHz to 1 GHz—Part 4: Direct RF Power Injection Method*, Standard IEC 62132-4:2006, Feb. 2006.
[33] F. Grassi and S. A. Pignari, "Bulk current injection in twisted wire pairs with not perfectly balanced terminations," *IEEE Trans. Electromagn. Compat.*, vol. 55, no. 6, pp. 1293–1301, Dec. 2013.
[34] G. Spadacini, F. Grassi, and S. A. Pignari, "Field-to-wire coupling model for the common mode in random bundles of twisted-wire pairs," *IEEE Trans. Electromagn. Compat.*, vol. 57, no. 5, pp. 1246–1254, Oct. 2015.
[35] A. Ahmadi, C. Serratoni, V. Bendotti, and P. Crovetti, "Simulation analysis of the bit error induced by EMI on galvanically isolated data-link embedded in an automotive battery management IC," in *Proc. Int. Conf. Electromagn. Adv. Appl. (ICEAA)*, vol. 21, Oct. 2023, pp. 605–610.
[36] J. Wu, A. Boyer, J. Li, B. Vrignon, S. Ben Dhia, E. Sicard, and R. Shen, "Modeling and simulation of LDO voltage regulator susceptibility to conducted EMI," *IEEE Trans. Electromagn. Compat.*, vol. 56, no. 3, pp. 726–735, Jun. 2014.
[37] F. Fiori and P. S. Crovetti, "Nonlinear effects of radio-frequency interference in operational amplifiers," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 49, no. 3, pp. 367–372, Mar. 2002.
[38] P. Crovetti and F. Fiori, "A linear voltage regulator model for EMC analysis," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2282–2292, Nov. 2007.
[39] F. L. Fiori and P. S. Crovetti, "Prediction of high-power EMI effects in CMOS operational amplifiers," *IEEE Trans. Electromagn. Compat.*, vol. 48, no. 1, pp. 153–160, Feb. 2006.
[40] P. Crovetti and F. Musolino, "Digital suppression of EMI-induced errors in a baseband acquisition front-end including off-the-shelf, EMI-sensitive operational amplifiers," *Electronics*, vol. 10, no. 17, p. 2096, Aug. 2021.



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