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RESEARCH ARTICLE

# A 400 mV, 17.79 nW Floating-Inverter-DIGOTA-Based First-Order Continuous-Time ΣΔ Modulator in 180 nm

**HOSSEIN FIROUZKOUHI, (Student Member, IEEE), AND PAOLO STEFANO CROVETTI, (Senior Member, IEEE)**
Department of Electronics and Telecommunications (DET), Politecnico di Torino, Turin, Italy

Corresponding author: Hossein Firouzkouhi (hossein.firouzkouhi@polito.it)

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**ABSTRACT** This paper presents a low-power first-order continuous-time sigma-delta (CT-ΣΔ) modulator featuring a continuous-time integrator based on a fully differential floating-inverter-input digital operational-transconductance-amplifier (FI-DIGOTA). From post-layout simulations in 180 nm CMOS, the proposed CT-ΣΔ modulator operates at 400 mV supply with a total power consumption of 17.79 nW and achieves a signal-to-noise-and-distortion ratio (SNDR) of 50.92 dB, a spurious-free dynamic range (SFDR) of 55.14 dB, and an effective number of bits (ENOB) of 8.166 bit across 500 Hz bandwidth at 100 oversampling ratio (OSR), resulting in a peak Schreier figure-of-merit ($FOM_{SCh}$) of 155.4 dB. Post-layout simulations across process corners and Monte Carlo simulations reveal consistent operation across process, supply voltage and temperature variations, and confirm its suitability to energy-constrained IoT sensor interfaces.

**INDEX TERMS** Digital-based operational transconductance amplifier (DIGOTA), floating-inverter (FI), isolation resistor-based frequency compensation ($R_{iso}$-based), ΣΔ modulator, ultra-low-power (ULP).

## I. INTRODUCTION

Energy-autonomous sensor nodes and wearable devices for emerging Internet of Things (IoT) applications demand low-cost integrated circuits operating reliably from a supply voltage below 0.5 V with an overall power consumption well below 1 $\mu$ W and dimensions in the sub-mm$^2$ scale. Meeting these stringent requirements in sensor interfaces demands data converters that balance scalability, energy efficiency, resolution, robustness, and portability to advanced CMOS nodes [1], [2].

Aiming to address these challenges, recent literature consistently highlights the progressive shift of analog functionality toward the digital domain [1], [3], [4], [5], [6], [7], [8]. Within this trend, inverter-based and digitally intensive topologies such as the Digital Operational-Transconductance amplifiers (DIGOTAs) have emerged as promising solutions, offering compact architectures with reduced design effort and high energy efficiency.

In this context, Digital Operational-Transconductance-Amplifiers (DIGOTAs) which are inherently compatible with a low-effort digital design flow, have demonstrated operation down to 300 mV with a power consumption down to the sub-nW range [9] and a high energy efficiency, thanks to the suppression of static power consumption related to their inherently digital operation. However, DIGOTAs exhibit intrinsic limitations in their frequency response (e.g., limited gain-bandwidth product due to relatively large output capacitor) and limited speed [9], [10], [11], [12], [13], [14], [15], [16], [17], [18].

To address the aforementioned limitations, a Floating-Inverter-based DIGOTA (FI-DIGOTA) featuring isolation-resistor ($R_{iso}$)-based frequency compensation has been proposed in [19]. In this paper, which extends [19], the FI-DIGOTA has been further optimized and it is employed in the integrator of a first-order continuous-time (CT)-ΣΔ

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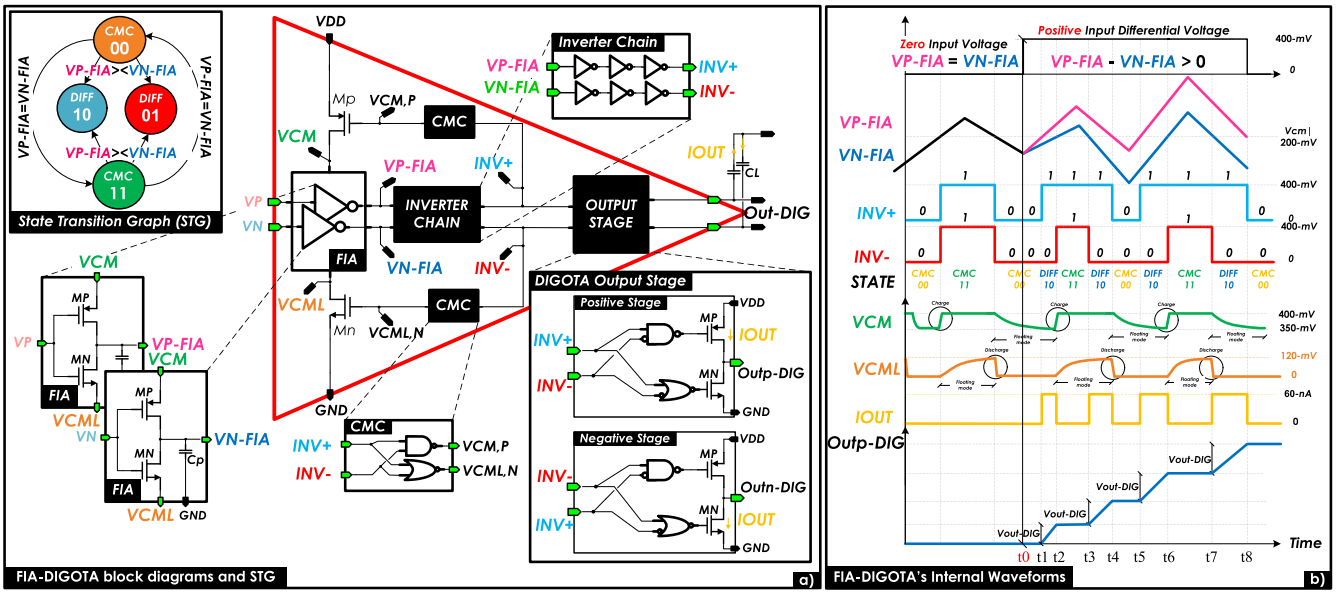



**FIGURE 1.** a) State-transition graph (STG) and FI-based DIGOTA block diagram, b) Waveforms of input/output of each block for zero and positive input differential voltage.

modulator, whose design is described in detail and validated by post-layout simulations. Based on simulation results, compared to the state of the art ΣΔ modulators [20], [21], [22], [23], [24], [25], [26], [28], the proposed circuit consumes less than 20 nW and achieves a favorable trade-off between energy efficiency, linearity, and robustness to technology variability [16], [21], [26] and mismatch.

The remainder of the paper is organized as follows. Section II presents the architecture and operation of the FI-DIGOTA and Section III details its integration within a CT-ΣΔ modulator. Section IV presents post-layout simulation results, including linearity, power, and area analysis, as well as validation across process, voltage, and temperature (PVT) corners and Monte-Carlo simulations. Section V provides a comparison with recent low-power modulators and is followed by the conclusions.

## II. FI-DIGOTA DESIGN

The architecture of the FI-DIGOTA adopted in this paper is depicted in Fig. 1. It comprises four primary functional blocks: (i) a FI-based differential input stage, (ii) an inverter chain responsible for digitizing the analog FI outputs (INV+ and INV-), (iii) a common-mode compensation (CMC) block, and (iv) an output stage.

The input stage employs a pair of floating inverters that are dynamically biased by the CMC block, enabling accurate sensing of the differential input signal ($V_P - V_N$) while rejecting its common-mode component ($V_P+V_N$)/2.

According to the state transition graph (STG) in Fig. 1, the FI-DIGOTA operates in two distinct modes: common-mode compensation (CMC) mode corresponding to logic states (INV+, INV-) 11 and 00, and differential signal amplification mode (DIFF) associated with states (INV+, INV-) 10 and 01. Transitions between these modes are governed by the digital outputs of the inverter chain fed by the FIA stage. Under zero differential input voltage ($V_P = V_N$), the system alternates between the CMC states (00 and 11), periodically maintaining the common-mode constant by resetting and setting the FIs output node.

The floating structure does not by itself impose a precise analog output common-mode target. Instead, the operating point of the stand-alone FI-DIGOTA is maintained by the common-mode compensation (CMC) mechanism, which alternates the circuit between the states 00 and 11 and dynamically charges or discharges the floating nodes to prevent common-mode drift. The floating structure primarily enables the inverter switching threshold to adapt to the input common-mode level, thereby supporting efficient differential sensing under ultra-low-voltage operation. In the complete CT-ΣΔ modulator, the output common-mode is further established by the total current injected by the current-steering DAC, which fixes the DC operating point of the integrator output nodes.

When a positive input differential voltage ($V_P > V_N$) is applied, starting from $t_0$ in Fig. 1b), the output capacitance of the FIAs are charged/discharged at a different rate, and their voltages diverge at a rate proportional to the differential input voltage. As a consequence, these voltages cross the trip points of the inverter chain at different time instants, resulting in INV+ and INV- assuming the logical values 10 or 01 for a time interval related to the integral of the input differential voltage. In such states, the output stage actively injects discrete current pulses to charge (discharge) the load capacitor ($C_L$) (see $t_{1-7}$ and $I_{OUT}$ in Fig. 1b).

When INV+ and INV- assume identical logical values (00 or 11), on the other hand, the CMC block is activated

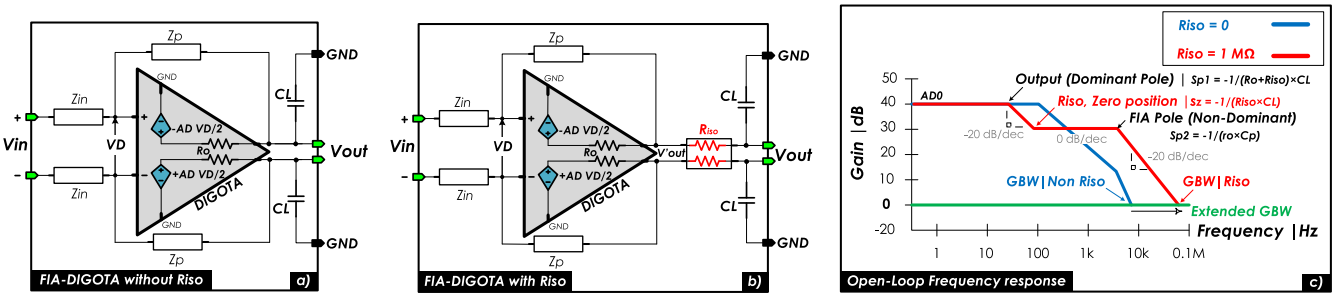



**FIGURE 2.** a,b) Frequency compensation circuit with/without attenuation resistor (*R*iso) on closed-loop gain configuration, c) bode gain plot for with(out) attenuation resistor in open-loop gain configuration.

and dynamically biases the FI stages by turning on the PMOS ($M_P$) or the NMOS ($M_N$), so that to connect the sources of the PMOS (NMOS) devices of the input FIs to the VDD (GND), respectively. This dynamic biasing (dis)charges the FIs' parasitic capacitance ($C_p$), thereby preparing the FIs for the next evaluation cycle (see Fig. 1b).

The proposed FI-DIGOTA should be interpreted as a digital-based transconductance element embedded in continuous-time loop rather than as a conventional continuous-current OTA. In the traditional OTA, the input differential voltage is converted into the continuous output current largely independent of the input common-mode level. While in the proposed FI-DIGOTA approach, the same function role is obtained, but the voltage-to-current conversion is realized through dynamically generated current pulses whose timing and duration encode the differential input. This approach is particularly attractive for energy-efficient alternative for ultra-low-power operation [9].

Compared to previous Digital-based Operational Transconductance Amplifier (DB-OTAs) and DIGOTAs [13], [20], the proposed FI-based input stage enhances energy efficiency, since the input transistors are dynamically operated most of the time close to their threshold voltage (near-threshold region), where they achieve the highest transconductance efficiency ($g_m/I_{DD}$) [29], and the same charge from the power supply is reused by the PMOS and NMOS transistors, which both contribute to the output differential current [10], [30], resulting in ultra-low-power consumption. This capability comes from the floating structure, which dynamically adapts the switching threshold of the input inverters to the common-mode input voltage.

### A. ISOLATION RESISTOR-BASED FREQUENCY COMPENSATION

Similarly to the DIGOTA analyzed in [15], the open-loop gain transfer function (see equation 1) of the fully-differential FI-DIGOTA presented in this work presents two poles. The dominant pole of the amplifier, $s_{p1} = -1/R_O C_L$ is related to the equivalent output resistance ($R_O$) of the FI-DIGOTA and the output capacitance $C_L$, which is introduced to reconstruct the analog output from the pulsed current injected by the output stage. The non-dominant pole located at $s_{p2} = -1/r_o C_p$, is associated to the FIs output resistance $r_o$ and to the parasitic capacitance $C_p$ at the output node of the FIs (see Fig. 2).

As in [9], [10], [11], [12], [13], [15] and [31], dominant-pole frequency compensation can be achieved by adjusting $C_L$ so that $|s_{p1}| \leq |s_{p2}/A_{D0}|$, where $A_{D0}$ denotes the low-frequency gain of the amplifier. This ensures a phase margin (PM) of more than 45° in any resistive feedback configuration. However, this approach requires a large $C_L$ [9], [10], [11], [12], [13], [18], which in turn limits the gain-bandwidth product (GBW) to be much less than $|s_{p2}|/2\pi$ and significantly degrades the slew rate.

In order to mitigate these limitations, the isolation resistor-based frequency compensation scheme [32] illustrated in Fig. 2 is introduced in this paper in the FI-DIGOTA topology. In detail, an attenuation resistor ($R_{iso}$) is connected in series to $C_L$ to introduce a zero in the loop gain transfer function, which now takes the form:

$$\frac{V'_{out}(s)}{V_D(s)} = \frac{A_{D0} \cdot (1 + s \cdot R_{iso} \cdot C_L)}{(1 + s \cdot (R_O + R_{iso}) \cdot C_L) \cdot (1 + s \cdot r_O C_p)} \quad (1)$$

$$\frac{V_{out}(s)}{V_D(s)} = \frac{A_{D0}}{1 + s \cdot (R_O + R_{iso}) \cdot C_L} \quad (2)$$

Thanks to the left-half-plane zero related to $R_{iso}$, the PM is improved without significant GBW and slew-rate degradation. Moreover, taking the voltage $V_{out}$ across $C_L$ as the amplifier output, the zero introduced by $R_{iso}$ is canceled by the pole $s_{p3} = -1/R_{iso}C_L$ of the $R_{iso}C_L$ passive filter (see equation. 2), with no impact on the external transfer function besides the increase of the closed-loop output resistance and a minor shift of the dominant pole to lower frequencies, which is almost negligible for $R_O \gg R_{iso}$.

## III. FIRST-ORDER CONTINUOUS-TIME (CT-ΣΔ) MODULATOR

A fully differential FI-DIGOTA featuring attenuation resistor-based frequency compensation has been employed in the integrator of a first-order continuous-time (CT)-ΣΔ modulator. The architecture and the main waveforms of the proposed system are shown in Fig. 3. In detail, Fig. 3(a) presents the system-level block diagram, which comprises five primary building blocks: a fully differential integrator based on the FI-DIGOTA described in Section II, a 1-bit

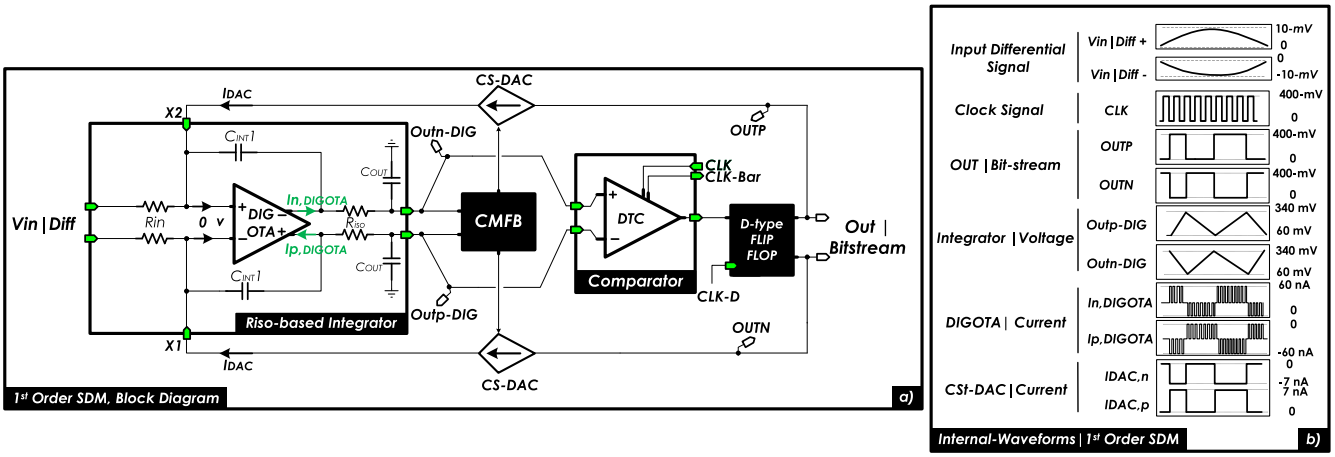



**FIGURE 3.** a) Sigma-Delta modulator block diagram, b) Waveforms of critical section of each block.

current-steering digital-to-analog converter (CSt-DAC), a Common-Mode Feedback Block (CMFB), a double-tail comparator (DTC) for 1-bit quantization, and a D-type flip-flop.

To provide additional insight into the operation of the proposed FI-DIGOTA within the ΣΔ modulator structure, Fig. 4 reports representative time-domain waveforms of the circuit under sinusoidal differential excitation. The figure shows the differential input signal ($V_{\text{in|Diff}}$), the analog differential integrator output voltages ($V_{Outp,int}$ and $V_{Outn,int}$), the resulting common-mode voltage (see (3)), the common-mode control voltages ($V_{CM}$ and $V_{CML}$), and the generated digital output signals.

$$V_{CM,int} = \frac{V_{Outp,int} + V_{Outn,int}}{2}, \tag{3}$$

As observed, $V_{Outp,int}$ and $V_{Outn,int}$ exhibit complementary behavior with comparable amplitudes, confirming the balanced differential operation of the FI-DIGOTA. Moreover, after the initial transient, the common-mode voltage remains confined within a limited operating range without noticeable drift, demonstrating the effectiveness of the common-mode compensation mechanism discussed in Section II. The corresponding control voltages dynamically adjust the operating point of the floating-inverter stage, while the generated digital outputs illustrate the conversion of the analog differential information into timing-encoded digital signals.

Table 1 provides a systematic summary of the key sizing and design parameters of the proposed FI-DIGOTA. The reported design parameters are included to improve design transparency and enable easier replication and verification of the proposed architecture.

While the FI-DIGOTA circuit adopted in the integrator has been previously discussed in Section II, the remaining circuit blocks and their role within the proposed CT-ΣΔ modulator are presented in the following subsections.

**TABLE 1.** Key transistor dimensions of the proposed FI-DIGOTA and CMFB circuitry for reproducibility.

| Circuit | Block | Device | W (nm) | L (nm) | NF |
|---|---|---|---|---|---|
| FI-DIGOTA | FIA Stage | MP | 1250 | 180 | 8 |
| | | MN | 1250 | 180 | 8 |
| | Output Stage | MP | 800 | 180 | 1 |
| | | MN | 220 | 1250 | 1 |
| | CMC | MP | 2000 | 180 | 5 |
| | | MN | 1000 | 180 | 1 |
| CMFB, DAC | CM-Sensing | Mp3 | 400 | 180 | 1 |
| | | Mn-in | 220 | 180 | 1 |
| | | Mn3 | 220 | 180 | 1 |
| | CSt-DAC | Mp2 | 400 | 180 | 1 |
| | | Mp1 | 220 | 180 | 1 |
| | | Mp-inv | 220 | 180 | 1 |
| | | Mn-inv | 220 | 180 | 1 |
| | | Mn1, Mn2 | 220 | 180 | 1 |
| | Bias Point | Mb1 | 22000 | 180 | 1 |
| | | Mb2 | 220 | 180 | 1 |
| | | Mb3 | 220 | 180 | 1 |

### A. COMMON-MODE FEEDBACK (CMFB) BLOCK

A 1-bit differential CSt-DAC, whose schematic is shown on the right side of Fig. 6, is employed to convert the 1-bit digital output of the CT-ΣΔ modulator into a differential current, which is then fed back to the integrator. The maximum differential input signal range is set by the CSt-DAC current. Specifically, the CSt-DAC is designed to deliver up to 7 nA into the summing node ($X_1, X_2$, see Fig. 3b), corresponding to a maximum differential-mode swing of $V_{\text{FS}} = \pm R_{\text{in}} I_{\text{DAC}} = \pm 140\,\text{mV}$.

The common-mode component of the currents injected by the CSt-DAC in the input nodes is set by a negative feedback loop by the CMFB block, so as to set the common-mode of the integrator output voltage at $V_{DD}/2$, aiming to maximize the differential mode output swing of the integrator by keeping the FI-DIGOTA output transistors in saturation for the largest possible amplitude of the differential signal even in the presence of PVT variations and mismatch.

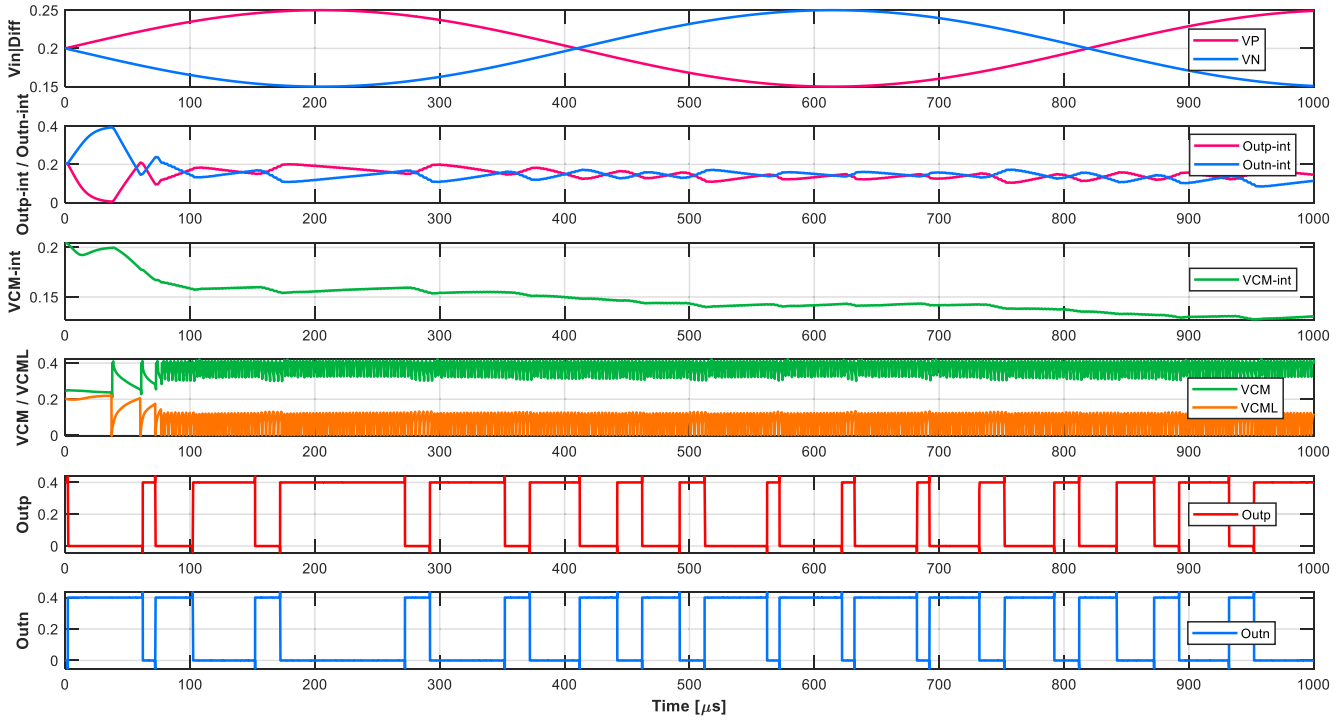



**FIGURE 4.** Time-domain waveforms of the proposed FI-DIGOTA under differential sinusoidal excitation. From top to bottom: differential input signal ($V_{\text{in|Diff}}$), differential integrator output voltages ($V_{Outp,int}$ and $V_{Outn,int}$), resulting integrator output common-mode voltage ($V_{CM,int}$), common-mode control voltages of the FI-DIGOTA ($V_{CM}$ and $V_{CML}$), and corresponding digital output signals.

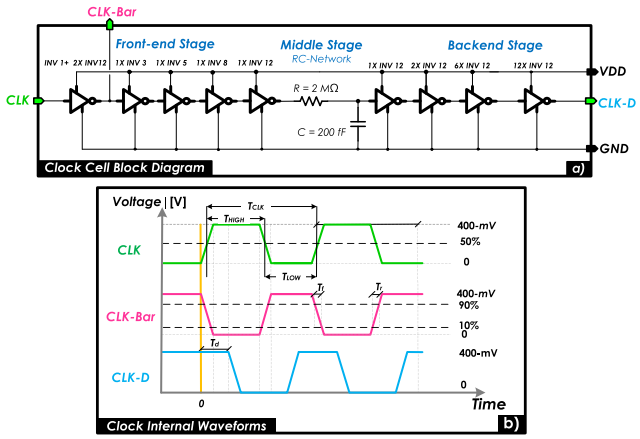



**FIGURE 5.** a) Clock generation block b) Internal clock timing waveforms.

For this purpose, the difference between the actual CM output voltage of the integrator and of the target CM voltage (DCLVL) is converted into a current by the differential transconductance stage in the CM Sensing Block shown in Fig. 6 on the left, and is added to the bias of the NMOS pair of the CSt-DAC, so that when the CM output voltage of the integrator is less than $V_{DD}/2$, the bias current of the NMOS pair of the DAC is increased, resulting in a net CM current drawn from the integrator inputs and in an increase of its CM voltage. Similarly, when the CM output voltage of the integrator exceeds $V_{DD}/2$, the NMOS pair is reduced so that a net CM current is sunk from the integrator inputs and the integrator CM output voltage is reduced.

The CSt-DAC and the CMFB block are designed so that for a full input swing signal at $V_{\text{FS}} = 280\,\text{mV}$ centered around half the supply voltage ($V_{\text{CM}} = V_{\text{DD}}/2 = 200\,\text{mV}$), the output of the integrator ranges approximately from 60 mV to 340 mV, guaranteeing a sufficient headroom of 40 mV per device to the supply rails.

### B. DOUBLE-TAIL COMPARATOR

The DTC is based on a dynamic double-tail architecture, chosen for its low voltage compatibility, energy efficiency, and negligible static power consumption [33], [34], and it is designed with minimum length and minimum width MOS transistors. It receives the differential output from the integrator and compares it against zero in correspondence with the rising edge of an external clock source (CLK) with $T_{\text{CLK}} = 10\,\mu\text{s}$ period, as shown in Fig. 5. Since the DTC requires a finite regeneration time ($T_{\text{d}} = 1\,\mu\text{sec}$) to resolve its output, a delayed clock signal (CLK-D) is generated using tapered inverter chains and RC-network delay line [35]. This structure provides a controlled propagation delay while maintaining symmetric rise/fall time transitions as illustrated in Fig. 5. The comparator output is then sampled by the D flip-flop triggered on the falling edge of the delayed clock signal CLK-D.

To ensure minimal area occupation and ultra-low energy consumption, most of the transistors within the active

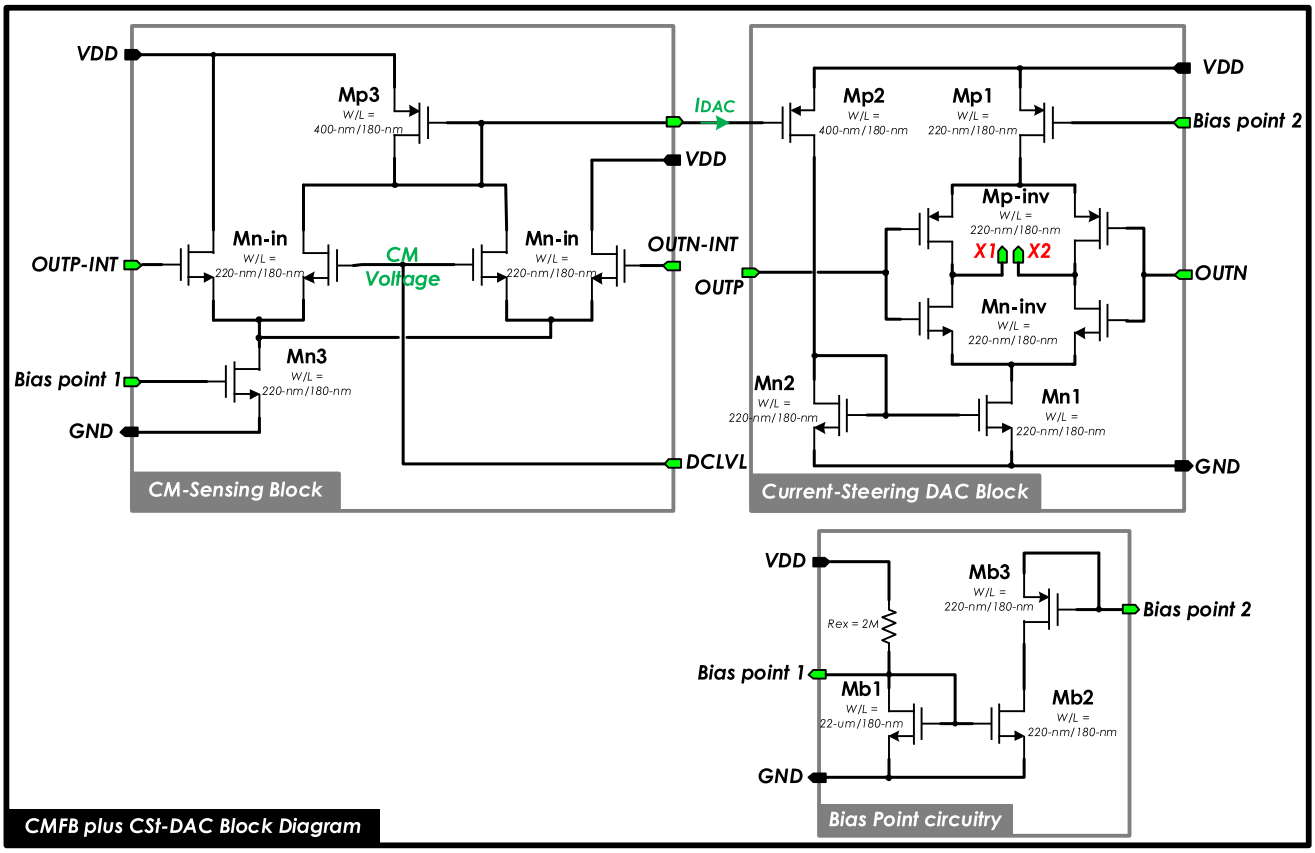



**FIGURE 6.** CMFB block diagram including CM-mode sensing, current-steering DAC, and bias circuitry.

elements including CSt-DAC, DTC blocks are implemented using minimum width/length (W/L = 220/180) geometries.

## IV. SIMULATION RESULTS

Fig. 7 illustrates the layout of the proposed first-order FI-DIGOTA-based continuous-time (CT-ΣΔ) modulator simulated in 180 nm CMOS technology under 400 mV supply voltage. The top part of the figure shows the chip view, where the modulator occupies a compact active area of 0.045 $mm^2$. The enlarged view highlights the floor-plan of the fully differential FI-DIGOTA occupying an area of (0.0203 mm × 0.041 mm).

The proposed FI-DIGOTA adopts a mixed implementation methodology that combines digital-oriented and custom analog design techniques. The inverter chain, digital control logic, and associated circuitry are compatible with standard-cell-based implementation methodologies. In contrast, the floating-inverter input stage, clock generation circuitry, and passive components, including the compensation resistor ($R_{iso}$) and on-chip capacitors ($C_{INT}$ and $C_{OUT}$), require custom analog design and manual layout. Furthermore, the common-mode feedback (CMFB) circuitry incorporates both digital-oriented and custom-designed blocks to ensure robust common-mode regulation under ultra-low-voltage operation. Therefore, the proposed architecture should be regarded as a mixed digital-oriented/custom analog implementation rather than a fully synthesized standard-cell realization.

The simulation results are organized into two main sections, (i) the characterization of the FI-DIGOTA in a unity-gain feedback (UGFB) configuration, and (ii) the performance analysis of the ΣΔ modulator.

### A. FI-DIGOTA SIMULATION RESULTS

Table 2 summarizes the post-layout UGFB performance of the proposed FI-DIGOTA with attenuation resistor and compares it with an extensive set of representative state-of-the-art works. The proposed circuit was evaluated using the test configuration shown in Fig. 2(a) under the operating conditions listed in Table 3. As observed from the open-loop differential Bode plots in Fig. 8, the proposed amplifier achieves a DC gain of 39.78 dB, a GBW of 60 kHz, and a phase margin of 47.8° while dissipating only 7 nW from a 400 mV supply. The comparison reported in Table 2 highlights that the proposed design achieves stable UGFB operation together with a competitive tradeoff among gain, bandwidth, stability, and power consumption under ultra-low-voltage conditions.

**TABLE 2. Comparison of State-of-the-Art OTAs Works; UL-power, UL-voltage; $V_{DD}$ = 400 mV, and T = 27 ° C. (Best in bold).**

| State-of-art works | This Work | [36] | [37] | [38] | [10] | [31] | [11] | [9] | [20] | [12] | [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Validation | Sim. | Sim. | Meas. | Meas. | Sim. | Sim. | Sim. | Meas. | Meas. | Sim. | Meas. |
| Year | 2026 | 2024 | 2020 | 2020 | 2019 | 2020 | 2024 | 2021 | 2024 | 2024 | 2022 |
| Supply voltage [mV] | 400 | 400 | 300 | 300 | 300 | 300 | 300 | 300 | 300 | 300 | 400 |
| Technology node [nm] | 180 | 180 | 180 | 180 | 180 | 180 | 180 | 180 | 180 | 180 | 180 |
| OTA Architecture | Digital | Folded-cascode | Class AB | Class AB | Digital | Digital | Digital | Digital | Class AB | Digital | Digital |
| Design style | Std-cell/custom | custom | custom | custom | std cell | std cell | std cell | std cell | std cell | std cell | std cell |
| Frequency compensation | Isolation resistor ($R_{iso}$) | Not-required | Nested Miller | Nested Miller | Dominant pole | Dominant pole | Dominant pole | Dominant pole | Nested Miller | Dominant pole | Dominant pole |
| Power dissipation [nW] | 7 | 8.03 | 12.6 | 13/12.88 | 7.37 | 10.5 | 2.147 | **0.407** | 1,800,000 | 4.1 | 95 |
| Current [nA] | 17.5 | 20.075 | 42 | 43.34 | 24.567 | 35 | 7.156 | **1.356** | 6,000,000 | 13.67 | 237.5 |
| $A_{D0}$ [dB] | 39.78 | 69.14 | 64.7 | **98.4/98.1** | 35 | 22.6 | 34.3 | 31 | 46.2 | 54.4 | 35 |
| GBW [kHz] | 60 | 26.79 | 2.96 | 3.1/3.56 | 0.47 | 8 | 2.823 | 0.229 | **2450** | 0.265 | – |
| Load capacitor [pF] | 10 | 1 | 30 | 30 | 80 | 10 | 150 | 80 | 2 | 150 | 10 |
| Phase margin [°] | 47.8 | **89.9** | 54.7 | 53.9/54.2 | 57 | 86 | – | 57.3 | 52 | 69 | 50 |
| CMRR [dB] | 52 | 71.6 | **110 (1)** | 60 (1) | – | – | – | – | – | 93 | 62 |
| PSRR [dB] | 50 | **78.14** | 50 (1) | 61 (1) | – | 76.8 | – | – | – | 63.9 | 55 |
| THD [%] | **0.3** | 1.25 | 1 | 0.49 (2) | 3 | – | 1.3 | 1.26 | 0.7 | 0.7 | 1.8 |
| Input-referred Noise $a^*$[$\mu$V] | 1.27 | – | 3.2 | 3.19/3.1 | – | – | – | 1.1 | - | – | – |
| $SR_{avg}$ [V/$\mu$s] $b^*$ | 0.075 | 2, 200 | 4, 150 | **9,200** | 0.0005 | – | $14.5e-5$ | $264e-6$ | 2.4 | $7e-5$ | $1.26e-5$ |
| Input offset [mV] | 5.426 | – | 3.2 | 3.19/3.1 | – | – | – | **1.1** | – | – | – |
| FOMS [kHz·pF/nW] $c^*$ | 85.72 | 3.34 | 7.05 | 7.154 | 34 | 7.62 | **197.23** | 45 | $2.72e-3$ | 9.7 | 4.21 |
| FOML [V·pF/($\mu$s·nW)] $d^*$ | 107.14 | $2.74e+5$ | **9.88 e+6** | $2.12e+7$ | 20 | – | 10.1 | 51.9 | $2.67e-3$ | 2.56 | $1.26e-3$ |

$a^*$ Input-referred noise integrated in UGFB configuration over the 60 kHz noise bandwidth.

b* : $\mathrm{SR_{avg}} = \frac{\mathrm{SR_{(+)}}+\mathrm{SR_{(-)}}}{2}$, $c^*$ : $\mathrm{FOMS} = \frac{\mathrm{GBW}\cdot C_L}{\mathrm{Power}}$, $d^*$ : $\mathrm{FOML} = \frac{\mathrm{SR}\cdot C_L}{\mathrm{Power}}$

(1) At DC input frequency. (2) At 10-Hz, with $V_{\mathrm{in|@ac}} = 250$ mV. (3) At 10-Hz, with $V_{\mathrm{in@ac|PKPK}} = 100$ mV.
(4) At 0-Hz, with $V_{\mathrm{in_{ac}|PKPK}} = 100$ mV.

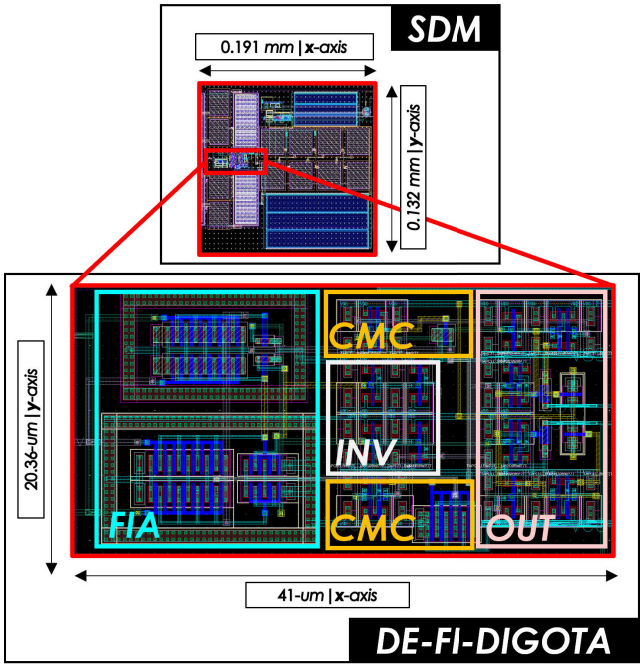



**FIGURE 7. Chip layout view for the proposed modulator and fully differential FI-DIGOTA (DE-FI-DIGOTA).**

### B. FI-DIGOTA'S ROBUSTNESS VERSUS PVT VARIATION

The floating-inverter stage in the FI-DIGOTA topology operates in weak inversion region, with $g_m/I_D = 25\,\mathrm{V}^{-1}$. In this regime, the drain current depends exponentially on gate-source voltage and threshold voltage, making the circuit inherently more sensitive to PVT-induced variations in bias current and transconductance. In order to assess the robustness of FI-DIGOTA under PVT variations, both corner analysis (SS/FF/TT) and Monte-Carlo simulations were performed, as can be seen in Table. 4. The process Corner evaluation demonstrates that the design maintains stable operation across PVT variations, with DC-gain varying only from 37.8-39.78 dB and GBW remaining within 56-65 kHz. Power consumption remains below 8 nW in all corners, while CMRR and PSRR stay above 47.8 dB and 49.1 dB, respectively.

Monte-Carlo analysis, performed on 200 samples and including both mismatch and process variations, shows a limited statistical spread around the nominal operating point. The mean DC-gain is 37.72 dB with a standard deviation of 4.78 dB, while GBW exhibits a mean value of 54.1 kHz and a standard deviation of 7.2. The power consumption remains tightly centered around 6.7 nW with the low variation ($\sigma$ = 1.47 nW). The CMRR and PSRR distributions (mean value

**TABLE 3. Key implementation parameters of the proposed CT-ΣΔ modulator.**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage | $V_{\mathrm{DD}}$ | 400 | mV |
| Input DC level | $V_{\mathrm{in,DC}}$ | 200 | mV |
| Full-scale differential input | $V_{\mathrm{FS,diff}}$ | 280 | $\mathrm{mV_{pp}}$ |
| Signal bandwidth | BW | 500 | Hz |
| Sampling frequency | $f_{\mathrm{s}}$ | 100 | kHz |
| Clock period | $T_{\mathrm{CLK}}$ | 10 | $\mu$s |
| Oversampling ratio | OSR | 100 | – |
| Clock-to-DFF delay | $T_{\mathrm{d}}$ | 1 | $\mu$s |
| Input resistance | $R_{\mathrm{in}}$ | 20 | MΩ |
| Isolation resistor | $R_{\mathrm{iso}}$ | 1 | MΩ |
| Integrator capacitance | $C_{\mathrm{INT}}$ | 2 | pF |
| Output capacitance | $C_{\mathrm{OUT}}$ | 5 | pF |
| DAC current | $I_{\mathrm{DAC}}$ | 7 | nA |

**TABLE 4. UGFB Corner and Monte Carlo Summary (VDD = 400 mV, T = 27°C), 200 samples.**

| Set | Case | $A_{D0}$ [dB] | GBW [kHz] | Power [nW] | CMRR [dB] | PSRR [dB] | $V_{OS}$ [mV] |
|---|---|---|---|---|---|---|---|
| Corners (single-point values) | | | | | | | |
| Corner | TT | 39.78 | 60 | 7.0 | 52.0 | 50.0 | – – |
| Corner | SS | 38.4 | 56 | 7.8 | 50.7 | 49.1 | – – |
| Corner | FF | 37.8 | 65 | 7.9 | 47.8 | 51.2 | – – |
| Monte Carlo (Mean/Standard Deviation): ($\mu/\sigma$) | | | | | | | |
| MC | All = Mismatch + Process | 37.72 / 4.78 | 54.1 / 7.2 | 6.7/ 1.47 | 38.31 / 10.8 | 43.47 / 12.22 | 0.587 / 11.21 |

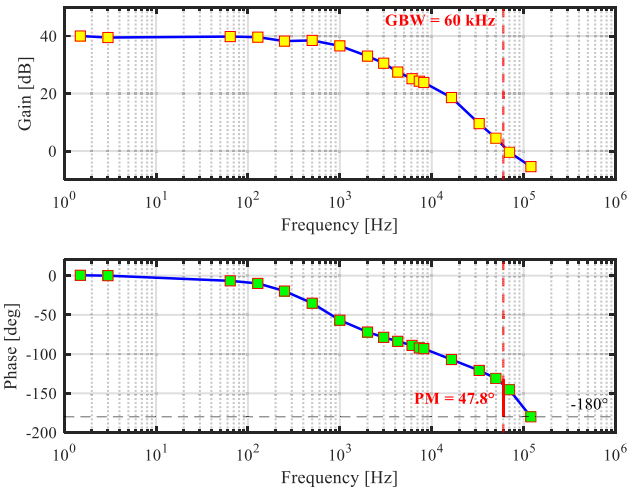



**FIGURE 8. Bode plots of the differential voltage amplification of the FI-DIGOTA.**

of 38.31 dB and 43.47 dB) confirm the overall resilience of the proposed architecture over random device variations.

The MC statistical distribution of the input offset voltage for UGFB configuration, obtained from 200 simulation samples is shown in Fig. 9. The resulting histogram demonstrates an approximately Gaussian distribution (see Table. 4), with a mean value ($\mu$) of 0.587 mV and a standard deviation ($\sigma$) of 11.21 mV. These results account for both process variations and local device mismatches across all transistors, thereby providing a realistic assessment of offset variability under practical fabrication conditions. The Monte Carlo analysis confirms that the offset is a mismatch-related effect distributed across the circuit. Since the proposed amplifier operates under ultra-low-voltage conditions and relies on weak-inversion-sensitive devices, such offset is expected to affect symmetry and may contribute to residual distortion.

The power supply dependency of the UGFB configuration is illustrated in Table. 5. Across 350 mV to 450 mV, the FI-DIGOTA in UGFB configuration exhibits a strong sensitivity to variation of supply voltage. Raising power supply (VDD) from 350 mV to 450 mV, the GBW improves markedly from 19 kHz to 171 kHz, while the DC-gain increases from 16.76 dB to 64.93 dB. However, these enhancements are accompanied by a rise in power consumption from 3.07 nW to 19.9 nW.

**TABLE 5. Power supply variations for UGFB configuration (TT process, T = 27° C).**

| Supply Voltage [mV] | MIN [350] | TYP [400] | MAX [450] |
|---|---|---|---|
| $AD_0$ [dB] | 16.76 | 39.78 | 64.93 |
| GBW [kHz] | 19 | 60 | 171 |
| Power Dissipation [nW] | 3.07 | 7 | 19.9 |
| $f_{os}$ [MHz] | 0.19 | 0.33 | 0.828 |
| CMRR [dB] | 50.3 | 52 | 41.7 |
| PSRR [dB] | 59.31 | 50 | 57 |
| FOMS [kHz·pF/nW] | 61.89 | 85.72 | 85.47 |

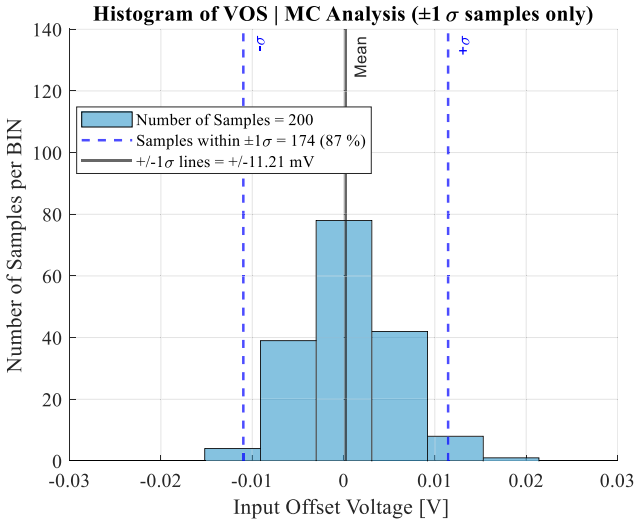



**FIGURE 9. Distribution of the input offset voltage of the FI-DIGOTA in UGFB configuration based on 200 samples Monte-Carlo simulations including process variations and mismatch.**

To interpret the gain improvement and power growth, the behavior can be explained by examining the self-oscillation mechanism of the FI-DIGOTA. In UGFB operation, the oscillation frequency is primarily set by the cumulative delay of the internal feedback loop as expressed in equation 4). This delay is the cumulative contribution of the floating-inverter output charging time ($\tau_{FI}$), inverter-chain propagation delay ($\tau_{INV}$), and the response time of the common-mode compensation block as illustrated in Fig. 10. According to equation 5 [9], $\tau_{FI}$ is inversely proportional to the current delivery by the CMC stage ($I_{CMC}$), where $I_{CMC}$ refers to the equivalent subthreshold current delivery of FI-DIGOTA to $C_p$ during CM phase. An increase in the

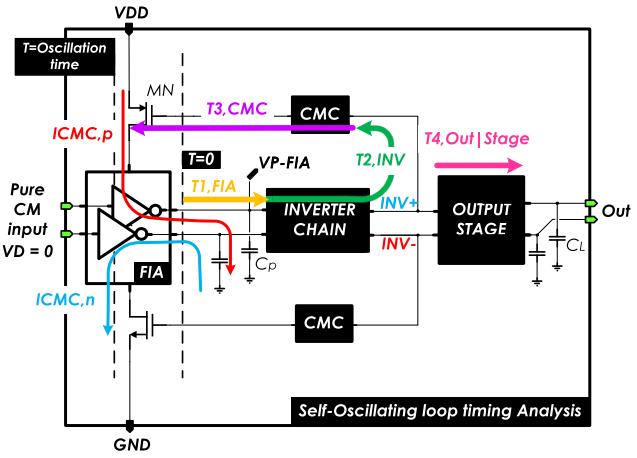



**FIGURE 10.** FI-DIGOTA self oscillation timing loop analysis under pure common-mode input condition.

supply voltage results in exponential rise of $I_{\mathrm{CMC}}$, which in turn reduces $\tau_{\mathrm{FI}}$ and shortens the overall delay of the internal feedback loop. Consequently, the self-oscillation frequency $f_{\mathrm{os}}$ increases, leading to higher dynamic power consumption. At the same time, a higher oscillation frequency shortens the loop period, allowing finer temporal resolution of the current injection pulses, resulting in improved gain and bandwidth performance.

$$f_{\mathrm{os}} = \frac{1}{\tau_{\mathrm{D,Total}}} = \frac{1}{\tau_{\mathrm{FI}} + \tau_{\mathrm{INV}} + \tau_{\mathrm{CMC}}} \tag{4}$$

$$\tau_{\mathrm{FI}} \approx \frac{C_p \cdot V_{\mathrm{DD}}}{I_{\mathrm{CMC}}} \tag{5}$$

Although operation at 450 mV yields the highest DC gain (64.93 dB), oscillation frequency and gain-bandwidth product (171 kHz, 2.83 times versus typical case), these benefits achieved at the cost of substantial increase in power consumption (19.9 nW, 2.84 times compared to the typical case). However, the small signal figure of merit (FOMS) proves that 400 mV offers an optimal and well-balanced compromise between power efficiency and small-signal performance, consistent with the design objectives for sub-10 nW analog circuitry in IoT nodes.

According to Table. 6, the UGFB configuration is characterized over −20° C to 85° C temperature range. Across this interval, the thermal voltage ($V_{\mathrm{T}} = kT/q$) increases from 20.1 mV to 30.4 mV, exhibiting a positive temperature coefficient approximately 0.085 mV/° C. Operating in the weak inversion region, the transconductance efficiency ($g_{\mathrm{m}}/I_{\mathrm{D}} = 1/nV_{\mathrm{T}}$) correspondingly decreases from 31 $V^{-1}$ to 23 $V^{-1}$. In contrast, the MOSFET threshold voltage decreases with the negative temperature coefficient of 1 mV/° C from 0.392 V at 85° C to 0.497 V at −20° C. This reduction in threshold voltage dominates the thermal voltage variations and consequently results in an exponential rise in subthreshold bias current with temperature.

At −20° C, the circuit achieves its highest small-signal figure of merit (FOMS) of 636.36 kHz · pF/nW, with a DC gain of 37.64 dB, unity-gain bandwidth of 70 kHz, and ultra-low power consumption of 1.1 nW. At 85° C, GBW increases to 105 kHz due to the elevated bias current, while the power rises to 44.1 nW. Despite the significant temperature variation, the UGFB configuration maintains stable and power-efficient operation over a wide temperature range. The results indicate that the proposed FI-DIGOTA remains functional across the investigated temperature range, although low-temperature operation reveals increased sensitivity in terms of common-mode and supply-noise rejection.

At low temperature, the circuit exhibits very low power consumption and therefore a high small-signal figure of merit. However, the reduction of CMRR and PSRR at −20° C indicates that the improvement in power efficiency is obtained at the expense of degraded common-mode and supply-noise rejection. This behavior can be attributed to the temperature dependence of the inverter operating point under the severe 400 mV supply constraint. As temperature decreases, the threshold voltages of both NMOS and PMOS devices increase, reducing the available gate overdrive. Consequently, some devices in the floating-inverter stage may operate closer to the weak-inversion or near-cutoff region, shifting the inverter operating point and modifying the balance between the pull-up and pull-down devices. As a result, the common-mode compensation mechanism operates farther from its nominal equilibrium condition, reducing its ability to suppress common-mode disturbances. This effect increases the conversion of common-mode signals into differential components, leading to the observed reduction in CMRR. A similar mechanism affects PSRR, since the shifted operating point increases the sensitivity of the inverter-based signal path to supply-voltage perturbations, thereby enhancing the coupling of supply noise into the output. These results highlight the increased sensitivity of ultra-low-voltage inverter-based amplifiers to temperature-induced operating-point variations.

**TABLE 6.** Temperature ranges for UGFB configuration (VDD = 400 mV, TT process).

| Temperature Range [°] | MIN [−20] | TYP [27] | MAX [85] |
|---|---|---|---|
| $V_{\mathrm{T}}$ [mV] | 20.1 | 25.85 | 30.4 |
| $V_{\mathrm{th}}$ [mV] | 497 | 450 | 392 |
| $\mathrm{AD}_0$ [dB] | 37.64 | 39.78 | 20.13 |
| GBW [kHz] | 70 | 60 | 105 |
| Power Dissipation [nW] | 1.1 | 7 | 44.1 |
| $g_{\mathrm{m}}/I_{\mathrm{D}}$ [$\mathrm{V}^{-1}$] | 31 | 25 | 23 |
| CMRR [dB] | 21.3 | 52 | 48.9 |
| PSRR [dB] | 18.1 | 50 | 47.6 |
| FOMS [kHz·pF/nW] | 636.36 | 85.72 | 23.8 |

### C. ΣΔ MODULATOR RESULTS; LINEARITY ANALYSES

Fig. 11 presents the output spectrum of the first-order ΣΔ modulator under input signal amplitudes of 200 mV within 500 Hz signal bandwidth (signal-BW). To evaluate the linearity and performance of the modulator across frequency, key dynamic parameters including Signal-to-Noise-and-Distortion Ratio (SNDR), Spurious-Free Dynamic Range

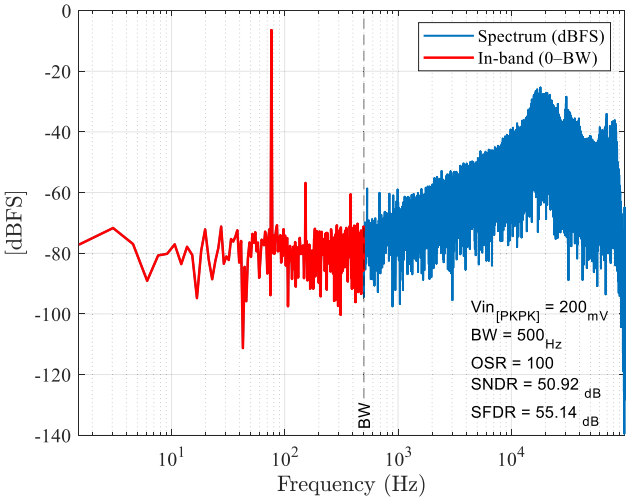



**FIGURE 11.** Output spectrum of the first-order ΣΔ modulator for a 76.3 Hz sine-wave with the input peak-to-peak amplitude of 200 mV.

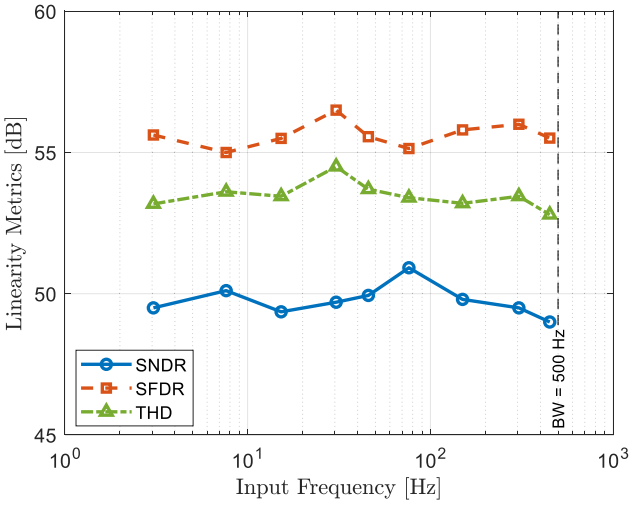



**FIGURE 12.** SNDR, SFDR and THD of the first-order ΣΔ modulator versus frequency under 200 mV peak-to-peak input amplitude over signal bandwidth.

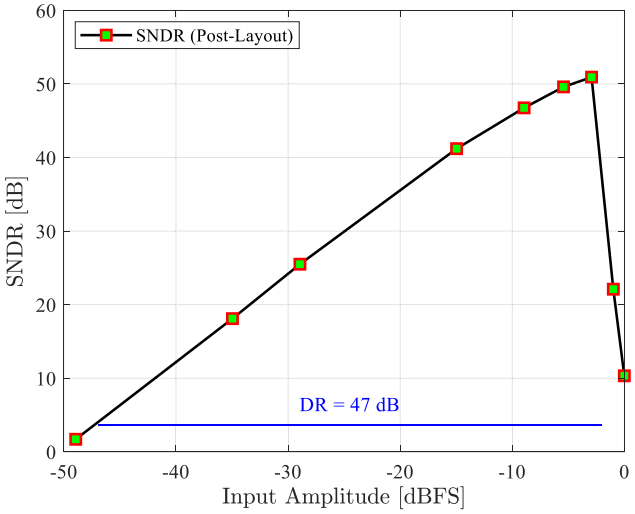



**FIGURE 13.** SNDR versus input amplitude of the first-order ΣΔ modulator for a sine-wave input signal from post-layout simulation.

(SFDR), Total Harmonic Distortion (THD), and Effective Number of Bits (ENOB) were extracted from post-layout simulations over a wide range of input frequencies and input amplitudes.

As shown in Fig. 12, the modulator is tested under sine-wave input with a constant peak-to-peak amplitude of 200 mV across a range of input frequencies from 3.05 Hz to 500 Hz. At each frequency, the spectral metrics were obtained from a $2^{16}$-point FFT-based analysis of the output signal. The results confirm that the modulator maintains an SNDR of about 49 dB across the target bandwidth, with only limited variation in SFDR and THD. The extracted post-layout results show that the modulator consistently maintains an SNDR of approximately 49 dB within the bandwidth of interest (BW) of 500 Hz, confirming the modulator's linearity and stable performance across input frequencies. Although a fully differential architecture ideally suppresses even-order harmonics, in the proposed implementation a residual second harmonic distortion (HD2) component is observed due to practical asymmetries in the CSt-DAC feedback paths. In particular, the current injected into the summing nodes $X_1$ and $X_2$ during the charging/discharging phases (see Fig. 3 a) is not perfectly symmetric, because the corresponding bias currents and switching conditions are affected by mismatch and parasitic imbalance. This degrades the ideal differential symmetry and results in a measurable second-order distortion component.

Table 7 evaluates ΔΣ modulator's robustness over PVT fluctuations. The results are evaluated under the input amplitude of 50 mV peak to peak signal and input frequency of 76.3 Hz. Across different corners (TT/SS/FF), the Schreier figure of merit $\text{FOM}_{\text{SCh}}$ varies only by 3.56 dB, SNDR remains above 41.64 dB and power stays below 20 nW. These results indicate adequate loop-gain and bias margin for stable, energy-efficient operation across corners. Although the FI-based integrator is inherently sensitive to PVT shifts due to weak-inversion operation, the post-layout results show that both the FI-DIGOTA and the complete CT-ΣΔ modulator preserve functional operation and acceptable performance across process corners, supply variation, temperature variation, and Monte Carlo mismatch conditions.

**TABLE 7.** Corner analysis for ΣΔ modulator (VDD = 400 mV, $V_{\text{in,DC}}$ = 200 mV, $V_{\text{in,ac[PKPK]}}$ = 50 mV, $f_{\text{in}}$ = 76.3 Hz, $T$ = 27°C).

| Corner | $\text{FOM}_{\text{SCH}}$ [dB] | Power [nW] | SNDR [dB] |
|---|---|---|---|
| TT | 155.40 | 17.79 | 50.92 |
| SS | 150.67 | 15.70 | 45.64 |
| FF | 148.50 | 18.25 | 44.12 |

FOM definitions: $\text{FOM}_{\text{SCh}} = \text{SNDR} + 10 \times log_{10}\left(\frac{\text{BW}}{\text{P}}\right)$

Fig. 13 shows the dynamic range versus input amplitude. The modulator is tested under 280 mV peak-to-peak differential input full-scale level, sampling frequency of 0.1 MHz, and input signal frequency of 76.3 Hz.

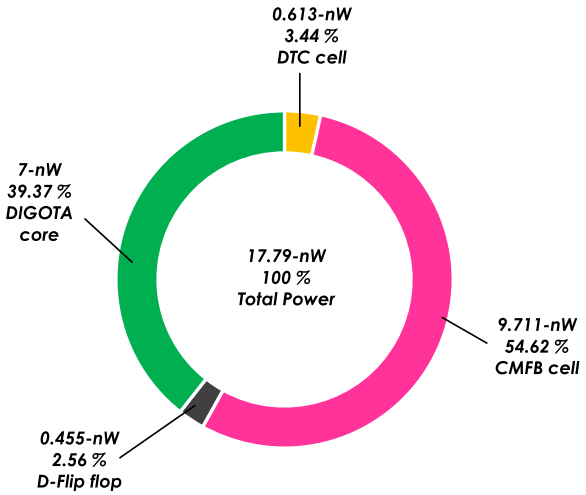



**FIGURE 14.** Power distribution of the whole system in percentage.

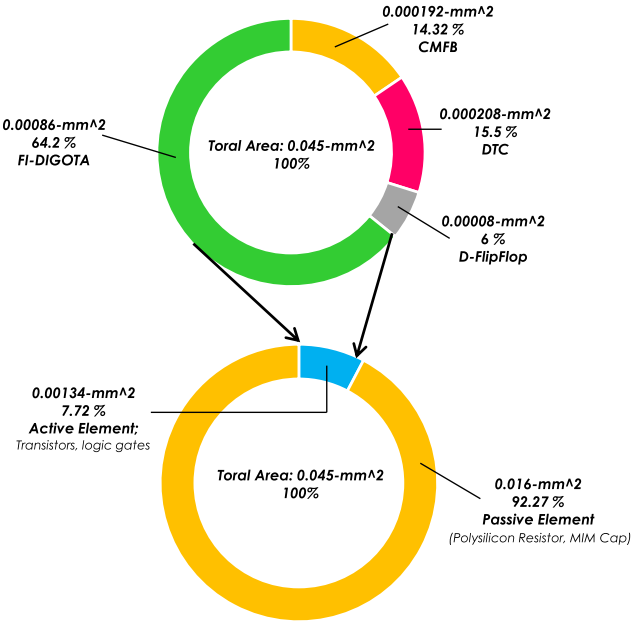



**FIGURE 15.** Area distribution of the whole system in percentage.

### D. POWER AND AREA BREAKDOWN

The total power consumption of the proposed modulator is 17.79 nW and the power breakdown is shown in Fig. 14. From the figure, most of the power is consumed in the CMFB circuitry (9.711 nW) and in the FI-DIGOTA core (7 nW), which account for the 54.62% and for the 39.37% of the overall power consumption. The double-tail comparator and D-type flip-flop exhibit significantly lower consumption, dissipating 0.613 nW (3.44%) and 0.455 nW (2.56%), respectively.

Fig. 15 summarizes the area utilization of the proposed ΣΔ modulator. The bottom pie chart, which partitions the device-level layout into passive versus active elements (i.e., poly silicon resistors and MIM-capacitors vs. logic gates/transistors). Passive components dominate the area occupation with 0.016 $mm^2$, corresponding to 92.27% of the total layout area, while active components occupy only 0.00134 $mm^2$ or 7.72%. The top pie chart further breaks down the active-silicon footprint which highlights the FI-DIGOTA as the largest contributor with the area of 0.00086 $mm^2$ or 64.2%, followed by double-tailed comparator (15.5%), CMFB (14.32%), and D-type flip flop (6%).

## V. DISCUSSION

Table 8 presents a performance summary of the proposed first-order CT-ΣΔ modulator and other state-of-the-art ADC designs. In this design, the $FOM_{SCH}$ is calculated to be 155.4 dB, demonstrating a decent balance between low-power operation and high resolution compared to other state of the art works.

Prior studies have shown that asynchronous and inverter-based first-order modulators can reach power levels as low as 2–28 nW at 250–300 mV supplies, but at the cost of limited SNDR and narrow bandwidths in the order of tens of Hertz [22], [23], [25]. On the other hand, the design trend in the literature indicates that achieving high resolution (SNDR$>$ 60 dB) over large BW typically requires significantly higher power consumption at non-scalable supply voltages, as reported in [20], [26], and [28]. More importantly, when the design trend tends to scale down the supply voltage down to 500 mV, the adoption of inverter-based topologies becomes essential to maintain efficiency and functionality in ultra-low power designs [20], [22], [23]. The use of first-order architecture was intentionally motivated the ultra-low-voltage and ultra-low power design target of this work. Although higher order ΣΔ modulators can achieve higher SNDR, they generally require additional active stages, more stringent loop stabilization, and higher power consumption. In the present design, the primary objective is to assess the feasibility of employing the proposed FI-DIGOTA in a continuous-time modulator under severe energy constraints. Therefore, the proposed modulator is intended as a balanced compromise among power, resolution, bandwidth, and robustness, rather than as a resolution-optimized architecture.

More advanced designs, such as body-biased inverter-based CT modulators [26], bulk-driven asynchronous modulators [23], and SAR ADC with duty-cycled references [25], improve linearity, PVT robustness, and $FOM_{SCH}$ but require higher order and complex design considerations. By contrast, the proposed modulator offers a well-balanced compromise across power, resolution, bandwidth, design effort, and PVT robustness, making it particularly suitable for ultra-low-power sensor interfaces where balanced performance is more valuable than excelling in a single figure of merit.

Although silicon measurements are not yet available, the proposed robustness claim is supported by an extensive post-layout extracted validation campaign carried out in a mature 180-nm CMOS technology. In particular, both the FI-DIGOTA and the complete CT-ΣΔ modulator were evaluated under process-corner variations, supply-voltage variations, temperature variations, and Monte Carlo simulations

**TABLE 8. Comparison with the State-of-the-Art of low-power oversampling ADCs (best in bold).**

| **State-of-art works** | [20] | [21] | [22] | [27] | [23] | [24] | [25] | [26] | [28] | This work |
|---|---|---|---|---|---|---|---|---|---|---|
| Validation | Meas. | Meas. | Meas. | Meas. | Meas. | Meas. | Meas. | Meas. | Meas. | Sim. |
| Year | 2019 | 2023 | 2020 | 2025 | 2015 | 2008 | 2016 | 2021 | 2022 | 2026 |
| ADC Architecture | CTΔΣ | DTΔΣ | DTΔΣ | ASΔΣ | ASΔΣ | DTΔΣ | SAR | CTΔΣ | DTΔΣ | CTΔΣ |
| Process Technology, [nm] | 130 | 180 | 180 | 180 | 130 | 500 | 65 | 28 | 65 | 180 |
| Power Supply Voltage, [mV] | 400 | 300 | 300 | 300 | **250** | 1200 | 800 | 600 | 1000 | 400 |
| Silicon Area [$mm^2$] | 0.014 | 0.027 | **0.00256** | 0.059 | 0.141 | 0.6 | 0.077 | 0.12 | 0.04 | 0.045 |
| OTA core architecture | custom+Inverter | Inverter | Inverter | custom | custom | Class-AB | custom | Inverter | Inverter | Digital |
| Design Style | custom | std cell | std cell | custom | custom | custom | custom | std cell | custom | cust./std cell |
| Modulator Order | 3 | 2 | 1 | 1 | 1 | 2 | – | 3 | 2 | 1 |
| OSR ratio | 128 | 256 | 32 | 35 | - | 64 | – | 160 | 256 | 100 |
| Signal Bandwidth [Hz] | **50,000** | 3.9 | 67.2 | 81 | 30 | 25 | – | 40,000 | 19,500 | 500 |
| Sampling rate [MS/s] | 6.4 | 0.002 | 0.0043 | 0.3 | – | 0.0032 | 0.8 | **12.8** | 10 | 0.1 |
| Power [nW] | 26300 | 10.4 | **4** | 34 | 28 | 140 | 106 | 33,600 | 43,500 | 17.79 |
| Peak SNDR [dB] | 68.5 | 73.9 | 37.9 | 57.1 | 58 | 62.6 | 52 | 83 | **85.5** | 50.92 |
| Peak SFDR [dB] | 82.6 | - | 41.7 | – | – | – | 78 | **94.2** | 97.9 | 55.14 |
| ENOB [Bit] | 11 | 12 | 6 | 9.2 | 9.34 | 10.1 | 9.1 | **13.49** | 13.9 | 8.166 |
| $\mathrm{FOM_W}\left[\frac{\mathrm{fJ}}{\mathrm{conv.step}}\right]$ $a^*$ | 120.94 | 340.86 | 436.96 | 358.66 | 719 | 2540.12 | **2.414** | 36.37 | 72.44 | 61.93 |
| $\mathrm{FOM_{SCH}}$ [dB] $b^*$ | 161.3 | 159.6 | 140.1 | 150.9 | 148.3 | 145.12 | – | **173.8** | 172 | 155.4 |

FOM definitions: $a^*)\ \mathrm{FOM_W} = \frac{\mathrm{P}}{2^{\mathrm{ENOB}} \cdot 2\mathrm{BW}}$, $b^*)\ \mathrm{FOM_{SCH}} = \mathrm{SNDR} + 10\log_{10}\left(\frac{\mathrm{BW}}{\mathrm{P}}\right)$.

including mismatch and process spread. Therefore, the reported results should be interpreted as strong pre-silicon evidence that the proposed architecture preserves functionality and acceptable performance across realistic PVT conditions, while final experimental confirmation is left to future silicon measurements [39], [40].

## VI. CONCLUSION

This work presented a fully differential floating-inverter digital OTA (FI-DIGOTA) with isolation resistor-based frequency compensation, offering a improved gain-bandwidth performance, silicon area, energy efficiency, and robust operation across PVT variations. Building on this foundation, a first-order CT-ΣΔ modulator was implemented using the FI-DIGOTA as its core integrator, demonstrating reliable noise shaping behavior, strong linearity, and ultra-low power consumption. Due to its minimal analog complexity and compatibility with digital design flow, the proposed modulator offers a promising solution for energy-constrained IoT interfaces where energy and area efficiency are critical.

## ACKNOWLEDGMENT

This manuscript reflects only the authors' views and opinions, neither European Union nor European Commission can be considered responsible for them.

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**HOSSEIN FIROUZKOUHI** (Student Member, IEEE) was born in Sari, Iran, in 1992. He received the B.Sc. degree in electrical and electronic engineering from Iran University of Science and Technology, Tehran, Iran, and the M.Sc. degree in analog mixed-signal (AMS) IC design engineering from the Polytechnic University of Shahrud, Iran. He is currently pursuing the Ph.D. degree with the Politecnico di Torino, Turin, Italy. His current research interests include ultra-low-power subthreshold AMS circuit design, focusing on floating-inverter digital-centric operational transconductance amplifier (FI-DIGOTA) and sigma-delta modulators for energy-efficient sensor interfaces.



**PAOLO STEFANO CROVETTI** (Senior Member, IEEE) was born in Turin, Italy, in 1976. He received the Laurea (summa cum laude) and Ph.D. degrees in electronic engineering from the Politecnico di Torino, Turin, in 2000 and 2003, respectively. He is currently an Associate Professor with the Department of Electronics and Telecommunications (DET), Politecnico di Torino, where he leads a Research Group in analog, mixed-signal and power microelectronics with several international collaborations and teaches courses on basic and automotive electronics. He has co-authored more than 120 papers appearing in journals and international conference proceedings. His recent research activities are focused on non-conventional digital-based information processing techniques and ultra-low-voltage, ultra-low-power IC design for the Internet of Things. In 2009 and 2019, he was co-recipient of the Excellent Paper Award of the EMC'09 Kyoto Symposium and of the Best Student Paper Award of the International Symposium of Circuits and Systems ICECS 2019. He served as the Co-Chair for the IEEE EMC Society—Italy Chapter, from 2024 to 2025. He serves as the Editor-in-Chief of *IET Electronics Letters* and as a Senior Associate Editor of IEEE Transactions on Circuits and Systems—Part I: Regular Papers and IEEE Transactions on Very Large Scale of Integration.