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A Dual-Branch Flux-Based Extended Memristor Model With Machine-Learning-Assisted Calibration

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ABSTRACT

Resistive switching devices based on complex oxide heterostructures exhibit rich, history-dependent electrical responses arising from polarity-selective transport mechanisms, defect dynamics, and interfacial phenomena. Accurately capturing these nonlinear behaviors remains a major challenge for predictive device modeling and for the reliable design of large-scale memristive systems. Here, we introduce a dual-branch, flux-controlled extended memristor model that provides a physically interpretable asymmetric conduction in multilayer Au/HfO_x/Al_2O_3/TiO_2/TiN devices. The model is calibrated and validated against experimental current–voltage characteristics measured on laboratory-fabricated devices. The approach decomposes the device memductance into two polarity-activated branches that reproduce the distinct forward and reverse transport regimes, while embedding flux as the internal state variable governing long-term evolution and hysteresis shaping. A hybrid machine-learning calibration pipeline—combining Latin Hypercube Sampling, Bayesian Optimization, and gradient-based refinement—enables robust parameter identification directly from current–voltage experimental measurements, ensuring quantitative agreement across a broad range of time- and frequency-dependent excitations. The resulting model captures key physical signatures such as lobe asymmetry, history dependence, and flux accumulation, providing a unified framework suitable for device characterization, circuit-level simulation, and neuromorphic hardware design. Owing to its modular structure and physical consistency, the methodology can be readily extended to other classes of resistive switching materials and memory devices.

1 | Introduction

Memristive devices are central to next-generation electronic and neuromorphic platforms, where their inherently history-dependent conductance enables compact, energy-efficient, and non–von Neumann information processing architectures [1–4]. In multilayer oxide stacks, however, the interplay of oxygen-vacancy transport, interfacial barrier modulation, and multi-step electronic conduction produces strongly nonlinear and polarity-dependent current–voltage (I–V) characteristics. These behaviors, widely reported for valence-change and electrochemical-metallization mechanisms in transition-metal oxides [5], remain challenging to capture with classical compact models. Chua's ideal memristor, defined solely through a flux–charge relationship, offers an elegant theoretical foundation [6]. Yet, its single-state formulation cannot reproduce the asymmetry, threshold behavior [7, 8], and multi-physics transport observed in real oxide-based devices [9]. Chua's broader taxonomy of extended memristors [10] accommodates these effects by allowing the memductance $G(\mathbf{x}, v)$ to depend simultaneously on internal states and instantaneous excitation [11, 12]—an essential requirement for capturing Schottky emission, trap-assisted tunneling,

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and vacancy-driven dynamics in nanoscale resistive switching systems [13–17]. A persistent open challenge is the modeling of intrinsic lobe asymmetry in experimental I–V curves [7, 8, 18–20], where opposite voltage polarities activate distinct conduction mechanisms [21] that cannot be embedded in a single scalar constitutive surface. Many existing approaches handle this complexity by introducing highly parametric behavioral models or machine-learning surrogates [22–24], often sacrificing physical interpretability or SPICE compatibility. Physics-based compact models for RRAM and VCM devices have been developed to describe filamentary evolution, barrier modulation, or thermodynamic effects [13, 25–27]. However, these formulations do not naturally reproduce polarity-selective asymmetric curves. Here, we address this limitation by introducing a physically grounded dual-branch flux-controlled extended memristor model that retains the structure of Chua's original formulation while enabling accurate reproduction of complex asymmetric I–V characteristics with a single compact circuit realization. The model decomposes the memductance into two polarity-selective nonlinear branches, each governed by flux as the internal state variable, thereby capturing SET and RESET mechanisms within a unified and interpretable framework. Unlike black-box neural or purely data-driven models, our formulation relies exclusively on passive, polarity-selective nonlinear elements—diodes, nonlinear resistors, and flux-controlled branches—preserving analytical consistency with memristive theory and ensuring full SPICE compatibility [28, 29]. To identify device-specific parameters, we develop a hybrid machine-learning calibration pipeline that combines Latin Hypercube Sampling, Gaussian-process Bayesian Optimization, and gradient-based refinement [30–32]. This automated strategy efficiently navigates the high-dimensional parameter space and extracts physically meaningful parameters directly from experimental I–V data. Importantly, the pipeline enhances—but does not replace—the physical model: the resulting calibrated device retains a compact analytical structure. As a result, the proposed model is able, for the first time, to reproduce the full spectrum of nonlinear, history-dependent, and asymmetric I–V features of multilayer Au/HfO_x/Al_2O_3/TiO_2/TiN devices with high accuracy across widely varying excitation frequencies and waveforms. Building on these considerations, the present work develops and validates a compact flux-controlled extended memristor model tailored to the asymmetric transport dynamics of multilayer devices. The following sections experimentally characterize the device, outline the limitations of ideal memristor theory, formalize the dual-branch modeling framework, and evaluate its accuracy against measured I–V characteristics across a wide range of excitation conditions.

2 | Results and Discussion

2.1 | Device Structure and Physical Origins of Asymmetry

The device considered in this work incorporates a multilayer functional stack composed of TiO_2, Al_2O_3, and HfO_x, as illustrated in Figure 1 [33]. The intrinsic asymmetry of this stack is the primary driver of the polarity-dependent electrical behavior observed experimentally. The 15 nm TiO_2 bottom layer forms a stable interface with the TiN electrode and acts as an oxygen reservoir, while the ultrathin Al_2O_3 layer (regrown by oxidation of a sputtered Al film) regulates vacancy formation and redistribution at the Al_2O_3/HfO_x interface. The upper HfO_x layer ($x \approx 1.98$) constitutes the active switching medium in which field-driven vacancy drift modulates the interfacial barrier. Under positive bias, vacancies migrate toward the Al_2O_3/HfO_x interface, reducing the effective barrier height and enabling the SET transition. Under negative bias, vacancies drift away from the interface, restoring the barrier and producing a RESET response. These two drift directions activate distinct transport mechanisms, including Schottky emission, vacancy drift, and trap-assisted tunneling, yielding the pronounced asymmetry of the measured I–V characteristics shown in Figure 7. This intrinsic physical asymmetry directly motivates the polarity-dependent modeling strategy adopted in this work, where two antiparallel extended memristor branches describe the forward and reverse conduction pathways, as shown in Figure 5. All electrical measurements used for model development and validation were performed on experimentally fabricated Au/HfO_x/Al_2O_3/TiO_2/TiN memristive devices, following the experimental protocol reported in Supporting Information Section S2.

2.2 | Limitations of the Ideal Memristor Model

The ideal memristor relies on a single internal state variable—the flux $\phi(t) = \int_0^t v(\tau)\, d\tau$—which uniquely defines the memductance $G(\phi)$ and the device current:

$$i(t) = G(\phi)\, v(t) \tag{1}$$

This formulation constrains all admissible trajectories to a two-dimensional manifold in the (I, V, ϕ) domain. As shown in Figure 2 in the left part, evaluating the constitutive law over a (ϕ, V) grid produces a smooth single-sheet surface. The system evolution is restricted to this single surface for any input waveform. This geometric constraint directly imposes the canonical orientation rules of the ideal memristor. When driven by a zero-mean periodic excitation, the sign of $dG/d\phi$ alone determines the rotation direction of the pinched hysteresis loop: a decreasing memductance yields clockwise rotation in the positive lobe and counterclockwise rotation in the negative one; an increasing $G(\phi)$ reverses the pattern. The two configurations shown in Figure 3 exhaust all possible orientations admissible under the ideal formulation. No additional lobe-specific deformation, polarity dependence, or threshold behavior can emerge, because the device evolution cannot leave the single flux-controlled surface [12]. These inherent restrictions stand in sharp contrast with the behavior of oxide-based resistive switching devices, which exhibit asymmetric I–V lobes, distinct SET and RESET conduction regimes, and coexistence of multiple transport mechanisms. Such phenomena require the current trajectory to access different regions of the (I, V, ϕ) space, as illustrated in Figure 2 (right). The ideal memristor therefore provides a mathematically consistent but physically incomplete description of resistive switching devices. Its single-state formulation lacks the dimensionality needed to represent polarity-dependent transport in real devices.

Such limitations directly motivate the need for a constitutive representation capable of generating a multi-surface current domain. As illustrated in the right panel of Figure 2, real oxide-based devices occupy a thick three-dimensional region in the

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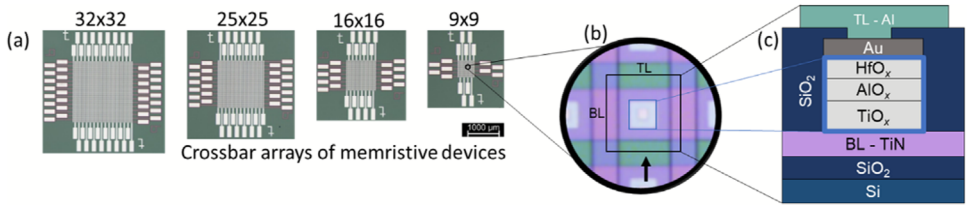

FIGURE 1 | (a) Optical microscope image of passive crossbar arrays fabricated in a 4-inch wafer thin-film technology with 32×32, 25×25, 16×16 and 9×9 memristive devices. (b) Enlarged image of a crosspoint memristive device: the horizontal line marks the bottom electrode line (BL), the vertical line marks the top electrode line (TL), the highlighted black square indicates the position of the device, and the blue square indicates the position of the functional layer stack. (c) Detailed cross-section of the fabricated device stack includes, from bottom to top: Si wafer, SiO_2 layer, TiN BL, a three-layer functional stack of $HfO_x/Al_2O_3/TiO_2$, Au top electrode, SiO_2 passivation layer, and Al TL.

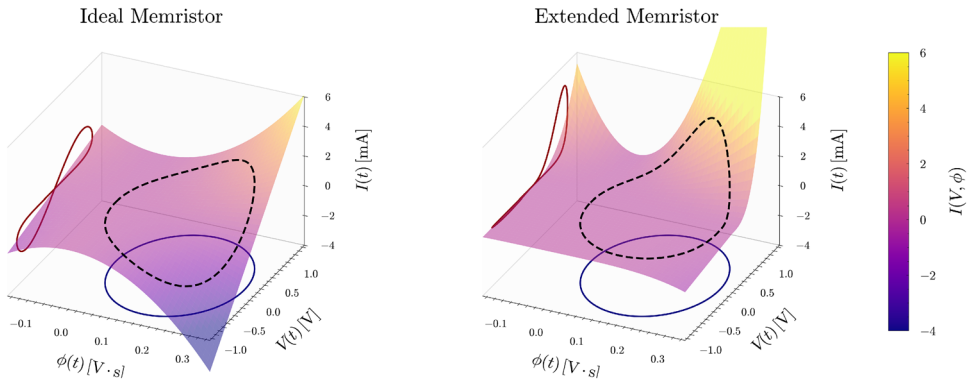

FIGURE 2 | Three-dimensional (I, V, ϕ) representations of the ideal (left) and extended (right) memristor models under the sinusoidal excitation $v(t) = A\sin(2\pi f t)$ with $A = 1$ V and $f = 1$ Hz. For each model, the semi-transparent *plasma* surface visualizes the full current domain obtained by evaluating the constitutive equation over the (ϕ, V) meshgrid. The black dashed curve denotes the actual system trajectory generated by the applied input, while the dark-red and navy curves represent its projections onto the (I, V) and (ϕ, V) planes, respectively. In the ideal case, the current collapses onto a single flux-dependent manifold $I = G(\varphi)V$, here illustrated using $G(\phi) = \beta \cdot \phi^2$ with $\beta = 0.04$, resulting in symmetric lobes. Conversely, the extended memristor produces a fully shaped and non-collapsing (I, V, ϕ) domain, enabling asymmetric and device-specific behaviors; the illustrative memductances $G_+(\varphi, V) = 3\beta \cdot \phi^2 \cdot V^2$ and $G_-(\varphi, V) = \beta \cdot \varphi^4$ are used solely to demonstrate this generalized framework. ϕ is obtained as the time integral of the voltage and it has initial condition $\phi(0) = 0$.

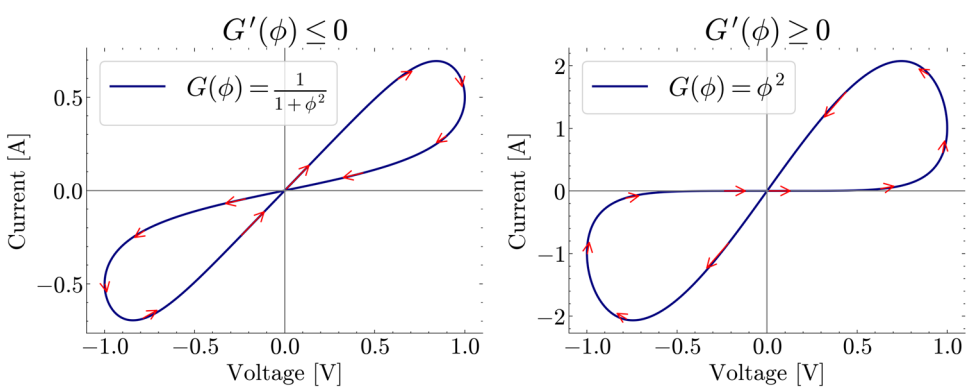

FIGURE 3 | Simulated I vs. V curves of two distinct periodically-forced memristors with the indication of the direction of motion of the point trajectory along them over time, as induced by different memductance trends: decreasing $G(\phi)$ (a) and increasing $G(\phi)$ (b). A sinusoidal voltage input of unitary amplitude is applied across the ideal memristor in both cases.

(I, V, ϕ) space rather than the single flux-controlled surface. This behavior arises because opposite voltage polarities activate fundamentally different physical pathways—such as field-enhanced vacancy drift during SET and barrier reconstruction during RESET—which cannot be embedded in a single scalar function $G(\phi)$. To capture these polarity-selective transport modes, the memductance must depend not only on the internal state but also explicitly on the applied voltage, leading naturally to the extended

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formulation $G(\phi, v_M)$:

$$i_M(t) = G(\phi, v_M)\, v_M(t) \tag{2}$$

In multilayer Au/HfO_x/Al_2O_3/TiO_2/TiN structures, the SET and RESET processes are governed by distinct conduction mechanisms. This motivates the decomposition of the total memductance into two voltage-activated branches, schematically represented in Figure 5:

$$G(\phi, v_M) = H(v_M)\, G_+(\phi, v_M) + H(-v_M)\, G_-(\phi, v_M) \tag{3}$$

where $H(\cdot)$ is a smooth Heaviside function. This polarity-based decomposition allows the current trajectory to access different regions of the (I, V, ϕ) domain during positive and negative bias, thereby overcoming the single-surface constraint of the ideal memristor. As observed experimentally and reflected in Figure 2 (right), the extended formulation provides precisely the additional dimensionality required to reproduce asymmetric hysteresis, lobe deformation, different directionality, and the thick multi-surface current domain characteristic of real oxide-based resistive switching devices.

2.2.1 | Flux Accumulation and Experimental Evidence

Flux accumulation is a direct consequence of the flux-controlled formulation $\dot{\phi} = v_M(t)$ and constitutes one of the most distinctive signatures of memristive behavior. Under symmetric periodic excitation with zero mean ($\langle v_M \rangle = 0$), the flux remains bounded and the resulting hysteresis loop is stable across cycles. However, when the applied waveform contains even a small DC component, the flux begins to drift monotonically, leading to an *unbounded* evolution of the internal state. This mechanism is illustrated in Figure 4, where a simplified ideal memristor is driven by symmetric and asymmetric inputs. In the latter case, the flux grows without bound, progressively modifying the memductance and distorting the associated I–V trajectory over successive cycles. This phenomenon is not merely a theoretical artifact. Experimental measurements from the Au/HfO_x/Al_2O_3/TiO_2/TiN device exhibit the same qualitative behavior as shown in Figure 4. In particular, Figure 4b shows the experimentally applied voltage and the corresponding measured current, while the flux variable is numerically reconstructed from the experimental voltage waveform by time integration, consistently with the flux-controlled formulation of the proposed model. This reconstruction allows the sign and magnitude of the accumulated voltage imbalance to be directly compared with the measured current evolution. Under the same measurement configuration, three voltage profiles were intentionally selected to impose positive, approximately zero, and negative average values over one period. In the first row, the triangular waveform spans from +3 V to −2 V and produces a progressive increase of the reconstructed flux. In the second row, the waveform spans from +3 V to −3 V and yields a zero flux average value. In the third row, the waveform spans from +3 V to −4 V and drives the reconstructed flux in the opposite direction. Therefore, the observed flux drift is sign-reversible and follows the intentionally imposed voltage asymmetry, rather than a fixed instrumental DC offset. Zero-mean voltage inputs generate stable, repeatable hysteresis loops, whereas even slight asymmetries in the excitation induce a gradual drift of the flux extracted from the voltage waveform. As the flux accumulates, the device transitions into a new conduction regime, producing a shifted and distorted I–V trajectory. Nevertheless, unlike the ideal memristor—which must follow a fixed (I, V, ϕ) surface and therefore cannot prevent indefinite deformation—the experimental device reaches a new quasi-steady operating condition, reflecting the coexistence of multiple conduction mechanisms, threshold nonlinearities, and strong polarity dependence intrinsic to its multilayer structure. Taken together, the simulated and experimental results show that the reconstructed flux provides a consistent descriptor of the observed cycle-to-cycle current evolution. The ideal memristor framework captures the emergence of flux drift under nonzero-mean excitation, but it cannot reproduce the long-term quasi-stabilized response of the experimental device. This discrepancy suggests that real devices may exhibit slow equilibration mechanisms that counterbalance flux drift and drive the system toward a quasi-steady operating condition. In a generalized formulation, this effect could be described by

$$\frac{d\phi}{dt} = v_M(t) - \frac{\phi}{\tau} \tag{4}$$

where τ is an effective relaxation time. In the present compact model, we consider the operating regime in which the relaxation time is much longer than the excitation time scale, i.e., $\tau \gg T_{\mathrm{op}}$. The model therefore operates in the large-relaxation-time limit $\tau \to \infty$, for which

$$\frac{d\phi}{dt} = v_M(t), \qquad \phi(t) = \int_0^t v_M(\tau')\, d\tau' \tag{5}$$

This approximation preserves consistency with Chua's flux-controlled memristive framework and with the charge–flux description of memristive circuits [6, 34], while keeping the state equation compact. Finite relaxation terms become relevant over longer time scales, such as retention, conductance drift, and post-programming equilibration, where slow defect and interface relaxation mechanisms influence the device state, as discussed for this device technology in Ref. [35].

2.3 | Circuit Model and Analytical Formulation

The proposed dual-branch extended memristor is implemented as a fully passive, SPICE-compatible circuit [29], shown in Figure 5. This structure mirrors the intrinsic material asymmetry of the Au/HfO_x/Al_2O_3/TiO_2/TiN stack, where positive and negative bias activate distinct SET and RESET pathways. The architecture consists of two antiparallel branches. Each branch ensure smooth polarity activation and contains:

- an extended memristor element $M_\pm$ encoding the memory-dependent contribution,
- a nonlinear resistor $R_\pm$ reproducing instantaneous transport.

The terminal current follows the polarity-weighted superposition

$$i_M = H(v_M)\, i_+ + H(-v_M)\, i_- \tag{6}$$

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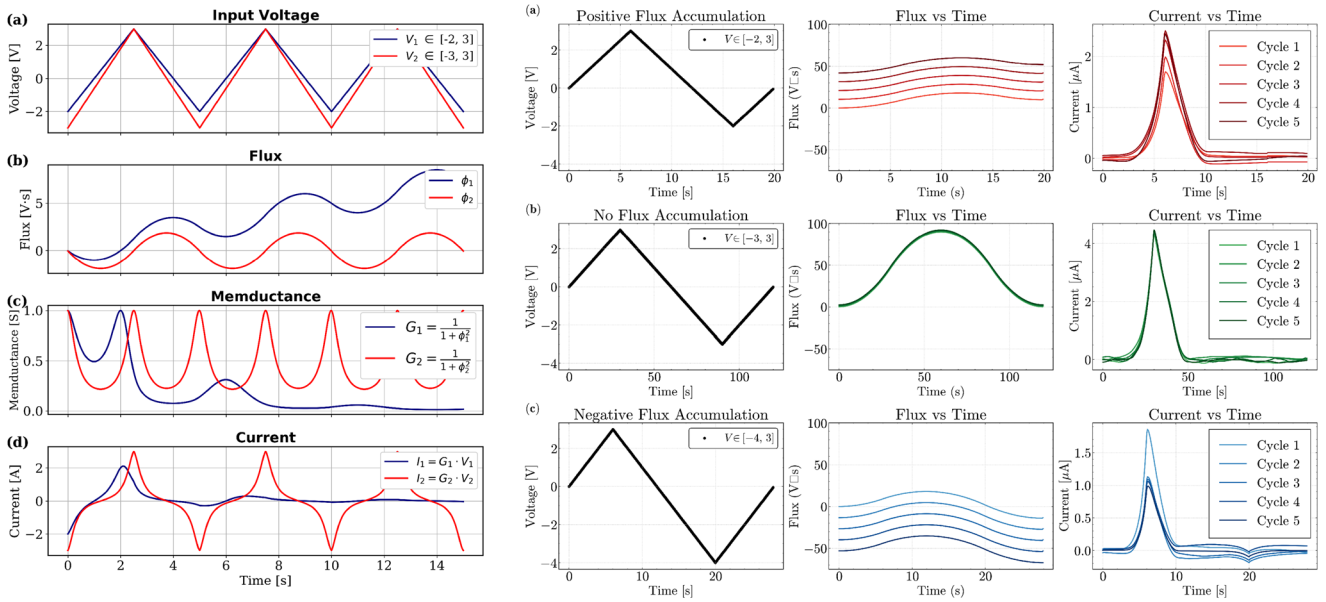

(a) Simulated ideal memristor **(b)** Experimental device behavior

FIGURE 4 | Comparison between simulated and experimental manifestations of flux accumulation. (a) Simulation of a flux-controlled ideal memristor under symmetric (red) and asymmetric (navy) inputs. A nonzero mean voltage induces unbounded drift of the flux $\phi(t)$, progressively deforming the hysteresis loop. (b) Experimental voltage, flux, and current traces from the Au/HfO_x/Al_2O_3/TiO_2/TiN device under three excitation profiles: (a) positive flux accumulation due to net positive bias, (b) bounded flux under zero-mean excitation, and (c) negative flux accumulation under asymmetric input. Experimental results confirm the flux-drift phenomenon predicted by theory, while also revealing richer nonlinear dynamics that cannot be captured by an ideal memristor model.

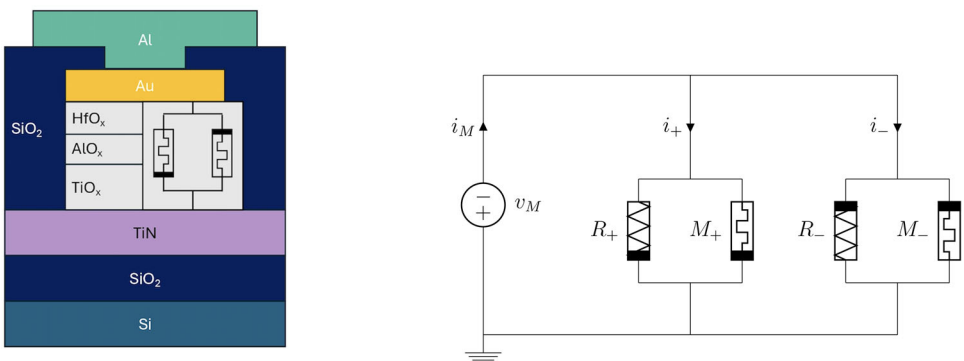

FIGURE 5 | Combined representation of the physical multilayer memristive device and its SPICE-compatible dual-branch extended memristor model. The left panel shows the Au/HfO_x/Al_2O_3/TiO_2/TiN stack, whose intrinsic material asymmetry leads to polarity-dependent conduction. The right panel illustrates the dual-branch circuit implementation, where two extended memristors and nonlinear resistors are activated under opposite voltage polarities, enabling accurate modeling of asymmetric SET and RESET dynamics.

with branch currents decomposed as

$$i_{\pm}(\phi, v_M) = i_{M,\pm}(\phi, v_M) + i_{R,\pm}(v_M) \tag{7}$$

This dual-branch decomposition also clarifies the distinction between the proposed formulation and classical threshold-based compact models such as TEAM and VTEAM. In these models, SET and RESET are described through a single internal state variable and a single effective switching law, while polarity dependence is introduced by current or voltage thresholds and fitting parameters. Although this approach is compact and computationally efficient, the positive and negative hysteresis lobes remain coupled through the same state-evolution framework, as further detailed in the benchmark-oriented comparison reported in the Section S7. Consequently, large differences in lobe magnitude, curvature, and saturation can only be reproduced indirectly through parameter tuning and window functions. In contrast, the proposed model assigns separate analytical current laws to the two voltage polarities, allowing independent control of the SET and RESET current scales while retaining a common flux-based memory variable. This structure is general and allows the model to represent different classes of resistive-switching

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devices by selecting appropriate voltage- and flux-dependent expressions for the two branches. For the specific multilayer $Au/HfO_x/Al_2O_3/TiO_2/TiN$ devices investigated in this work, the instantaneous (non-memory) conduction terms take the form

$$i_{R,+} = I_0(e^{\eta v_M} - 1) \tag{8}$$

$$i_{R,-} = I_0'\left(e^{\eta' v_M} - 1\right) \tag{9}$$

which reflect the dominant Schottky-type and barrier-mediated transport mechanisms active under positive and negative bias, respectively, without affecting internal state evolution. The internal state evolves according to $\phi(t) = \int_0^t v_M(\tau)\, d\tau$, following Chua's original circuit-theoretic definition of the memristor, in which device memory is associated with the flux–charge relation and flux is obtained as the time integral of the terminal voltage [6, 34]. In the present model, ϕ is used as an effective electrical memory coordinate that compactly captures the cumulative influence of the applied voltage history on the device conductance.

2.3.1 | Negative-Polarity Memcurrent (RESET)

The RESET dynamics are dominated by interface-limited transport and partial recovery of the potential barrier when vacancies drift away from the active interface. This behavior is modeled by the negative-polarity memcurrent

$$i_-(\phi, v_M) = a\,(e^{-\gamma v_M} - 1)\sqrt{\phi''} \tag{10}$$

with the flux-dependent factor

$$\phi'' = \frac{\phi^2}{\phi_0} \tag{11}$$

The exponential dependence in v_M reproduces Schottky-type conduction and barrier-limited processes under negative bias [14], while the $\sqrt{\phi''}$ term introduces a controlled history dependence derived empirically. In this way, the RESET transition remains sensitive to the accumulated flux but does not diverge under long excitations.

2.3.2 | Positive-Polarity Memcurrent (SET)

The SET process is governed by the formation and reinforcement of a conductive interface driven by vacancy drift and field-induced barrier lowering. To capture this, the positive-polarity memcurrent is written as

$$i_+(\phi, v_M) = c(\phi)\left(v^3 + d\left(e^{\beta v} - 1\right)\right)\arctan(\phi') \tag{12}$$

with

$$\phi' = \frac{\phi^4}{\phi_0^3} \tag{13}$$

$$c(\phi) = c_0 + \frac{c_1}{1 + e^{-k(\phi - \phi_1)}} \tag{14}$$

The cubic term in v models the low-field conduction regime and is consistent with the polynomial behavior reported for

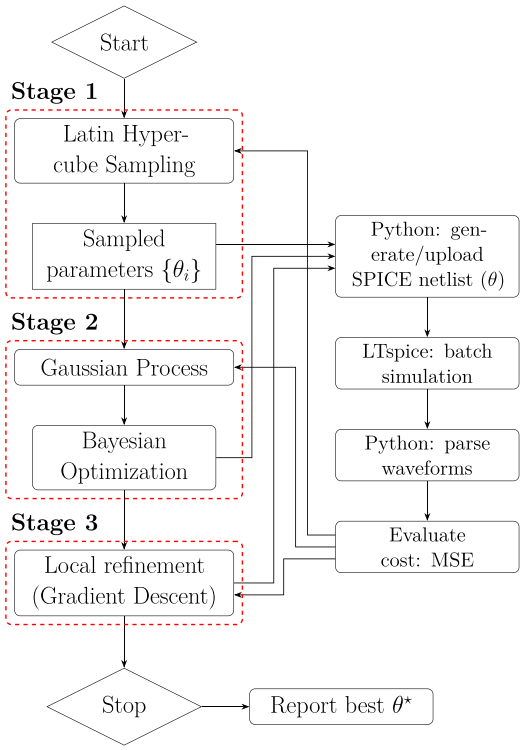

FIGURE 6 | Closed-loop pipeline for ML-based parameter optimization, integrating Python control with LTspice simulations.

multilayer vacancy-drift memristors in neuromorphic settings [36]. This choice is physically compatible with the low-bias expansion of nonlinear transport mechanisms in thin insulating and disordered oxide layers. In tunneling-type descriptions, the low-bias current can be expressed as an odd power expansion of the applied voltage, where the cubic contribution represents the first nonlinear correction beyond the quasi-linear conductance term [37]. Similar superlinear behavior may also arise from trap-assisted tunneling and trap-limited or space-charge-limited conduction, which are commonly reported in resistive-switching oxides [38, 39]. The exponential contribution $d(e^{\beta v} - 1)$ captures the high-field Schottky-type transport and field-assisted vacancy drift that is typically observed during the SET transition in oxide-based RRAM [14]. The functions $\arctan(\phi')$ and $c(\phi)$ are phenomenological compact-model terms. They are introduced to impose a smooth and bounded dependence of the SET branch on the accumulated electrical history. In particular, $\arctan(\phi')$ acts as a saturating memory-dependent activation factor, preventing unphysical divergence of the memductance under long excitation times, while the logistic prefactor $c(\phi)$ describes the gradual transition toward a saturated high-conductance regime. This bounded evolution is consistent with the experimentally observed stabilization of the conductive state after SET and with compact modeling strategies in which nonlinear window or saturation functions are used to preserve physical and numerical consistency [7, 8, 20].

Overall, presented equations define a physics-informed compact formulation that links the dominant transport signatures of the investigated stack to a SPICE-compatible analytical structure. For the present $Au/HfO_x/Al_2O_3/TiO_2/TiN$ devices, the voltage-dependent exponential terms capture barrier-mediated

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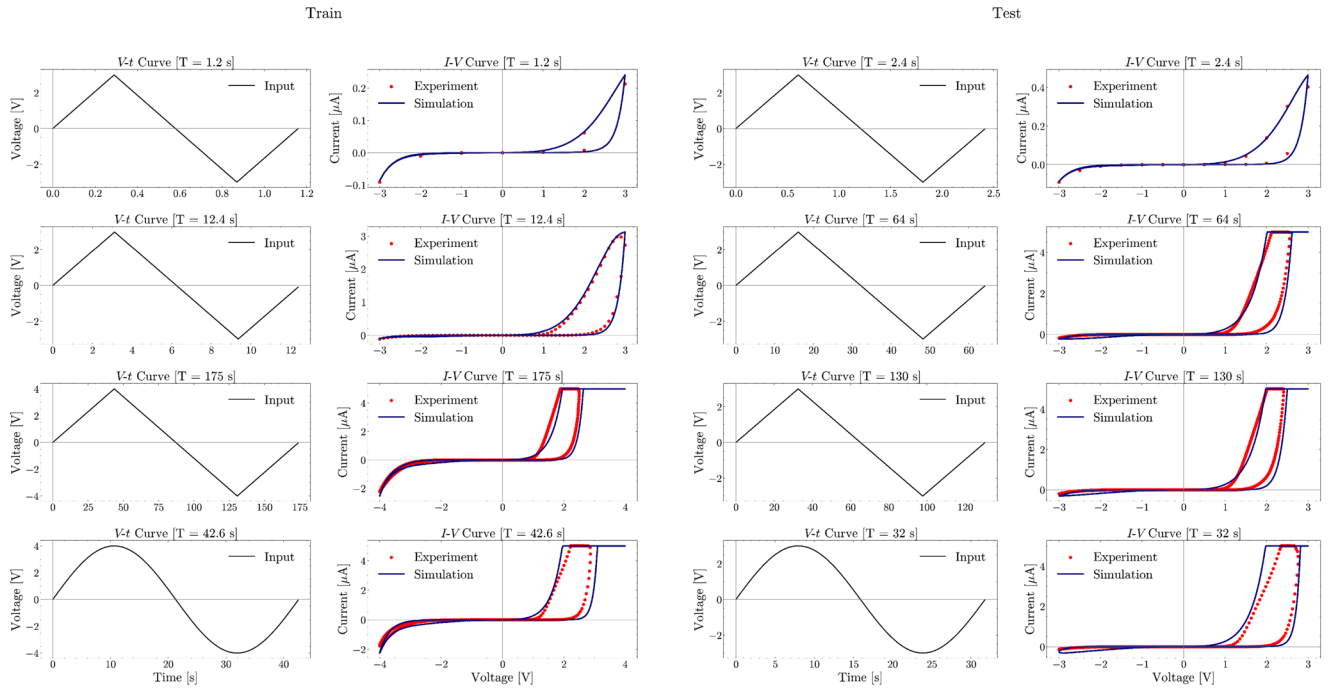

(a) Calibration dataset (Train) **(b)** Validation dataset (Test)

FIGURE 7 | Experimental and simulated I–V characteristics for the $HfO_x/Al_2O_3/TiO_2$ device. **Left**: training dataset used for parameter calibration under triangular and sinusoidal excitations. **Right**: validation dataset acquired under waveforms not included during calibration. The model accurately reproduces nonlinear conduction, hysteresis deformation, and frequency-dependent loop narrowing across all conditions. Red markers denote experimental I–V measurements acquired from the $HfO_x/Al_2O_3/TiO_2$ device, whereas blue curves denote the corresponding simulated response of the calibrated model.

high-field transport [13, 20], whereas the polynomial [36] and bounded flux-dependent factors encode the measured low-field curvature and memory saturation while preserving numerical stability. Owing to the modular branch-based structure of the model, the framework can be extended to other material stacks by replacing or recalibrating the branch-specific conduction laws.

2.3.3 | Flux scaling

The auxiliary flux variable is normalized through the scaling

$$\phi_0 = v_0 \Delta \tag{15}$$

where Δ is the excitation period and v_0 is a voltage scaling constant. This choice ensures dimensional consistency and binds the effective saturation thresholds of ϕ' and ϕ'' to the time scale of the applied waveform. Practically, this normalization allows the model to describe both quasi-DC and higher-frequency excitations with a single parameter set, while keeping the internal state evolution bounded.

This unified formulation links circuit topology, mathematical structure, and physical transport mechanisms into a compact model that reproduces asymmetric SET/RESET behavior, nonlinear conduction, and history-dependent hysteresis in multilayer oxide memristors.

2.4 | Machine Learning-Based Parameter Optimization

Accurate identification of the parameters governing the dual-branch extended memristor model requires exploring a high-dimensional and strongly nonlinear design space, where conventional manual tuning is impractical and often insufficient to guarantee reproducibility. To address this, we adopt a three-stage machine-learning (ML) optimization pipeline that combines global sampling, probabilistic surrogate modelling, and local deterministic refinement. The workflow, summarized in Figure 6, enables automated and data-driven calibration of the SPICE-level circuit model against experimentally measured I–V characteristics.

Stage 1: Global Exploration Via Latin Hypercube Sampling (LHS). The optimization begins with LHS, a stratified sampling strategy well-suited for high-dimensional parameter spaces [30]. LHS efficiently populates the admissible domain while avoiding clustering, thereby revealing global trends and highlighting regions that minimize the mismatch between simulated and experimental data. For each sampled parameter vector θ_i, a SPICE transient simulation is executed and compared to the measured I–V curve using the Mean-Squared Error (MSE), which serves as the cost function driving subsequent refinement.

Stage 2: Bayesian Optimization (BO) With Gaussian-Process (GP) Surrogate Models. After initial exploration, a GP

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TABLE 1 | RMSE between experimental and simulated I–V curves for the calibration dataset.

Input excitation	Period T [s]	RMSE [μA]	$\text{RMSE}_{\text{norm}}$
Triangular 3V	1.2 s	3.23×10^{-3}	1.52%
Triangular 3V	12.4 s	9.34×10^{-2}	3.13%
Triangular 4V	175 s	4.11×10^{-1}	8.22%
Sinusoidal 4V	42.8 s	5.44×10^{-1}	10.87%

surrogate model [40] is trained on the LHS results to approximate the mapping $\theta \mapsto \text{MSE}(\theta)$. The GP provides both a prediction of the objective function and an uncertainty estimate, enabling principled exploration–exploitation through an acquisition function. We employ Expected Improvement (EI) [31], which selects new parameter vectors that are likely to improve over the current best performance while still probing regions of high uncertainty. This stage efficiently steers the search toward promising portions of the landscape while significantly reducing the number of expensive SPICE simulations.

Stage 3: Local Refinement Via Gradient-Based Optimization. The most promising candidates identified by BO serve as initialization points for a local deterministic optimizer. We adopt the L-BFGS method [32], which exploits curvature information to converge rapidly to a high-accuracy solution. This final refinement ensures that fine-scale features of the experimental hysteresis loops—such as local curvature, lobe asymmetry, and transition slopes—are faithfully reproduced by the calibrated model.

2.4.1 | Parameter Identifiability

Because the proposed model contains coupled nonlinear voltage- and flux-dependent terms, the RMSE landscape is non-convex, and different parameter combinations may lead to comparable fitting errors. Therefore, the purpose of the optimization pipeline is not to prove uniqueness of each individual coefficient, but to identify a robust low-error region that yields physically meaningful and reproducible I–V characteristics. The three-stage strategy mitigates sensitivity to initialization by combining broad stratified sampling, uncertainty-aware Bayesian exploration, and local deterministic refinement. Parameter identifiability is therefore assessed at the level of the reproduced device response rather than by requiring strict uniqueness of every fitted coefficient. This interpretation is consistent with compact-model calibration, where several correlated parameters may compensate each other while preserving the same experimentally observed hysteresis behavior.

The ML-driven calibration pipeline yields a robust, reproducible, and computationally efficient approach for fitting the proposed model to experimental data, enabling accurate prediction of device dynamics across multiple excitation regimes and frequencies.

2.5 | Model Calibration and Experimental Validation

To quantitatively validate the proposed dual-branch extended memristor model, experimental I–V characteristics were acquired from the multilayer $HfO_x/Al_2O_3/TiO_2$ device. Measurements were carried out under triangular and sinusoidal excitations with amplitudes up to 4 V (Figure 7), while enforcing a compliance current of 5 μA to ensure safe and repeatable SET operation. Higher-voltage or higher-current regimes were not investigated because they fall outside the safe operating window of the devices and may lead to irreversible degradation or permanent failure. The dataset covers input periods ranging from 1 s (1 Hz) to 175 s (67 mHz), thereby probing a wide range of dynamical regimes from fast transitions to quasi-static switching. The model parameters were optimized using the machine-learning-based pipeline. The optimization procedure was performed by using experimental I–V curves as calibration targets. In particular, the voltage waveforms taken in the simulations correspond to the experimental stimuli, while the simulated current was compared point-by-point with the measured current. Thus, the extracted parameters are not arbitrarily selected, but are obtained by fitting the compact-model response to the measured electrical behavior of the fabricated devices. The fitting quality was evaluated through the root-mean-square error (RMSE) between measured and simulated currents. These metrics provide a robust assessment of the local and global agreement between the model and the device. Table 1 summarizes the RMSE values for the calibration dataset. The model accurately reproduces the nonlinear conduction, lobe asymmetry, and hysteresis evolution across all tested waveforms. As expected from the flux-controlled structure, increasing the excitation frequency reduces the hysteresis width and current magnitude, while slower inputs yield wider loops—fully consistent with experimental trends. To assess generalization capability, the optimized parameter set was tested against additional I–V cycles acquired under voltage profiles not used during calibration. These inputs differ in sweep rate and waveform structure (Figure 7), providing an independent evaluation of predictive robustness. The RMSE values reported in Table 2 confirm that the model preserves accuracy under unseen conditions, capturing the frequency dependent narrowing of the hysteresis and the stabilized lobes at lower frequencies.

2.6 | Benchmark-Oriented Comparison

To further position the proposed framework with respect to established compact memristor models, Table 3 compares the dual-branch formulation with VTEAM [8] and the Yakopcic model [20]. These models provide two relevant voltage-driven references, respectively based on voltage-threshold state evolution and behavioral polarity-dependent switching. The comparison emphasizes the main modeling gain of the proposed topology. By assigning the positive and negative responses to separate flux-dependent branches, the model can represent polarity-dependent conduction and strongly different hysteresis-lobe magnitudes without forcing both regimes into a single effective

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TABLE 2 | RMSE between experimental and simulated *I–V* curves for the validation dataset.

Input excitation	Period T [s]	Amplitude [V]	RMSE [% of I_{max}]
Triangular 3V	2.4 s	5.66×10^{-3}	1.41%
Triangular 3V	64 s	2.54×10^{-7}	5.07%
Triangular 3V	130 s	3.36×10^{-7}	6.73%
Sinusoidal 3V	32 s	5.09×10^{-7}	10.19%

state-dependent relation. This capability, demonstrated here for the multilayer Au/HfO_x/Al_2O_3/TiO_2/TiN device, can be extended to other memristive devices where opposite voltage polarities activate distinct conduction or switching mechanisms. It is obtained with a moderate increase in parameter count and transient-simulation cost, while retaining a compact SPICE-compatible structure.

3 | Discussion

The results demonstrate that the dual-branch flux-controlled formulation is not only sufficient to reproduce the measured behavior of multilayer Au/HfO_x/Al_2O_3/TiO_2/TiN devices, but also essential to capturing their underlying physics. This is supported by the direct comparison between experimental I–V characteristics and the calibrated model response, which confirms that the proposed dual-branch formulation can reproduce the experimentally observed asymmetric SET and RESET behavior. By allowing the SET and RESET dynamics to evolve on distinct current–voltage–flux surfaces, the model reveals the intrinsic multi-mechanism nature of oxide resistive switching. This multi-surface structure provides a direct physical explanation for the experimentally observed lobe asymmetry, polarity-selective conduction regimes, and the nonuniform hysteresis scaling with excitation frequency—features that cannot be represented within classical single-state or single-branch compact models.

Importantly, this enhanced descriptive capability is achieved without sacrificing compactness or interpretability. The model maintains a fully analytical and SPICE-compatible structure, enabling its direct use in circuit and array simulations. The flux-controlled framework unifies fast transport and cumulative interface modification within a single state variable, avoiding empirical switching rules and black-box abstractions.

The machine-learning-assisted calibration pipeline further strengthens the practicality of the approach. By combining global and local search strategies, it significantly reduces the time required for parameter identification while yielding robust and physically meaningful parameter sets across diverse waveforms and excitation rates. The consistency of the extracted parameters confirms that the dual-branch formulation captures the fundamental device mechanisms rather than overfitting individual I–V curves. Experimental measurements performed on different devices from the same stack show the same asymmetric hysteretic shape, with device-to-device differences mainly limited to small variations in the peak current value; such dispersion can be incorporated by recalibrating the amplitude-related branch parameters.

Finally, the modularity of the branch-dependent conduction laws makes the proposed framework broadly applicable to other classes of resistive-switching technologies, including valence-change, electrochemical–metallization, and interfacial systems. This generality, combined with computational efficiency, positions the model as a practical compact-modeling tool for neuromorphic circuits, large-scale crossbars, and device-engineering workflows.

4 | Conclusion

We have introduced and experimentally validated a dual-branch, flux-controlled compact model for asymmetric resistive switching in multilayer Au/HfO_x/Al_2O_3/TiO_2/TiN memristive devices. By calibrating the model against measured I–V characteristics, the proposed framework reproduces the experimentally observed lobe asymmetry, polarity-dependent SET/RESET dynamics, history dependence, and frequency-dependent hysteresis evolution. These results demonstrate that separating the device response into two polarity-activated branches provides a physically interpretable and compact description of the multiple transport and interfacial mechanisms governing oxide-based resistive switching. This modeling framework establishes a clear pathway toward a unified and physically consistent description of resistive-switching phenomena in complex oxide stacks.

Looking ahead, integrating relaxation dynamics, long-term defect evolution, and stochastic fluctuations will enable the framework to capture operating regimes that are critical for memory retention [41], learning rules, and endurance under realistic workloads. Embedding these slow and probabilistic processes into the same analytical structure will transform the model from a device-level descriptor into a more precise predictive tool for large-scale neuromorphic and in-memory systems.

Extending the methodology to diverse material platforms will further broaden its relevance, providing a consistent lens through which different switching mechanisms can be compared, optimized, and engineered. By enabling fast, automated exploration of design spaces while maintaining physical interpretability, this framework lays the foundation for the next generation of compact models that can support both technological development and fundamental understanding of emerging resistive-switching hardware.

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TABLE 3 | Benchmark-oriented comparison between VTEAM, the Yakopcic model, and the proposed dual-branch extended memristor model. The VTEAM and Yakopcic entries are based on their original compact-model formulations [8, 20]. The comparison emphasizes structural modeling capability, fitting-parameter count, and relative transient-simulation cost for voltage-driven memristive-device simulations.

Metric	VTEAM model	Yakopcic model	Proposed model
Model class	Voltage-threshold adaptive compact model	Behavioral voltage-controlled compact model	Dual-branch flux-controlled extended memristor
Control and state variables	Voltage v and one bounded internal state w	Voltage V and one bounded internal state $x \in [0,1]$	Voltage v_M and one flux state $\phi = \int v_M dt$
State evolution	Piecewise threshold law for dw/dt, activated by v_{on} and v_{off}	$dx/dt = g(V)f(x)$, with polarity-dependent voltage thresholds and state-window functions	Flux-controlled evolution, $d\phi/dt = v_M$
Current–voltage relation	Not uniquely fixed by the model; linear or exponential $G(w,v)$ relations can be selected	Polarity-dependent hyperbolic-sine law with different amplitudes for positive and negative bias	Separate nonlinear SET and RESET branch currents depending on both v_M and ϕ
Typical fitting-parameter count	~10 model parameters in the standard linear-resistance realization, plus the initial state	11 model parameters plus the initial state x_0	15 fitted parameters
SET/RESET separation	Parametric, through voltage thresholds and switching-rate coefficients	Parametric/behavioral, through polarity-dependent amplitudes, thresholds, and state-window functions	Structural, through two independent polarity-selective branches
Ability to reproduce strongly different lobe magnitudes	Limited by the single-branch formulation; both polarities must be represented by one effective state-dependent law	Moderate; polarity-dependent parameters are included, but the two polarities remain coupled through one effective state variable and one behavioral current law	High; positive and negative lobes are described by separate SET/RESET branch laws
Accuracy-relevant structural feature	Accuracy depends on how effectively the selected single-branch $G(w,v)$ relation can absorb the positive/negative lobe imbalance	Accuracy benefits from polarity-dependent thresholds and amplitudes, but remains constrained by the single effective behavioral branch	Accuracy is favored by the explicit separation of the two polarity-dependent conduction regimes
Relative transient simulation cost	Low; single internal state and compact piecewise dynamics	Low–moderate; single internal state with exponential threshold and window functions	Moderate; additional cost arises from the dual-branch structure and flux-computation circuit
Simulation-speed interpretation	Fast per transient evaluation; absolute runtime depends on solver settings, timestep control, and implementation	Fast to moderate per transient evaluation; absolute runtime depends on solver settings, timestep control, and implementation	SPICE-compatible transient simulation; absolute runtime depends on solver settings, waveform length, and optimization depth
Main advantage	Simple and flexible voltage-threshold formulation	Flexible behavioral fitting of voltage-driven memristive responses	Polarity-selective asymmetric dynamics and flux-dependent hysteresis shaping
Main limitation for the present device	No intrinsic separation of positive and negative conduction paths	No independent SET/RESET conduction branches	Higher parameter complexity than single-branch models

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data supporting the findings of this study are available from the corresponding author upon reasonable request.

References

1. D. Ielmini and H.-S. P. Wong, "In-Memory Computing with Resistive Switching Devices," *Nature Electronics* 1, no. 6 (2018): 333–343.

2. S. Yu, "Neuro-Inspired Computing with Emerging Nonvolatile Memories," *Proceedings of the IEEE* 106, no. 2 (2018): 260–285.

3. X. Zhang, A. Huang, Q. Hu, Z. Xiao, and P. K. Chu, "Neuromorphic Computing with Memristor Crossbar," *Physica Status Solidi A: Applications and Materials Science* 215, no. 13 (2018): 1700875.

4. D. S. Jeong, K. M. Kim, S. Kim, B. J. Choi, and C. S. Hwang, "Memristors for Energy-Efficient New Computing Paradigms," *Advanced Electronic Materials* 2, no. 9 (2016): 1600090.

5. R. Waser, "Redox-Based Resistive Switching Memories," *Journal of Nanoscience and Nanotechnology* 12, no. 10 (2012): 7628–7640.

6. L. Chua, "Memristor—The Missing Circuit Element," *IEEE Transactions on Circuit Theory* 18, no. 5 (1971): 507–519.

7. S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM: Threshold Adaptive Memristor Model," *IEEE Transactions on Circuits and Systems I: Regular Papers* 60, no. 1 (2013): 211–221.

8. S. Kvatinsky, M. Ramadan, E. G. Friedman, and A. Kolodny, "VTEAM: A General Model for Voltage-Controlled Memristors," *IEEE Transactions on Circuits and Systems II: Express Briefs* 62, no. 8 (2015): 786–790.

9. D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The Missing Memristor Found," *Nature* 453, no. 7191 (2008): 80–83.

10. L. Chua, "If It's Pinched It's a Memristor," in *Handbook of Memristor Networks* (Springer, 2019), 15–88.

11. A. Ascoli, S. Slesazeck, H. Mähne, R. Tetzlaff, and T. Mikolajick, "Nonlinear Dynamics of a Locally-Active Memristor," *IEEE Transactions on Circuits and Systems I: Regular Papers* 64, no. 4 (2017): 1165–1174.

12. F. Corinto, M. Gilli, and M. Forti, "Flux-Charge Description of Circuits with Non-Volatile Switching Memristor Devices," *IEEE Transactions on Circuits and Systems II: Express Briefs* 65, no. 5 (2018): 642–646.

13. Y. Yang and W. Lu, "Nanoscale Resistive Switching Devices: Mechanisms and Modeling," *Nanoscale* 5, no. 21 (2013): 10076–10092.

14. D. Ielmini, "Modeling the Universal Set/Reset Characteristics of Bipolar RRAM by Field- and Temperature-Driven Filament Growth," *IEEE Transactions on Electron Devices* 58, no. 12 (2011): 4309–4317.

15. J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive Devices for Computing," *Nature Nanotechnology* 8, no. 1 (2013): 13–24.

16. D. S. Jeong, R. Thomas, R. Katiyar, et al., "Emerging Memories: Resistive Switching Mechanisms and Current Status," *Reports on Progress in Physics* 75, no. 7 (2012): 076502.

17. C. Du, F. Cai, M. A. Zidan, W. Ma, S. H. Lee, and W. D. Lu, "Reservoir Computing Using Dynamic Memristors for Temporal Information Processing," *Nature Communications* 8, no. 1 (2017): 2204.

18. L. Gao, Q. Ren, J. Sun, S.-T. Han, and Y. Zhou, "Memristor Modeling: Challenges in Theories, Simulations, and Device Variability," *Journal of Materials Chemistry C* 9, no. 47 (2021): 16859–16884.

19. M. D. Pickett, D. B. Strukov, J. L. Borghetti, et al., "Switching Dynamics in Titanium Dioxide Memristive Devices," *Journal of Applied Physics* 106, no. 7 (2009): 074508, https://doi.org/10.1063/1.3236506.

20. C. Yakopcic, T. M. Taha, G. Subramanyam, R. E. Pino, and S. Rogers, "A Memristor Device Model," *IEEE Electron Device Letters* 32, no. 10 (2011): 1436–1438.

21. Y. Wang, X. Chen, Y. Shang, et al., "Coexistence Mechanisms of Negative Differential Resistance and Resistive Switching Effects in a WO_x-Based Memristor," *New Journal of Chemistry* 47, no. 31 (2023): 14943–14949.

22. T. D. Dongale, S. S. Sutar, Y. D. Dange, et al., "Machine Learning-Assisted Design Guidelines and Performance Prediction of CMOS-Compatible Metal Oxide-Based Resistive Switching Memory Devices," *Applied Materials Today* 29 (2022): 101650.

23. X. Zheng, L. Wu, Y. Xie, et al., "Lifetime Improvement of 28 nm Resistive Random Access Memory Chip by Machine Learning-Assisted Prediction Model Collaborated with Resurrection Algorithm," *Advanced Electronic Materials* 10, no. 5 (2024): 2300504.

24. B. Spetzler, M. Fritscher, S. Park, N. Kim, C. Wenger, and M. Ziegler, "AI-Driven Model for Optimized Pulse Programming of Memristive Devices," *APL Machine Learning* 3, no. 2 (2025): 026103, https://doi.org/10.1063/5.0251113.

25. D. Ielmini and V. Milo, "Physics-Based Modeling Approaches of Resistive Switching Devices for Memory and In-Memory Computing Applications," *Journal of Computational Electronics* 16, no. 4 (2017): 1121–1143.

26. S. Kim, S. Choi, and W. Lu, "Comprehensive Physical Model of Dynamic Resistive Switching in an Oxide Memristor," *ACS Nano* 8, no. 3 (2014): 2369–2376.

27. S. Menzel, U. Böttger, M. Wimmer, and M. Salinga, "Physics of the Switching Kinetics in Resistive Memories," *Advanced Functional Materials* 25, no. 40 (2015): 6306–6325.

28. A. Ascoli, F. Corinto, and R. Tetzlaff, "A Class of Versatile Circuits, Made Up of Standard Electrical Components, Are Memristors," *International Journal of Circuit Theory and Applications* 44, no. 1 (2016): 127–146.

29. F. Corinto, "Modelling Memristive Devices via Ideal Memristor and Nonlinear Resistors," in *2023 19th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)* (IEEE, 2023), 1–4.

30. M. D. McKay, R. J. Beckman, and W. J. Conover, "A Comparison of Three Methods for Selecting Values of Input Variables in the Analysis of Output from a Computer Code," *Technometrics* 42, no. 1 (2000): 55–61.

31. J. Snoek, H. Larochelle, and R. P. Adams, "Practical Bayesian Optimization of Machine Learning Algorithms," *Advances in Neural Information Processing Systems* 25 (2012): 2951–2959.

32. J. Nocedal and S. J. Wright, *Numerical Optimization* (Springer, 2006).

33. S. Park, S. Klett, T. Ivanov, A. Knauer, J. Doell, and M. Ziegler, "Engineering Method for Tailoring Electrical Characteristics in $TiN/TiO_x/HfO_x/Au$ Bi-Layer Oxide Memristive Devices," *Frontiers in Nanotechnology* 3 (2021): 670762.

34. F. Corinto, M. Forti, L. O. Chua, et al., *Nonlinear Circuits and Systems with Memristors* (Cham, Switzerland: Springer, 2021).

35. S. Park, B. Spetzler, T. Ivanov, and M. Ziegler, "Multilayer Redox-Based $HfO_x/Al_2O_3/TiO_2$ Memristive Structures for Neuromorphic Computing," *Scientific Reports* 12, no. 1 (2022): 18266.

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36. K. Nikiruy, T. Ivanov, M. Ziegler, et al., "Next Generation Memristor Reservoir Computing," in *2024 IEEE International Conference on Metrology for eXtended Reality, Artificial Intelligence and Neural Engineering (MetroXRAINE)* (IEEE, 2024), 912–917.

37. I. Bâldea, "Important Issues Facing Model-Based Approaches to Tunneling Transport in Molecular Junctions," *Physical Chemistry Chemical Physics* 17, no. 31 (2015): 20217–20230.

38. E. W. Lim and R. Ismail, "Conduction Mechanism of Valence Change Resistive Switching Memory: A Survey," *Electronics* 4, no. 3 (2015): 586–613.

39. M. A. Lampert and R. B. Schilling, "Current Injection in Solids: The Regional Approximation Method," in *Semiconductors and Semimetals*, vol. 6 (Elsevier, 1970), 1–96.

40. P. I. Frazier, "A Tutorial on Bayesian Optimization," *arXiv* (2018), arXiv:1807.02811.

41. A. Fadeev and K. Rudenko, "To the Issue of the Memristor's HRS and LRS States Degradation and Data Retention Time," *Russian Microelectronics* 50, no. 5 (2021): 311–325.

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