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Design and test results of a 110 nm monolithic CMOS sensor with internal gain for sub-100 ps time-of-flight detectors

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Summary

New experiments must be conceived to exploit the capabilities of the High-Luminosity upgrade of the Large Hadron Collider at CERN. ALICE 3 is a future experiment designed with this goal in mind. It will be installed during the Long Shutdown 4 (2034 - 2035), with the data taking starting in 2036 (run 5). The experiment target is to fully exploit the heavy-ion physics potential achievable at LHC, bridging the gaps left by the current ALICE experiment.

To reach all its intended goals, ALICE 3 requires a detector capable of identifying particles down to very low transverse momenta: the Time-of-Flight system (TOF). This detector should provide a 20 ps time resolution over a 40 m^2 area, requirements that place it among state-of-the-art systems. Experimental studies demonstrated that such performance can be met using Low-Gain Avalanche Diode sensors (LGAD), silicon devices in which a gain layer is implemented in the pn junction to achieve a controlled charge multiplication. However, the costs and production complexity associated with the hybrid approach (sensor and electronics produced on separate substrates) suggest that LGADs are a suboptimal choice for ALICE 3.

Monolithic CMOS sensors enable better integration, robustness, and assembly, while reducing material budget and costs; therefore, they are an attractive option also due to the low data rate ($< 200\,\mathrm{kHz/cm^2}$) and modest radiation environment expected in ALICE 3. However, although their excellent tracking capabilities have been demonstrated, timing optimization has only recently been explored, and a large-area demonstrator in a commercial process, achieving sub-100 ps MIP time resolution is not yet available. Therefore, the TOF group has started an R&D campaign to reach the 20 ps target by introducing a gain layer into a commercial CMOS process, thereby creating the CMOS LGAD.

This work presents the CMOS LGAD design and the results obtained with a prototype developed to demonstrate the feasibility of gain layer implantation in a standard CMOS CIS process. The work builds upon the sensor technology developed at INFN by the ARCADIA project, which features a fully depleted monolithic sensor. In the last engineering run of ARCADIA (beginning of 2023),

the CMOS LGAD prototype, named MadPIX, was manufactured.

MadPIX (Monolithic CMOS Avalanche Detector) is a pixelated ASIC divided into eight matrices of 64 pixels each. The sensor is based on an n-collection electrode implanted on a 48 μm n-type epitaxial layer grown on a p^+ substrate. Deep p-wells host the electronics and prevent charge collection from the n-weel of the PMOS transistors. A p^+-gain layer is implanted beneath the collection electrodes.

The in-pixel front-end is AC-coupled to the collection electrode, and is based on a trans-impedance amplifier followed by a differential buffer working in the 1.2 V domain. The analog signals are then buffered off-chip with 3.3 V buffers placed in the periphery. The first production demonstrated full substrate depletion and internal charge multiplication. However, the measured gain was three times lower than expected, impacting the time resolution.

A second production (beginning of 2024) followed the characterization campaign, which guided the tuning of the gain-layer implant to better match simulations and measurements. A total time resolution of 72 ± 1 ps was achieved in beam tests, including contributions from electronics jitter and intrinsic sensor resolution. Test beam measurements performed with a tracking telescope showed a detection efficiency of 95 % and a time resolution of 58 ps measured considering only the pixel centre. MadPIX performances was mainly limited by the sensor design due to its thickness ($48\,\mu$m) and sub-optimal pixel size ($250 \times 100\,\mu\text{m}^2$). Monte Carlo simulations matched with experimental measurements stated that the 20 ps target can be achieved by increasing the pixel size and reducing the active thickness to $15\,\mu$m.

The results obtained with MadPIX demonstrate that the CMOS LGAD technology is robust and represents the most promising candidate for the ALICE 3 TOF system. A third production is expected for mid-2026 and will feature thin active sensors ($15\,\mu$m) targeting the 20 ps timing goal.

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A nonna Annita,
simbolo di grinta e perseveranza

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Introduction

The ALICE experiment will end its measurements campaign in 2033 at the end of Run 4 [1]. A new experiment, ALICE 3 [2], is under development, and it is planned to be installed during the long shutdown 4. ALICE 3 represents a next-generation experiment to study heavy-ion physics. Its goal is to address the open questions that emerged from more than a decade of precision measurements with ALICE. ALICE 3 will be capable of exploiting the high-luminosity heavy-ion program of the HL-LHC through an innovative detector concept, based on silicon detectors, featuring ultra-low material budget, continuous readout, and outstanding vertexing and tracking capabilities. Its physics program is centred on the detailed characterisation of QGP properties via rare probes, including heavy-flavour hadrons, low-mass dileptons, and hyper-nuclei, with particular emphasis on measurements at very low transverse momentum over a large acceptance. This experiment aims to provide decisive insights into physics problems such as colour deconfinement, chiral symmetry restoration, and hydrodynamic effects of the quark-gluon plasma.

One of the core detectors of ALICE 3 is the Time-of-Flight system, which is needed for the identification of particles down to very low momenta over a wide acceptance. This system requires a time resolution below 20 ps, a hit rate below 200 kHz/cm^2 and a granularity of 1×1 mm^2 over a surface of ≈ 40 m^2. These specifications, along with a modest radiation environment ($< 10^{13}$ MeVn$_{\mathrm{eq}}$/cm^2), allow for a possible monolithic solution in which sensor and electronics are implemented in the same silicon substrate. However, there are currently no monolithic systems capable of achieving resolutions below 20 ps over an m^2 area. The most developed and used silicon sensors in high-energy physics for systems requiring outstanding timing resolution are Low-Gain Avalanche Diodes (LGADs), capable of achieving sub-50 ps performance [3, 4, 5]. LGADs provide controlled charge multiplication through a gain layer, permitting a power reduction in the front-end electronics when timing below ns is required. The main drawbacks of standard LGAD are the need for bump or wire bonding between the sensor and readout ASIC. This coupling introduces additional material budget, production complexity, cost, and yield losses, especially for large-area detectors, such as the ALICE 3 time-of-flight

system. Instead, monolithic sensors eliminate the need for bump bonding, significantly reducing material, power consumption, and production complexity [6, 7].

Different groups have been trying to create sub-100 ps monolithic devices with or without the introduction of a gain layer implemented in the sensor active area [8, 9, 10, 11]. Also, the ALICE 3 time-of-flight group has started an R&D campaign to design a monolithic CMOS sensor with an internal gain layer: the CMOS LGAD. This R&D is based on the ARCADIA technology platform, which features a fully depleted Monolithic Active Pixel Sensor (MAPS) in the 110 nm node of LFoundry. The main advantage of the ARCADIA tecnhnology is the fast charge collection required for radiation sensors with sub-100 ps time resolution; however, due to the limited signal-to-noise ratio, the 20 ps goal is not achievable. Hence, the ALICE 3 time-of-flight group, during its R&D program, introduced in the ARCADIA platform a gain layer beneath the collection electrode to multiply the deposited charge.

This work describes the development of the CMOS LGAD prototype. Chapter 1 presents the physics motivations and the detector layout of the ALICE 3 experiment. The state-of-the-art monolithic CMOS sensors with and without a gain layer that have been developed for sub-100 ps time resolution are presented in Chapter 2 alongside the ARCADIA technology with and without a gain layer. Then, the Monte Carlo simulations used to predict the CMOS LGAD sensor timing performance are reported in Chapter 3, while Chapter 4, focuses on the electronics design and simulations. Finally, Chapter 5 summarises the laboratory results of MadPIX and its time resolution measured during CERN and DESY test beams. In-pixel studies and efficiency are also reported in this chapter.

Chapter 1

From physics motivations to detector layout: the ALICE 3 experiment

Over the past decades, High-Energy Physics (HEP) has progressed through advances in accelerator technology and the evolution of particle detectors. The High-Luminosity Large Hadron Collider (HL-LHC) upgrade represents both a culmination of the current accelerator technologies and a stepping stone toward future collider concepts such as the Future Circular Collider (FCC).

As for particle detectors, silicon is gradually becoming the basis of every experiment under construction. The new technologies enable precise tracking and timing in environments dominated by high particle multiplicities. Continuous improvements in sensor granularity, readout speed, radiation tolerance, and material budget have made all-silicon detector concepts not only feasible but essential for next-generation experiments.

The ALICE 3 experiment is conceived as a compact, ultra-light, and high-precision detector, centred on an all-silicon layout optimised for vertex resolution, low material budget, and extended acceptance. Its design is closely tied to a physics program that exploits the HL-LHC heavy-ion program.

In this chapter, the physics motivations which led to the design of the ALICE 3 experiment are presented (Sec. 1.1). Section 1.2 provides an overview of ALICE 3 subsystems apart from the Time-of-Flight detector, which is described in detail in Sec. 1.3.

1.1 Physics motivations

Understanding the behaviour of strongly interacting matter under extreme conditions is one of the central objectives of nuclear and sub-nuclear physics. At sufficiently high temperatures and energy densities, hadronic matter undergoes a transition into a deconfined phase composed of quarks and gluons: the Quark Gluon Plasma (QGP). Experimental studies of QGP provide a unique opportunity to investigate the properties of Quantum Chromodynamics (QCD), including confinement, chiral symmetry breaking, and transport phenomena [12]. The ALICE 3 experiment is conceived as a next-generation heavy-ion detector optimised to address limitations of the existing ALICE experiment. Its design prioritises low-momentum sensitivity, large pseudorapidity coverage, and precise vertexing. In this context, ALICE 3 [2] is not an ALICE [1] upgrade but a completely new experiment.
In the next paragraphs, the physics motivations will be summarised.

Heavy Quarks as Probes of the QGP Heavy quarks production, in particular for charm and beauty, is well described by perturbative QCD. Their large masses ensure that they are produced in initial hard scattering processes, occurring on timescales much shorter than the formation time of the QGP. As a consequence, heavy quarks propagate through the entire evolution of the medium, from its earliest stages to hadronisation, retaining memory of their interactions with the surrounding QGP [13].

The dynamics of these heavy quarks is governed by their interactions with the medium constituents (quarks and gluons), i.e. through elastic or inelastic scattering. In the first condition, the charm or bottom quarks are subjected to a Brownian motion [14]. Instead, the inelastic scattering is dominated by gluon radiation [15]. These processes encode fundamental information about the transport properties of the QGP and its coupling strength.

While existing measurements have constrained heavy-quark transport parameters to a certain extent, significant uncertainties persist at low transverse momentum, where heavy quarks are most sensitive to the late stages of the QGP evolution.

ALICE 3 will be capable of selecting B-mesons and Λ_c baryon with a higher purity compared to ALICE, allowing for a high-accuracy measure of production and expansion of particles containing the beauty quark down to $p_T = 0$.

Azimuthal Decorrelation Measurements While inclusive spectra provide valuable baseline information, a detailed understanding of in-medium dynamics

requires more differential observables. Correlation measurements involving heavy-flavour hadrons, jets, and electromagnetic probes offer direct sensitivity to the microscopic mechanisms of energy loss and momentum diffusion. For example, azimuthal correlations between charm/anti-charm hadron pairs probe the degree to which the initial back-to-back kinematics is modified. Such correlations are expected to be significantly broadened in the limit of strong coupling and long interaction times, reflecting partial or full thermalisation [16].

ALICE 3 will require a high readout rate, precision tracking and pointing resolution to reduce the combinatorial background for correlation studies.

Quarkonium Production and Dissociation Quarkonium states provide complementary information on QGP properties.

Colour screening in a deconfined medium weakens the binding potential between heavy quarks, potentially leading to the dissociation of bound states [17]. The production suppression of charmonium and bottomonium in heavy-ion collisions compared to pp is interpreted as evidence of QGP existence [18]. At the same time, high heavy-quark multiplicities at LHC energies enable regeneration processes during the later stages of the collision, decreasing the total suppression compared to other experiments [19].

The simultaneous measurement of ground and excited quarkonium states is essential for disentangling these two effects. ALICE 3 will reconstruct such states down to zero transverse momentum, enabling precise studies of their production patterns.

Electromagnetic radiation Electromagnetic radiation, in the form of photons and dileptons, constitutes one of the most interesting probes of the QGP. Since these components interact only electromagnetically, they carry information from all collision stages, including the earliest and hottest QGP phases (pre-hydrodynamic phase) [20]. The momentum spectrum slope of photons allows for a measurement of the temperature and expansion velocity. Instead, the dilepton mass spectrum depends only on the temperature. By comparing these two behaviours, the temperature and the radial flow can be extracted [21].

ALICE 3 will improve the performance of the ALICE experiment thanks to the higher statistics, larger acceptance and tracking capabilities of photon conversion products. In addition, to reduce the background, a very thin and light tracker with outstanding low-p_T reconstruction will be used. It will reduce the photon conversions in the beam pipe and in the first two tracking layers.

Chiral Symmetry Chiral symmetry, which arises in the QCD Lagrangian for the massless limit, is proven to be broken by analysing the hadrons mass spectrum

[22]. However, it is expected to be restored at high temperatures in the deconfined phase. Electromagnetic probes such as photons and dileptons provide direct access to the in-medium spectral functions of vector mesons, which are sensitive to this restoration [23].

ALICE 3 will precisely measure the dilepton invariant-mass spectra, which allow the study of the ρ meson and its chiral partner modifications through medium-induced broadening and mixing effects caused by chiral symmetry restoration.

Electrical conductivity The electrical conductivity of QGP is predicted by different theoretical models: lattice QCD [24], perturbative QCD [25], and AdS/CFT correspondence [26]. However, experimental data place no constraints on its value due to the high background from dielectrons and photons produced in the pions, hadrons and neutral mesons decays [27].

ALICE 3 will be able to identify and suppress this background using a selection on the mass and transverse momentum. The low momentum electrons will be measured and identified using the inner TOF system, while the photon will be detected with the electromagnetic calorimeter and forward conversion tracker.

Collective effects In the ALICE experiment, collective effects are studied in high multiplicity pp and p-Pb collisions [28]. During these collisions, the system should behave as a small collision system. Enhancements in the production of multi-strange baryons and flow-like correlations are two examples observed in pp collisions, which imply that the system exhibits a collective behaviour and it is thermalising [29].

ALICE 3 will be able to separate proper high-multiplicity events from single high-multiplicity jets, removing the bias present in ALICE data.

Hadronic physics Hadronisation is often described using fragmentation-based approaches that neglect medium effects [30]. By contrast, the high parton densities achieved in heavy-ion collisions undergo alternative mechanisms as quark recombination [31]. Recombination models naturally account for the observed enhancement of baryon-to-meson ratios at low transverse momentum. Extending these studies to the heavy-flavour sector allows for the investigation of whether charm quarks participate in collective hadron formation and to what extent they approach local thermal equilibrium. Additionally, the high heavy-quark densities achievable in nuclear collisions enhance the discovery potential for previously unobserved exotic states, including those containing multiple heavy quarks (tetraquark). Such measurements would represent a significant advance in the understanding of hadron spectroscopy and strong-interaction dynamics.

ALICE 3 will study different measurements in the multi-charm sector thanks to the large p_T interval and to the innovative design of the vertex detector, which will track hyperons before their decay. In addition, ALICE 3 will study light-, hyper-, super-, and anti-nuclei formation, which are extremely rare processes that will be measurable thanks to the HL-LHC increased interaction rate.

Physics Beyond the Standard Model Photon-mediated processes in ultra-peripheral collisions provide sensitivity to physics beyond the Standard Model.

In ALICE 3 heavy-ion collisions, it will be possible to study light-by-light scattering processes, axion-like particle searches and $\tau\, g-2$ measurement down to low transverse momenta [32]. ALICE 3 will be able to investigate the axion particle mass in the range from 50 to 5000 $\mathrm{MeV/c^2}$, while other experiments such as ATLAS [33] and CMS [34] cannot go below 1 $\mathrm{GeV/c^2}$.

1.2 Experiment layout

From the physics studies presented in the previous section, the most important specifications of the ALICE 3 are summarised:

- Large pseudorapidity range: $-4 < \eta < 4$
- Precise pointing resolution
- Particles identification system capable of discerning particles over a large p_T range

Different experiment layouts are proposed to satisfy multiple budget ranges. In this section, the complete ALICE 3 layout (*v1*) is presented and its 3D model is shown in Fig. 1.1, while the section is reported in Fig. 1.2. This configuration will achieve all the physics goals presented in the previous section.

Two other versions are under study to lower the total costs: *v2* and *v3*. In *v2*, the electromagnetic calorimeter is removed, while in *v3* the acceptance is also reduced to $|\eta < 2|$. In addition, for *v2*, two different magnetic fields (2 T and 1 T) are under consideration, and simulations are ongoing to predict the impact on physics performance [35].
The ALICE 3 *v1* subsystems are:

- Superconducting Magnet
- Inner Tracker
- Outer Tracker

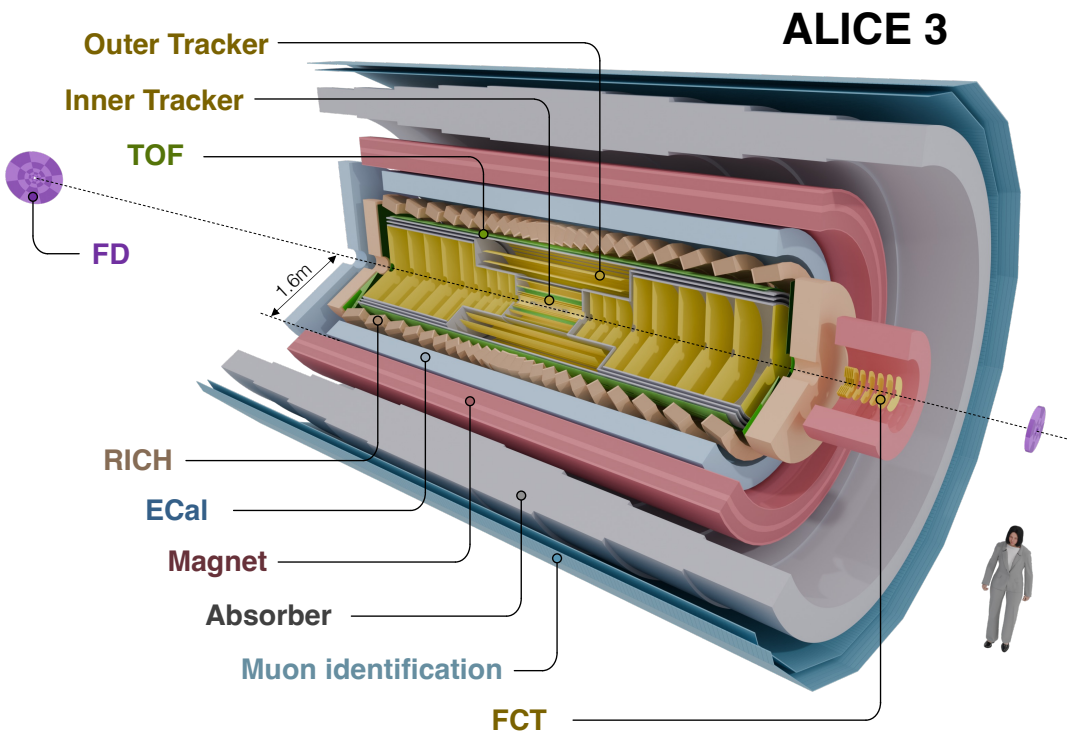


Figure 1.1: 3D model of the ALICE 3 experiment. Image taken from [35].

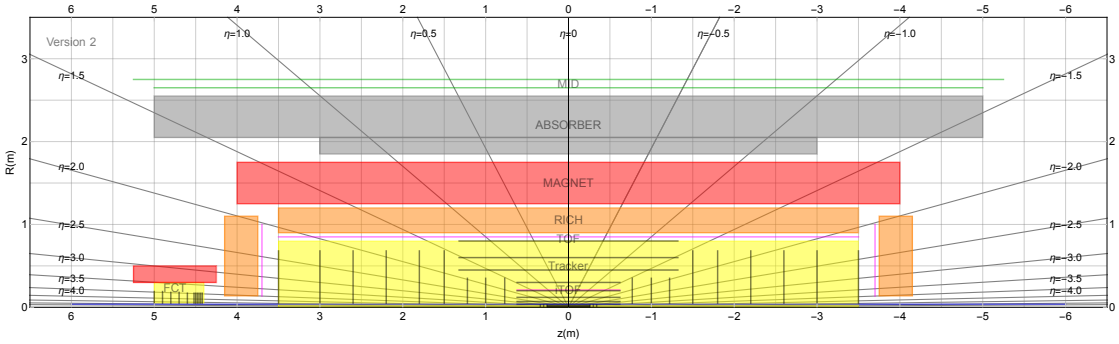


Figure 1.2: ALICE 3 top section. The z axis corresponds to the beam path. Image taken from [35].

- Time-of-Flight Detector
- Ring-Imaging Cherenkov Detector
- Electromagnetic Calorimeter
- Muon Identifier Detector
- Forward Conversion Tracker
- Forward Detector

In the next paragraphs, all systems will be presented except for the Time-of-Flight, which will be discussed in Sec. 1.3.

Superconducting Magnet In HEP experiments, a magnet is needed to bend the particles generated in the collisions to reconstruct their transverse momenta. The reference design for the ALICE 3 superconducting magnet (*v1* and *v2*) consists of a solenoidal coil of approximately 7.5 m radius, capable of providing a central magnetic field between 1 and 2 T.

The superconductive cable material has not yet been decided. The magnet architecture is based on a cold mass comprising a two-layer superconducting coil wound on a support cylinder and cooled by liquid helium. Thermal uniformity is ensured through the use of high-conductivity aluminium thermal paths, while quench protection strategies such as redundant voltage taps are employed to avoid disruptive breakdown. The three superconductors considered for the coils are: Nb-Ti/Cu with aluminium cladding, Nb-Ti/Cu with copper stabiliser or MgB_2 with copper stabiliser. The final material choice will be based on cost, feasibility and availability.
In the *v3* layout, the magnet length is reduced to 5.5 m to reduce the costs.

Inner Tracker The inner tracker is composed of two parts: the vertex detector and the middle layers. The first one is divided into three concentric cylinders placed inside the beam pipe. They will be 50 cm long placed at 0.5, 1.2 and 2.5 cm from the LHC beam. To provide the $|\eta| < 4$ coverage, three disks are placed inside the beam pipe as well, at 26, 30 and 34 cm from the interaction point with a radius going from 0.5 to 2.5 cm (Fig. 1.3).
Their positions represent an engineering challenge from a mechanical perspective, being placed inside the beam pipe. A four-petal structure enclosed in the secondary vacuum will allow for a layer retraction to 15 mm from the beam during LHC injection. The vertex detector will allow a track pointing resolution better than 10 μm for $p_T > 250$MeV/c [36].

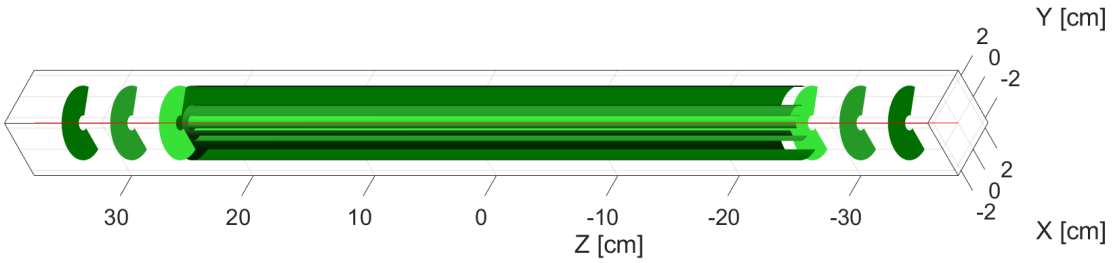


Figure 1.3: 3D model of the vertex detector in green. The beam is plotted in red.

The middle layer is designed with three disks and four barrel layers positioned outside the beam pipe. The layers are 124 cm long and will be installed at 3.75, 7, 12, 20 cm from the beam. The three disks have a radius between 5 and 35 cm and they will be placed at 77, 100 and 122 cm from the interaction point to cover the required pseudorapidity range. The middle layers are needed for the p_T measure, which can be extracted from the trajectory bending. These layers provide the particle trajectory reconstruction using the impinging points on each layer.

The inner tracker structure is depicted in Fig. 1.4, while table 1.1 summarises the performance of the inner tracker.

The inner tracker will be composed of CMOS Monolithic Active Pixel Sensors (MAPS) produced in Tower Partners Semiconductor Co. Ltd. (TPSCo) 65-nm

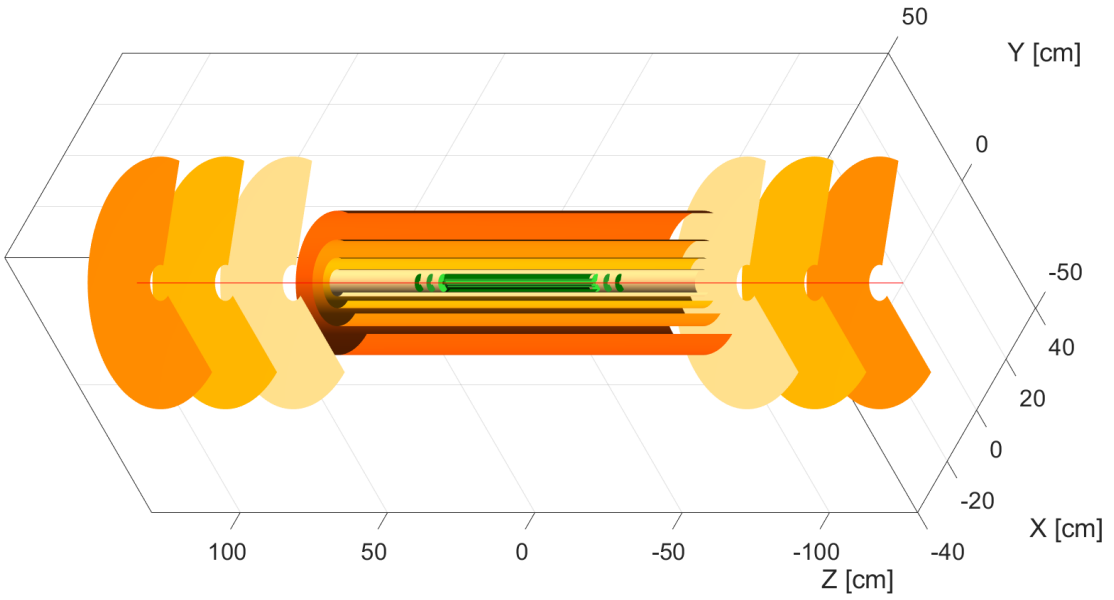


Figure 1.4: 3D model of the inner tracker composed of the vertex detector in green and middle layers in orange. The beam is plotted in red.

Table 1.1: Key requirements for the inner tracker.

Type	**Vertex detector**	**Middle layers**
Material budget	$0.1\%X_0$	$1\%X_0$
Spatial resolution	$2.5\,\mu$m	$10\,\mu$m
Time resolution	100 ns	100 ns
Power consumption	$70\,\mathrm{mW/cm^2}$	$20\,\mathrm{mW/cm^2}$
Total radiation dose	$10^{16}\,\mathrm{MeV\,n_{eq}/cm^2}$	$2\times10^{14}\,\mathrm{MeV\,n_{eq}/cm^2}$
Rate capability	$95\,\mathrm{MHz/cm^2}$	$1.3\,\mathrm{MHz/cm^2}$

CMOS imaging process. The ongoing R&D is the continuation of the ALICE ITS3 upgrade [37].

In the *v3* layout, the three innermost disks are removed, and the remaining ones are shrunk in radius.

Outer Tracker The Outer Tracker (OT) is positioned outside the beam pipe and provides coverage over the same pseudorapidity range of the inner tracker ($|\eta| < 4$). Its goal is to add trajectory points to the middle layers. It is composed of four cylindrical barrel layers and six forward disks on each interaction point sides. The total sensitive area is approximately $50\,\mathrm{m^2}$, implying the installation of a large number of silicon sensors (around 2000 wafers, considering yield and pre-production). The detector is composed of CMOS Monolithic Active Pixel Sensors (MAPS) implemented in the 65 nm CMOS imaging process used for the future ALICE ITS3 upgrade [37]. An intrinsic spatial resolution of $10\,\mu$m with a material thickness of $1\%X_0$ is sufficient for the physics goals. Sensors are then assembled into modules in a two-by-four matrix.

The mechanical integration of the OT is based on lightweight carbon-fibre support structures designed as longitudinal staves in the barrel and planar disks in the end caps. Cooling is achieved via cold plates with high thermal conductivity derived from the ITS2 and MFT detectors [38]. A staggered layout with controlled overlaps between sensors and modules is employed to compensate for inactive periphery regions and ensure 100 % coverage. The R&D programme is now focusing on the CMOS sensor optimisation to achieve the required timing resolution (≈ 25 ns) and low power consumption ($30 - 50\,\mathrm{mW/cm^2}$).

The outer tracker structure is displayed in Fig. 1.5.

In *v3* layout, the three outermost disks are removed, and the remaining ones are decreased in radius to achieve a coverage up to $|\eta| = 2.5$.

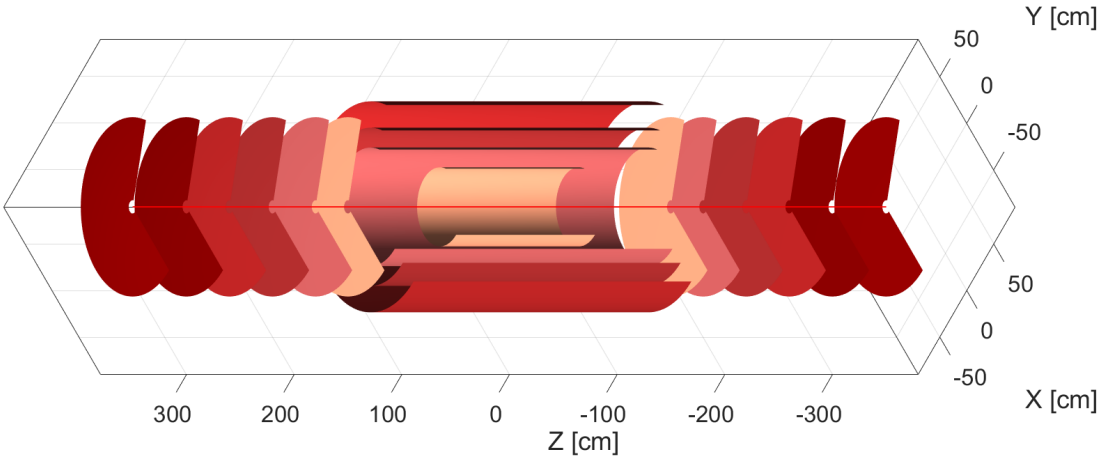


Figure 1.5: 3D model of the outer tracker. The beam is the red line.

RICH detector The Ring-Imaging Cherenkov (RICH) detector is responsible for Particle Identification at high p_T, where the Time-of-Flight detector loses its separation power. It is composed of two complementary subsystems: a barrel RICH (bRICH) surrounding the outer TOF barrel and a forward RICH (fRICH) covering the forward and backward rapidity regions. The bRICH is 7 m long with a radius in the $0.9 \div 1.2$ m range, while the fRICH end-caps extend the acceptance to cover the full pseudorapidity range ($|\eta| < 4$). Both detectors employ silica aerogel tiles as Cherenkov radiators.

With the photon detection plane positioned approximately 20 cm downstream of the radiator, the RICH enables the extension of electron/pion separation from 500 MeV/c to about 2 GeV/c and provides proton/kaon separation to 10 GeV/c. In addition, to optimise particle identification performance while limiting the overall detector surface, a modular projective cylindrical geometry is adopted, resulting in a total photosensitive area of $\approx 28\,\mathrm{m}^2$ and an aerogel coverage of $22\,\mathrm{m}^2$. The fRICH adds $\approx 9\,\mathrm{m}^2$ to the total area.

Cherenkov radiation generated inside the aerogel is detected using silicon photomultipliers (SiPMs) due to their high photon detection efficiency, insensitivity to magnetic fields, compactness, and excellent timing performance. The proposed detection plane consists of SiPM arrays integrated with front-end electronics through a PCB or silicon interposer, forming a modular unit of approximately $20 \times 20\,\mathrm{cm}^2$, with an optimised SiPM pixel size of about $2 \times 2\,\mathrm{mm}^2$. The R&D programme is concentrating on both the radiator and the SiPMs to optimise the aerogel refractive index and transparency reproducibility, and the SiPMs tolerance to radiation [39].
The fRICH is not present in the *v3* layout.

Electromagnetic Calorimeter The electromagnetic calorimeter is designed for energy measurements of photons, and it is composed of a barrel detector and an end-cap system. The barrel is installed inside the solenoidal magnet within a cylindrical volume with a spanning radius between approximately 1.25 and 1.55 m. The barrel is subdivided into two regions: a central section based on high-resolution lead tungstate crystals ($PbWO_4$), and an outer section employing Pb-scintillators as in the end-cap system. Both barrel regions are segmented azimuthally into four sectors, providing approximately 93 % coverage of the full azimuthal angle. All calorimeter cells are designed with a projective geometry, with transverse cell dimensions increasing from the central barrel to the end-cap.

The scintillation light generated inside the crystals is detected using silicon photomultipliers, with a geometry optimised for the required dynamic range and energy resolution. For the central part, a hybrid configuration with SiPMs with different pixel pitches is under study to have a dual-gain photodetector readout. Commercially available Hamamatsu Multi-Pixel Photon Counters are considered the baseline devices.

Due to the temperature dependence of the $PbWO_4$ light yield, the central barrel requires operation at approximately $-25\,^{\circ}\mathrm{C}$ with temperature stability at the level of $0.1\,^{\circ}\mathrm{C}$, imposing constraints on the cooling system design. The sampling calorimeter cells are realised as multilayer stacks of lead absorber and plastic scintillator, with wavelength-shifting fibres used to collect and transport the scintillation light to the SiPMs. The front-end electronics digitise both amplitude and timing information for groups of channels.

The R&D programme focuses on the optimisation and qualification of SiPM-based photodetectors for the expected photon fluxes and dynamic range, as well as the development of dedicated front-end electronics.
This detector is eliminated from the *v2* and *v3* layouts.

Muon Identifier Detector The Muon Identifier Detector (MID) is designed to provide efficient muon tagging for reconstructed tracks, and it is installed outside the superconducting solenoid. It consists of a steel absorber followed by muon detection layers. The absorber thickness decreases from 70 cm in the central region to roughly 38 cm at larger acceptance.

Downstream of the absorber, the muon detection system employs scintillator bars read out by wavelength-shifting fibres coupled to silicon photomultipliers. Two orthogonal layers of scintillator bars are foreseen to provide two-dimensional position measurements, with bar dimensions optimised for efficiency, timing, and cost. Test-beam measurements and cosmic-ray studies have demonstrated that low-cost extruded plastic scintillators achieve $\simeq 100\%$ detection efficiency along metre-scale lengths (FNAL-NICADD [40]), with time resolutions around 2 ns [41].

Although the detector technologies under consideration are mature, a dedicated R&D programme is required to ensure the best matching with the specific requirements of ALICE 3 [42]. These include an integration time compatible with the 100 ns time window of the silicon tracker, sufficient radiation tolerance to withstand the expected non-ionising and ionising dose over the ALICE 3 lifetime, and the ability to maintain a hadron rejection ratio close to 1/100. Furthermore, high and uniform detection efficiency over the full acceptance is essential.

Forward Conversion Tracker The forward conversion tracker is foreseen to extend the photon measurement capabilities of ALICE 3 into the forward region. This system is conceived as an array of eleven silicon tracking disks located at longitudinal positions between approximately 4.4 and 5.0 m from the interaction point, providing coverage in the pseudorapidity range $4 < \eta < 5$ (only on one side of the experiment). Before tracking, the photons are converted through a thin foil placed upstream of the first tracking layer or, as an alternative option, directly within the first tracking layer itself.

The detector operates inside a magnetic field of about 0.25 T oriented transversally to the beam axis. To optimise track reconstruction, the first six layers are closely spaced, while larger separations are adopted for the outer layers. The tracking planes employ the same silicon pixel technology as the inner tracker middle layers. Approximately $1\,\mathrm{m}^2$ of silicon sensors is required. Alternative geometries are under consideration, including rectangular sensor planes positioned above the beam pipe.

Forward Detectors The forward detector is designed to provide fast interaction triggering, luminosity monitoring, preliminary vertex determination, forward multiplicity counting, and precise collision time stamping for the time-of-flight particle identification system. The forward detectors also contribute to the collision centrality measurement and to the selection of ultra-peripheral events.

Two alternative layouts are under consideration for the forward region, covering either $5 < \eta < 7$ or $4 < \eta < 7$, while a dedicated detector on the opposite side of the interaction point covers the backward interval, $-7 < \eta < -4$. The design is based on the proven FIT FV0 concept [38] and consists of segmented scintillator disks located at large longitudinal distances from the interaction point. The light will be collected via optical fibres coupled to photomultiplier tubes. The granularity is chosen to provide uniform acceptance, and a time resolution of approximately 200 ps across the full detector surface.

The R&D programme focuses on the development of fast and radiation-tolerant readout electronics and detector components. The front-end electronics must support event recording at 25 ns intervals and is derived from the existing FIT FT0

system. A partial transition from analogue to digital processing is foreseen to extend the dynamic range for online pile-up and background rejection.

1.3 The ALICE 3 time-of-flight detector

Together with the RICH and vertex detector, the Time-of-Flight system is one of the ALICE 3 key detectors for which a committed and extensive R&D is required.

The TOF is needed for particle identification at very low momenta down to $15-60\,\mathrm{MeV/c}$ depending on the intensity of the magnetic field (1 or 2 T) [43]. This system is composed of three parts: Inner TOF (iTOF), Outer TOF (oTOF) and Forward TOF (fTOF). iTOF and oTOF are two barrel layers placed at a distance of 19 and 85 cm from the beam. The iTOF is placed between the inner and outer trackers, while the oTOF and fTOF are installed outside the outer tracker, in front of the RICH. The iTOF and oTOF are respectively 104 and 700 cm long, while the fTOF is placed at ± 370 cm from the interaction point, and it is composed of disks with a radius going from 15 to 100 cm.

In table 1.2, the coverage and total area of the three TOF components are summarised, while its structure is displayed in Fig. 1.6. The TOF position compared to the inner and outer trackers is shown in Fig. 1.7.

The fTOF, which is needed to measure the collision time, the time zero for single particle time stamp, and to identify particles with acceptance $2 < |\eta| < 4$, is not present in the ALICE 3 *v3* layout.

Table 1.2: Area and acceptance of iTOF, oTOF and fTOF.

	iTOF	**oTOF**	**fTOF**
Total area [m^2]	1.5	36	6
Acceptance	$\eta < 1.9$	$\eta < 2$	$2 < \eta < 4$

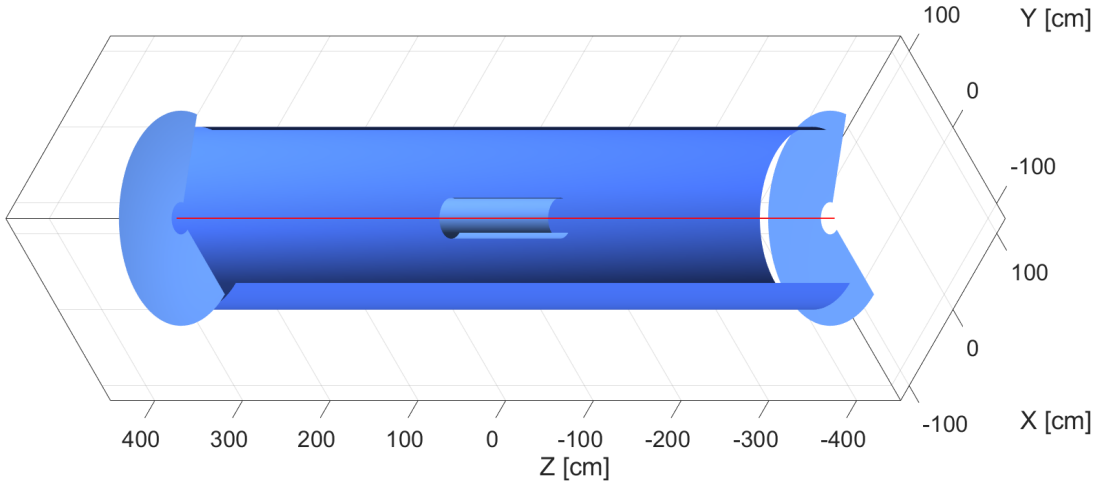


Figure 1.6: 3D model of the time-of-flight detector. The beam is plotted in red.

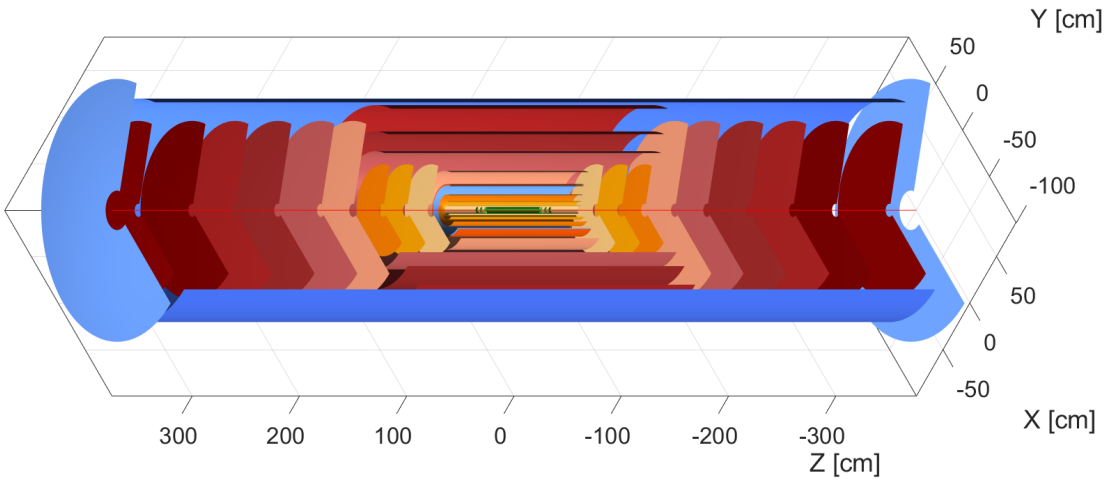


Figure 1.7: 3D model of the time-of-flight detector in blue, outer tracker in red, middle layer in orange and vertex detector in green. The beam is plotted in red.

Using MC simulations of the detector, the performance required to address all the physics goals can be extracted and summarised in table 1.3. The hit rate is selected as the maximum hit rate extracted from MC physics simulations using pp collisions at 14 TeV, Pb-Pb collisions at 5.52 TeV, and Pb-Pb events selected by centrality 0-5%. The highest rate is achieved in fTOF for the most central Pb-Pb collisions, where a high number of particles is produced.

From table 1.3, the most stringent and difficult requirement is the time resolution below 20 ps. This specification, σ_t, represents the timing accuracy with which the passage of a particle through a detector can be measured. Many aspects contribute to its increase, but it can mainly be broken down into six factors [44, 45]:

$$\sigma_t = \sqrt{\sigma_{LN}^2 + \sigma_D^2 + \sigma_J^2 + \sigma_{TW}^2 + \sigma_{TDC}^2 + \sigma_{CDN}^2} \tag{1.1}$$

Each term of Eq. 1.1 must be minimised and monitored to achieve the 20 ps goal. A brief description of each component is provided:

- *Landau Noise*, σ_{LN}. The Most Probable Value of the total number of deposited charges in a set thickness of material can be predicted by the Landau theory. Nevertheless, stochastic fluctuations generate non-uniform deposition and hence identical particles crossing the material induce different signals in the collection electrode. This contribution is intrinsic to the sensor and cannot be removed, but it can be lowered by reducing the material thickness crossed by the particle. This term can be precisely predicted using Monte Carlo software such as *Garfield++* or *Allpix*^{2}.

- *Distortion*, σ_D. The finite pixel pitch produces electric field variations at sensor edges. This non-uniformity generates position-dependent delays in the signals induction, worsening the total time resolution. The non-saturation of carrier velocity is also included in this contribution. The distortion term can be reduced by increasing the pixel size. Its behaviour depends on the ratio

Table 1.3: Area and acceptance of iTOF, oTOF and fTOF.

	iTOF	**oTOF**	**fTOF**
Granularity [mm^2]	1×1	5×5	1×1 to 5×5
Hit rate [kHz/cm^2]	130	8	250
Material budget	1 to 3 % X_0		
Power density	200 mW/cm^2		
Time resolution	20 ps		
Total Radiation Dose	$< 10^{13}$ MeVn$_{\text{eq}}$/cm^2		

between pixel pitch and device thickness, and it can be predicted using Monte Carlo software such as *Garfield++* or *Allpix*^{2} combined with Technology Computer-Aided Design (TCAD) tools (*Sentaurus* or *Comsol*).

- *Jitter*, σ_J. The Jitter term is defined as:

$$\sigma_J = \frac{\sigma_V}{{}^{dV}/_{dt}} \tag{1.2}$$

where σ_V is the electronics noise and ${}^{dV}/_{dt}$ is the slew rate. To minimise this term, the signal must be as large as possible with the shortest rise time (given a fixed noise).

- *Time Walk*, σ_{TW}. Signals with different amplitudes cross a fixed threshold at different times, introducing an amplitude-dependent effect. This term can be decreased via hardware, using specific electronics architectures (constant fraction discriminators or double threshold discriminators), or software, compensating for a correlated quantity such as the time for which the signal is above a threshold or the maximum amplitude. This term could be completely removed if the signal rise time is constant during the acquisition.

- *Time to Digital Converter (TDC)*, σ_{TDC}. TDCs are electronics blocks that convert a discriminated signal into a digital word. This term can be negligible because converters with a time resolution in the picosecond range, sampling rate on the order of a few hundreds of picoseconds, and low power consumption are already well established [46, 47, 48].

- *Clock Distribution Network (CDN)*, σ_{CDN}. The delivery of the clock signal to the full chip affects the time resolution. The routing layout is essential to avoid line delays and high skew. High-performance clock management systems have shown continuous improvements in recent years, and CDN with a resolution below 20 ps are achievable [4, 46, 49].

As reported in the previous list, the Landau and distortion factors depend on the sensor itself. From preliminary MC simulations ≈ 16 ps can be achieved for an active thickness of 15 μm. To stick to the budget of 20 ps, all other terms can be derived. Table 1.4 reports the budget that can be allocated to each term. The time resolution of the TDC is assigned considering a Least Significant Bit (LSB) of 10 ps.

Currently, there are no detectors or sensors capable of achieving 20 ps over a m^2 area. The most developed and used silicon sensors in HEP for timing applications, which can be considered as TOF candidates, are Low Gain Avalanche Diodes

Table 1.4: Timing budget allocated to each term contributing to the total system time resolution.

Term	**Resolution** [ps]
$\sqrt{\sigma_{LN}^2 + \sigma_D^2}$	16
σ_J	10
σ_{TW}	3
σ_{TDC}	3
σ_{CDN}	5
σ_t	20

(LGADs) or Silicon PhotoMultipliers (SiPMs). SiPMs are mainly used for photon detection [50], while LGADs are employed for charged particles.

Experiments such as CMS [4] and ATLAS [51], will use LGAD sensors for their timing systems in the next upgrade, requiring a time resolution of 50 ps at the end of their lives. Measurements on sensor and electronics showed that this performance could be achieved [52, 53, 54, 5].

For the ALICE 3 TOF system, extensive characterisation campaigns on SiPM and LGAD were carried out to understand if these two technologies can satisfy the 20 ps requirement.

SiPMs are conventionally regarded as sensors insensitive to charged particles in the sense that ionising radiation generates a negligible signal compared to the one generated by photons. Nevertheless, they are capable of directly detecting relativistic charged particles due to the resin applied on their surface. If the particle velocity is high enough to generate Cherenkov radiation, multiple SPAD cells of the SiPM can fire, and hence a signal compatible with the one generated by photons is produced [55]. Time resolution study in beam tests demonstrated that the 20 ps limit can be achieved with 4 OverVoltage defined as the difference between bias and breakdown voltages [56, 57]. However, SiPMs are considered a fallback solution due to their high sensitivity to radiation [58, 59]. The expected cumulative dose of ALICE 3 does not allow a proper use of these sensors due to the very high dark count rate, which increases with the total absorbed ionising dose.

In parallel to the SiPM study, different beam tests were conducted to characterise the performance of ultra-thin LGAD sensors developed by FBK. The measurements focused on devices with active thicknesses down to 15 μm, including sensors of 20, 25 and 35 μm. The active area spanned from $1 \times 1\,\mathrm{mm}^2$ (25 and 35 μm), to $1.3 \times 1.3\,\mathrm{mm}^2$ (15 and 20 μm). Standard 50 μm-thick LGAD sensors manufactured by Hamamatsu Photonics were also considered. The devices were

mounted on a V1.4-SCIPP-08/18 Santa Cruz front-end board featuring a low-noise, 2 GHz inverting trans-impedance amplifier with a gain of 470 Ω. This board was designed for $30 \div 50\,\mu$m LGAD and allowed the characterisation of the sensor time resolution without jitter contribution (< 5 ps). Full signal waveforms were acquired using a high-bandwidth oscilloscope and analysed offline to extract the performances. Several beam-test campaigns between 2021 and 2024 at the CERN PS T10 beam line were conducted using a 10 GeV/c beam.

The $50\,\mu$m LGAD showed a time resolution of $\simeq 34$ ps, while the thinner FBK sensors demonstrated a significant improvement due to the Landau term reduction. The $35\,\mu$m LGAD achieved a time resolution of (22 ± 2) ps with a bias voltage of 240 V. The $25\,\mu$m device reached (25 ± 3) ps at 120 V, despite being manufactured with a substrate not optimised for timing [60].
The study was extended to thinner LGAD sensors with 20 and $15\,\mu$m active thicknesses and a time resolution of ≈ 21 ps and ≈ 30 ps was measured. The increase observed for the lower thickness was attributed to the non-optimised front-end board, which read a sensor with a larger capacitance and a smaller signal compared with what was designed for [61].
The results demonstrated that the Landau contribution was reduced by thinning the active substrate thickness, and that the 20 ps requirement could be satisfied. Nevertheless, as for SiPMs, LGADs are considered a fallback solution due to the high production and assembly costs.

The major R&D effort has been focused on the development of a monolithic CMOS sensor capable of reaching the 20 ps target. Indeed, the large volume production and lower costs make this approach very attractive, considering the readout rate required by ALICE 3. However, the time resolution of a monolithic sensor is still far from what the experiment needs.
The solution proposed by the TOF group has been the introduction of a moderate gain (10-30) in the active region of a standard 110 nm CMOS imaging node. The idea has been to create a monolithic CMOS LGAD sensor capable of satisfying the TOF requirements of the ALICE 3 experiment.

In the following chapters, the CMOS LGAD prototype is described, and the results obtained so far are presented.

Chapter 2

MAPS for high resolution timing applications in HEP

Silicon-based tracking detectors play a central role in modern high-energy and space physics experiments [62]. Traditionally, these detectors have been realised using hybrid pixel or strip geometries, in which the sensor and readout electronics are implemented on separate substrates and then interconnected via bump or wire bonding [63, 64, 65, 66, 67, 68, 69]. While hybrid detectors have demonstrated excellent radiation tolerance, timing performance, and readout flexibility, their relatively high material budget, production complexity, and cost have motivated the exploration of alternative solutions for future experiments.

Monolithic Active Pixel Sensors (MAPS) represent an alternative, as they integrate both the sensing volume and the readout electronics within a single silicon substrate using commercial CMOS processes [70, 71]. In MAPS devices, charge carriers generated by ionising radiation are collected in an epitaxial layer and read out by in-pixel or out-pixel electronics. This monolithic approach eliminates bump or wire bonding, enabling detectors with reduced material budget, potentially improved spatial resolution, and lower production costs. The use of industrial CMOS technologies also provides access to advanced feature sizes and large-scale production, which are critical for next-generation collider experiments.

The adoption of monolithic sensors in high-energy physics has accelerated significantly over the past decade, driven by advances in CMOS imaging technologies and by the stringent requirements of experiments at LHC [72]. Notably, the ALICE Inner Tracking System upgrade represented the first large-scale deployment of MAPS, demonstrating that monolithic sensors can achieve excellent tracking efficiency, spatial resolution at the level of a few micrometres, and radiation tolerance compatible with multi-year operation [73, 74]. These achievements have established MAPS as a mature and competitive technology for vertexing and tracking applications in low- to moderate-radiation regions.

Ongoing research and development efforts are extending the capabilities of monolithic sensors beyond traditional tracking applications. New device concepts, such as Depleted MAPS (DMAPS), employ high-resistivity substrates and high-voltage CMOS processes to increase the depleted volume, enabling faster charge collection (mainly by drift) and radiation tolerance [75, 76, 7, 77, 78, 79]. These developments aim to close the performance gap with hybrid detectors, particularly in terms of timing resolution and operation in harsher radiation environments. As a result, monolithic sensors are increasingly considered for a broad range of detector systems. However, the time resolution of a monolithic system is not yet at the level of hybrid detectors when sub-ns or sub-100 ps resolutions are required.

In the next sections, an overview of the monolithic sensors for timing applications which have been developed in recent years is presented. In particular, Sec. 2.1 presents the prototypes in which no gain layer has been implemented, while Sec. 2.2 reports the solutions in which a gain layer has been adopted.

2.1 MAPS without gain layer

In this section, the monolithic prototypes designed for timing applications which do not use an internal gain layer for charge multiplication are presented. The discussed prototypes are: CAcTμS, MiniCACTUS, APTS, FASTPIX and SiGe BiCMOS - MONOLITH.

CAcTμS The CAcTμS (CMOS ACtive pixel Timing μ Sensor) chip was designed in the framework of the HL-LHC upgrade [80, 81].

With the increase of pp interaction per bunch crossing, to avoid pile-up in the vertices reconstruction, it is mandatory to assign precise time information to each track. Solutions with a time resolution below 100 ps and a mm granularity are very attractive, also for future experiments at FCC. CAcTμS is a DMAPS implemented in the 150 nm CMOS process from LFoundry, which allows for High Resistivity (HR) wafers ($> 2\,\mathrm{k\Omega cm}$) capable of sustaining high bias voltages ($\simeq 300\,\mathrm{V}$). The sensor concept is based on earlier prototypes (LF-MONOPIX[82] and LF-CPIX [83]), which were designed as a tracking chip candidate for the ATLAS Inner Tracker (ITk) upgrade envisioned for the High-Luminosity LHC.

CAcTμS implements two pixel sizes: $1\times1\,\mathrm{mm}^2$ and $1\times0.5\,\mathrm{mm}^2$. This geometry was chosen for different reasons. First, larger collection electrodes show a more uniform electric field and parallel drift lines, allowing for a lower distortion term contributing to the time resolution. In addition, timing application requires a fast signal with a steep rise time and hence higher front-end power compared to a chip designed for tracking. Smaller pitches lead to higher channels density per cm^2, resulting in unacceptable power consumption.

The CAcTμS sensor is based on a large n-collection electrode realised with deep n-well implants (Fig. 2.1). Inside this deep implant, the electronics is implemented in a buried deep p-well where NMOS and PMOS transistors are placed. Two wafers were produced and thinned down to 100 and 200 μm from the original thickness of 725 μm. Then, they were post-processed, and a p implant was implanted on the substrate back. It allows the full depletion due to the pn junction. Two different guard ring layouts were implemented: the standard, which is identical to the one used in LF-CPIX (V2) and a second one capable of reaching higher breakdown voltages.

The in-pixel front-end electronics fills a small part of the pixel area, and it is based on a Charge-Sensitive Amplifier (CSA) architecture followed by a leading-edge discriminator. The threshold non-uniformity is corrected with a 4-bit DAC implemented in-pixel. The collection electrode is biased with a diode-connected NMOS transistor used as a high impedance component. The collection electrode and front-end electronics are AC-coupled.

The CAcTμS chip size is $10 \times 10\,\mathrm{mm}^2$ and it is divided into three main areas. One part is dedicated to 42 pixels of 1 mm pitch (7×6), another is allocated for 42 other pixels with a size of $1 \times 0.5\,\mathrm{mm}^2$ (6×7). The third part contains the column control logic, the global configuration register and an analog buffer connected to all the pixels. The pixels of the chip can be read out via the analog buffer or via the global digital output signal.

The measured and simulated capacitances differed by more than an order of magnitude due to a parasitic capacitance between the power rail and the n-collection electrode. The poor SNR allowed for the characterisation of the 200 μm thick wafer (lower C and greater signal) and pixel size of $1 \times 0.5\,\mathrm{mm}^2$ (lower C).

A 97 % efficiency was measured with a threshold corresponding to 0.6 MIP. The 3 % loss was attributed to multiple scattering in the tracking telescope. A time resolution of 443 ps was achieved using the analog signal and applying a threshold

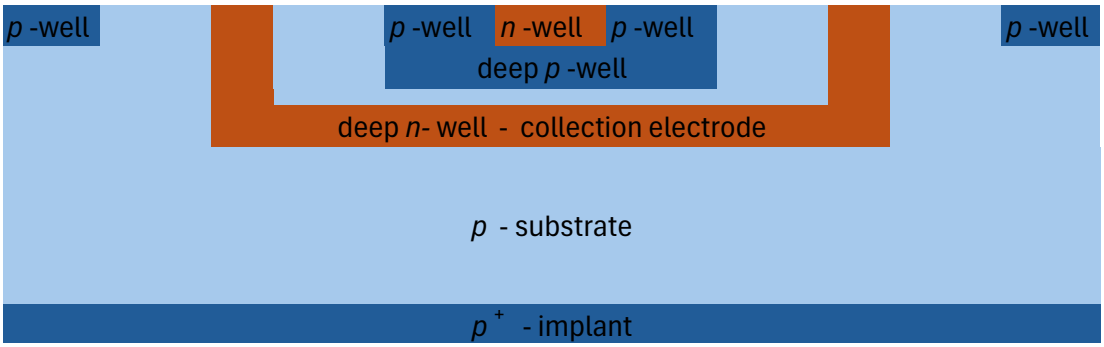


Figure 2.1: CAcTμS sensor cross section drawn not to scale.

of 1.9 MIP ($< 10\%$ efficiency). 511 ps were achieved with the digital output and a threshold of 0.3 MIP ($> 97\%$ efficiency).

Table 2.1 summarises the specifications and results of CAcTμS.

MiniCACTUS MiniCACTUS is a monolithic CMOS sensor developed in the same framework of CAcTμS to reach a time resolution better than 100 ps [9]. This prototype is a pixel matrix of 2×4 pixels. The pixel size (1 and 0.5 mm^2) and the sensor layout are identical to CAcTμS, while the front-end electronics is placed outside the pixel to avoid the increase in input capacitance observed in the other prototype due to parasitic metal lines crossing the collection electrode. The front-end architecture is based on CAcTμS with minor modifications, while the periphery is identical. In particular, one of the eight pixels has the coupling capacitance between the sensor and front end implemented on the collection electrode, while the other pixels have the capacitance in the feedback loop.

The prototype was tested at CERN SPS and a time resolution of 65 ps was achieved with a 185 μm thick substrate (200 μm minus the passivation), a 0.5 mm pixel pitch (1×0.5 mm^2) and the coupling capacitance outside the feedback loop [84]. The discriminated signal was used to extract the time resolution, which was then corrected for the time walk effect using the amplitude extracted using the analog signal probe. Before the time walk correction, 226 ps were measured.
Table 2.2 summarises the specifications and results of MiniCACTUS.

Table 2.1: CAcTμS specifications and results.
The first part of the table summarises the specifications and the simulations predictions. The second part presents the results obtained from measurements.

	CAcTμS	
Technology	LFoundry 150 nm LF15A	
Pixel size [mm^2]	1×1	1×0.5
Simulated input capacitance [pF]	1.5	1
Thickness [μm]	100, 200	
Charge collection time [ns]	< 5	
Power consumption [mW/cm^2]	145	290
Simulated time resolution [ps]	180 and 60 (200 and 100 μm thick)	
Breakdown [V]	230 or 350 (guard ring layout)	
Measured input capacitance [pF]	20	15
Efficiency	-	$> 97\%$
Time resolution [ps]	-	443

Table 2.2: MiniCACTUS specifications and results.
The first part of the table summarises the specifications and the simulations predictions. The second part presents the results obtained from measurements.

	MiniCACTUS
Technology	LFoundry 150 nm LF15A
Pixel size [mm^2]	1×0.5
Simulated input capacitance [pF]	1.5
Thickness [μm]	185
Power consumption [mW/cm^2]	300
Time resolution [ps]	65

A second version of the prototype was implemented and tested: MiniCACTUS_V2 [85], where a new amplifier with a faster recovery time was designed and produced with different active substrate thicknesses (200, 175, 150 μm). Two front-end architectures were developed: a CSA optimised for timing similar to MiniCACTUS and a voltage pre-amplifier in which the feedback capacitor was removed. The best time resolution was achieved with a $0.5 \times 0.5\,\mathrm{mm}^2$ pixel with the new CSA version and a 175 μm thick substrate.
Table 2.3 summarises the specifications and results of MiniCACTUS_V2.

APTS In the ALICE ITS3 upgrade context [37], different test structures were designed to fully exploit the Tower Partners Semiconductor Co (TPSCo) 65 nm process performances. The Analog Pixel Test Structure (APTS) was specifically designed to probe timing performances [86]. It is based on fast per-pixel operational amplifiers reading a four-by-four pixel matrix. The pixels have small

Table 2.3: MiniCACTUS_V2 specifications and results.
The first part of the table summarises the specifications and the simulations predictions. The second part presents the results obtained from measurements.

	MiniCACTUS
Technology	LFoundry 150 nm LF15A
Pixel pitch [mm]	0.5
Thickness [μm]	175
Power consumption [mW/cm^2]	155
Time resolution [ps]	63

collection electrodes and a non-uniform electric field.

The chip size is $1.5 \times 1.5\,\mathrm{mm}^2$ and the pixel has a $10\,\mu$m pitch. Three different versions of the sensor layout, shown in Fig. 2.2, were implemented: standard, modified and modified with gap [77]. All of them are based on an n-collection electrode in a p^--epitaxial layer ($\approx 10\,\mu$m) grown on a p^+ substrate. The electronics is implemented all around the collection electrode inside a deep p-well. The modified version adds a low-dose n-implant under the full pixel area, creating a planar deep np junction. The modified with gap adds a gap of $\approx 2.5\,\mu$m between pixels beneath the deep p-well. The three versions differ in the depletion volume. In the first one, a balloon-shaped depletion is obtained around the electrode; the charges generated outside of it are collected by diffusion. In the modified ones, all the p^--epitaxial layer and the low-dose n-implant are depleted. In particular, the third one creates a higher electrical field at the border, decreasing the charge sharing between pixels. The depletion is obtained by applying a negative voltage to the substrate (up to $-4.8\,\mathrm{V}$).

The in-pixel front end is composed of two consecutive source follower buffer stages with low input capacitance. They are followed by a fast operational amplifier stage and an output stage driving a $50\,\Omega$ line, both placed outside the pixel due to area limitations. The input transistor is DC coupled to the sensor and is linked to a PMOS transistor providing the reset current and compensating for sensor leakage current. The power consumption of the two in-pixel source followers is

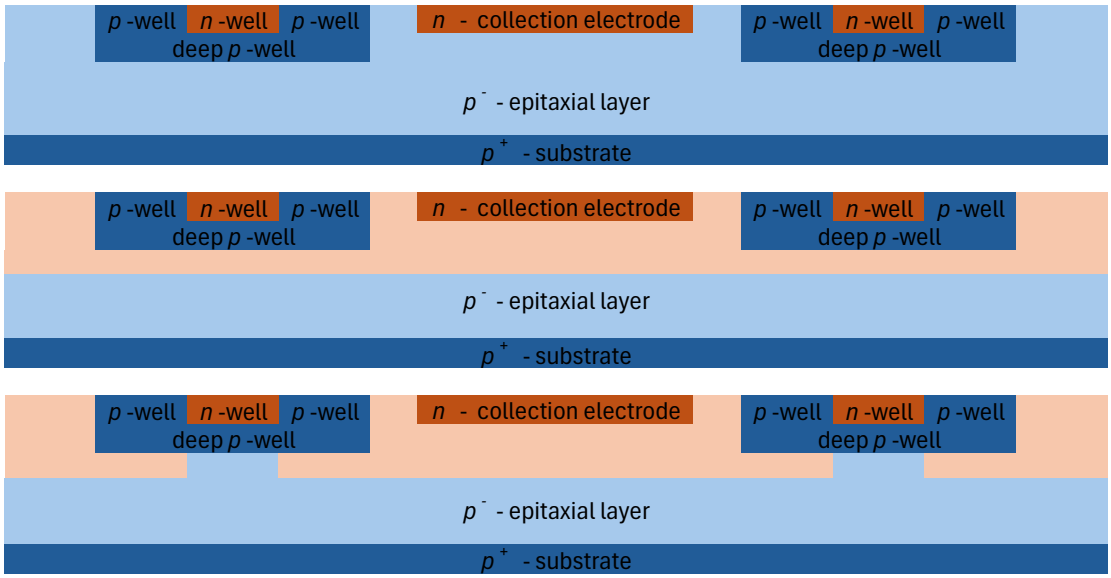


Figure 2.2: APTS sensor cross section not to scale. From the top: standard, modified and modified with gap versions.

150 μW, while for the other stages, 3.1 mW.

The APTS structures with and without a gap were characterised at CERN SPS with different substrate biases. An efficiency higher than 99 % was measured up to 150 e^- (≈ 6 RMS$_{noise}$) and a time resolution of 63 ps was achieved with a time walk correction based on the signal amplitude and cluster size. No major variations were observed for the two modified sensor layouts. In-pixel timing structures are evident; particles crossing the edges generate slower signals with a worse time performance compared to central hits. A 120 ps total delay from signals generated in the centre to signals formed in the corner, and a time resolution variability from 58 to 72 ps moving inside the pixel, were extracted.

The main specifications and characteristics of the APTS structure are shown in table 2.4.

FASTPIX The FASTPIX project investigated a monolithic sensor for future colliders such as the FCC. The goal was to design a monolithic CMOS sensor in the 180 nm technology with a sub-ns timing performance and small collection electrode [10].

The sensor design is similar to APTS and ALPIDE chips. In addition to the low-dose n-implant with and without gap presented in the previous paragraph, an extra deep p-implant was proposed below the edge, placed in the same area of the n-implant gap. The goal was to increase the electric field at the pixel edge and speed up charge collection at the borders [87].

In FASTPIX, a hexagonal pixel shape was chosen to minimise the drift path from border to centre and to allow the charge to be collected by a maximum of three pixels instead of four (square geometry), increasing signals amplitude when

Table 2.4: APTS specifications and results.
The first part of the table summarises the specifications and the simulations predictions. The second part presents the results obtained from measurements.

	APTS
Technology	TPSCo 65 nm
Pixel pitch [μm]	10
Simulated input capacitance [fF]	2÷6
Thickness [μm]	10
Charge collection time [ns]	< 1
Power consumption [mW/cm^2]	150×10^3
Efficiency	$> 99\%$
Time resolution [ps]	63

the charge is shared among the pixels.
The prototype chip has 32 matrices with 68 pixels each (64 with binary and 4 with analog readout). Four different pixel pitches are present (8 matrices each): 8.66, 10.0, 15.0 and 20.0 μm. The in-pixel circuit is composed of a source follower stage followed by a second stage placed in the periphery. The two stages have a feedback network compensating for the gate–drain and bulk-drain capacitance at the input node. The four analog pixels of each matrix are connected to four output stages, which buffer the signal to 50 Ω lines, while the other 64 are connected to 64 discriminators whose outputs are linked to a fast-OR followed by a LVDS driver.

FASTPIX performances were measured at CERN SPS using the discriminated signal exiting the fast-OR [88]. A maximum delay of 500 ps was measured between particles impinging in the centre and the border. An efficiency higher than 99 % was measured for the standard and modified process with the 20 μm pitch. Instead, the 8.66 μm pitch showed a 62 % efficiency with the standard sensor, while 98 % in the modified version. This difference was attributed to lower signals in the standard process due to diffusion in the epitaxial layer. Time resolution was measured to be 102 and 121 ps for pixel pitches of 20 and 10 μm, respectively, in the modified version of the sensor.

Table 2.5 summarises the specifications and results of FASTPIX.

SiGe BiCMOS - MONOLITH The Silicon-Germanium Hetero junction Bipolar Transistors (SiGe HBT) technology offers fast signal amplification, low noise and low amplifier current density. These characteristics make the SiGe BiCMOS process very attractive for monolithic sensors in HEP were low power and good time resolution are mandatory. The MONOLITH project used the e IHP SG13G2

Table 2.5: FASTPIX specifications and results.
The first part of the table summarises the specifications and the simulations predictions. The second part presents the results obtained from measurements.

	FASTPIX
Technology	TowerJazz 180 nm
Pixel pitch [μm]	8.66, 10.0, 15.0 and 20.0
Simulated input capacitance [fF]	< 10
Thickness [μm]	25
Charge collection time [ns]	< 2
Power consumption [mW/cm^2]	$24 \div 4.5 \times 10^3$ (pitch dependent)
Efficiency	$> 99\%$
Time resolution [ps]	102

130 nm BiCMOS process to achieve state-of-the-art performances.

The ASIC prototype developed by the MONOLITH project has a 12×12 pixel matrix with digital readout [8]. The front end (CSA), discriminator and an 8-bit DAC are implemented in-pixel, while the control and timing logic are placed in the periphery. The ASIC has three TDCs connected to the pixel with fast-OR lines. The pixel is hexagonally shaped with a 65 μm edge (pitch $\approx 100\,\mu$m). The sensor is an n-collection electrode in a p-substrate that can be fully depleted with a negative bias.

In order to fully exploit the timing performance of the design, the ASIC has four pixels connected to a preamplifier and an analog driver placed outside the pixels. These four channels were tested at CERN SPS, where an efficiency higher than 99 % was measured for a threshold lower than $7\,\sigma_{\mathbf{noise}}$. For the time resolution analysis, 36 ps were achieved considering only events above $6\,\sigma_{\mathbf{noise}}$ and correcting for the time walk effect using the signal maximum amplitude.

A second prototype was designed to overcome instability and cross-talk between pixels [89]. The sensor design and the pixel pitch are identical to the previous chip; however, a 50 μm-thick epitaxial layer with a higher resistivity is used (350 $\Omega\,$cm). This new substrate, in combination with an improved guard ring, allows to bias the sensor up to 300 V, assuring the carriers velocity saturation. At CERN SPS, an efficiency higher than 99.5 % was measured for a front-end power consumption spanning from 0.04 to 2.7 W/cm^2 and for a threshold of 7 σ_{noise}. In addition, no efficiency drop was observed at the pixel edges. Time resolutions of 21 and 30 ps were achieved with a power consumption of 2.7 and 0.36 W/cm^2, respectively. These values are stable inside the pixel, and no time resolution degradation was observed at the pixel edges.

Table 2.6 summarises the specifications and results of the prototype.

Table 2.6: MONOLITH ASIC specifications and results.
The first part of the table summarises the specifications and the simulations predictions. The second part presents the results obtained from measurements.

	MONOLITH ASIC	
Technology	IHP SG13G2 130 nm BiCMOS	
Pixel pitch [mm]	100 (hexagonal)	
Simulated input capacitance [pF]	0.08	
Thickness [μm]	50	
Power consumption [mW/cm^2]	2.7×10^3	360
Efficiency	$> 99.5\%$	
Time resolution [ps]	21	30

2.2 MAPS with gain layer

The monolithic prototypes presented in the previous section showed good timing performances. However, the main limitation for structures with large pixel pitches is the poor Signal-to-Noise Ratio (SNR), while for small pixel pitches, the major constraint is the power consumption.

The introduction of a gain layer inside the sensor, by using the Low Gain Avalanche diode (LGAD) concept, can improve the signal and thus increase the SNR.
In this section, the prototypes in which a gain layer has been implemented inside the sensor are presented: CASSIA and PicoAD.

CASSIA The CASSIA project (CMOS Active SenSor with Internal Amplification) has been integrating a gain layer in the 180 nm TowerSemiconductor imaging technology to have a 4D tracking device with small pixel pitches ($< 50\,\mu$m) and a good time resolution. The sensor is designed to operate in two modes: LGAD or SPAD. In the first case, the device is below the breakdown voltage, while in SPAD mode, the sensor is in Geiger mode. The starting point was the process developed by the MALTA collaboration [90] with an active thickness of 30 μm, and a sensor structure similar to the one described for APTS (modified version). In addition, a deep p-well gain layer was implanted beneath the collection electrode. Different sensor layouts were fabricated.
In this prototype, the readout electronics was composed of an external CIVIDEC amplifier, which did not allow for time measurement of the prototypes. The achieved gain in LGAD mode was between 10 and 100, while in SPAD mode, gains above 4000 were measured [91]. The results are preliminary but suggest a future implementation of the LGAD design also in the 180 nm Tower Semiconductor imaging technology applied to small pixel pitches.

PicoAD The MONOLITH project, in parallel to the no-gain version described in the previous section, developed a new type of sensor, the Picosecond Avalanche Detector (PicoAD) [11]. It is based on a multi-junction substrate np_{pixel} - np_{gain} which allows for a 100 % efficient sensor and a uniform gain, different from LGAD, and also for a minimisation of Landau noise.

The PicoAD is just a "substrate"; the same electronics designed for a standard monolithic sensor can be implanted on these wafers. Indeed, the same chip described in the *SiGe BiCMOS* paragraph of the previous section was fabricated on the PicoAD wafer, whose cross-section is shown in Fig. 2.3. Starting from the bottom, an epitaxial layer (p^-) is grown on low resistivity substrates of 0.1 Ωcm up to the red line in the figure: the *absorption region*. Then, the first np_{gain} junction

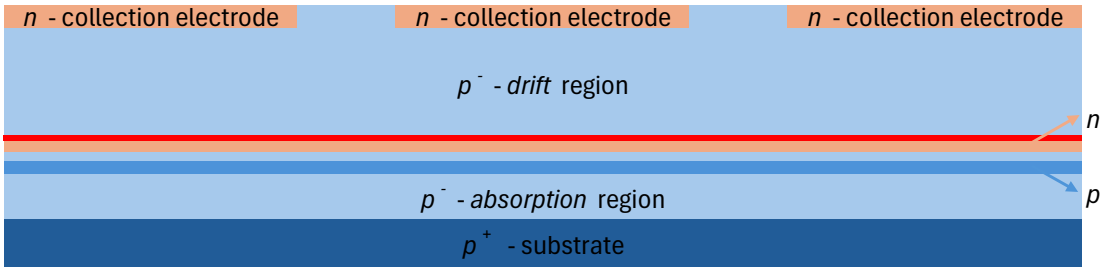


Figure 2.3: PicoAD section with the implants not designed in scale. The structure is described in the text.

is implanted. Its goal is to create a field inside the junction high enough to trigger the onset of the avalanche process. Next, a second epitaxial layer (p^-) is deposited, i.e. the *drift region*, on which the full CMOS electronics can be manufactured.

The n-electrode collects electrons generated inside the two regions; however, the e^- created in the *absorption region* are multiplied crossing the np_{gain} junction. The multiplied charges drift toward the electrode in the *drift region*, contributing to the greatest part of the signal. Also, the holes generated in the *absorption region* are multiplied in the np_{gain} junction, but the amplification is $6 \div 7$ times lower than electrons.

The main drawback of the PicoAD technology lies in its manufacturability. The process is time-consuming and susceptible to surface defects due to the thick epitaxial drift layer in which the electronics are implanted. Moreover, the gain structure requires dedicated wafer pre-processing prior to the CMOS/BiCMOS fabrication steps, including epitaxial growth, gain-layer implantation, and a second epitaxial growth stage. As a result, both the supply chain and process integration become more complex compared to implementing the gain layer directly as an additional mask within a standard CMOS process flow. In particular, wafer flatness, surface quality, and defect density after epitaxial growth must be carefully controlled to ensure compatibility with fine-pitch CMOS lithography. These parameters are strongly process-dependent, but they were successfully controlled in the demonstrated implementation.
In addition, the current BiCMOS processing capability at IHP is not well suited for large-scale production volumes. Nevertheless, the PicoAD manufacturing process could be transferred to foundries capable of high-volume industrial production while always taking into account the complexity of the PicoAD manufacturing process.
In the first production, the *absorption* and *drift region* were 5 and 10 μm, respectively. The *drift region* thickness was not optimised due to process limitations in boron concentration, hence some non-uniformity in the weighting field and gain

were observed. Indeed, the *drift region* should be thicker than the inter-pixel distance.

The first PicoAD prototype implementing the first chip version described in the previous section was tested at CERN SPS [8]. As mentioned above, the gain was not uniform inside the pixel and, combined with charge sharing, resulted in a four times lower signal at the borders compared to the one generated by a MIP crossing the pixel centre.

An efficiency above 99 % was still measured with a power density of 2.7 W/cm^2 and a threshold up to 13 σ_{noise}. A 2 % efficiency drop was observed at low substrate voltages due to the gain non-uniformities. The best time resolution achieved, measuring one pixel, is 17 ps with a power consumption of 2.7 W/cm^2; 30 ps were extracted with 0.4 W/cm^2.

These results can be compared with the first version of the SiGe BiCMOS prototype without PicoAD (no gain). The same time resolution can be obtained with less than one-third of the power, justifying the introduction of the gain layer. A second version of the PicoAD is presented in [92]. 15 different flavours were produced changing the *drift* (15 and 25 μm) and the *absorption* (3 and 5 μm) *region* thicknesses and different doses of np$_{gain}$ junction implants. The chip fabricated on top of this new PicoAD version is the second SiGe BiCMOS version described in the previous section.
The best results were obtained with a 5 μm *absorption* layer, 15 μm *drift* layer, and the highest dose implanted corresponding to an electron gain of 50 (highest bias voltage, 20 V before breakdown).

At CERN SPS, an efficiency higher than 99.9 % was achieved for different substrate voltages with a power consumption of 2.6 W/cm^2 and a threshold up to 7 σ_{noise} (same threshold used for the time analysis). By lowering the power to 0.4 W/cm^2, the efficiency was still above 99%.
The efficiency drop observed below the pixel edges in the first PicoAD version was corrected thanks to a higher gain and a thicker *drift region*.

The outstanding time resolutions after time walk correction of 12, 19, 42 ps were measured with power consumption of 2.6, 0.3 and 0.05 W/cm^2. Without time walk correction, the resolutions increase to 24, 34 and 74 ps. As for the efficiency, the time resolution was uniform inside the pixel.

Table 2.7 summarises the specifications and results of the second prototype.

2.3 The monolithic CMOS LGAD

The previous sections demonstrate that MAPS have been rapidly evolving and gradually replacing conventional hybrid sensors. In this environment, two INFN projects, named Sensor with Embedded Electronics Development (SEED) and

Table 2.7: MONOLITH ASIC + PicoAD specifications and results. The first part of the table summarises the specifications and the simulations predictions. The second part presents the results obtained from measurements.

	MONOLITH ASIC	
Technology	IHP SG13G2 130 nm BiCMOS + PicoAD	
Pixel pitch [mm]	100 (hexagonal)	
Thickness [μm]	5+15 (*absorption* and *drift*)	
Power consumption [mW/cm^2]	2.6×10^3	300
Efficiency	$> 99.9\%$	
Time resolution [ps]	12	19

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays (ARCADIA), developed, in tight collaboration with LFoundry [6], a fully depleted monolithic CMOS sensor able to compete with current MAPS technologies.

ARCADIA technology The 110 nm technology node of LFoundry features 6 metal layers, 1.2 / 3.3 V transistors and deep p-well. It represented a good starting point for a DMAPS sensor due to its manufacturing capability (several thousand wafers per week), performance, increased robustness, and lower production costs compared to more aggressive technologies. Nevertheless, some modifications were necessary to switch from the CIS process to a radiation sensor [93]. The conventional p-type substrate was substituted with an n-type floating-zone wafer in which an n-implant behaves as a collection electrode.

A backside lithography is required to form a junction on the rear surface to allow the full depletion of the substrate. This junction is realised by implanting a shallow boron-doped layer on the back side and activating it through laser annealing. For thick substrates, the full depletion requires bias voltages higher than 150 V; therefore, a dedicated edge-termination scheme based on multiple guard rings is mandatory on the back to ensure safe operation. For thicknesses of $\approx 100\,\mu$m, the backside lithography is not needed due to the lower bias required to deplete the substrate. A thin epitaxial layer with a slightly higher n-doping concentration is grown on top of the high resistivity n-region to limit the punchthrough current between the backside p^+ and the deep p-wells. Deep p-wells are mandatory to avoid charge collection by the n-wells accommodating PMOS transistors.

With the same technology, very thin sensors ($< 50\,\mu$m) can be realised starting from a p^+-substrate on which two epitaxial layers are manufactured in sequence; a high resistive n-type layer is grown before a second one used to limit the punchthrough current, as in thicker sensors.

The sensor cross-section for different thicknesses is shown in Fig. 2.4.

Within the ARCADIA project, different side projects were fabricated alongside the full-size system-ready Main Demonstrator (MD) featuring a low-power, high-density pixel matrix. The side ASIC production was possible due to the single-project wafer engineering runs of ARCADIA. This characteristic allowed for different splits of starting substrate, process options, and wafer thicknesses were investigated. A list of ARCADIA projects fabricated in three engineering runs is reported in [6]. Among these, two ASICs were developed to achieve time resolutions below 100 ps: HERMES and MadPIX.

ARCADIA technology for timing applications In the second engineering run of ARCADIA, a prototype with sub-ns time resolution was designed and then tested in the laboratory: HERMES [94, 95]. HERMES has an area of 5×5 mm and features a pixel matrix with a 50 μm pixel pitch based on an optimised implementation of the ARCADIA sensor for timing (larger collection electrodes). The active substrate thickness is 50 μm. The device integrates 48 readout channels, each employing fast front-end electronics located along the periphery of the pixel columns. The channel architecture is based on a CSA followed by a single-ended discriminator.

The electrical characterisation demonstrated that the sensor operated reliably

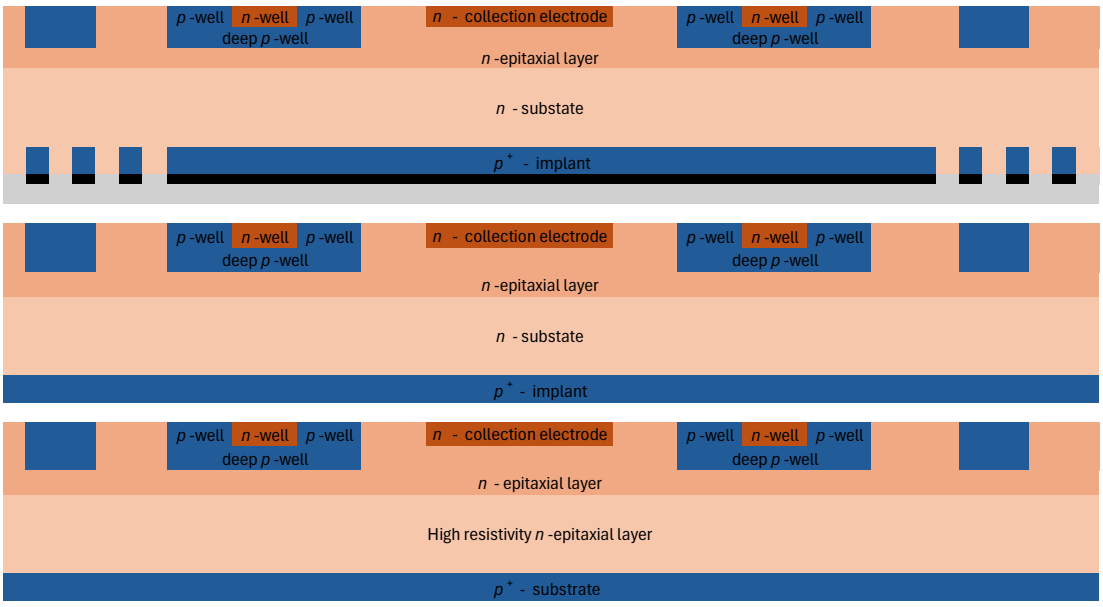


Figure 2.4: ARCADIA sensor section for different active thicknesses with the implants not designed in scale. From the top substrate section for: $\geq 200\,\mu$m, $\simeq 100\,\mu$m and $\leq 50\,\mu$m.

over a broad bias range under full-depletion conditions. Using a ^{90}Sr beta source, the Most Probable Value (MPV) of 76 mV was found and used to predict the time resolution of the ASIC. The jitter was evaluated using the transient current technique with an infrared laser source: 950 ps were measured with a signal amplitude of 74 mV (MPV found with the radioactive source). while 48 ps were achieved with a signal of 327 mV. Although beam tests with charged particles are required to directly assess the timing resolution for MIPs, the results suggest that the prototype cannot reach sub-100 ps timing performance. However, thanks to the skills acquired studying this prototype, a second ASIC for sub-100 ps applications named MadPIX was designed and produced in the third engineering run of ARCADIA.

MadPIX is a monolithic CMOS LGAD prototype implemented in the 110 nm process node of LFoundry and developed to overcome the limitations of HERMES. Its goal was to prove that an internal gain layer could be implemented in the ARCADIA technology. An additional mask was added in the fabrication process for the gain layer. A deep, highly doped, *p*-type layer was implanted beneath the collection electrode (dark blue line in Fig. 2.5).

In particular, MadPIX implements two sensor *layouts* named *1* and *2* [96, 97]. The difference lies in the different terminations of the borders. Figure 2.6 shows the edge implants for *layouts 1* and *2*.
In the first configuration, *layout 1*, the deep p-wells are adjacent to the gain layer, leading to an enlarged multiplication region. In this geometry, primary charge carriers generated by impact ionisation beneath the *p*-well can also undergo amplification after drifting toward the gain layer. However, due to a longer drift path, the carriers arrive at the *n*-implant with a delay compared to those originating within the central active area. *Layout 1* should therefore have greater efficiency, but poorer timing resolution.
The second design, *layout 2*, introduces a narrow gap between the two implants. As a consequence, the particles crossing pixels below the deep *p*-wells pass through this separation and reach the collection electrode directly, without being multiplied. This layout, therefore, enables a distinction between signals originating in the

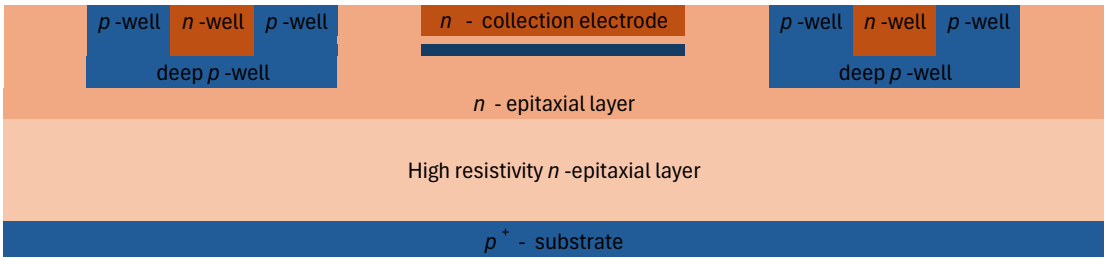


Figure 2.5: ARCADIA sensor section with the introduction of the gain layer. The implants are not in scale.

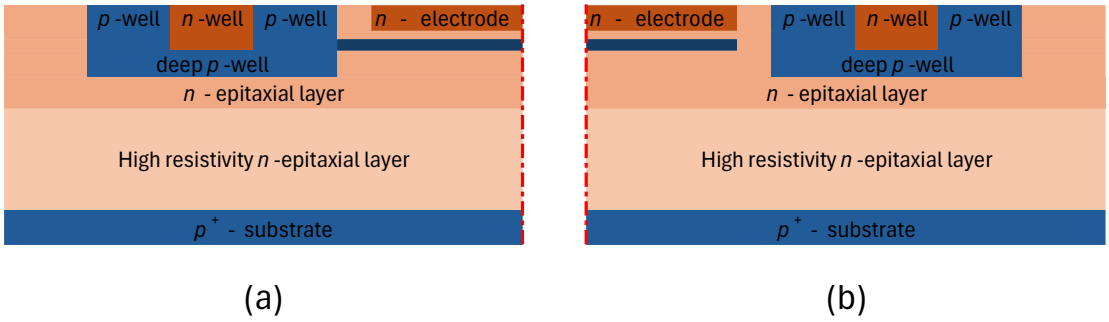


Figure 2.6: Termination layouts of the CMOS LGAD sensor. *Layout 1* is depicted in (a), while *layout 2* is depicted in (b). The gain layer implant is the dark blue line beneath the *n*-electrode.

gain region (pixel centre) and the periphery that do not experience multiplication (pixel borders). *Layout 2*, unlike *layout 1*, should thus have lower efficiency but better timing resolution.

MadPIX was produced in two runs: ARCADIA *Run 3* and ARCADIA *Run 3.2*. *Run 3* was the first production in which MadPIX was introduced in the reticle, while the second was a short loop, i.e. a production using the same mask set as *Run 3*, but with a different gain implantation dose. An additional short loop (*Run 3.3*) was submitted in June 2025 with the same masks and gain layer dose, but using thinner substrates (15 and 25 μm).

The development of the CMOS LGAD prototype was made possible through multiple iterations of simulations and experimental tests. However, in this thesis, the conventional development flow of a monolithic CMOS sensor is followed, starting from the optimisation of the sensor pitch, geometry, and thickness in order to maximise charge collection efficiency, electric-field uniformity, and timing performance. In this context, the Monte Carlo simulations performed to estimate the performance of the CMOS LGAD sensor are presented in the next chapter.
The resulting sensor parameters, such as capacitance, collected charge, and operating bias conditions, subsequently defined the requirements and constraints for the design of the front-end electronics implemented in the prototype, MadPIX, which is described in Chapter 4. Finally, the CMOS LGAD simulations were validated through the experimental characterisation of MadPIX in terms of charge collection, noise, timing resolution, and overall detector performance, as discussed in Chapter 5.

Chapter 3

Monte Carlo simulations of the CMOS LGAD sensor

As the CMOS technology nodes become smaller, the cost of ASIC production rises. This requires a reliable and fast simulation environment that allows prototypes to be developed and produced with a high probability of success. In particular, in the design of a monolithic ASIC where the sensor and the CMOS electronics are manufactured in the same substrate, it is necessary to thoroughly simulate both the electronic circuitry and the sensor itself, i.e. the active area where radiation is detected.

This chapter reports on Monte Carlo simulations of the monolithic CMOS silicon sensor with internal gain designed within the ARCADIA collaboration for the ALICE 3 Time of Flight detector. The Monte Carlo simulations were used to predict the characteristics of the CMOS LGAD sensor implemented in MadPIX (Chapter 4), such as timing performance, intrinsic gain and efficiency.

Section 3.1 describes the MC simulation framework, focusing on the steps performed by *Garfield++* to generate a realistic signal (Sec. 3.1.1, 3.1.2, 3.1.3 and 3.1.4) and on how the gain and time resolution are evaluated (Sec. 3.1.5). While in Sec. 3.2, the simulation results are reported. The first analysis was performed on the data given to the foundry for the first production (Sec. 3.2.1). Then, the simulations using the parameters tuned with experimental results (Sec. 3.2.2) are presented. Subsequently, the study on the second production is reported (Sec. 3.2.3), also with efficiency estimations. The studies presented in this chapter are based on sensors featuring a 48 μm active layer thickness, with the objective of providing a detailed interpretation of the experimental measurements discussed in Chapter 5.

This chapter also includes a preliminary investigation of different pixel pitches, aimed at predicting the time-resolution performance as a function of pixel pitch for sensors with a 48 μm active thickness (Sec. 3.2.4). Furthermore, the final

section presents simulation results for sensors with a 15 μm active layer. These studies represent an important first step toward future productions based on thinner substrates and demonstrate that the 20 ps target for ALICE 3 is achievable.

3.1 Simulation framework

To push the time resolution of a monolithic sensor towards the state of the art, the simulations of the entire radiation detection chain must be studied in detail. From the sensor point of view, the interaction between radiation and matter must first be simulated. Next, the transport of the ionised charges generated by the passage of radiation inside a medium is evaluated, and finally, the signal induced by the charges moving to the collection electrode is extracted. The electrode is then connected to the front-end electronics, which amplifies and therefore reads out the signal generated by the sensor as described in Chapter 4.

With the development of fast computing, it is possible to easily simulate the full detection chain. Indeed, the time resolution of the intrinsic silicon sensor with or without a gain layer can be predicted using Monte Carlo (MC) methods. Monte Carlo methods simulate realistic signals in semiconductor particle detectors using probabilistic models and predict the stochastic variability which arises in physical problems.

Two different software packages are commonly used in particle physics to extract the induced signal generated by particle interaction in a medium: *Allpix2* [98] and *Garfield++* [99]. The former was specifically tailored for silicon sensors, while the latter was initially designed for simulating gaseous detectors, but was then modified to also support silicon devices. Both are continuously developed and maintained to better match reality.

To extract the sensor performance, for the presented work, the *Garfield++* software was used to evaluate the signal generated by a charge particle impinging on the CMOS LGAD. *Garfield++* was preferred over *Allpix2* due to its better implementation of the multiplication mechanism inside the device, which is needed for CMOS LGAD simulations. Charge multiplication in *Garfield++* was extensively validated on gaseous detectors, while in *Allpix2*, the introduction of gain is still in development and the results are not yet fully validated on experimental data.

3.1.1 Charge deposition

In Garfield++, the interaction between medium and radiation is evaluated through the High-Energy Electro Dynamics (HEED) [100], a C++ program that

implements the Photo-Absorption Ionisation (PAI) model [101], which is included as a *Garfield++* module.

When the radiation crosses matter, it transfers energy to atoms through inelastic collisions, generating a cascade of electrons and photons which continue to ionise the medium until they fall below the minimum ionisation potential. The electrons and ions produced in this process constitute the primary ionisation.
The PAI model is based on the assumption that the ionisation rate depends on the cross-section between atoms and real photons, and on the permeability of the medium. It models the cross-section of the energy transferred from particles, which can then be used in Monte Carlo algorithms such as HEED. It was first created for gaseous detectors, but it also performs well for simulating particles crossing through solids such as silicon.

HEED can simulate different charged particles (protons, electrons, pions, ...) and also photons. For a given particle with a set momentum $\vec{p}$, it returns an object which contains the position, time and energy deposited during the ionising collisions inside the medium. For each collision, a vector of electrons is generated, containing all the conduction electrons associated with the generated cluster. HEED also simulates the energy loss due to δ and the secondary electrons generated during the ionisation.
HEED approximates the total energy deposited with better accuracy than analytical models such as Bichsel, Landau, Shulek, and Hancock, as shown in [102].

The simulations reported in the present work were performed with MIPs, i.e. 180 GeV pions. Different simulations with X-rays were also launched to better comprehend the experimental results obtained with the ^{55}Fe radioactive source; however, they are not reported here because they are currently under study.

3.1.2 Charge transport

Each electron-hole pair belonging to a cluster generated in a specific position $(\vec{x}, t)$ is then propagated inside the medium, following the drift lines, until the border of the device. *Garfield++* includes a class that simulates electron-hole drift with various additional effects such as attachment, recombination, diffusion, fluorescence and avalanche amplification in high-field regions.

The charge transport inside a medium follows the first-order equation of motion:

$$\dot{\mathbf{r}} = \mathbf{v}_d\big(\mathbf{E}(\mathbf{r}), \mathbf{B}(\mathbf{r})\big) \tag{3.1}$$

where $\mathbf{r}$ is the position, $\mathbf{E}(\mathbf{r})$ is the electric field, and $\mathbf{B}(\mathbf{r})$ is the magnetic field, both of which are position dependent. $\mathbf{v}_d$ is the drift velocity.
The simulations were performed with the hypothesis of a zero magnetic field. To demonstrate the validity of this assumption, a first approximation can be made to

calculate how strong the field must be to affect charge carriers. Indeed, if we equal the Lorentz force F_B and the centripetal force F_c in the silicon drift area, we have:

$$F_B = qv_dB = F_c = \frac{m_e v_d^2}{r} \tag{3.2}$$

Solving for B:

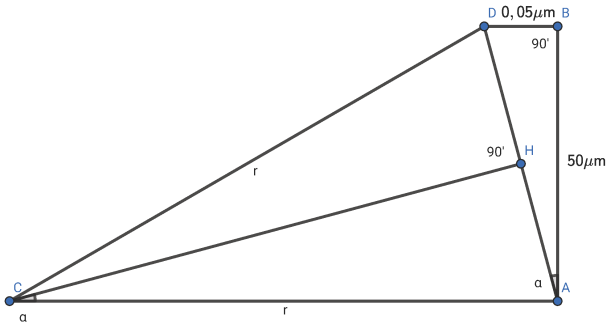
$$B = \frac{m_e v_d}{qr} \tag{3.3}$$

Considering the saturated velocity in silicon (10^7 cm/s), the mass of an electron, the elementary charge and a radius of curvature of 25 mm (0.1 % deviation from the carrier trajectory using Eq. 3.5), the magnetic field should be roughly 30 μT. This value is comparable to the magnetic field of Earth, spanning from 22 μT and 67 μT.

Hence, Eq. (3.1) can be simplified to:

$$\mathbf{v_d} = \mu\mathbf{E} \tag{3.4}$$

The drift velocity shares the same mesh of electric fields and angles.



$$r = \frac{\sqrt{\overline{AB}^2 + \overline{BD}^2}}{2\sin\alpha} \tag{3.5}$$

Figure 3.1: Curvature radius sketch for a 0.1% carrier track shift.

Mobility In *Garfield++* different mobility models are implemented (Minimos [103], Canali [104], Reggiani [105]). The Canali model was used in the simulations, since it is also used by the TCAD software [106]. The electron/hole mobility $\mu^{e,h}$ as a function of the electric field (Fig. 3.2a) was evaluated as follows:

$$\mu^{e,h}(E) = \frac{\mu_\rho^{e,h}}{\left(1 + \left(\frac{\mu_\rho^{e,h} E}{v_{\text{sat}}^{e,h}}\right)^{\beta^{e,h}}\right)^{\frac{1}{\beta^{e,h}}}} \tag{3.6}$$

The β was evaluated with the following formula:

$$\begin{aligned} \beta^e &= 1.109 \left(\frac{T}{T_0}\right)^{0.66} \\ \beta^h &= 1.213 \left(\frac{T}{T_0}\right)^{0.17} \end{aligned} \tag{3.7}$$

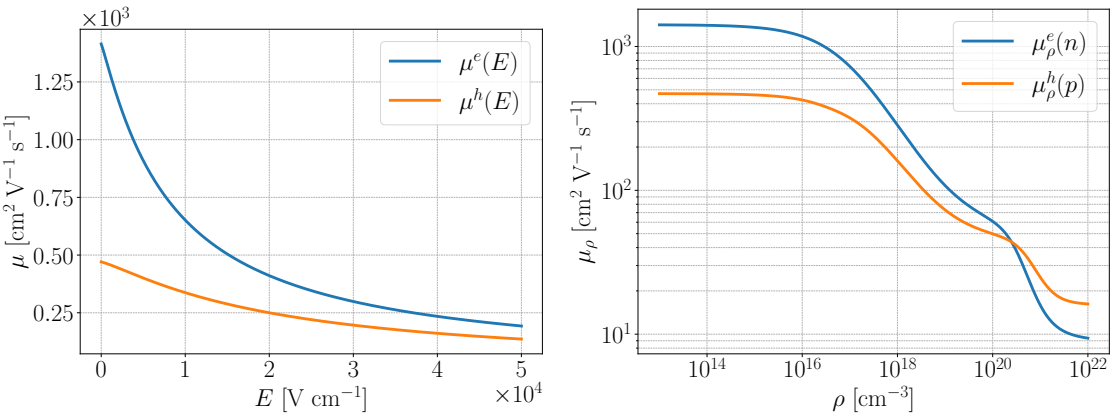
The μ_ρ was extracted considering the impact of the doping concentration on the mobility (Fig. 3.2b). The Massetti model[107] was used in the simulations to compute μ_ρ if the doping concentration (n or p) was above $10^{13}\,\mathrm{cm}^{-3}$:

$$\begin{aligned} \mu_\rho^e &= \mu_0^e + \frac{\mu_{max}^e - \mu_0^e}{1 + \left(\frac{n}{C_r^e}\right)^{\alpha^e}} - \frac{\mu_1^e}{1 + \left(\frac{C_s^e}{n}\right)^{\beta_*^e}} \\ \mu_\rho^h &= \mu_0^h e^{-\frac{p_c}{p}} + \frac{\mu_{max}^h}{1 + \left(\frac{p}{C_r^h}\right)^{\alpha^h}} - \frac{\mu_1^h}{1 + \left(\frac{C_s^h}{p}\right)^{\beta_*^h}}; \end{aligned} \tag{3.8}$$

If the doping concentration was lower than $10^{13}\,\mathrm{cm}^{-3}$, the mobility was considered fixed to the value μ_{max}.

The parameter values of Eq. 3.8 are reported in table 3.1. The values are given for electrons (arsenic) and holes (boron).

μ_{max} is the ohmic (pure-lattice) electron mobility, and its behaviour was set in agreement with *Sentaurus* TCAD model [106], where the lattice mobility is only



(a) (b)

Figure 3.2: Hole (orange) and electron (blue) mobility as a function of (a) the electric field evaluated from Eq. (3.6) and (b) the doping concentration evaluated from Eq. (3.8). The temperature was set to K and in (a) the doping concentrations n and p were set to $10^{13}\,\mathrm{cm}^{-3}$.

Table 3.1: *Sentaurus* TCAD lattice mobility parameters [106, 108].

Parameter	**Electrons**	**Holes**
μ_0 [$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]	52.2	44.9
μ_1 [$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]	43.4	29.0
C_r [$\mathrm{cm^{-3}}$]	$9.68 \cdot 10^{16}$	$2.23 \cdot 10^{17}$
C_s [$\mathrm{cm^{-3}}$]	$3.43 \cdot 10^{20}$	$6.10 \cdot 10^{20}$
p_c [$\mathrm{cm^{-3}}$]	–	$9.23 \cdot 10^{16}$
α	0.680	0.719
β_*	2.00	2.00

temperature dependent (Fig. 3.3a):

$$\mu^{e,h}_{max}(T) = \mu^{e,h}_{max}(T_0)\left(\frac{T}{T_0}\right)^{\beta^{e,h}} \tag{3.9}$$

$\beta^{e,h}$ and $\mu^{e,h}_{max}(T_0)$ have the fixed following values reported in table 3.2.
The v_{sat} of Eq. 3.6 is defined by the Canali model [104, 106], as in Eq. 3.10.

$$\begin{aligned} v^e_{\mathrm{sat}} &= 1.07 \cdot 10^7 \left(\frac{T_0}{T}\right)^{0.87} \ \mathrm{cm/s} \\ v^h_{\mathrm{sat}} &= 8.37 \cdot 10^6 \left(\frac{T_0}{T}\right)^{0.52} \ \mathrm{cm/s} \end{aligned} \tag{3.10}$$

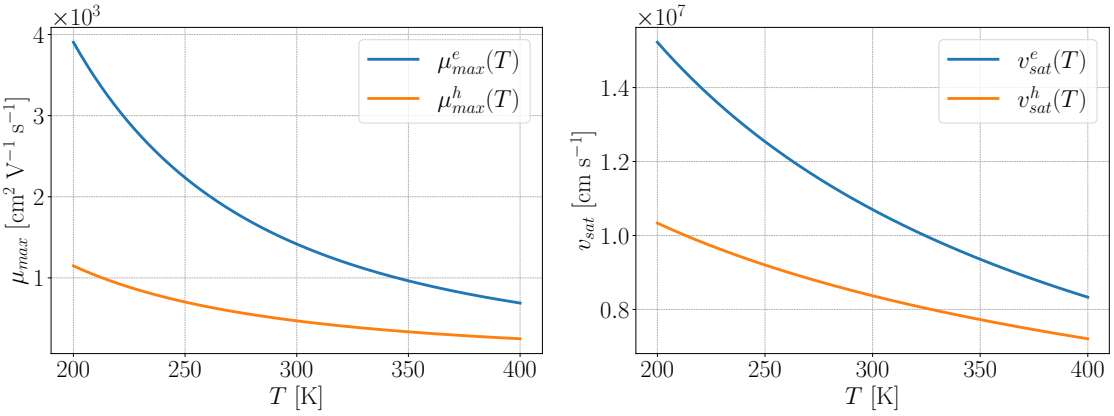
v_{sat} behaviour as a function of the temperature is plotted in Fig. 3.3b.

Transport equation solution In *Garfield++*, in order to solve Eq. 3.1, two possible transport methods are available:

- Runge-Kutta-Fehlberg integration [109]
- Monte Carlo integration [99]

Table 3.2: *Sentaurus* TCAD lattice mobility parameters [106].

Parameter	**Electrons**	**Holes**
β	-2.5	-2.2
μ_{max} [$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]	1417	470.5



(a) (b)

Figure 3.3: (a) Hole (orange) and electron (blue) mobility as a function of the electric field evaluated from Eq. (3.9). The saturated velocity evaluated from Eq. (3.10) in (b). The temperature was set to 300 K.

The Runge-Kutta-Fehlberg integration calculates the drift lines by numerically solving the differential equation (3.1) using a third-order approximation.
The Monte Carlo integration, which was used for this study, is based on a stochastic approach that computes the position based on two components:

- *Drift component*: The electron or ion propagation in the direction of $\mathbf{v}_d$ is evaluated using the trivial equation of motion $\Delta s = \mathbf{v}_d \, \Delta t$, where one of Δs and Δt is provided by the user. $\mathbf{v}_d$ is computed following Eq. (3.4), and its value as a function of the electric field is plotted in Fig. 3.4.

- *Diffusion component*: The diffusion component parallel to $\mathbf{v}_d$ is sampled from three uncorrelated Gaussian distributions with a standard deviation $\sigma_L = D_L\sqrt{\Delta s}$. The same applies to the component of diffusion perpendicular to the motion, i.e. $\sigma_T = D_T\sqrt{\Delta s}$.

The two components are added, and the location is updated. The process is repeated until the carrier reaches the end of the active area. It is also possible to couple the MC method with a second-order Runge-Kutta-Fehlberg to extract an average velocity over each step to improve the carrier path estimation.
Usually, a step of about 0.5 μm was used for silicon devices with gain.
D_T and D_L, used for the standard deviations in the diffusion component calculation, are the diffusion coefficients given by the Einstein relation:

$$D = \frac{\mu^{e,h} k_B T}{q} \tag{3.11}$$

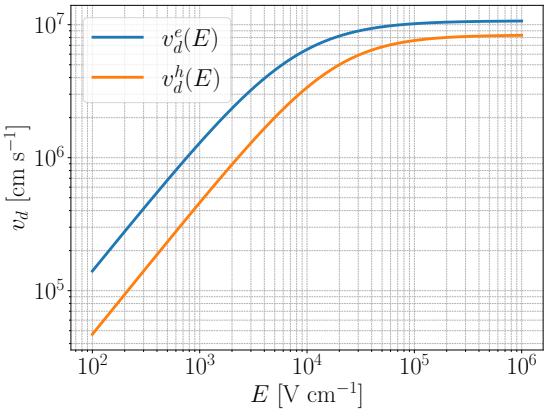


Figure 3.4: Drift velocity of holes (orange) and electrons (blue) as a function of the electric field. The mobility is extracted for a doping concentration n and p of $10^{13}\,\mathrm{cm}^{-3}$ at a temperature of 300 K.

where μ is the electrical mobility evaluated from Eq. 3.6, k_B is the Boltzmann constant, T the temperature and q the elementary charge.

3.1.3 Charge multiplication

During drift, electrons and holes, passing through a high electric field (greater than $300\,\mathrm{kV\,cm}^{-1}$ in silicon), can acquire enough energy to ionise the medium, hence they can trigger the onset of an avalanche. The number of electron-hole pairs generated in the avalanche depends on a coefficient α and on the length d of the high electric field region [45].

$$N_{e,h}(d) = N_{e,h}(0)e^{\alpha_{e,h}d} \tag{3.12}$$

In LGAD, the electric field is tuned to multiply only electrons and not holes, hence only the evaluation of α_e is reported.

The ionisation models are based on the Chynoweth model [110]:

$$\alpha_e(E) = A_e e^{-\frac{B_e}{E}} \tag{3.13}$$

Where A_e and B_e are phenomenological coefficients evaluated differently depending on the model.

The only exception is Okuto Crowell model [111], where α_e is parametrized as follow:

$$\alpha_e(E) = A_e E e^{-\left(\frac{B_e}{E}\right)^2} \tag{3.14}$$

Four ionisation models are implemented in *Garfield++*:

- van Overstraeten and de Man [112]
- Okuto and Crowell [111]
- Massey [113]
- Grant [114]

In table 3.3 and 3.4, A_e and B_e are reported for different models.

Table 3.3: Ionisation parameter A_e for different ionisation models.

Model	$E\,[\mathrm{V/cm}]$	A_e
Massey	–	$4.43 \cdot 10^5\,[\mathrm{cm}^{-1}]$
Okuto and Crowell	–	$0.426 \times [1 + 3.05 \cdot 10^{-4}(T - T_0)]\,[\mathrm{V}^{-1}]$
van Overstraeten and de Man	$< 6 \cdot 10^5$	$7.03 \cdot 10^5\,[\mathrm{cm}^{-1}]$
Grant	$< 2.4 \cdot 10^5$ $2.4 - 5.3 \cdot 10^5$ $> 5.3 \cdot 10^5$	$2.60 \cdot 10^6\,[\mathrm{cm}^{-1}]$ $6.20 \cdot 10^5\,[\mathrm{cm}^{-1}]$ $5.05 \cdot 10^5\,[\mathrm{cm}^{-1}]$

Table 3.4: Ionisation parameter B_e for different ionisation models.

Model	$E\,[\mathrm{V/cm}]$	$B_e\,[\mathrm{V/cm}]$
Massey	–	$9.66 \cdot 10^5 + 4.99 \cdot 10^2\,T$
Okuto and Crowell	–	$4.81 \cdot 10^5\,[1 + 6.86 \cdot 10^{-4}\,(T - T_0)]$
van Overstraeten and de Man	$< 6 \cdot 10^5$	$1.231 \cdot 10^6$
Grant	$< 2.4 \cdot 10^5$ $2.4 - 5.3 \cdot 10^5$ $> 5.3 \cdot 10^5$	$1.43 \cdot 10^6$ $1.08 \cdot 10^6$ $9.90 \cdot 10^5$

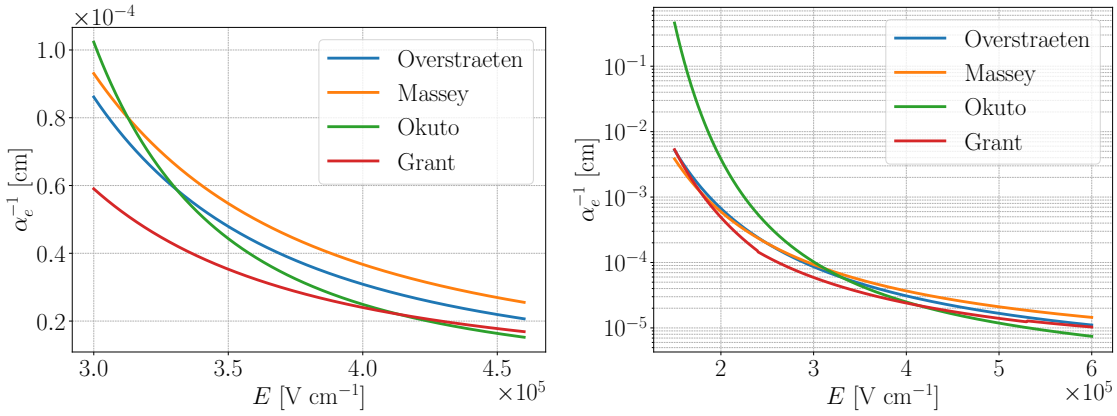


Figure 3.5: Mean free path of electrons for different ionisation models at 300 K (b) and zoom in the electric field range of LGAD (a).

The van Overstraeten and de Man and the Grant models do not consider temperature variabilities. To introduce this dependence, a factor γ (taken from *Sentaurus* TCAD models) is multiplied to A_e and B_e.

$$\gamma = \frac{\tanh\left(\frac{0.063}{2k_bT_0}\right)}{\tanh\left(\frac{0.063}{2k_bT}\right)} \tag{3.15}$$

The behaviour of the mean free path $1/\alpha_e(E)$ as a function of the electric field E is shown in Fig. 3.5a, while the T dependence is plotted in Fig. 3.5b.
The gain estimation using Eq. 3.12 and the van Overstraeten and de Man model is plotted in Fig. 3.6 at different temperatures. While Fig. 3.7 plots the gain layer depth dependence. Clearly, the gain value obtained depends substantially on the depth of the implant and on the electric field applied, i.e. the doping concentration. Temperature also affects the gain value, although not as strongly.

In this study, the model used by default was the van Overstraeten and de Man model. Also, the Okuto and Crowell was used, even though the van Overstraeten and de Man better matched the experimental data.

A limit on the maximum electron-hole pair was set to avoid a breakdown situation, i.e. when the avalanche is exponential and grows without a limit. Experimentally, the breakdown is quenched using different techniques, while via software is stopped by setting a limit to the generated electron-hole pairs.

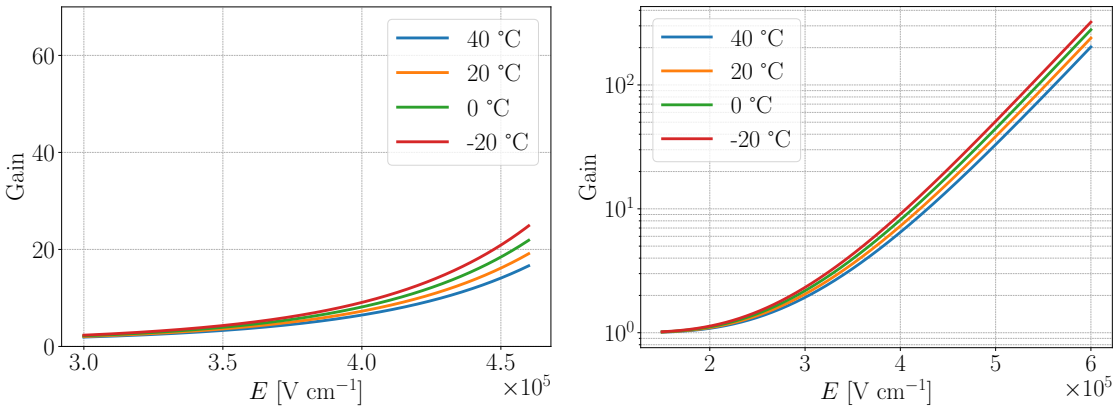


Figure 3.6: Electron gain for a high electric field region implanted at a depth of 0.6 μm evaluated at different temperatures for the van Overstraeten and de Man model (b). (a) zoom in the high electric field region characteristic of LGAD.

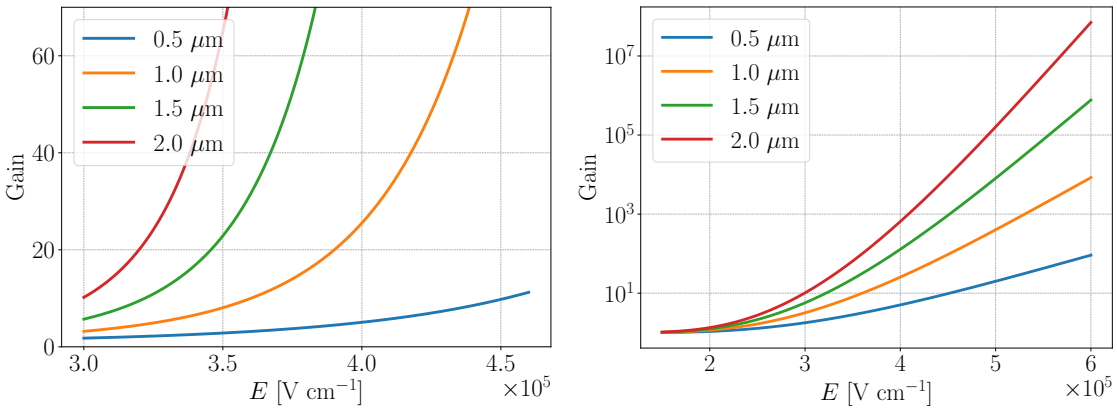


Figure 3.7: Electron gain for a high electric field region implanted at a variable depth evaluated at 300 K for the van Overstraeten and de Man model (b) and its zoom (a).

3.1.4 Signal induction

After the generation and the drift of the carriers, the signal induced on the electrode was evaluated.

The signal formation follows the Shockley-Ramo theorem [115], [116]. This theorem binds the current i induced in an electrode with a particle of charge q placed in $\mathbf{r}$ moving at a velocity $\mathbf{v}$:

$$i(t) = -q\mathbf{v}\mathbf{E}_W(\mathbf{r}) \tag{3.16}$$

Where $\mathbf{E}_W$ is the Weighting Field (WF) for the electrode to be read out.

The induced signal can also be calculated using the integral form of Eq. 3.16:

$$\int_{t_1}^{t_2} i(t)\,dt = q\left[\phi_W(\mathbf{r}_2) - \phi_W(\mathbf{r}_1)\right] \tag{3.17}$$

ϕ_W is the weighting potential. $\mathbf{E}_W$ and ϕ_W are the electric field and potential that would exist in $\mathbf{r}$, where q is placed, if the selected electrode is at 1 V and the other electrodes are at 0 V.

In MC simulations, Eq. 3.17 is solved by discretising time with a certain degree of refinement, and thus it can be rewritten as:

$$i(t_j) = \frac{q\left[\phi_W\left(\mathbf{r}\left(t_{j+1}\right)\right) - \phi_W\left(\mathbf{r}\left(t_j\right)\right)\right]}{\Delta t} \tag{3.18}$$

In the *Garfield++* simulations a Δt of 0.5 ps was set.

From Eq. 3.17, ϕ_W should not have any dimensions due to charge conservation, i.e. $0 < \phi_W < 1$. Therefore, an arbitrary bias voltage V_0 can be applied to the electrode under study in computational modelling, and then the weighting potential is the computed electric potential divided by V_0. This potential can be seen as the fraction of the moving charge q that is induced on the electrode.
In addition, a corollary of the Shockley–Ramo theorem states that the charge induced by q is independent of the actual bias voltages applied and of the space charge distribution. This allows for having different electrodes biased at different voltages when the weighting field or potential is extracted.

The above information gives an operational method for extracting weighting potentials using deterministic simulation programs such as *Sentaurus* TCAD.

- All the electrodes are biased at their operational voltages, and the electric potential map V_0 is extracted.
- The bias voltage of the collection electrode under study is increased by V_{step} and the second electric potential map V_1 is extracted.

- The weighting potential is evaluated as follows:

$$\phi_W = \frac{V_1 - V_0}{V_{step}} \tag{3.19}$$

The increase must be such that it does not substantially change the device working range, e.g. 1 % of the voltage applied to it.
An example of WP is plotted in Fig. 3.8.

The same process can be applied to the weighting field:

$$\mathbf{E}_W = \frac{\mathbf{E}_1 - \mathbf{E}_0}{V_{step}} \tag{3.20}$$

$\mathbf{E}_W$ does not span from 0 to 1 as for ϕ_W because a V_{step} increase on the studied electrode does not imply a variation in the electric field of the same quantity. However, for computational reasons, it was easier to use the potential, being a scalar and not a vector quantity.
After obtaining the induced current for each carrier, the total current is the sum of all the contributions.

Garfield++ cannot evaluate the electrostatic potential needed for the weighting potential by solving the Poisson equation (Eq. 3.21). It can only estimate an analytic field. However, to investigate the performance of modern silicon devices, a more in-depth study must be performed. It was therefore necessary to rely on external programs, such as *Sentaurus* TCAD, to extract the maps.

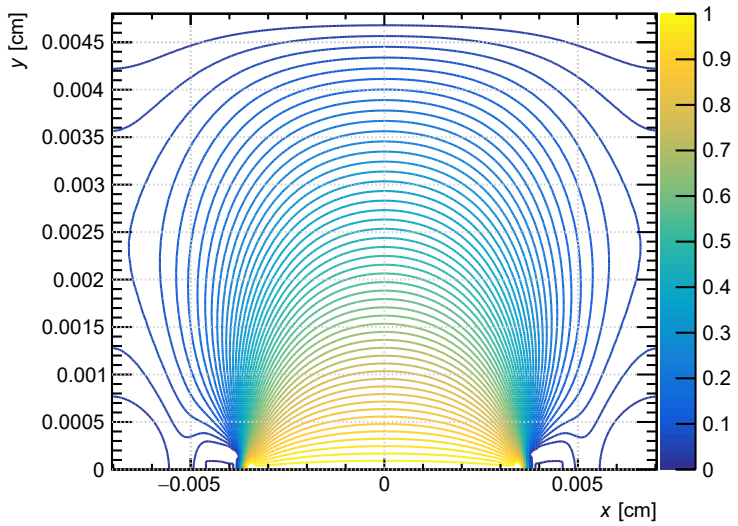


Figure 3.8: Weighting potential map extracted using TCAD maps imported in *Garfield++*.

$$\nabla \cdot \mathbf{E} = \frac{\rho}{\varepsilon_0 \varepsilon_{Si}} \tag{3.21}$$

Indeed, *Sentaurus* TCAD software was used to evaluate the electric field, the drift velocity and all intrinsic properties of silicon using the real doping profiles given by the foundry.

3.1.5 Performance estimation

Gain evaluation Monte Carlo simulations were used to predict the gain of a prototype given its bias condition. The gain G of an LGAD is defined in Eq. 3.22 as the collected charge of the LGAD (Q_{LGAD}) divided by the charge collected by the same device with any multiplication Q_0. Q_0 was evaluated by disabling the ionisation models, i.e. only the primary ionisation created by the impinging particle was considered.

$$G = \frac{Q_{LGAD}}{Q_0} \tag{3.22}$$

However, in MC tools, as in reality, the charge deposition is stochastic; thus, it was not possible to employ just one signal to infer the gain. Hence, the gain was extracted by taking 1000 events, integrating them, plotting the integrated charge distribution and performing a fit with the Landau function convoluted with a Gaussian.
Different models predict the analytical form of this distribution (Bichsel, Landau, Shulek, and Hancock); however, for thin silicon devices, the Landau model does not approximate well the deposited charge distribution. The solution was to modify the energy loss by using a modified cross-section to consider the electron binding energy. Experimentally, the fit was performed by convolving the Landau distribution with a Gaussian one [117]. Shulek et al. proposed an analytical expression with this functional form to predict the experimental values [102].

The gain extracted from MC simulations was evaluated as:

$$G = \frac{MPV_{LGAD}}{MPV_0} \tag{3.23}$$

where MPV_{LGAD} and MPV_0 are the Most Probable Values (MPVs) of the fit performed with and without the activation of the multiplication.

Time resolution evaluation Several algorithms can be employed to extract the time resolution (Constant Fraction, Leading Edge, Dual slope). The choice of algorithm also depends on the type of front-end electronics used to read the sensor. However, the performed simulations aimed to understand the intrinsic

resolution of the sensor itself to choose the most suitable operating conditions for the prototype. The Constant Fraction algorithm on the integrated charge was preferred because the other algorithms are usually applied after the convolution of the front-end electronics transfer function.

Each signal was integrated, and the time at which the signal reached a certain percentage of total charge was determined (Fig. 3.9). The values for this specific percentage were collected in a histogram from which the time resolution could be extracted as a Gaussian sigma, or as RMS if the distribution had tails or non-Gaussian behaviour.

In the next sections, the time resolution study of the CMOS LGAD is analysed through *Garfield++* simulations.

3.2 Simulations of the CMOS LGAD sensor

The objective of the simulations presented in this section was to estimate the gain and time resolution of the MadPIX sensor. For computational and convergence reasons, instead of simulating the 3D pixel, a 2D map of the electric field and potential was extracted from *Sentaurus* TCAD and then extended in *Garfield++* along a fictitious third dimension. In this way, an infinite strip was obtained, with a width determined by the width of the 2D map extracted from TCAD.

The short side of the MadPIX pixel was simulated because the temporal resolution is limited by this dimension, due to the non-uniformity of the weighting potential (distortion term in Eq. 1.1). Indeed, as shown in [118], the time resolution of a silicon sensor depends on the pixel pitch. In particular, it depends on the ratio between pitch w and thickness d of the silicon active area. The w of MadPIX

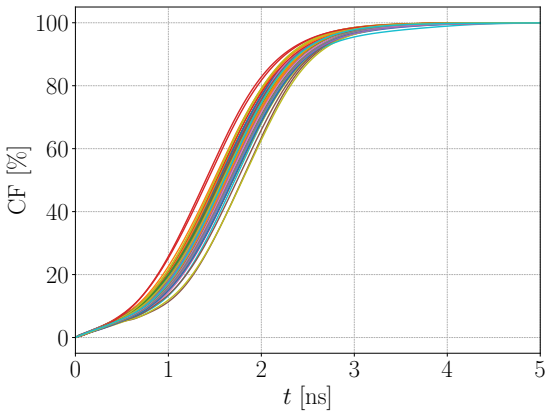


Figure 3.9: Normalised integral of the signals as a function of time. On the vertical axis, the CF thresholds.

is 50 μm and, therefore, the w/d is 2 for the short side, while it is equal to 5 for the long side. A higher w/d means a lower distortion term.

The cross-section of the simulated sensor is shown in Fig. 3.10. It is very similar to the pixel implemented in MadPIX (see Sec. 2.3, *layout 2*). The dimensions of the collection electrode, the gain layer, deep p-well are equal to those of the fabricated sensor *layout 2*. *Layout 1* showed non-convergence problems due to the higher electric field at borders. Also, the clearances between implants are respected. The main difference lay in the position of the n-guard ring, which is positioned at a greater distance. This element does not affect the time resolution, but is used to separate pixels. Since only one pixel was studied, the deep p-well structure was not implemented in the simulation. his implant does not affect charge sharing, nor the electric field and timing behavior, since it is located outside the n-guard ring implant which collects the deposited charge below the deep p-well.

Thus, using the TCAD tool, the electric field and the potential maps at two voltages separated by 0.01 V were extracted from the 2D cross-section. Four biases were supplied to four electrodes:

- n^+-collection electrode - V_{top}
- p^+-substrate - V_{back}
- p^+-implant - V_{dp}
- n-guard ring - V_{gr}

The maps were then imported into *Garfield++*, and the WP was extrapolated. Table 3.5 summarises the parameters used for the simulations. These parameters were not changed unless expressly stated in the text.

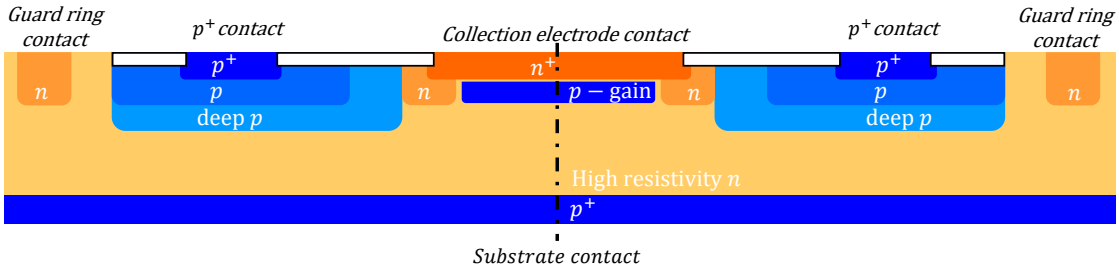


Figure 3.10: 2D section implemented in *Sentaurus* TCAD and used for the Monte Carlo simulations. The dimensions are not to scale.

Table 3.5: Default parameters used in MC simulations.

Parameter	Value
T	300 K
Δt	0.5 ps
Δs	0.5 μm
Particle type	Positive Pion (π^+)
Particle energy	180 GeV
Avalanche limit	None
Ionisation model	van Overstraeten and de Man

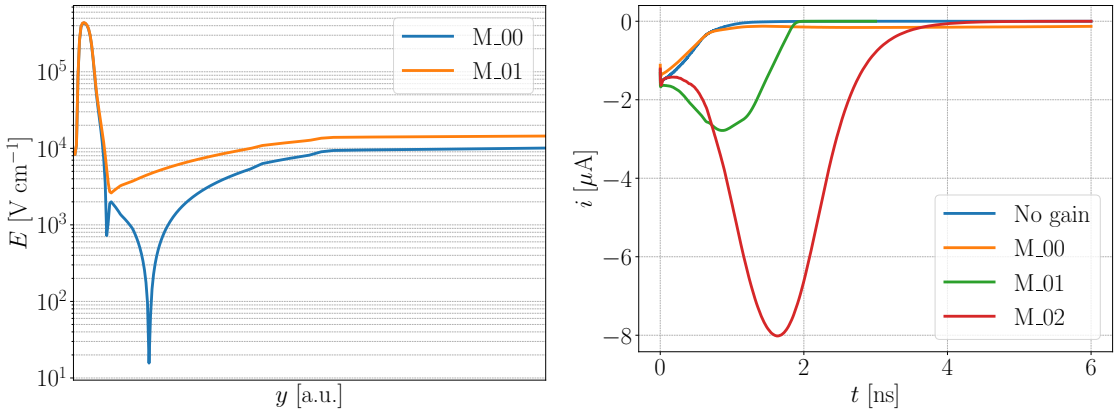
3.2.1 Preliminary simulations

Using the profile shared with the foundry, a first analysis of the first production was conducted. The objective was to predict the gain and time resolution of the prototype. In addition, the nominal profiles were employed to extract the gain dependence on the *Garfield++* parameters Δs, Δt and on the ionisation model. Two dose splits of the p-gain doping were studied, the reference one (0 %) and the first subsequent +3 %. The maps extracted with the nominal profile (M_00, M_01, M_02, M_03) and their biases are summarised in table 3.6. The biasing was chosen using the *Sentaurus* TCAD Current-Voltage (IV) and gain simulations.

The first map, M_00, showed a very low gain even though the electric field peak beneath the collection electrode was high enough to trigger the onset of the avalanche. Indeed, the electric field profile shows a minimum between substrate and gain layer where its value reaches $\simeq 0\,\mathrm{V\,cm^{-1}}$ (Fig. 3.11a). In this region, the carriers diffusion is more significant than the drift component towards the collection electrode. Hence, the electrons, which drift toward it, spread out laterally as can be seen in Fig. 3.12a.

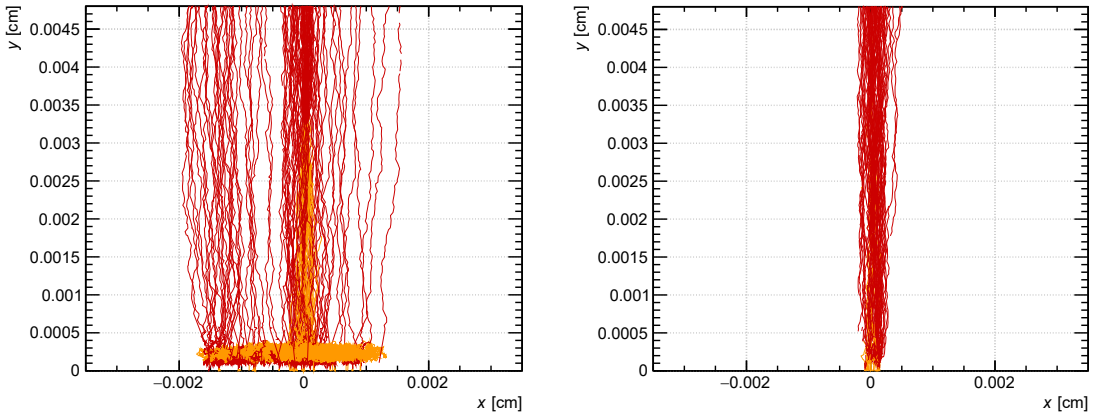
Table 3.6: Biases applied in *Sentaurus* TCAD using two dose splits for the nominal p-gain profiles given to the foundry.

Contact	M_00	M_01	M_02	M_03
Dose split	0%	0%	3%	3%
Collection electrode	35 V	45 V	35 V	45 V
Guard ring	9.5 V			
p^+	0 V			
Substrate	−30 V	−40 V	−40 V	−40 V



(a) (b)

Figure 3.11: Electric field of M_00 (blue) and M_01 (orange) as a function of depth extracted in $x = 0$ cm (a), i.e. centre of the structure. The electric field of M_01 still has a minimum, but it is not sufficient to stop the electrons. (b) mean signals for M_00 (orange), M_01 (green) and M_02 (red) generated by a particle impinging in the centre of the structure. In blue, a signal simulated without the multiplication.



(a) (b)

Figure 3.12: Electrons (orange) and holes (red) drift lines for (a) M_00 and (b) M_01 generated by a particle impinging in the centre of the structure. The collection electrode is in $y = 0$ cm and the map is symmetrical with respect to $x = 0$ cm. The diffusion component below the gain layer is higher for M_00 map; indeed, the electrons diffuse for 30 μm longitudinally. Instead, in M_01, the diffusion in x is contained in 2.5 μm.

Only a few electrons manage to pass through the gain zone, thus creating a signal that is very similar to the one generated in a common silicon sensor.

The M_01 map was extracted with a higher bias applied to the sensor to overcome the problem found in M_00. The electric field shapes extracted in the device centre of M_00 and M_01 are compared in Fig. 3.11a. The minimum is still present, however, in M_01 the drift component is greater than the diffusion one (Fig. 3.12b). Thus, the electrons successfully pass through the gain layer and get amplified.

In parallel to M_01, M_02 and M_03 were extracted with the same layout, but with a 3 % increase in the gain layer doping concentration. However, M_03 was not usable due to the non-symmetric ϕ_W. This effect was a *Sentaurus* TCAD artefact generated because the electric field inside the gain layer was too high, and the breakdown phenomena occurred. Figure 3.11b shows the mean signal generated by a particle impinging on the device centre. M_02 is bigger than M_01 due to the higher implantation dose and slower due to the lower bias applied to the collection electrode.

M_02 was also used to establish the impact of Δt and Δs on sensor gain and on time resolution. The scan was performed, and the results are summarised in table 3.7; the gain dependence on Δs is plotted in Fig. 3.13. The Δs parameter has a strong dependence on the simulated gain; however, by decreasing it, the simulation time exponentially grows. Δs was chosen to be equal to 0.05 μm as it was a good point that optimised simulation time and accuracy. Instead, Δt did not change the results of simulations, hence a Δt of 0.5 ps was chosen.

With the parameter extracted by the previous study, two multiplication models, i.e. the van Overstraeten and the Okuto, were used to predict the gain. The results

Table 3.7: Scan on Δt and Δs. The configuration of the last row has proven to be computationally too heavy to produce results within a reasonable duration.

Δs [μm]	Δt [ps]	**Gain**	σ_t[ps]
1.000	0.50	32.6	61
0.500	0.50	18.4	61
0.050	0.50	14.7	58
0.050	0.05	14.1	55
0.010	0.50	12.0	60
0.005	0.50	−−	−−

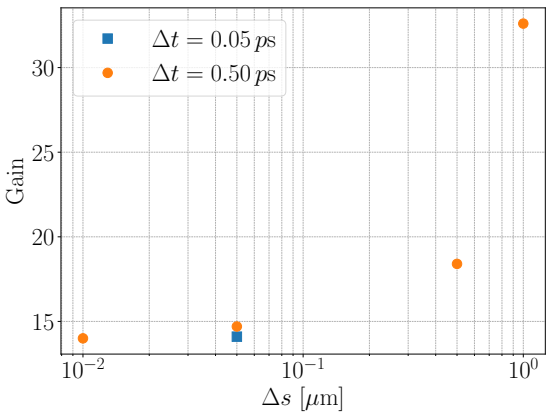


Figure 3.13: Gain as a function of Δs parameter.

Table 3.8: Gain and time resolution dependence from the ionisation model.

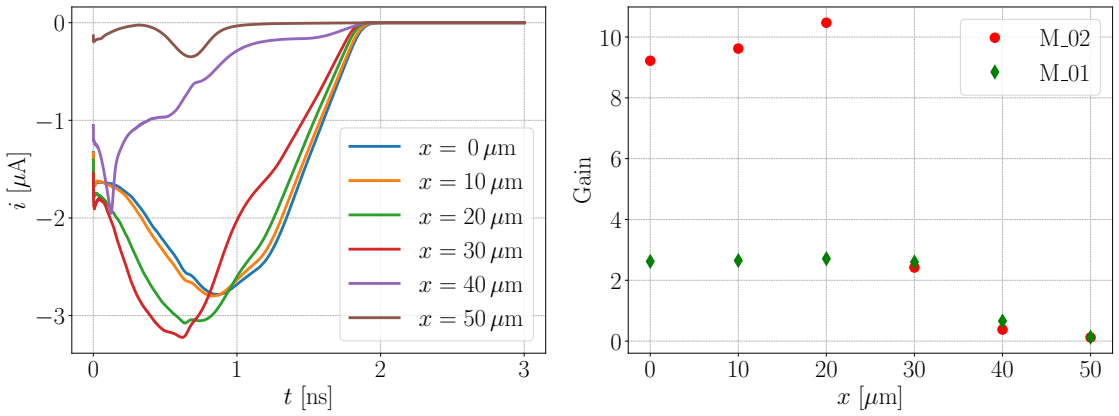
Ionisation model	**Gain**	σ_t[ps]
Okuto and Crowell	43.7	64
van Overstraeten and de Man	14.7	58

are presented in table 3.8. This model was used because the simulation results were more in line with the gain predictions extracted from *Sentaurus* TCAD.

All the previous simulations were performed by impinging a pion in the device centre. By changing the incident position, the gain and signal shape were studied as a function of the distance from the central position. The mean signals generated using M_01 are plotted in Fig. 3.14a, while the gain dependence for M_01 and M_02 is reported in Fig. 3.14b. Signals generated at the pixel borders are faster and higher than the central ones due to a higher electric field. The collection electrode has a dimension of around 60 μm, hence the gain drops after 35 μm from the centre.

Lastly, the time resolution was evaluated. The impinging position was chosen randomly between $-50\,\mu$m and $50\,\mu$m for a dataset of 10000 events. Figure 3.15 shows the time distribution residual, i.e. the Time Of Arrival (TOA), for some CF thresholds considering all the signals induced.

Two peaks are identified: the one corresponding to shorter arrival times is represented by signals without gain, i.e. those that hit the edges. Then, a second



(a) (b)

Figure 3.14: Mean of 1000 events generated using M_01 by shooting a pion at different distances from the device centre (a). Gain as a function of the distance from centre for M_01 and M_02 (b).

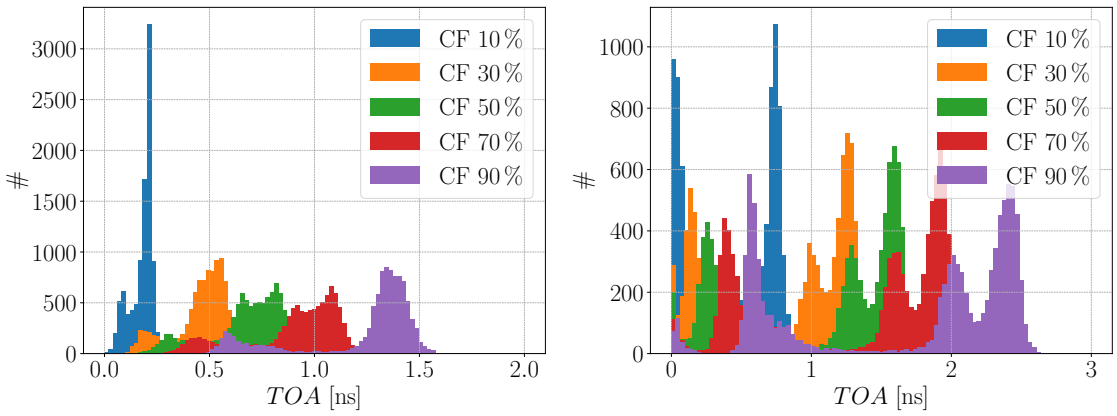
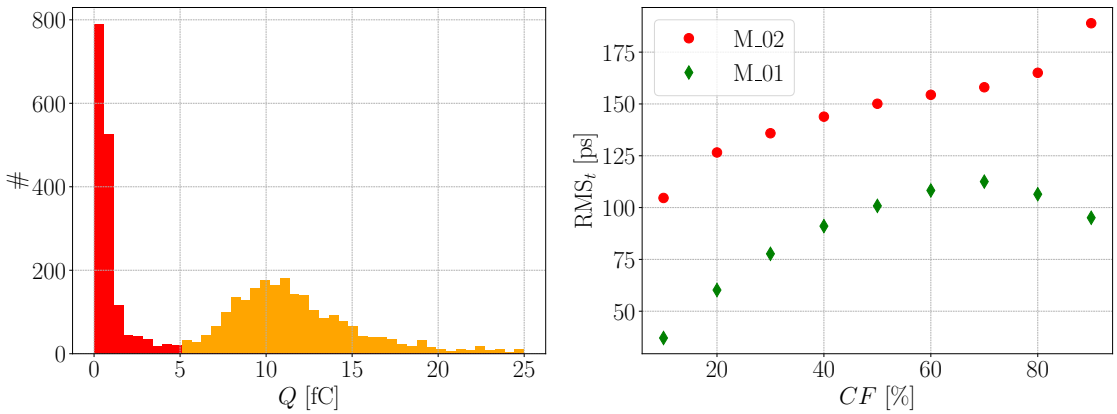


Figure 3.15: TOA distribution for M_01 (a) and M_02 (b) generated by a random pion impinging in range $[-50 < x < 50\,\mu\text{m}]$.

peak at longer arrival times, which, as the CF increases, splits into two components (central and lateral signals) for M_02 (Fig. 3.16b). The first peak was eliminated by separating events experiencing charge multiplication from those without gain, by applying a threshold on the colleted charge (Landau distribution) as shown in Fig. 3.16a. The separation of the second peak is due to the electric field depression under the collection electrode. In M_02 the top voltage is 35 V while in M_01 it is 45 V; these 10 V of difference are responsible for this effect. Indeed, in Fig. 3.17 the distribution of arrival times as a function of the particle incidence position can be observed. The fastest signals are the ones hitting the edges, as shown also in Fig. 3.14a. The same effect can be observed in Fig. 3.11b where the M_02 peak arrives later than the one of M_01. Figure 3.17 also shows that higher CFs imply more delayed TOAs. Furthermore, at larger CFs, the separation between central and lateral arrival times increases. This behaviour is due to the effect of the minimum electric field present under the electrode (Fig. 3.11a) on holes. The holes component is the major contribution to the signal above 0.5 ns where the electrons induced current has run out.

The time resolution as a function of the CF threshold is plotted in Fig. 3.16b. The RMS was chosen instead of the Gaussian σ due to the non-Gaussian behaviour (Fig. 3.15).



(a) (b)

Figure 3.16: Landau distribution generated with the M_02 map (a). In red, the signals that are discarded for time resolution evaluation, in orange, the signals above threshold, i.e. 5.0 fC. In (b), the time resolution as a function of the CF threshold considering only signals with a collected charge higher than 1.5 fC for M_01 and 5.0 fC for M_02.

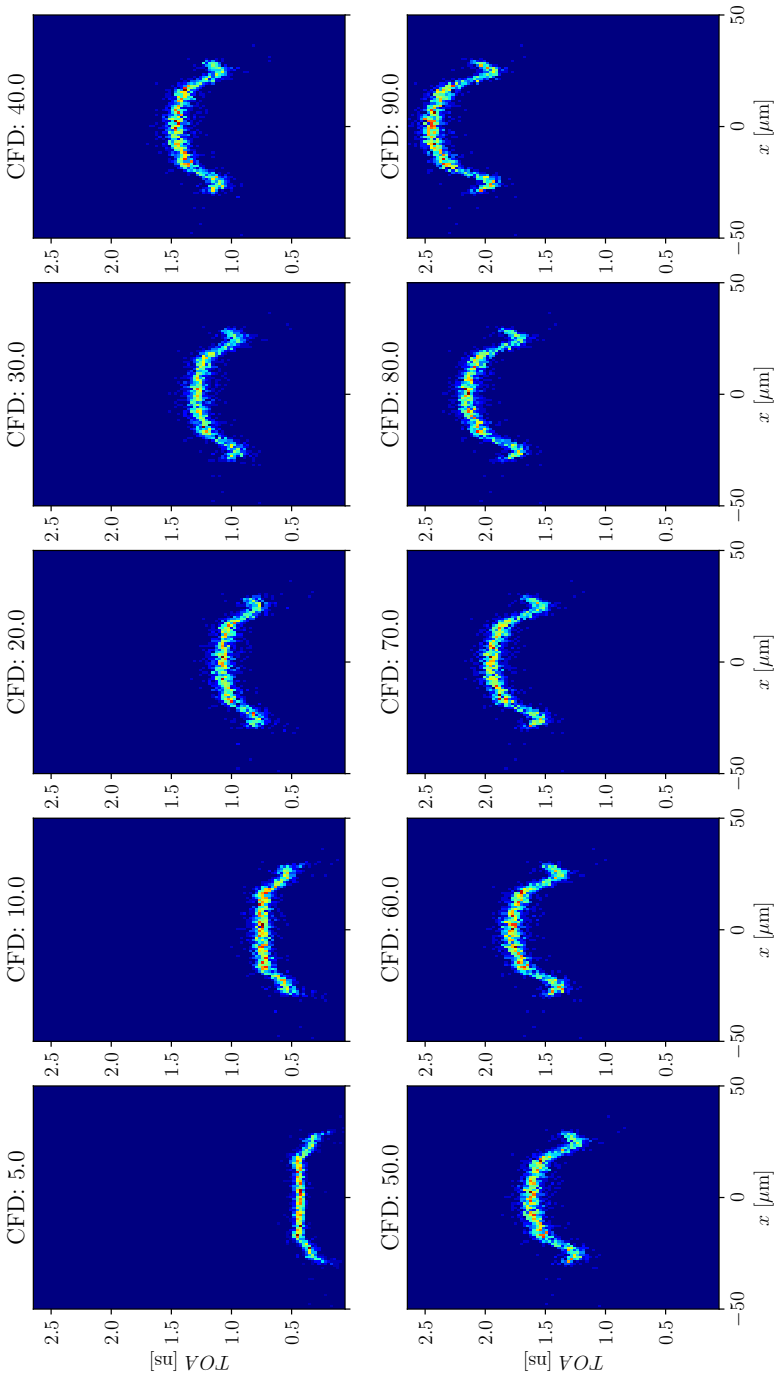


Figure 3.17: TOA as a function of the impinging position for each CF threshold using M_02 map.

3.2.2 ARCADIA *Run 3*

To verify the simulations results (sensor gain and time resolution), the structures of the 3rd ARCADIA run were tested statically, performing Current-Voltage (IV) and Capacitance-Voltage (CV) measurements as described in Chapter 5. The lateral CV profile, i.e. the capacitance between collection electrode voltage biased in range ($0 \rightarrow 20\,\mathrm{V}$) and p^+-contact ($0\,\mathrm{V}$), was used in *Sentaurus* TCAD to verify the gain layer implantation depth and doping concentration. The experimental data showed a shallower gain implant compared to the simulated one. This implied a lower gain, as can be seen in Fig. 3.7. The TCAD simulations were adjusted accordingly to match the measured implantation depth and doping concentration. Only one dose split was studied with MC simulations due to the minimal fluctuations in gain achieved with such a shallow gain layer and doping range.

The voltages applied to the four contacts present in the 2D profile (Fig. 3.10) were chosen by combining the IV performed with TCAD and the measured ones. The collection electrode and substrate contact voltage were the maximum points reached by the TCAD simulations before numerical convergence problems. The guard ring and the p^+-contacts were biased to the experimental voltages. In table 3.9 are summarised the biases applied for the following simulations. The M_13 map had lower substrate and guard ring voltages than the others due to convergence problems.

The average signals computed on a set of 1000 MC events for a particle impinging in the device centre are plotted in Fig. 3.18. Two different models were used, the Okuto (Fig. 3.18a) and the van Overstraeten (Fig. 3.18b), and no significant difference is present between their shapes. From the figure, the hole contribution is evident. Indeed, increasing the top voltage, signals finish faster, and the long tail/second peak is absorbed near the first part of the signal produced by electrons. This effect is due to the minimum of the electric field present beneath the electrode, which is stronger for lower voltages.

Figure 3.19 shows the gain extracted using the two ionisation models as a

Table 3.9: Biases applied in *Sentaurus* TCAD using profiles tuned on the produced structures of ARCADIA *Run 3*.

Contact	**M_10**	**M_11**	**M_12**	**M_13**
Dose split		0%		
Collection electrode	45 V	25 V	35 V	59.5 V
Guard ring	9.5 V	9.5 V	9.5 V	9.0 V
p^+		0 V		
Substrate	−40 V	−40 V	−40 V	−15 V

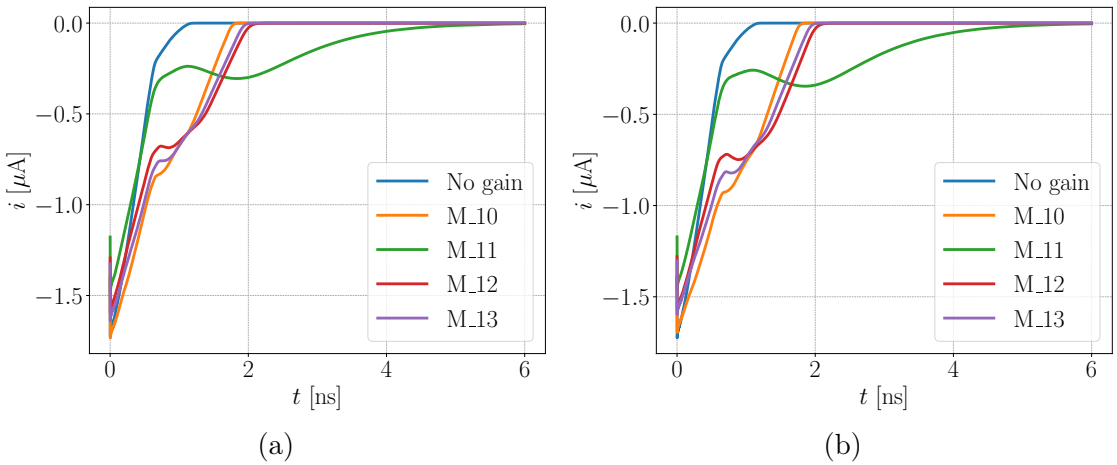


Figure 3.18: Signals generated by a central impinging pion using van Overstraeten (a) and Okuto (b) models.

function of the collection electrode voltage. The gain increase is minimal, around 5 % due to the shallow implantation of the gain layer as predicted in Fig. 3.7, which shows that for near-surface implants, the variation in gain when the electric field increases is negligible. The Okuto model exhibits a slightly higher gain for all applied biases, hence it is more compatible with the experimental results. This behaviour is expected as predicted by Fig. 3.6.

In Fig. 3.19, the gain at $V_{top} = 59.5\,\mathrm{V}$ (M_13) is more similar to the gain at $V_{top} = 35\,\mathrm{V}$ (M_12) than $V_{top} = 45\,\mathrm{V}$ M_10, even though the V_{top} difference is greater. This is due to a lower substrate voltage. If the total difference between V_{top} and V_{back} of the sensor is considered, M_10 has a difference of 85 V, M_13 of

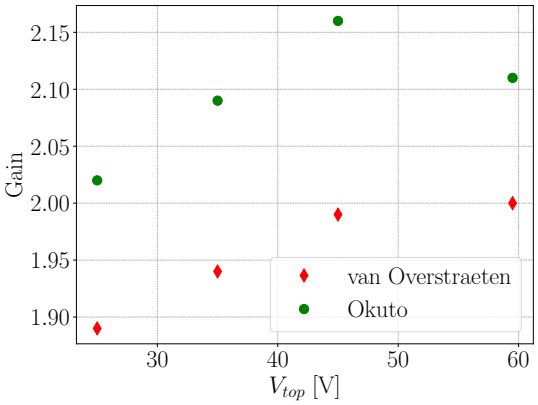
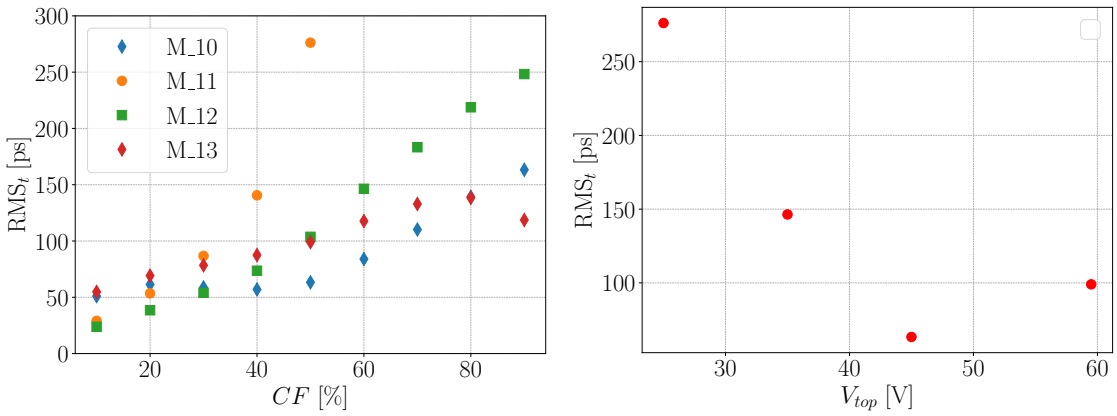


Figure 3.19: Gain as a function of the collection electrode V_{top} extracted with van Overstraeten and Okuto models.



(a) (b)

Figure 3.20: Time resolution as a function of the CF threshold considering only signals with a collected charge greater than 0.5 fC for different collection electrode voltages (a). Time resolution as a function of the bias given at a fixed threshold 50 %(b).

74.9 V and M_12 of 75 V, thus explaining the gain decrease for higher collection electrode voltages.

Then, the time resolution evaluated for a randomly impinging particle was extracted using the Okuto model (Fig. 3.20). Decreasing the bias, the resolution deteriorates significantly due to the electric field *bubble* beneath the collection electrode, which creates greater random fluctuations in arrival times. For low CFs, the time resolution is improving because the fast electron component has greater weight than the slow hole one, which experiences the electric field minimum beneath the collection electrode.

The worsening of time resolution in M_13 (Fig. 3.20) can be explained with the same justification given for the decrease in gain reported in Fig. 3.19. Additionally, M_13 is near breakdown at the pixel border, because the electric field between the pixel guard ring and the collection electrode increases faster than the electric field in the substrate region.

Simulated signals near the guard ring are much faster than the others, and particles crossing the device outside the guard ring induce signals also in the collection electrodes due to the high electric field in that region. These effects were studied in detail with the ARCADIA *Run 3.2* maps presented in the next section.

3.2.3 ARCADIA *Run 3.2*

To increase the intrinsic gain, a short loop was submitted where the foundry used the same mask set of the first production, but with a higher implantation

Table 3.10: Biases applied in *Sentaurus* TCAD using two dose split of p-gain tuned with the produced structures in *Run 3.2*.

Contact	**M_20**	**M_21**	**M_22**	**M_23**	**M_24**	**M_25**
Dose split	0%	0%	0%	0%	0%	−3.3%
Collection electrode	45 V	50 V	55 V	40 V	45 V	45 V
Guard ring	9 V					
p^+	0 V					
Substrate	−25 V	−25 V	−25 V	−40 V	−40 V	−40 V

dose for the $p-$gain layer (Fig. 3.10). After receiving the sensors, the gain profiles were tuned with the produced structures and then studied with *Garfield++* as it was already done for *Run 3*. The maps extracted from *Sentaurus* TCAD and used for simulations are summarised in table 3.10.

In Fig. 3.21a, the signals induced by a pion impinging in the centre are plotted. The same behaviour observed in *Run 3* can be spotted by increasing the collection electrode voltage; signals become much faster due to the disappearance of the electric field depression present beneath the pixel centre. This minimum can be decreased by increasing the collection electrode or the substrate voltages.

Table 3.11 reports for each map the gain values extracted for a particle impinging in the pixel centre.

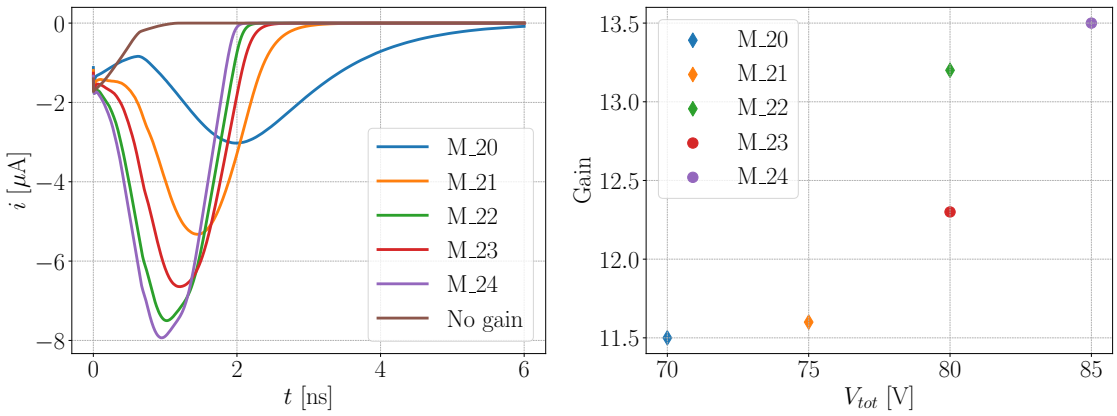
The extracted values show that the gain increases with the top voltage, but also if the substrate bias grows. Indeed, as was previously discussed, the difference between the collection electrode and the backside bias is the driving force for gain.

In Fig. 3.21b, the gain is plotted as a function of $V_{tot} = V_{top} - V_{back}$. For the same V_{tot}, a higher V_{top} implies a greater gain, as can be observed comparing M_22 and M_23. A minimum gain variation between M_20 and M_21 is observed because by increasing V_{top} from 45 V to 55 V, the electric field minimum beneath the collection electrode is removed while the peak responsible for the gain does not change. Indeed, in Fig. 3.21a, the M_20 signal shows a delayed component (holes) with respect to the one generated by M_21.

The time resolution extracted for a random impinging particle on the sensor

Table 3.11: Gain values extracted from Monte Carlo simulations with the doping profiles tuned with *Run 3.2* structures.

Contact	**M_20**	**M_21**	**M_22**	**M_23**	**M_24**	**M_25**
Gain	11.5	11.6	13.2	12.3	13.5	5.2

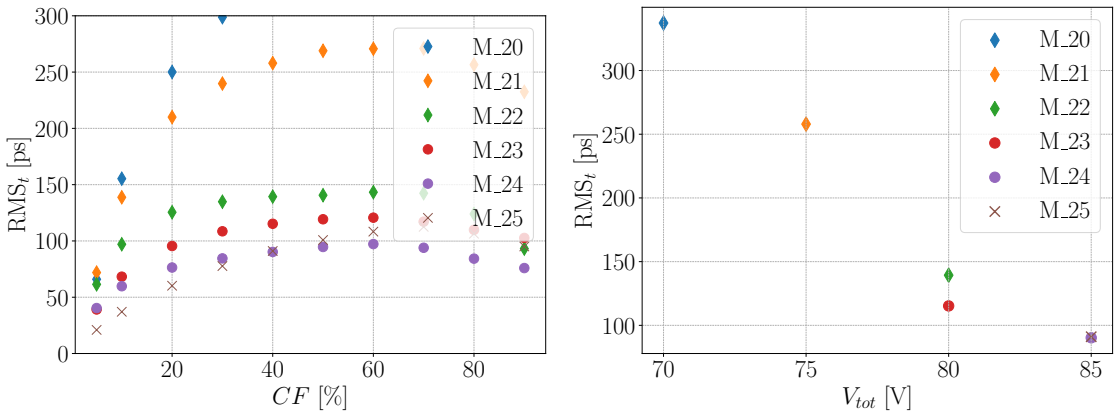


(a) (b)

Figure 3.21: Mean signal generated by a pion impinging in the pixel centre using *Run 3.2* profiles (a). Gain as a function of the difference between electrode and substrate voltages for the reference dose (b). The diamond points are evaluated at $V_{back} = -25\,\text{V}$, while the circle ones at $-40\,\text{V}$.

is plotted in Fig. 3.22a. While in Fig. 3.22b the time resolution at CF 50 % as a function of V_{tot} is plotted.

Due to the signal delay, M_20 displays a poor time resolution. However, by increasing V_{tot} up to 85 V a value below 100 ps was achieved. M_24 and M_25



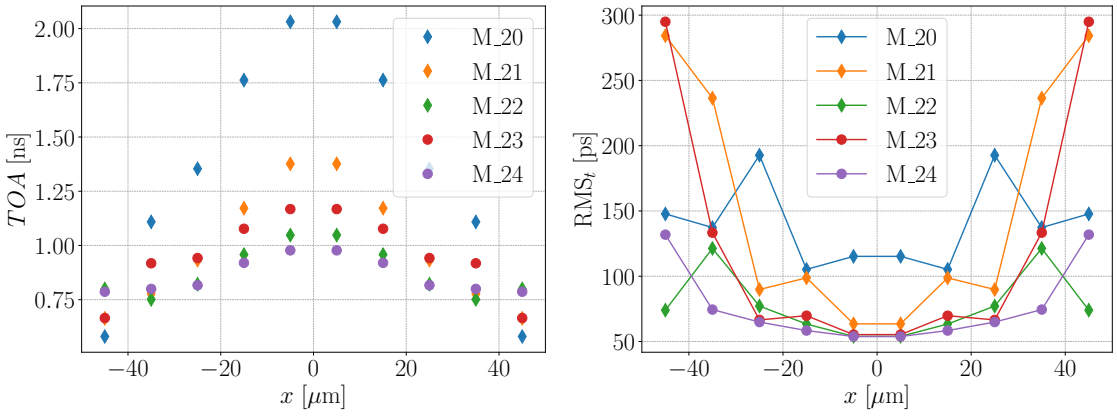
(a) (b)

Figure 3.22: Time resolution as a function of CF (a) and V_{top} for a fixed CF = 50 % (b) extracted for *Run 3.2*. The diamond points are evaluated at $V_{back} = -45\,\text{V}$, while the circle ones at $-25\,\text{V}$. The cross is used for the map with the $-3.3\,\%$ profile.

exhibit comparable performance even if they have different gain layer doses. The gain affects the jitter term, but has no deep impact on the centroid sensor time resolution. Although map M_22 shows a higher gain than map M_24, the time resolution is worse (Fig. 3.22b). Indeed, at equal V_{tot}, the increase in back bias voltage has a greater effect on the electric field depression than the increase in collector electrode voltage. If the Gaussian σ_t is considered in place of the RMS_t, a time resolution of 75 ps was achieved.

To understand which was the main contribution and how the 100 ps could be lowered, the TOA was analysed. This quantity was used to study the electric field inside the device and was extracted experimentally by knowing the particle impingement position in the pixel. Figure 3.23a shows the TOA behaviour inside the pixel for different V_{tot}. Increasing V_{tot}, the TOA spread in the pixel borders is minimised and for M_24 reaches 250 ps. The TOA delay is directly correlated to the minimum of the electric field present beneath the collection electrode.

The in-pixel time resolution was studied (Fig. 3.23b) and from the value at 0 μm the Landau contribution was extracted. M_20 and M_21 show a poor time resolution at 0 μm, while a minimum is reached for the other three maps, around 50 ps (same value extracted using particles impinging only in the centre). This value is in line with the theoretical prevision in [118] where the Landau term is valued to be between 50 ps and 60 ps if the PAI model is used (*Garfield++* default model) and a V_{tot} between 50 V and 100 V is applied. M_23 and M_24 show a time resolution worsening at the border because the carrier velocity is slower. This effect is not present in M_22, where the resolution improves at the edges



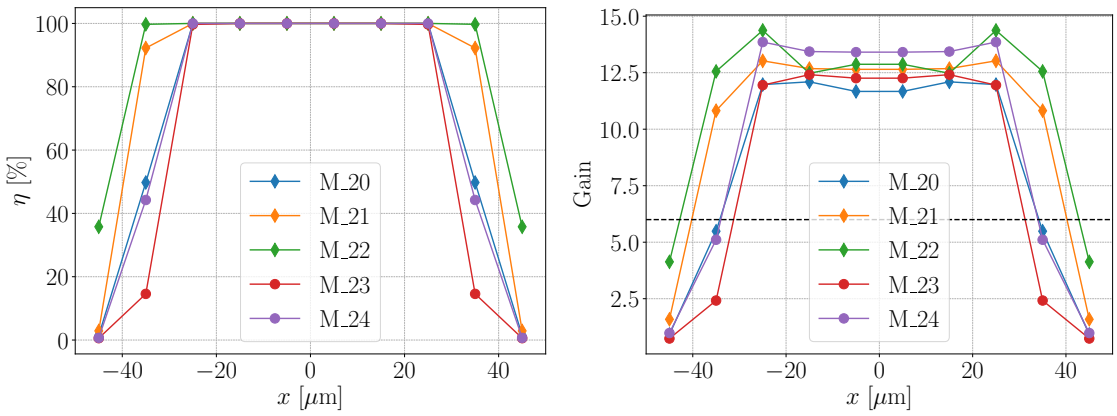
(a) (b)

Figure 3.23: TOA (a) and time resolution (b) for the different maps as a function of the impingement position for dose 0 %. The diamond points are evaluated at $V_{back} = -45$ V, while the circle ones at -25 V.

due to a very high uniform electric field (the collection electrode voltage of M_22 $V_{top} = 55\,\text{V}$ is higher than that of M_24 $V_{top} = 45\,\text{V}$). The 100 ps evaluated for a random particle is the sum in quadrature of the Landau term (50 ps) extracted for a particle impinging in the centre and distortion terms.

Lastly, the efficiency as a function of the position was studied (Fig. 3.24a). A fixed threshold of 3.0 fC (equal to gain 6 in a structure of 48 μm) was used for all the maps with reference dose profile. Below the collection electrode, the efficiency reaches 100 %, while at the pixel border, below the guard ring, is 0 %. Increasing the topside bias, the loss in efficiency below deep p-well is minimised and reaches 100 % in M_22 ($x \simeq \pm 37\,\mu$m). Also below the guard ring, a 40 % efficiency is reached ($x \simeq \pm 45\,\mu$m). From Fig. 3.24a, it can be noted that M_23 and M_24, which have higher V_{tot}, have lower efficiency compared to the other maps.
Indeed, the substrate voltage increases the electric field below the collection electrode, but also the one between the guard ring and the collection electrode, thus recovering the efficiency loss at borders. This behaviour can also be inferred from the study of sensor gain as a function of the impinging position (3.24b). At low collection electrode voltages, the gain is flat. While at higher biases, the maximum gain is between the centre and edge, where the electric field is higher. The substrate bias instead improves gain below the collection electrode.

The total pixel efficiency is summarised in table 3.12. This value is extracted as the ratio between signals higher than the threshold and total number of simulated interactions (with $-50\,\mu\text{m} < x < 50\,\mu\text{m}$). As expected, M_22 has the highest



(a) (b)

Figure 3.24: Efficiency (a) and gain (b) for the different maps as a function of the impingement position for the refernece dose. The diamond points are evaluated at $V_{back} = -45\,\text{V}$, while the circle ones at $-25\,\text{V}$. The dotted black line represents the threshold applied to obtain the efficiency plot.

Table 3.12: Efficiency values extracted from Monte Carlo simulations with the doping profiles tuned for *Run 3.2*.

Contact	**M_20**	**M_21**	**M_22**	**M_23**	**M_24**
Efficiency	69.7%	79.0%	87.9%	63.1%	69.9%

efficiency even if the V_{tot} is not the greatest (M_24) due to the efficiency recovery below the edges.

3.2.4 ARCADIA Next steps

To achieve the 20 ps required by the experiment, simulations were performed to understand the variables that have a greater impact on the time resolution.
A preliminary study on performance was carried out by modifying the pixel pitch. The edge termination was fixed while the collection electrode was stretched. The *Sentaurus* TCAD maps were extracted with the same bias voltages so that the only variable was the pixel pitch.

In table 3.13 are summarised the characteristics of the simulated maps. The *Run 3.2* doping profiles and an active thickness of 48 μm were used.

For these maps, only the random particle impingement position study was performed. The gain value of these maps is summarised in table 3.14, while the mean signals are plotted in Fig. 3.25a. A threshold of 3.0 fC (corresponding to gain 6) was set to discard the events not experiencing multiplication.

M_30 displays a higher gain due to a small pitch, i.e. the edges, where the electric field is higher, have a greater weight; the signal is also faster, as shown previously for signals generated at borders. The signal shapes extracted using M_33, M_34, and M_35 are equal due to a gradual decrease in the edges contribution.

Table 3.13: Biases applied in *Sentaurus* TCAD and pixel pitch using the 0 % dose split tuned with the produced structures of *Run 3.2*.

Contact	**M_30**	**M_31**	**M_32**	**M_33**	**M_34**	**M_35**
Dose split	0%					
Collection electrode	45 V					
Guard ring	8.5 V					
p^+	0 V					
Substrate	−30 V					
Pitch [μm]	50	100	150	250	500	1000

Table 3.14: Gain values extracted from Monte Carlo simulations with the doping profiles tuned for *Run 3.2* but changing pixel pitch.

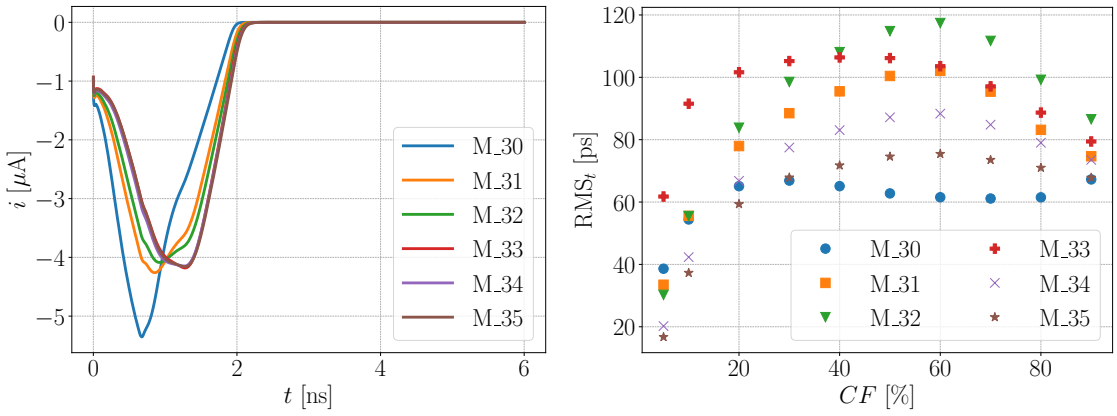
Contact	**M_30**	**M_31**	**M_32**	**M_33**	**M_34**	**M_35**
Gain	11.8	10.9	10.9	10.8	11.0	10.9

The time resolution as a function of the CF is plotted in Fig. 3.25b. The behaviour as a function of the CF is map-dependent due to the different signal shape, as can be seen from Fig. 3.25a. In particular, M_30 shows a maximum time resolution at 30 % CF while the others reach a maximum at 60 %.

Figure 3.26a displays the timing performance evaluated at 50 % CF as a function of the ratio w/l, where w is the pixel pitch while l is the substrate thickness.

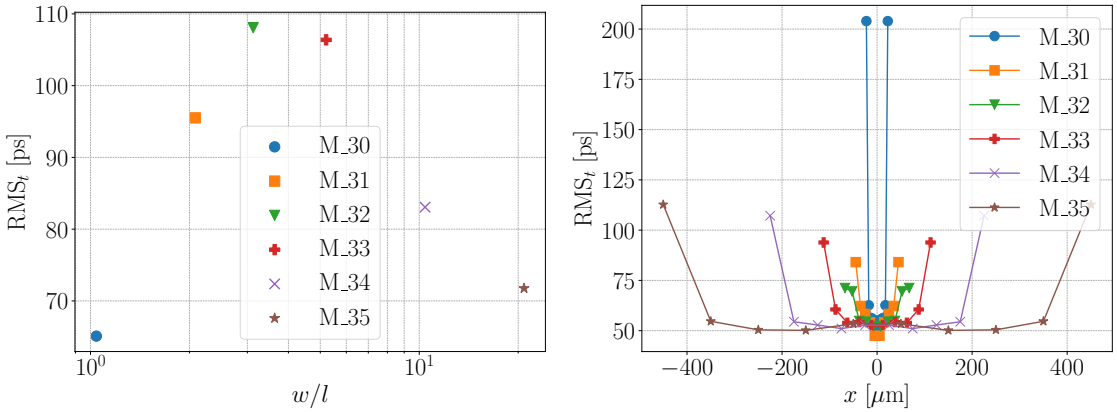
The simulation results follow the predicted behaviour in [118], where the LGAD time resolution dependence on this ratio is analysed. In MC simulations, the worst time resolution was obtained for w/l of 3, as predicted in [118]. Nevertheless, the worst time resolution value differs by a 40 % due to the different applied voltage. In [118], a time resolution of 80 ps is shown with a total voltage of 200 V. In the MC simulations performed on the CMOS LGAD, V_{tot} was only 75 V.

Figure 3.26b shows the time resolution as a function of the particle impingement position for different pixel pitches. The minimum value obtained in the device centre is similar to the one found for the other maps, i.e. Landau contribution, which is independent of the pitch.



(a) (b)

Figure 3.25: Mean signal generated by a pion impinging randomly on the pixel using *Run 3.2* profiles (a) and time resolution as a function of the CF (b) changing the pixel pitch.

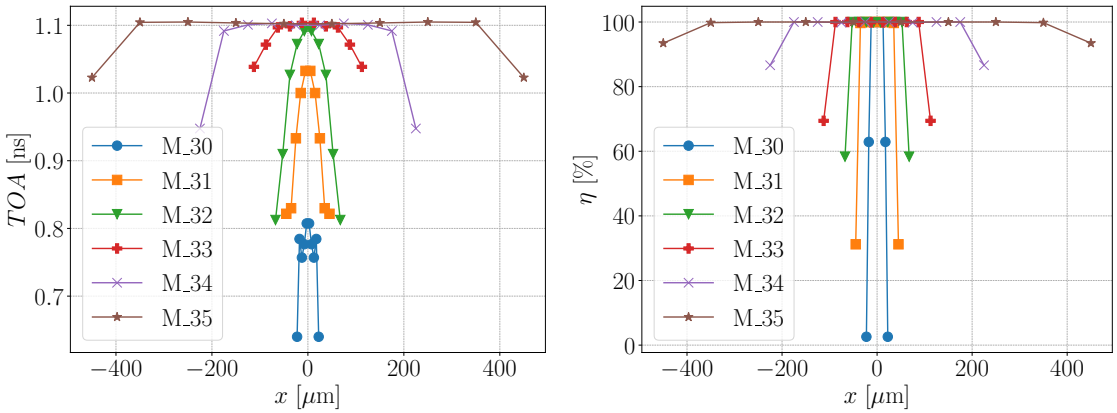


(a) (b)

Figure 3.26: Time resolution evaluated at 50 % CF as a function of the w/l ratio (a) and as a function of the particle impingement position (b). The active thickness l is constant (48 μm), while the pixel pitch changes.

The time of arrival as a function of the impinging position is shown in Fig. 3.27a, while the efficiency is displayed in Fig. 3.27b. M_30, M_31, and M_32 have faster signals due to a higher electric field but with a greater spread. The other maps reach the same central TOA, which is saturated to 1.1 ns.

The efficiency is very low for small pitches due to the prominent effect of edges, and increases with larger pitches. In the plots, each pitch has a fixed number of



(a) (b)

Figure 3.27: TOA evaluated at 50 % CF (a) and efficiency (b) as a function of the particle impingement position for different pitches. Each map is divided into 10 bins to equalise the statistics.

Table 3.15: Efficiency values extracted from Monte Carlo simulations with the doping profiles tuned for *Run 3.2* for different pixel pitches. The threshold was set to 3.0 fC (gain 6).

Contact	**M_30**	**M_31**	**M_32**	**M_33**	**M_34**	**M_35**
Efficiency	73.5%	85.5%	91.3%	93.9%	97.3%	98.7%

bins (10) to maintain the same per-bin statistic.

The total efficiency is reported in table 3.15 as a function of the pixel pitch. Increasing the collection electrode width, the edge contribution becomes negligible and hence the total efficiency increases.

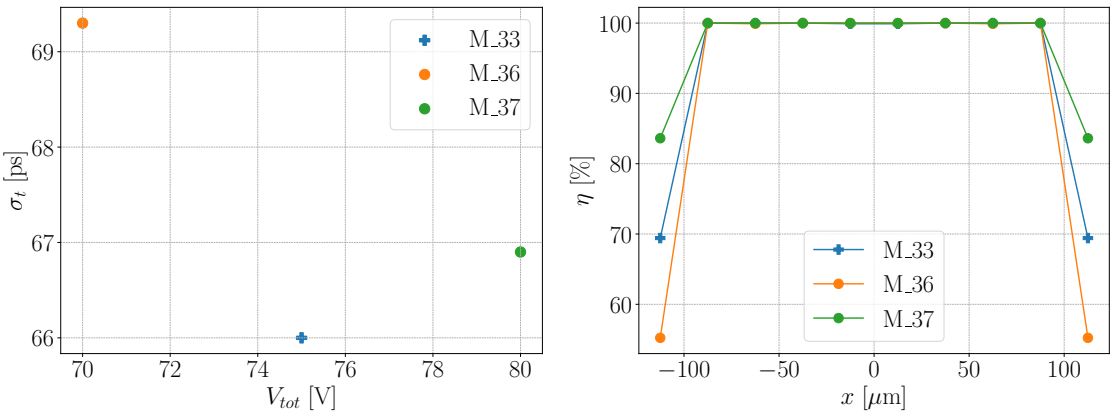
As explained earlier, the time resolution obtained from MC simulations is not compatible with the prediction of [118], mostly for M_32 and M_33. The mismatch is greater for these maps due to a higher distortion term contributing to the total time resolution, and generated by the unsaturated electron drift velocity. Thus, in order to study the distortion term, two additional topside voltages were studied starting from the M_33 pitch, i.e., 40 V (M_36) and 50 V (M_37). The characteristics of these two maps are summarised in table 3.16.

Figure 3.28a shows the time resolution as a function of V_{tot}. In M_37, the time resolution improvement is of $\simeq$ 5 ps compared to M_36 due to the 10 V difference on the collection electrode. In Fig. 3.28a, the standard deviation of the Gaussian fit is reported instead of the RMS_t due to the Gaussian shape of the time difference distributions. Furthermore, the standard deviation allows a direct comparison with the predictions of [118].

The additional effect of the collection electrode bias is reported in Fig. 3.28b, where the detection efficiency is plotted as a function of the in-pixel position. The 10 V difference between M_36 and M_37 increases the efficiency at borders from

Table 3.16: Biases applied in *Sentaurus* TCAD using the reference dose split tuned with the produced structures in *Run 3.2* for a 250 μm pitch.

Contact	**M_36**	**M_37**
Dose split	0%	
Collection electrode	40 V	50 V
Guard ring	8.5 V	
p^+	0 V	
Substrate	−30 V	
Pitch [μm]	250	



(a) (b)

Figure 3.28: Time resolution as a function of V_{tot} for a pixel pitch of 250 μm evaluated as σ_t of the Gaussian fit (a). Efficiency inside the pixel for a pixel pitch of 250 μm changing V_{tot} in (b).

55% to 85%.

The good match obtained between simulations and theoretical prediction of [118] (time resolution dependence on the w/l ratio) is fundamental for future designs, the Landau limit and the distortion term. Indeed, if a time resolution of 20 ps needs to be achieved, the pixel geometry should be optimised and producing different pixel pitches can be very costly and time-consuming. Hence, having a reliable simulation tool is mandatory.

Another important parameter which contributes to the time resolution, as shown in the previous analysis, is the Landau term. This contribution can only be lowered by decreasing the active thickness of the substrate. Simulations with 15 μm were performed, which should be the maximum thickness for which the Landau term is below 20 ps. The bias conditions are reported in table 3.17.

Table 3.17: Biases applied in *Sentaurus* TCAD using the 0 % dose split tuned with the produced structures in *Run 3.2*, but using a 15 μm thick sensor.

Contact	**M_40**
Dose split	0%
Collection electrode	40 V
Guard ring	8.5 V
p^+	0 V
Substrate	−30 V

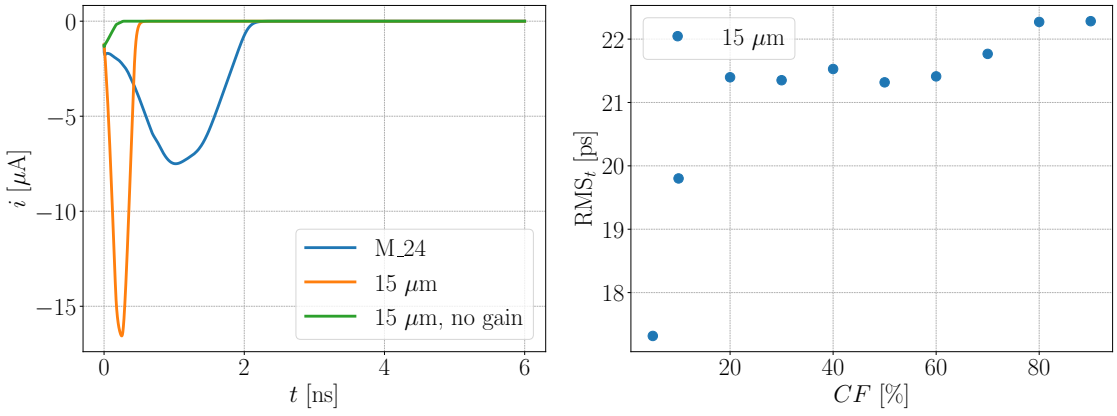
The substrate is biased at a much lower voltage because the punch-through arrives earlier and also because the full depletion of the substrate is achieved with just a few volts.

Figure 3.29a shows the comparison between signals generated in a 48 μm and 15 μm silicon sensors. The charge is collected much faster; however, the signal integral is lower, indeed, the charge deposited in silicon is lower due to the lower thickness. The charge loss can be compensated by increasing the gain; the electric field for a fixed bias condition increases if the electrodes are closer together, i.e. the gain is higher.

The time resolution that can be achieved is shown in Fig. 3.29b. Even if the pixel geometry is not optimised, a resolution of 21 ps was extracted.

In this case, also the distortion term is lowered by thinning the substrate; indeed, for a fixed w, the ratio can be increased by a factor of 3 using 15 μm substrates and designing a pixel of 250 μm ($w/l \approx 17$). For such a value, the distortion term is almost negligible as can be seen from Fig. 3.26a. Indeed, simulations performed considering particles impinging only in the pixel centre showed that the Landau term is $\approxeq$ 19 ps. Hence, the total time resolution worsening due to the distortion term is below 10 %.

Simulations performed on sensors with a 15 μm thick active substrate enables an intrinsic time resolution in the range of a 20 ps due to the reduced carrier drift path and faster charge collection dynamics. Nevertheless, the practical implementation of such thin devices introduces several technological and fabrication-related challenges.



(a) (b)

Figure 3.29: Mean signal (a) and time resolution (b) generated by a pion impinging randomly on the pixel using *Run 3.2* profiles for a thickness of 48 μm and 15 μm.

Achieving uniform thickness across such thin substrates is technologically demanding. Small variations in thickness or dopant concentration can lead to non-uniform electric fields, affecting charge collection efficiency, gain value, and timing response across the sensor matrix.

Furthermore, thinner active layers inherently generate less charge from impinging particles, which can negatively impact the signal-to-noise ratio and worsen electronic jitter unless compensated by increasing the gain layer doping. However, raising the gain above 40 will worsen the sensor's performance as it will introduce additional noise [45].

For these reasons, although very thin substrates appear very attractive from the perspective of timing performance, their practical adoption should be investigated. An additional short loop has been submitted, and the sensors are due to arrive in mid-2026.

As far as mechanical fragility is concerned, there should be no deterioration compared to the current 48 μm sensors, as the substrate wafer onto which the 15 μm active layer is grown will not be thinned. Furthermore, for such thin layers, a backside process is not required.

Chapter 4

Design and simulation of the CMOS LGAD electronics

Monolithic CMOS sensors implement electronics and the sensor active area in the same silicon substrate. The decision on the electronics position is crucial in the early design stages. Indeed, in monolithic sensors, the electronics can be implemented in-pixel or can be placed outside the pixel matrix area. Usually, in monolithic tracking detectors [119, 74, 120, 121, 122, 123], the collection electrode is very small and all around it, the analog and digital logic of the pixel are implemented. This layout brings a 100 % efficiency. However, for timing sensors, the collection electrode needs to be as large as possible to make the weighting field inside the sensor more uniform (see Sec. 3.2). Bigger electrodes mean lower space allocated for the electronics. The solution is then to have some part of the electronics between pixels, and then a large periphery outside the matrices.

The prototype of the CMOS LGAD implemented in a 110 nm CMOS process was thus developed with the idea of a very large collection electrode with some area dedicated to the electronics between pixels.
This chapter describes the electronics developed for the MadPIX ASIC. Section 4.1.1 presents the evaluation of the sensor capacitance, which is determined by the pixel geometry, sensor thickness and pixel layout. Sections 4.1.2, 4.1.3, and 4.1.4 describe the design and simulation of the individual readout channel electronics, while Sections 4.2 and 4.3 present the corresponding layouts and post-layout simulation results. Finally, Section 4.4 provides an overview of the complete MadPIX chip architecture.

4.1 Electronics design and simulations

Due to the monolithic approach, the front-end electronics was tailored to the sensor which was extensively investigated through simulations presented in the previous chapter. Usually, hybrid detectors must satisfy an input capacitance range. However, in monolithic sensors, the capacitance is fixed by the sensor layout, designed at the same time as the electronics. The capacitance and the electronics are coupled and cannot be separated.

4.1.1 Sensor capacitance

The first step was to extract the sensor capacitance using TCAD simulation. The perimeter and area are the main contributors to the total pixel capacitance. The first term depends on the pixel terminations (mainly doping and spacing). Thus, if a certain layout is chosen, the edge capacitance is evaluated as the pixel perimeter multiplied by the lateral capacitance per μm extracted from TCAD. The other contribution, i.e. the one coming from the area, can be evaluated using TCAD, but can also be approximated using the parallel plate geometry.

The perimeter capacitance can be reduced by increasing the distance between the collection electrode and the deep p-well implant. However, this would also reduce the charge-collection efficiency, as shown in Fig. 5.60b. The timing resolution would not be significantly affected, since the signals generated at the borders are not amplified and can therefore be rejected by applying a sufficiently high threshold.

Table 4.1 summarises the area and perimeter capacitance for different pixel pitches. The perimeter value was extracted from TCAD simulations (0.34 fF/μm) while the area capacitance per μm^2 (C_A) was evaluated using Eq. 4.1.

$$C_A = \frac{\epsilon_r \epsilon_0}{d} A \tag{4.1}$$

d is the active thickness (48 μm), A is the area and ϵ_r is the dielectric constant of silicon. The pixels are considered with square geometry.
For pixels larger than 500 μm the area contribution becomes significant, while for smaller pixels, the dominant contribution arises from the perimeter.

Figure 4.1a shows each contribution and the total capacitance for a 48 μm sensor. Figure 4.1b plots the same quantity for a 15 μm thick sensor. For $d = 48\,\mu$m the optimal pitch is 600 μm, while for $d = 15\,\mu$m the best one is 200 μm. Just these two thicknesses were analysed because the 48 μm was the standard wafer active depth in ARCADIA *Run 3*, while 15 μm is the thickness for which the Landau contribution is below 20 ps and also the thickness of the last short loop submitted to the foundry.

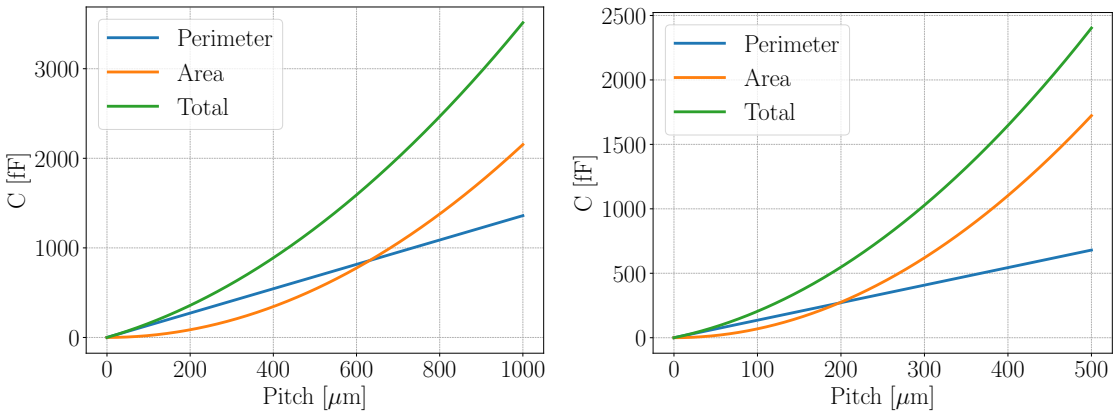
Table 4.1: Predicted sensor capacitance as a function of pixel size with a thickness of 48 μm.

Pixel [μm]	Perimeter [fF]	Area [fF]	Total [fF]
100	136	22	158
150	204	48	252
250	340	135	475
350	476	264	740
500	680	538	1218
750	1020	1211	2231

Initially, the idea was to design a pixel with a 500 μm pitch to have the largest collection electrode possible with the best area-perimeter ratio. However, due to Foundry density rules, the biggest pixel that could be implemented was $250 \times 100\,\mu m^2$ (density rules constraints). This geometry corresponds to a pixel capacitance of 290 fF. In future production, it will be possible to implement larger pixels and from Fig. 4.1b, their capacitance values can be extracted for an active thickness of 15 μm (pitch of 250 μm), which corresponds to $\approx$ 770 fF.

For the electronics simulations, the capacitance values of 290 and 770 fF were used to estimate the jitter component.

Once the sensor capacitance was defined, the signal waveform at the collecting electrode had to be modelled. Based on TCAD simulation outputs, an analytical signal shape was derived and then implemented within the electronics simulation



(a) (b)

Figure 4.1: Total sensor capacitance and main contributions (area and perimeter) for a sensor thickness of 48 μm (a) and 15 μm (b).

framework.

In the electronics simulations, only amplitude variations due to different sensor gain were considered. The time resolution obtained includes only the contribution from electronics jitter (Eq. 1.2), because the effects related to energy deposition fluctuations described by the Landau distribution, as well as distortions arising from non-uniform weighting fields, were neglected. These effects are described in Sec. 3.2 through MC simulations of the sensor part.

The signal parameters were chosen to reproduce the MC results shown in Sec. 3.2.3 and 3.2.4. A rise time $t_r = 1\,\text{ns}$ ($t_r = 0.2\,\text{ns}$), a fall time $t_f = 2\,\text{ns}$ ($t_f = 0.2\,\text{ns}$), and a peak current amplitude ΔI defined as

$$\Delta I = \frac{2n_e q}{t_r + t_f} \tag{4.2}$$

were used for 48 μm (15 μm) thick sensors. Here, q is the elementary charge and n_e is the number of electron-hole pairs generated by a Minimum-Ionising Particle (MIP) crossing silicon, multiplied by the sensor gain. In 48 μm the Landau distribution MPV corresponds to $\approx 0.50\,\text{fC}$, i.e. 3125 electron-hole pairs. In 15 μm, MC simulations predict $\approx 0.137\,\text{fC}$ corresponding to 856 electron-hole pairs. The charge deposited per μm extracted from MC simulations decreases for thicknesses below 30 μm as predicted in [102].

4.1.2 Amplifier

A typical readout chain for timing applications consists of a pre-amplifier, a shaper, a comparator, and a time-to-digital converter (TDC). For this prototype, only a pre-amplifier followed by an analog buffer was implemented. This choice avoids additional timing degradation sources such as time walk introduced by discriminators, quantisation errors associated with TDCs and deterioration due to the CDN.

The collection electrode of the CMOS LGAD needs to be biased by design to a voltage above 45 V to activate the internal gain mechanism. Hence, the input transistor cannot be directly DC-coupled to the sensor. In this 110 nm technology, the electronics is designed using 1.2 V or 3.3 V transistors depending on the function.

The pixel and front-end were AC-coupled, and a bias resistor was used to bias the sensor itself. R_{bias} should be in the order of MΩ to avoid signal splitting between FE and power supply. The coupling capacitor, C_{AC}, plays a crucial role. Indeed, it sustains the potential difference between the FE and collection electrode, but it must also be sufficiently large to minimise voltage division with the parasitic capacitance of the input transistor.

Figure 4.2a shows the gain as a function of $C_{ratio} = C_{AC}/C_i$, where C_i is the parasitic input capacitance. For C_{AC} ten times bigger than C_i, the signal loss is below 10%.

The foundry standard library provides capacitors tested up to 30 V. Nevertheless, the collection electrode can be biased at voltages above this value. Hence, a custom capacitor was designed, and two FE types were implemented. The first (flavour *a*) was implemented with a standard capacitor from the LFoundry library, while the second (flavour *b*) was based on a fully custom layout.

The amplifier architecture adopted for this prototype was inspired by the front-end electronics topology usually used for LGAD sensors [52]. It consists of a cascoded NMOS common-source stage (M0 and M1) with a resistive load R_L. An auxiliary branch composed of transistors M2 and M3 is included to increase the bias current through the input transistor M0 (Fig. 4.2b).

For a common-source amplifier, the voltage gain A_V is given by

$$A_V = -g_{m0} \left(R_L \parallel r_0 \right), \tag{4.3}$$

where g_{m0} is the transconductance of M0 and r_0 is its output resistance, equal to $1/(\lambda I)$. The parameter λ accounts for channel-length modulation. The negative sign reflects the inverting nature of this configuration.

To increase the gain for a fixed load resistance, both g_{m0} and r_0 were maximised. Instead, to improve r_0, M1 was cascoded to significantly enhance the output resistance, increasing it by approximately a factor $g_{m1}r_1$. In parallel, the transconductance was boosted by biasing M0 near weak inversion, improving current efficiency at the cost of a larger device area.

Since the current through the main branch can grow only by changing R_L, the auxiliary branch formed by M2 and M3 was used to increase the current flowing in M0. These transistors act as a cascoded current source.

With this configuration, the amplifier gain can be approximated as

$$A_V \simeq -g_{m0} R_L, \tag{4.4}$$

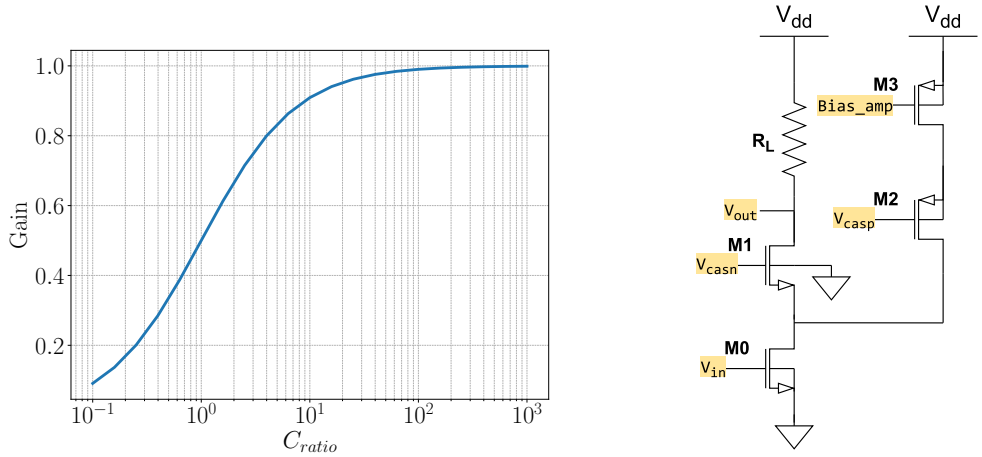
since the effective output resistance of the cascoded stage is much larger than R_L.

The transconductance of M0 can be predicted using the following equation, which is valid in all the regions of operation [124] (weak, moderate and strong inversion):

$$g_m = \frac{I}{n\phi_t} \frac{1}{\sqrt{I_C + 0.5\sqrt{I_C} + 1}}, \tag{4.5}$$

where I is the drain current, n is the slope factor, ϕ_t the thermal voltage, and I_C the inversion coefficient, which is defined in [44] as:

$$I_C = \frac{I}{2n\mu C_{ox}(W/L)\phi_t^2}. \tag{4.6}$$



(a) (b)

Figure 4.2: Gain loss as a function of the ratio between coupling and front-end input parasitic capacitance (a). Amplifier schematic (b).

In the previous equation, μ is the electrons or holes mobility, while C_{ox} is the gate capacitance per unit area.

For timing measurements, the jitter term should be as low as possible. So, in addition to the FE gain, the cut-off frequency of the input transistor was taken into account:

$$f_T = \frac{g_{m0}}{2\pi C_G}, \tag{4.7}$$

In the previous equation, the gate capacitance C_G is defined in [44] as:

$$C_G = \frac{n - (1+x)/3}{n} C_{ox} W L \tag{4.8}$$

with

$$x = \frac{(\sqrt{I_C + 0.25} + 0.5) + 1}{(\sqrt{I_C + 0.25} + 0.5)^2}. \tag{4.9}$$

To maximise slew rate and minimise jitter, both gain and bandwidth were optimised. However, rather than maximising gain and bandwidth without considering the power consumption, the efficiency of transconductance generation was evaluated through the figure of merit introduced in [125] and then substituting Eq. 4.7:

$$\text{FoM} = \frac{g_{m0} f_T}{I} = \frac{g_{m0}^2}{2\pi I C_G} \tag{4.10}$$

given by the product of transconductance (proportional to the gain A_V) and f_T and divided by the current sunk by the input transistor (proportional to the power consumption).

Using the previous equations, the FoM saturates at around 100 of I_C; however, the equations do not account for short-channel and velocity saturation effects. A more detailed analysis is reported in [126], where the figure of merit is maximised for $I_C \approx 3$, corresponding to operation in moderate inversion. In [126] a 80 nm technology was used, which is similar to the technology node used for this prototype.

To evaluate the current needed in the input transistor to achieve a 10 ps jitter (table 1.4), the noise was taken into account. The voltage noise spectral density v_n^2 for a transistor is given by the following expression (thermal noise):

$$v_n^2 = 4k_B T \alpha_w \gamma \frac{1}{g_m} \tag{4.11}$$

where α_w is the excess noise factor and γ is the level of channel inversion [44]:

$$\gamma = \frac{1}{2} + \frac{1}{6}\frac{I_C}{I_C + 1}. \tag{4.12}$$

In addition to the thermal noise of Eq. 4.11, flicker noise also contributes to the total. However, this term was made negligible by increasing the input transistor area. By chosing a W/L of $40\,\mu\text{m}/0.15\,\mu\text{m}$, the flicker contribution was reduced to $\approx 5\,\%$ of the total input transistor noise.

Then, starting from the standard definition (Eq. 1.2) and considering a linear slope, the jitter term was rewritten as

$$\sigma_J \approx \frac{t_d}{SNR} \tag{4.13}$$

where t_d is the total collection time of the signal (that should correspond to the FE peak time) and the SNR is the signal to noise ratio. This last term can be rewritten as:

$$SNR \approx \frac{V_{out,peak}}{\sqrt{\int_0^{1/t_d} |T(\omega)|^2 v_n^2 \omega^2 C_D \,\mathrm{d}\omega}} = \frac{Q_{in}/C_f}{v_n C_D \sqrt{\int_0^{1/t_d} 1/(\omega C_f)^2 \omega^2 \,\mathrm{d}\omega}} = \frac{Q_{in}\sqrt{t_d}}{v_n C_D} \tag{4.14}$$

where the numerator, $V_{out,\text{peak}}$, represents the maximum output signal amplitude, while the denominator corresponds to the output noise. Here, $T(\omega)$ denotes the transfer function of a simple integrator with feedback capacitance C_f, and the term $v_n \omega C_D$ represents the equivalent current noise generated by the input voltage noise v_n through the impedance shunting the amplifier input, namely the detector capacitance C_D. Finally, Q_{in} denotes the collected charge.

Table 4.2: Current needed to achieve a 10 ps jitter for different sensor gains and thicknesses evaluated using Eq. 4.15, 4.11 and 4.5.

Thickness	C_d [fF]	**Gain**	$Q_{\mathbf{in}}$ [fC]	t_d [ns]	σ_J [ps]	g_m [mS]	I [μA]
48 μm	290	10	5.00	3	10	1.04	76
48 μm	290	20	10.0	3	10	0.26	19
15 μm	770	20	2.74	0.8	10	8.17	600
15 μm	770	40	5.48	0.8	10	2.04	149

By combining Eq. 4.13 and 4.14, the jitter error σ_J can be evaluated as:

$$\sigma_J \approx \frac{v_n \sqrt{t_d} C_D}{Q_{in}} \tag{4.15}$$

From Eq. 4.15, v_n was extracted for C_D and t_d evaluated for 48 and 15 μm sensors. Then, from Eq. 4.11, the g_m value was found and finally, from Eq. 4.5, the current needed to achieve 10 ps was extracted.

In table 4.2, the current required to achieve 10 ps jitter is reported for 48 μm and 15 μm for the minimum and maximum gains extracted from MC simulations. 125 μA was the current chosen to be supplied to the input transistor, for which the CAD extracted a $g_m = 2.06$ mS.

The current has been selected to meet the 20 ps specification even with an active sensor thickness of 15 μm ($g_m > 2.04$ mS). Using CAD, a g_m of 2.06 mS was obtained for an input transistor current of 125 μA. This value is very similar to the one reported in table 4.2.

Given I_C and the current, the input transistor aspect ratio was evaluated.
The main amplifier parameters are summarised in Tab. 4.3. With these values, the simulated open-loop gain was approximately 17, while the bandwidth was 667 MHz. In addition, to evaluate timing jitter, a feedback resistor R_{feedback} of 370 kΩ, which allowed for a peaking time compatible with the collection time, was connected between the gate of M0 and the output node.

The performance of the first stage is presented in Fig. 4.3 for the two thicknesses. For the estimated sensor gain and capacitance value of table 4.2, a timing jitter of 10 ps was achieved. However, the jitter strongly depends on the load. The best performance was obtained with a higher detector capacitance and a lower charge due to the faster rise and fall times simulated in 15 μm thick sensors compared to 48 μm as reported at the beginning of this section. The jitter was computed using the standard definition (Eq. 1.2), considering the signal rise time as the time elapsed between 10 % and 90 % of the peak amplitude.

Table 4.3: Main amplifier parameters

R_{feedback}	370 kΩ
R_L	10.4 kΩ
I_{M1}	75 μA
$I_{M2/M3}$	50 μA
I_{M0}	125 μA
V_{dd}	1.2 V

4.1.3 Buffer

The amplifier discussed in the previous section exhibited a relatively high output impedance, mainly determined by the load resistor ($R_L \approx 10\,\text{k}\Omega$). As a result, its performance was strongly affected by the load capacitance. This behaviour is expected since a common-source stage operates as a transconductance rather than an ideal voltage amplifier.

To properly drive the following stage and reduce sensitivity to the load, a buffer was designed to provide impedance matching and a low output resistance.
Two buffer architectures were investigated: an NMOS source follower (SF) and a differential NMOS buffer. The source follower was intrinsically faster and generated less noise due to its simpler structure (Fig. 4.4b), consisting of only two transistors, whereas the differential solution employed five transistors (Fig. 4.4a). Despite these advantages, the source follower was discarded due to its limited dynamic range. It was saturating for signal amplitudes exceeding roughly 250 mV,

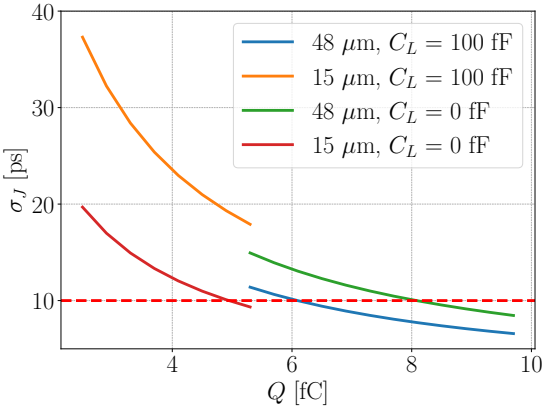


Figure 4.3: Jitter simulated with the capacitance extracted for 48 and 15 μm thick substrates. The orange and blue lines are evaluated with a 100 fF load on the output node.

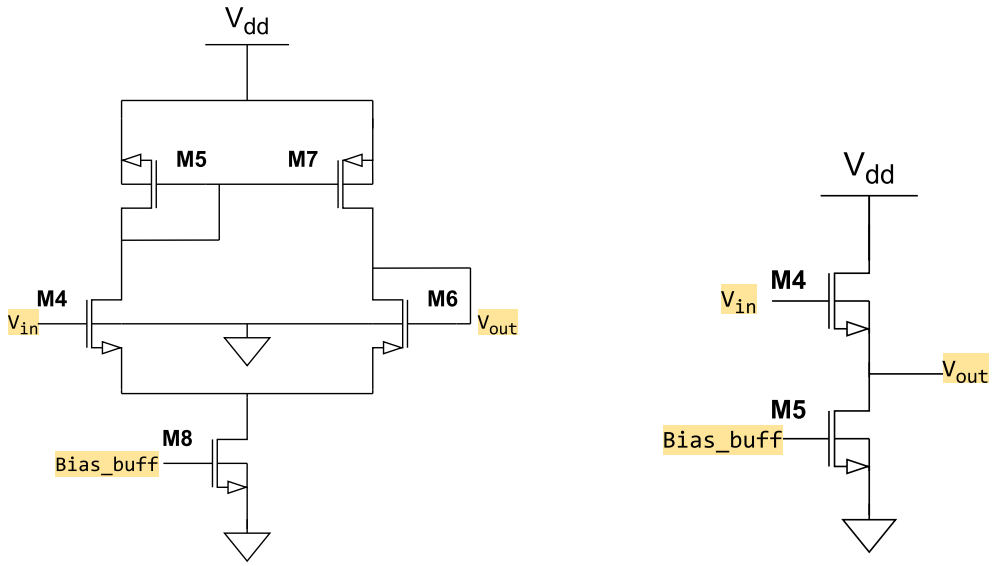


Figure 4.4: Differential amplifier used as a buffer (a) and source follower (b) schematics.

corresponding to a sensor gain of 20 ($\approx 10\,\mathrm{fF}$), resulting in a loss of linearity needed for time-walk correction (Fig. 4.5).

This limitation was mitigated in the differential buffer architecture, where the input and output nodes are maintained at the same potential through negative feedback, which connects the output node to the inverting input (gate of M6). This configuration preserved linearity over a wider range.

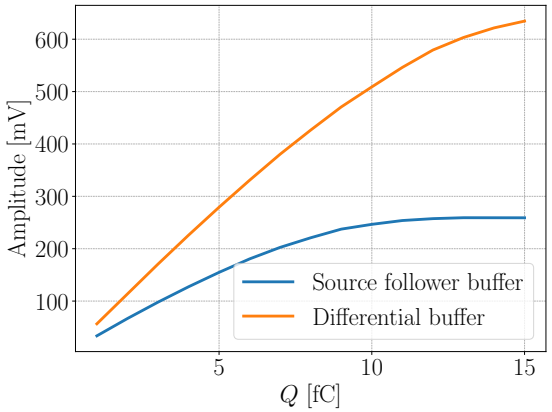


Figure 4.5: Amplitude as a function of the input charge using a source follower (blue) or differential (orange) buffers.

As in the amplifier design, transistor sizing was a critical aspect of the buffer. The transistor pairs M5-M7 and M4-M6 were designed with identical dimensions to ensure symmetry. The first transistor pair acts as a current mirror, evenly splitting the bias current between the two branches. The second pair operates in weak inversion to maximise transconductance efficiency. The lower transistor (M8), which mirrors the bias current of the buffer, was sized to guarantee sufficient drain-source voltage to remain in saturation.

The front-end (FE) architecture implemented in-pixel consisted of the amplifier followed by the differential buffer (Fig. 4.6a).
The open-loop bandwidth of the front-end was estimated using

$$BW = \frac{1}{2\pi R_L C_{GM4}} \tag{4.16}$$

which corresponds to the pole formed by the amplifier load resistance (R_L = 10 kΩ) and the gate capacitance of the buffer input transistor M4 ($C_{GM4} \approx 51$ fF). This yields an expected bandwidth of approximately 310 MHz.

An AC simulation resulted in an open-loop bandwidth of 273 MHz, in good agreement with the analytical prediction. The lower value was attributed to the other parasitic components, which were negligible compared to C_{GM4}. The simulated voltage gain was 16, slightly lower than the amplifier-only. This reduction is due to the finite gain of the buffer, whose closed-loop gain is given by $A_B/(1+A_B)$, where A_B is the buffer open-loop gain.

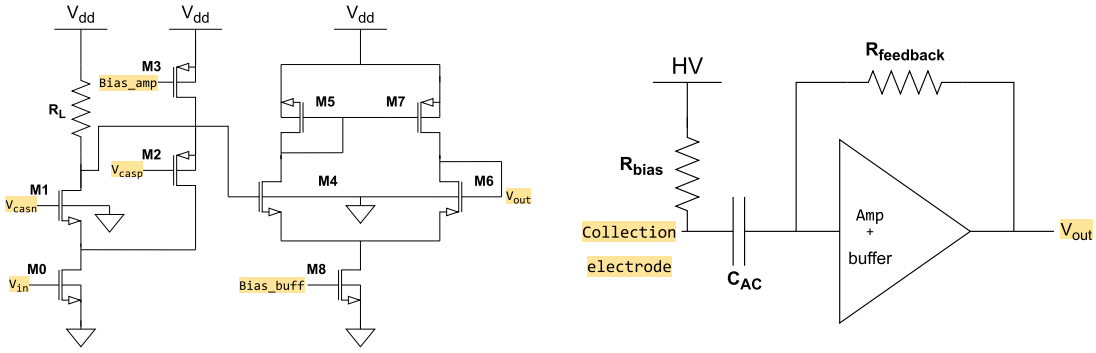
The front-end was closed by a resistive feedback network (370 kΩ) connecting the buffer output to the gate of M0 (Fig. 4.6b). For jitter simulations, a load capacitance of 100 fF was connected to the front-end output to emulate the parasitic input capacitance of the following stage. Table 4.4 reports the bias resistor R_{bias}, the coupling capacitor C_{AC}, and the feedback resistor $R_{feedback}$ values.

Simulations were performed for different bias currents, revealing that the buffer performance stabilised for currents exceeding the nominal design value of 25 μA (Fig. 4.7a).

As expected, the introduction of a buffer significantly reduced the timing jitter compared to the amplifier-only configuration (Fig. 4.7b) in the 48 μm. The bandwidth reduction observed by adding the buffer limited the noise and matched the signal bandwidth, decreasing the jitter. The 15 μm case showed a worsening

Table 4.4: Passive components values of the in pixel circuitry.

R_{bias}	1 MΩ
C_{coupling}	2.06 pF
R_{feedback}	370 kΩ



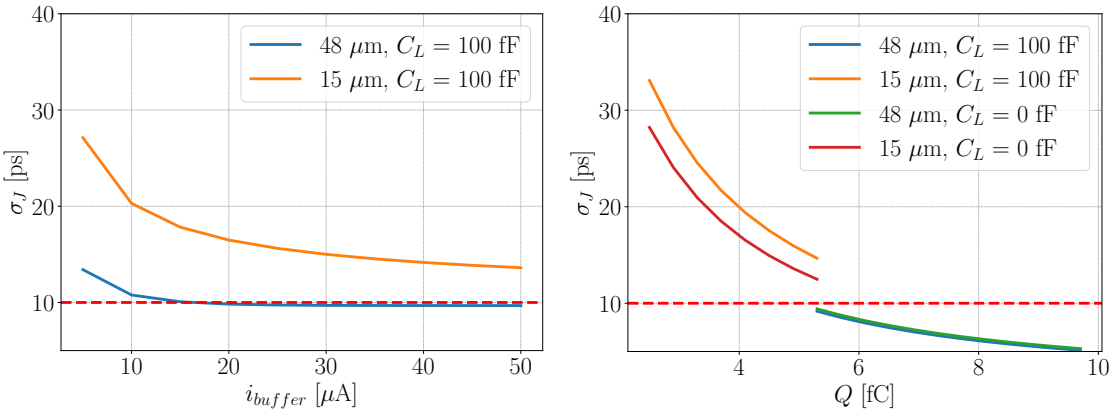
(a) (b)

Figure 4.6: Front end (a) and in pixel (b) circuitry.

in performance because, in this case, the bandwidth reduction did not exploit the 15 μm total signal bandwidth. However, the buffer introduction reduced the load dependence in both 15 and 48 μm. This confirmed that the buffer provides a lower output resistance and was therefore better suited to drive greater capacitive loads.

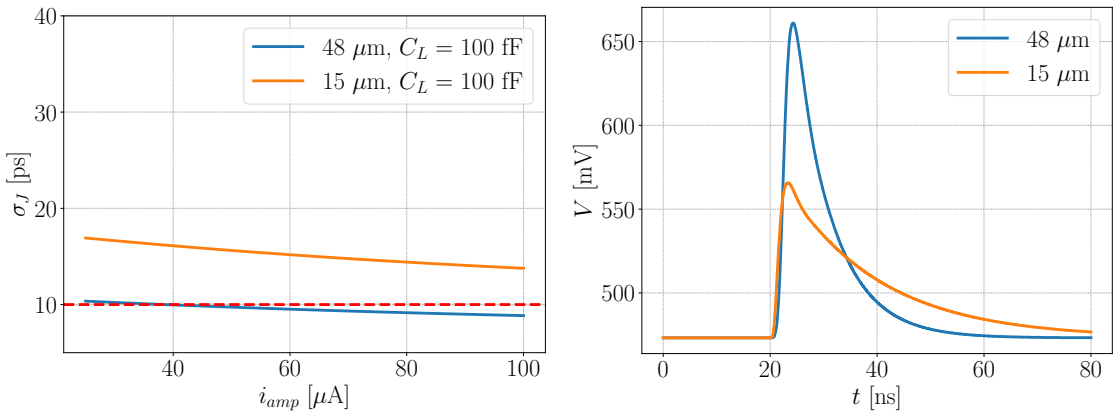
The jitter extracted as a function of the front-end input current injected with the split bias branch is plotted in Fig. 4.8a. The slight improvement was due to a higher g_m of the input transistor. The simulated front-end output waveforms for the two thicknesses are shown in Fig. 4.8b.

The front end was optimised for a 48 μm thick sensor. To obtain a jitter below 10 ps in thinner sensors, the buffer bandwidth must be increased to match the lower collection time. Nevertheless, a jitter below 15 ps was achieved in schematic



(a) (b)

Figure 4.7: Jitter as a function of the buffer current for an injected charge of 5 fC (a) and as a function of the injected charge with a buffer current of 25 μA (b).



(a) (b)

Figure 4.8: Jitter as a function of the amplifier current for an injected charge of 5 fC (a) and front-end output signals (b) with a 100 fF load.

simulations with MadPIX at lower thicknesses if the intrinsic sensor gain is higher than 40.

4.1.4 Output buffer

In order to study the intrinsic performances of the sensor and of the front-end, the full waveform was sent out off-chip using analog buffers. However, the electronics described in the previous section could not drive a capacitance as high as the input impedance of oscilloscopes (at least 1 pF) and PCB transmission lines.

A more robust buffer was designed, working in the 3.3 V domain. Higher bias voltage permits a greater dynamic range even with simpler architectures, such as the source follower topology. The major drawback of changing the power domain was the coupling capacitor needed to link the electronics at 1.2 V (front-end) to 3.3 V transistors, similar to the AC coupling of the FE to the collection electrode. Thus, the source follower input transistor required a biasing net to set its gate in the optimal working region (saturation).

The chosen buffer configuration was a basic NMOS-type source follower to which two additional transistors were added in series, one PMOS connected to 3.3 V and one NMOS linked to ground (Fig. 4.9). These two transistors enable a high output impedance state when the SW_n is low, allowing the same output pad to be shared among different buffers. An inverter was included in the design to control the switch block with a single line.

M0 (3.3 V) and M1 (3.3 V) sizes were designed to work in saturation with a 500 μA current.

The schematic parameters of the 3.3 V buffers are reported in table 4.5, while

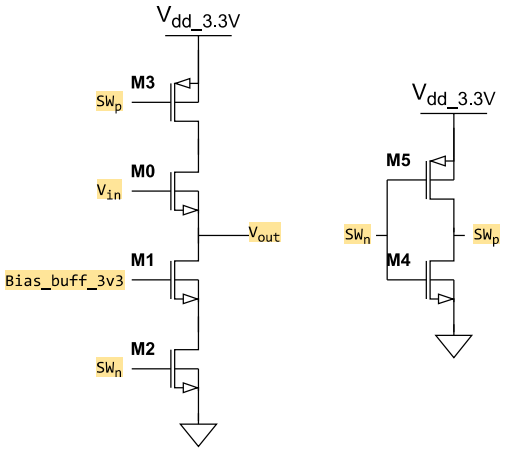


Figure 4.9: Schematic of the output buffer working in the 3.3 V domain. In the picture, the inverter controls the PMOS switch.

Table 4.5: Parameter of the 3.3 V output buffers.

$R_{baseline}$	1.4 MΩ
$C_{coupling}$	1.2 pF
$Baseline_{3.3V}$	1.7 V

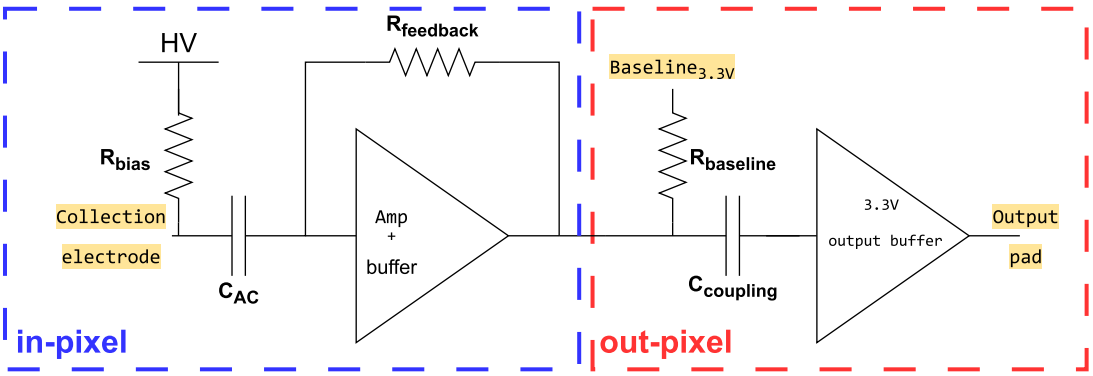


Figure 4.10: Channel architecture of MadPIX.

the channel architecture is shown in Fig. 4.10, where the in-pixel components are separated by the one placed outside it.

The timing performances were extracted with a capacitive load of 1 pF (test board line). A first scan on the FE differential buffer was performed to understand the optimal current required to drive the 3.3 V output buffer. Indeed, M0 gate capacitance of Fig. 4.9 is around 350 fF, while the results obtained in Fig. 4.7a were achieved with a 100 fF load. Figure 4.11a shows that a current higher than 35μA was not improving the jitter anymore, hence for the next simulations 35μA were used.

The jitter trend as a function of the deposited charge is shown in Fig. 4.11b. Its behaviour is very similar to the FE stage, even if a 1 pF capacitor was added to the output node.

An alternative evaluation of the timing performance was carried out using *transient-noise* simulations. In this approach, the noise component generated through a Monte Carlo process was superimposed on the nominal signal waveform shown in Fig. 4.8b. A fixed threshold was then applied, and the variation in the threshold-crossing time was measured. The jitter was defined as the root mean square of this time distribution.

The threshold was set at different fractions of the signal amplitude. For a constant fraction (CF) level of 30%, the resulting timing jitter was consistent with the value obtained from the analytical definition previously presented.

Monte Carlo simulations of process and mismatch were performed. The RMS of

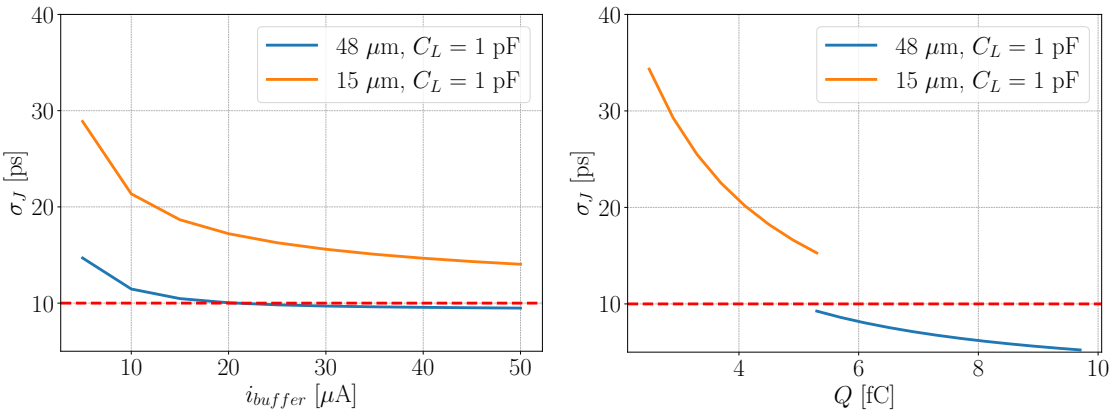


Figure 4.11: Jitter as a function of the FE differential buffer current when the 3.3 V source follower is attached to the front end (a) with an injected charge of 5 fC. Jitter after the 3.3 V output buffer as a function of the deposited charge (b). The load connected to the output buffer is 1 pF for both plots.

all variations (jitter, amplitude, noise and power) were within 10 % of the nominal value.

4.2 Layout

Pixel layout The layout of the final pixel is shown in Fig. 4.12. The white region enclosed by the brown lines (deep p-well) corresponds to the active pixel area. The two 8 μm $\times$ 250 μm strips located at the top and bottom of the pixel host the front-end electronics. The four light-green squares positioned in the centre are the four parallel capacitors corresponding to C_{AC}. The blue square in the middle is the contact element between the first metal and the n^+-collection electrode implant.

Two layouts of the coupling capacitor were implemented and the standard one provided in the foundry library is shown in Fig. 4.12. The other layout (custom) implements a capacitor where the distance between metal lines is doubled to withstand higher voltages (the foundry capacitor is validated up to 30 V). The area covered by this custom capacitor was doubled compared to the standard one in order to maintain the same capacitance value.

To minimise noise pickup, the amplifier was placed as close to the sensor as possible in the layout. It was arranged in a strip measuring 8 μm $\times$ 250 μm, located at the top or bottom of each pixel. In Fig. 4.12, the front-end is in the top right.

The front-end layout was strongly constrained by the limited area allocated to the electronics. The available deep p-well region of 8 μm $\times$ 250 μm between

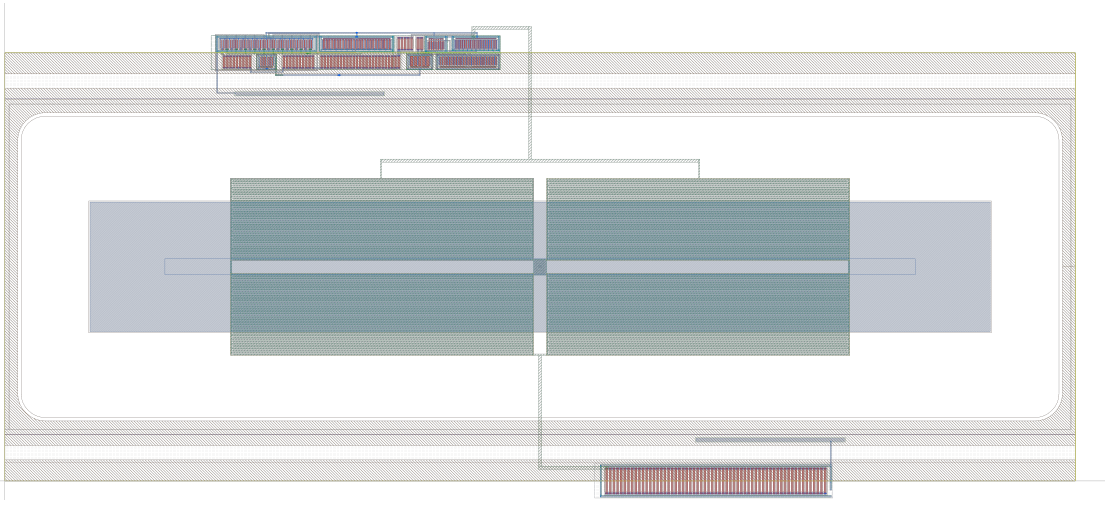


Figure 4.12: Pixel layout of MadPIX.

adjacent pixels was divided into two strips of 4 μm $\times$ 250 μm. The upper strip hosts the NMOS transistors (implemented in a p-well), while the lower strip contains the PMOS devices (implemented in an n-well).

In the bottom right, the biasing resistor, connected to the collection electrode, was manufactured.

A zoom on the front-end is shown in Fig. 4.13 where all the components are divided into blocks. To ensure good matching, the transistor pairs M4/M6 and M5/M7 (differential buffer) were laid out using a matched interdigitated configuration. A transistor with twice the required length was split into an even number of fingers, which were alternately assigned to each device in the sequence *AABBBAABB*. This approach is commonly used when matched devices share a common terminal in a differential architecture.

Output buffer All the elements from the schematic in Fig. 4.9 were placed off-pixel in an area of 100 μm $\times$ 62.5 μm. This layout was chosen to accommodate four 3.3 V buffers in 250μm (pixel length), thus allowing all eight pixels of a column to be connected in two rows of 3.3 V buffers placed exactly above it. The biggest elements were the coupling capacitors and the bias resistors. They fill more than 75 % of the total area allocated for the 3.3 V output buffer.

Matrix layout The pixels were arranged in an 8×8 matrix with the output buffers on top of it inside a guard ring. The matrix layout is shown in Fig. 4.14. The rectangular shape elements above the 8×8 pixels are the coupling capacitor between the front-end electronics and the 3.3 V output buffer. The wide lines crossing the matrix from left to right are the power lines (1.2 V near the front end and 3.3 V on top of the output buffers).

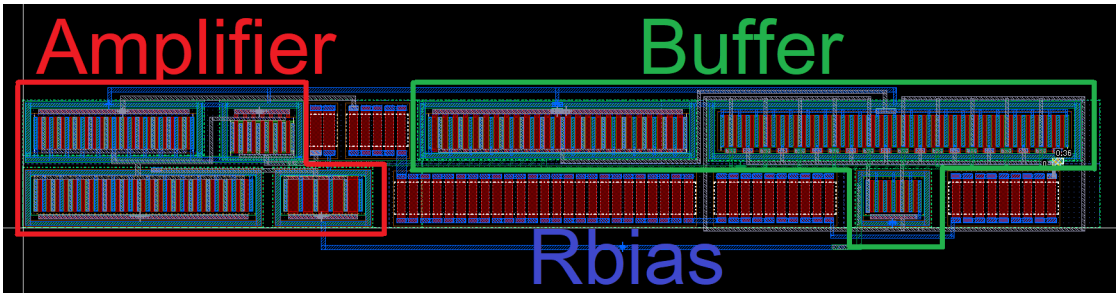


Figure 4.13: Front-end layout of MadPIX.

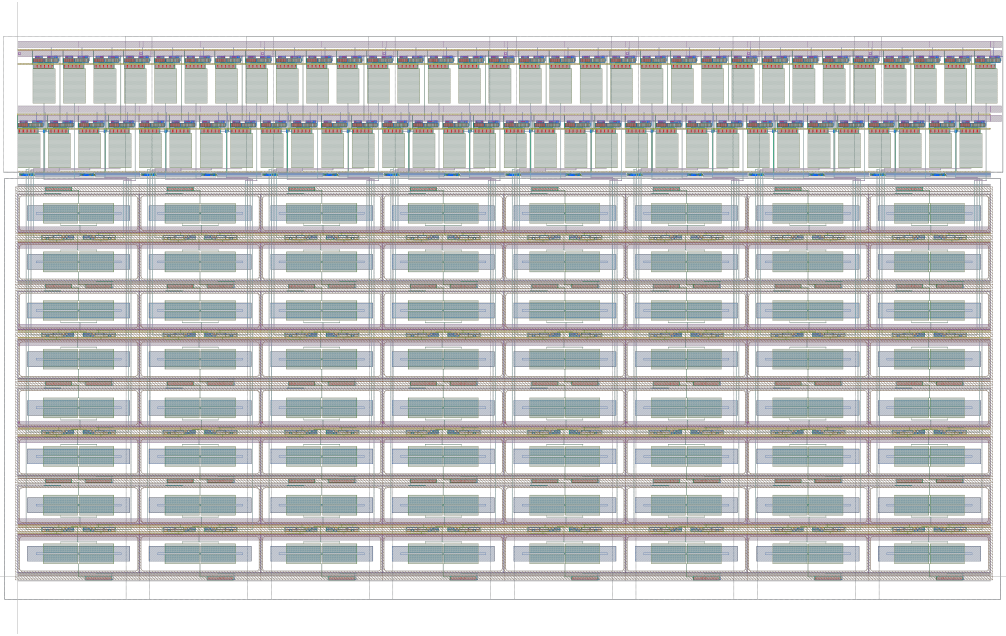


Figure 4.14: Layout of one MadPIX matrix.

4.3 Post-layout simulations

Post-layout simulations were carried out to assess the impact of parasitic capacitances and metal routing resistances, which were not accounted for in schematic-level simulations. As shown in Fig. 4.15a, a performance degradation was observed due to parasitic capacitance induced by connections. This simulation was performed without considering the line connecting the front end to the 3.3 V output buffer. If this connection is considered together with the line from the output buffer to the pad, the 10 ps threshold is no longer satisfied (Fig. 4.15b).

For a sensor gain of 20 with a thickness of 48 μm, a post-layout timing jitter σ_J below 15 ps was achieved (Fig. 4.15b). These results corresponded to a power consumption of 190 μW per channel (760 mW/cm^2).

In table 4.6, the noise and gain simulated after the output buffer, including also the pad line, are summarised. The gain and noise values obtained allow a 10 ps jitter for the 48 μm case. No major worsening was measured between schematic and post-layout simulations.

Post-layout simulations were performed for both capacitor implementations (flavours *a* and *b*), and identical performances were obtained, since both layouts implement the same effective capacitance value. *Flavours 1* and *2* were therefore not treated separately, as they only affect the sensor signal shape and not the

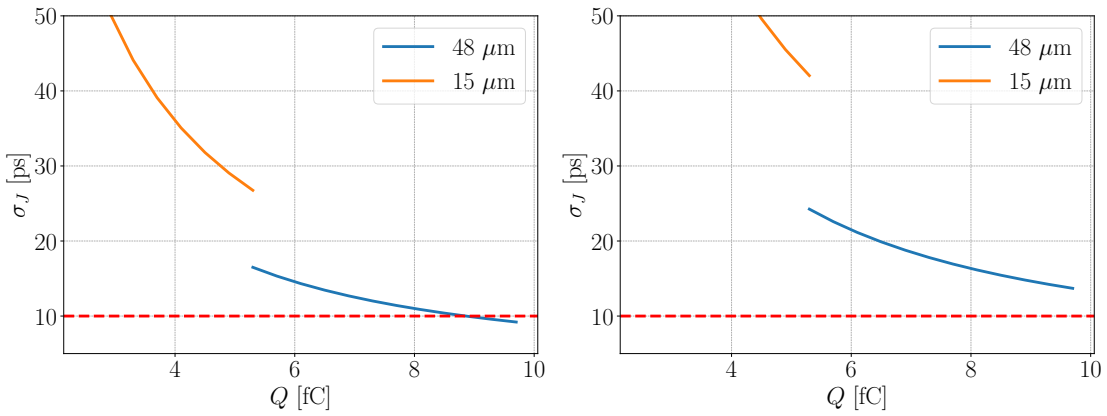


Figure 4.15: Jitter extracted from post-layout simulations without (a) and with (b) connection lines from 3.3 V output buffer to pixel and output pad.

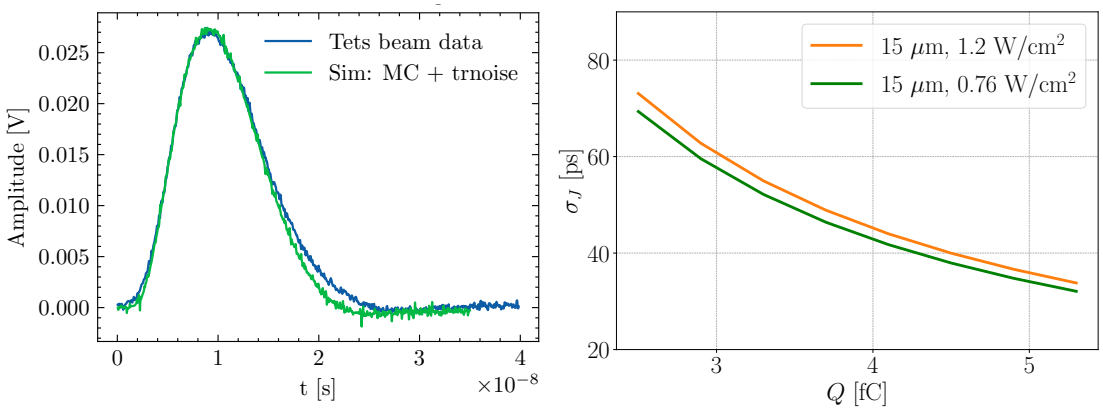
downstream electronics. Dedicated TCAD simulations of the sensor are required to evaluate these differences.

The transient noise simulations of the post-layout circuit required a large amount of physical memory (RAM); it was possible to perform some analysis only on a small dataset of signals. Figure 4.16a shows the MPV of a signal extracted using a transient noise simulation with MC waveforms used as inputs and the one measured for a MadPIX with a gain of ≈ 2.5 tested at CERN PS. The waveforms correspond to ARCADIA *Run 3* that is presented in Sec. 3.2.2 and 5.2. Simulations and data are compatible.

For 48 μm sensors, the time resolution was dominated by the Landau and distortion term; a jitter below 20 ps was enough for studying the intrinsic performances of MadPIX. Instead, the 15 μm sensors will have an intrinsic sensor time resolution of ≈ 20 ps. From Fig. 4.15b, the jitter limit was 40 ps. However, MadPIX front-end bias could be increased to 1.5 V, and a slightly higher current could be injected in the differential buffer. Figure 4.16b shows the jitter extracted

Table 4.6: MadPIX electronics gain and noise evaluated in post-layout simulations for different sensor thicknesses. The noise was extracted using an AC-noise analysis.

Thickness [μm]	48	15
Gain [mV/fC]	21.9	11.2
Noise [mV]	0.52	0.45



(a) (b)

Figure 4.16: Most probable signal extracted from simulation and compared to the one measured at CERN PS with ARCADIA *Run 3* samples (a). In (b), the jitter for a 15 μm sensor after post-layout parasitics extraction associated with two different front-end power consumptions.

with 1.5 V and 310 mW/ch (1.2 W/cm^2). The jitter decreased to < 30 ps for the highest sensor gain, reaching a value comparable to the intrinsic time resolution of the sensor.

Table 4.7 summarises MadPix performance extracted with post-layout simulations.

Table 4.7: MadPIX specifications and post-layout simulation predictions.

	MadPIX	
Technology	LFoundry 110 nm	
Pixel size [μm^2]	100×250	
Thickness [μm]	48	15
Simulated input capacitance [pF]	0.29	0.77
Charge collection time [ns]	≈ 3	≈ 0.8
Sensor gain	$10 \div 20$	$20 \div 40$
Injected charge [fC]	$5 \div 10$	$2.7 \div 5.5$
Power consumption [mW/cm^2]	760	1200
Simulated jitter [ps]	$25 \div 15$	$70 \div 30$

4.4 Top chip implementation

The chip designed is a 16.4 mm × 4.4 mm large MAPS composed of two symmetrical sides: *top* and *bottom*. Each side has 4 matrices (from left to right: *1a*, *2a*, *1b*, *2b*) of 64 pixels divided into 8 rows and 8 columns. The top and bottom pad lines are symmetrical, while the pads designed on the left and right edges are disposed as listed in table B.1. MadPIX top cell is shown in Fig. 4.17. There is no distinction between *top* and *bottom* matrices.

The matrix variants combine the two alternative terminations presented in Sec. 2.3 (1 and 2) with the two coupling capacitor layouts (*a* and *b*). The two halves (right and left) of the chip operate independently, so that if the standard foundry capacitor fails, the other half can still be tested.

Each matrix consists of an 8 × 8 pixel array; however, only 64 output pads are available per chip half. As a consequence, each output line is shared by four pixels, each belonging to a different matrix. The selection of the active pixel is performed through eight enable lines and 3 signals controlling a shift register. The shift register also allows control of the readout of all pixels with just 4 test board channels if the bonding is performed as shown in Fig. 4.18.

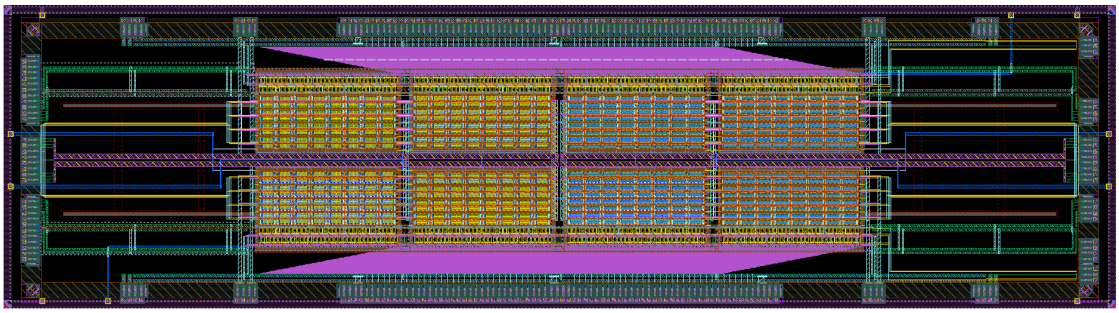


Figure 4.17: MadPIX top cell layout.

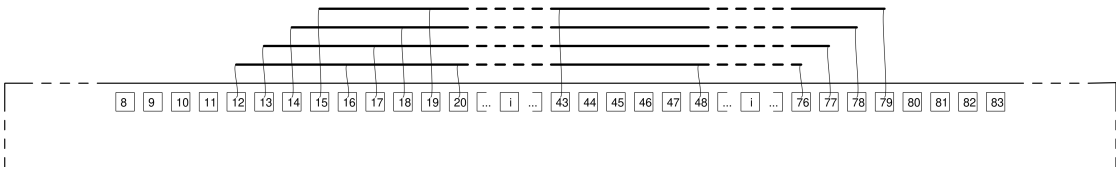


Figure 4.18: MadPIX pads connections to read all the pixels with just four channels implemented on a test board.

Readout In addition to the pixel matrices, the chip integrates a simple digital logic block that supports two different readout modes. The read-out modes are controlled by a set signal, a clock signal, and a start pulse (D_{in}). These signals introduce six input pads, arranged as two groups of three inputs for the top and bottom sections of the chip.

Two different readouts are implemented: *single matrix* or *rolling shutter*. The list of digital signals controlling the readout is:

- *Enable_2b_bot*
- *Enable_1b_bot*
- *Enable_2a_bot*
- *Enable_1a_bot*
- *Enable_2b_top*
- *Enable_1b_top*
- *Enable_2a_top*
- *Enable_1a_top*
- *D_in_bot*
- *D_in_top*
- *Set_in_bot*
- *Set_in_top*
- *Clk_in_bot*
- *Clk_in_top*

They all work in the 1.2 V domain. A 1.2 to 3.3 V converter is present for each 3.3 V output buffer.

Single matrix readout: it is active if a matrix *Enable_iα* is high and the others are low: all pixels of a matrix are linked to the 64 analog outputs, and they can be read out simultaneously. In addition, the digital signals *Clk_in*, *D_in* and *Set_in* need to be low. The timing diagram for single matrix readout is shown in 4.19.

Rolling shutter readout: this mode is active if all the *Enable_iα* are low and the *Set_in* is high, and allows the selection of four *out_buffers* of four pixels in sequence by driving the two transistors enclosing the 3.3 V output buffer.

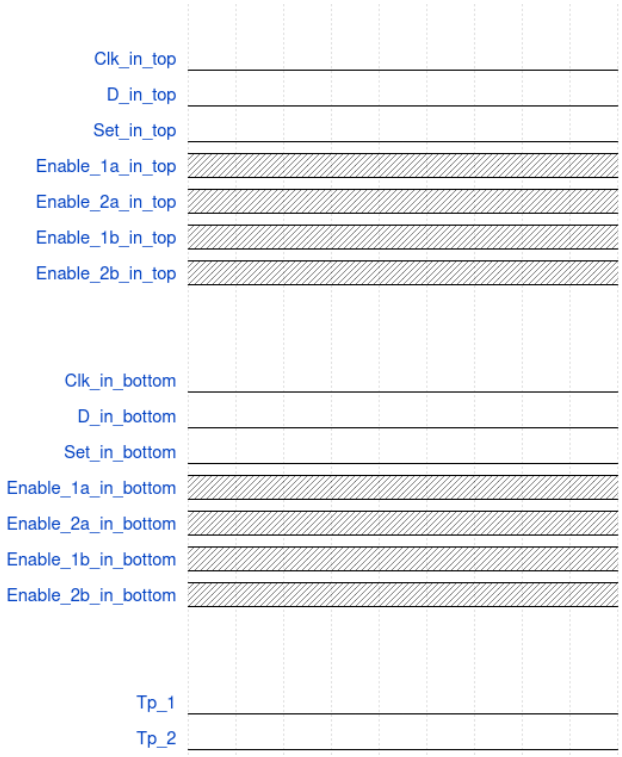


Figure 4.19: MadPIX timing diagram for the full matrix readout.

The control logic is implemented using a chain of flip-flops governed by a set signal that enables or disables their operation (Set_in_top and Set_in_bottom in the pad frame). This chain forms a shift register whose outputs are in logical OR with the matrix enable signals ($Enable\_i\alpha$).

Each flip-flop controls the two enabling transistors of four consecutive output buffers. These four pixels are thus connected to the output pads. For each clock cycle, the shift register activates the next four pixels. The Set_in resets the shift register while the D_in is the signal carried by it. 70 clock cycles allow to read all the pixels in the chip (16 for reading a matrix, 2 between two consecutive matrices). The clock signal and each enable line are distributed across the chip through a network of digital buffers placed approximately every 250 μm to ensure signal integrity.

The rolling-shutter mode is not intended for timing measurements but is useful for characterising the sensor response in test-beam experiments. In this configuration, a clock-driven logic block sequentially enables the 3.3 V buffers of four adjacent pixels within a column. With an appropriate shorting of the 64 output channels on the test board, it becomes possible to read out all 256 pixels on one

side of the chip using only four oscilloscope channels. The output lines need to be shorted together in 4 blocks composed by: Pad<j+0>, Pad<j+1>, Pad<j+2> and Pad<j+3> ($0 < j < 63$). Fig. 4.18 shows in detail how to connect the pads.

The timing diagram for the rolling shutter read-out is shown in Fig. 4.20.

The chip has two implementation of the previously presented readout: *top* and *bottom*. They are equal and can operate indipendently, hence *top* and *bottom* matrices can simulataneusly be readout.

Power In addition to the three high voltage lines (collection electrode, substrate and guard ring), the chip also has the following independent voltage domains:

- 1.2 V for the analog front-end *a* (left side)
- 1.2 V for the analog front-end *b* (right side)
- 1.2 V for the digital top side part
- 1.2 V for the digital bottom side part
- 3.3 V for the top side output buffers
- 3.3 V for the bottom side output buffers
- 1.2 V for the core power (pad frame bias)

Particular attention was devoted to the layout of the power supply lines. To limit the voltage drop, a maximum allowable $\Delta V_{\max}$ of 100 mV was required for each supply path. Based on this constraint, the metal width W and the number of stacked metal layers (n_{metal}) used for the interconnections were determined according to

$$W = \frac{LR_{\square}}{n_{\text{metal}}} \frac{I}{\Delta V_{\max}} \tag{4.17}$$

where $R_{\square}$ denotes the sheet resistivity of the metal layer (a fixed process parameter), L is the length of the rail, and I is the current flowing through it.
Each matrix is enclosed by guard rings, which are powered at 9 V, and all the previous voltages are set through Ext_[0,10] pads catalogued in Tab. B.1.

Bias cells There are four bias cells (*Bias_ buffer*, *Bias_ amp*, *Bias_ buffer_ 3v3*, and *Bias_ conv_ 3v3*) and four voltage levels that can be adjusted through the chip output pads (left and right sides of the pad frame). A brief description of each bias follows:

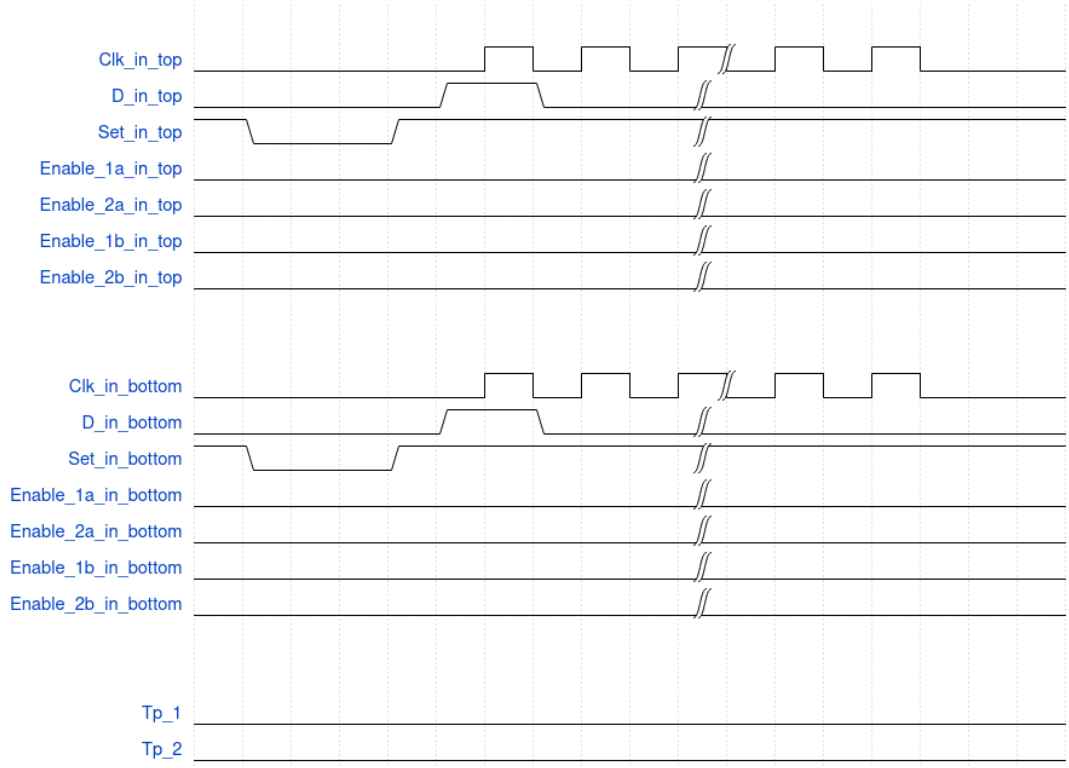


Figure 4.20: MadPIX timing diagram for the rolling shutter readout.

- *Bias_hv*: voltage required to increase the gain. It is common to all pixels in a matrix, and it is shared between matrices with the same sensor layout (up to 70 V).
- *Bias_amp_casn*: gate voltage of the NMOS cascode. It is shared by all matrices with the same coupling capacitor (0.85 V).
- *Bias_amp_casp*: gate voltage of the PMOS cascode used to better mirror the bias current of the amplifier, it is shared by all matrices with the same coupling capacitor (0 V).
- *Bias_amp*: M3 is linked to a P-type current mirror, it is shared by all matrices with the same coupling capacitor (50 μA).
- *Bias_buffer*: M8 is linked to an N-type current mirror. It is shared by all matrices with the same coupling capacitor (25 μA).
- *Bias_buffer_3v3*: NMOS current mirror, it is separated between the top and bottom matrices

- *Baseline_buffer_3v3*: voltage that sets the input voltage of the output buffer
- *Bias_conv_3v3*: PMOS current mirror, it is separated between the top and bottom matrices and converts 1.2 V controlling signals to 3.3 V logic

The current biases for the front-end amplifier and the FE buffer are defined by two dedicated current mirror cells, one associated with flavour *a* and the other with flavour *b*. These cells are located at the two ends of the chip. The 3.3 V output buffer and the 3.3 V level converter are biased by two separate cells placed on the right side of the chip, one serving the top section and the other the bottom section.

To ensure accurate current mirroring, the transistors used in these bias cells are designed with the same dimensions and layout as their counterparts within the pixel matrices. This approach guarantees symmetry between the reference currents applied at the bias pads and the mirrored currents distributed throughout the front-end electronics.

The node voltages at the bias pads are summarised in Tab. 4.8. These values are extrapolated through a top-cell simulation. The maximum and minimum represent the voltages in the maximum and minimum current conditions.
These values are needed to evaluate the off-chip resistors, which are connected to each pad to supply the desired current.

Pad frame In table B.1, all the pads and their functions are listed.

The placement of pads is shown in Fig. 4.21 where the power domains pads are underlined with colours.

MadPIX features 240 input/output pads. The pad frame is arranged symmetrically along the top and bottom sides, each hosting 92 pads, comprising 28 power pads and 64 output pads. The remaining pads are distributed along the vertical sides, with 30 pads on the left and 26 on the right. A detailed summary of pad functionality is provided in Appendix B, where all the pads are listed in a table.

Table 4.8: Voltage values simulated in each bias current pad for maximum and minimum currents

Bias	**Min**	**Max**
Bias_amp	10 μA - 0.71 V	200 μA - 0.13 V
Bias_buffer	25 μA - 0.38 V	75 μA - 0.45 V
Bias_buffer_3v3	250 μA - 0.85 V	1500 μA - 1.69 V
Bias_conv_3v3	1 μA - 2.15 V	5 μA - 1.48 V

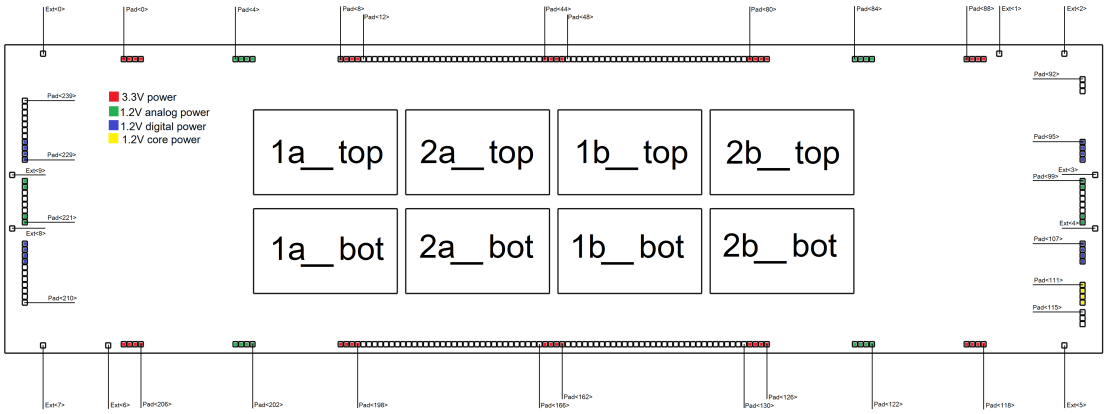


Figure 4.21: MadPIX pad frame with the power pads highlighted with different colours. This block diagram can be compared with the full chip layout of Fig. 4.17.

The 3.3 V supply domain has a higher number of pads compared to the 1.2 V domain. This choice was motivated by the fact that all 64 pixels within a matrix can be simultaneously enabled, leading to a total current consumption of approximately 32 mA. Using a single supply line in this scenario would result in significant resistive voltage drops between the pad frame and the pixel matrices.

The left side of the pad frame contains 30 pads dedicated to enable signals, digital control lines, front-end bias voltages for flavour *a*, and both digital and analog power supplies.

Conversely, the right side of the chip includes 26 pads that provide front-end biasing for flavour *b*, digital and analog power supply connections, biasing for the 3.3 V output buffers, and the supply for the pad frame itself.

To maximise the bandwidth, radio-frequency pads supplied by the foundry were employed. Furthermore, whenever different voltage domains coexist within the pad frame (analog 1.2 V, digital 1.2 V, and analog 3.3 V), isolation breakers were included to prevent unwanted coupling.

Finally, ten fully custom pads were placed outside the standard pad frame to supply high-voltage and guard-ring biasing. These include four pads for the in-pixel high-voltage bias, two pads for the matrix guard rings, and four pads for backside substrate biasing.

Chapter 5

Characterisation results of the CMOS LGAD

This chapter describes the CMOS LGAD setup used for the characterisation campaign and the results obtained so far. After the production and dicing of the MadPIX ASIC, the chip was bonded to a custom test board as described in Sec. 5.1.1. Then, a first characterisation of the electronics and sensor was performed for both productions (ARCADIA *Run 3* and *3.2*), using the setup described in Sec. 5.1, and the results are reported in Sec. 5.2 and 5.3.

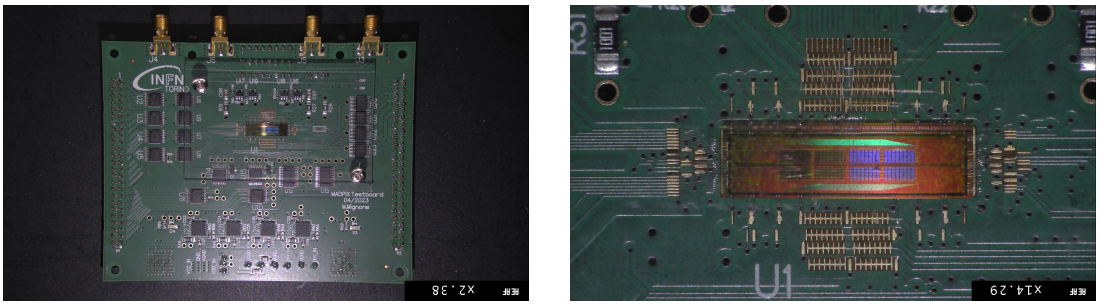
5.1 Test framework

The PCB specifications were forced by the test setup. As described in Sec. 4.4, the ASIC has 64 analog outputs; however, the readout was performed with an oscilloscope, hence only 4 channels can be simultaneously read. In this section, the test board designed to test MadPIX and the setup used in CERN and DESY beam tests is described.

5.1.1 Test board

The MadPIX Test Board (TB) was designed at INFN Torino to read the ASIC. It was designed to interface MadPIX with an FPGA through two IDC50 connectors and with an oscilloscope through 4 SMA connectors. The front of the TB and a zoom on the bonded sensor are depicted in Fig. 5.1.

Test Board power domains As described in Sec. 4.4, the chip has seven separate power domains. Four Low Drop Out regulator (TPS74301RGW) are used to separate the 1.2 V digital, 1.2 V analog, 1.2 V pad frame and 3.3 V ASIC



(a) (b)

Figure 5.1: Test board photo (a): 4 SMA connectors are soldered in the top part, two IDC50 are placed right and left of the TB. Zoom on the wire bonded ASIC (b).

domains. They all have the possibility of adjusting the output voltage (fine-tuning) through a manual potentiometer up to 1.5 V for 1.2 V and 3.7 V for 3.3 V biases. Two other LDOs are used to power all the TB Integrated Circuits (ICs), one for analog buffers and the other for Low-Voltage Differential Signalling (LVDS) buffers. The LDOs are powered by two separate lines (digital/analog) connected to an external power supply at 4.5 V. The power lines biasing the ASIC electronics are:

- V_{DDA}: ASIC analog power domain (1.2 V)
- V_{DDA1}: ASIC analog power domain (3.3 V)
- V_{CC}: ASIC digital power domain (1.2 V)

In addition to the low-voltage channels, the test board has four inputs for the HV. Two separated lines for the collection electrode bias are needed to separate matrices with custom capacitance from those with standard library capacitance. In this way, if the foundry capacitance breaks due to the high voltage applied, the other can be biased without problems. The HV bias names are:

- V_{gr}: Guard ring bias ($\simeq 9$ V)
- HV_1: Collection electrode bias of flavour a matrices ($45 \div 75$ V)
- HV_2: Collection electrode bias of flavour b matrices ($45 \div 75$ V)
- HV_{back}: Substrate bias ($15 \div 40$ V) which can be supplied from the substrate contact or from the dedicated ASIC pads

Test Board biases The test board supplies the chip with voltages and currents necessary for the electronics to operate at the correct working point.

Two Digital-to-Analog Converters (DAC) ICs are present on the TB (AD5684). Each one has 4 channels with 12-bit resolution. The output range is set to $0 \div 1.2\,\mathrm{V}$ for the first one and $0 \div 2.4\,\mathrm{V}$ for the second one. Ranges are assigned to the ASIC inputs as follows:

- *Bias_amp_casn_a*: $0 \div 1.2\,\mathrm{V}$
- *Bias_amp_casp_a*: $0 \div 1.2\,\mathrm{V}$
- *Bias_amp_casn_b*: $0 \div 1.2\,\mathrm{V}$
- *Bias_amp_casp_b*: $0 \div 1.2\,\mathrm{V}$
- *Baseline_buffer_3v3_top*: $0 \div 2.4\,\mathrm{V}$
- *Baseline_buffer_3v3_bot*: $0 \div 2.4\,\mathrm{V}$
- *Disc_level_A*: $0 \div 2.4\,\mathrm{V}$
- *Disc_level_B*: $0 \div 2.4\,\mathrm{V}$

Additionally, to bias voltages required by the MadPIX ASIC, two voltage levels, *Disc_level_A* and *Disc_level_B*, are needed as threshold voltage for four discriminators placed on the test board.

Two digital potentiometers ICs control the bias currents (AD8403ARUZ100 and AD8403ARUZ10). They are both 4 channels potentiometers, each channel is connected to 1.2 V, 3.3 V or ground depending on the transistor type in the ASIC (1.2 V/3.3 V, PMOS/NMOS). The current ranges that each channel can supply are:

- *Bias_amp_a*: $10 \div 200\,\mu\mathrm{A}$
- *Bias_amp_b*: $10 \div 200\,\mu\mathrm{A}$
- *Bias_buffer_a*: $25 \div 75\,\mu\mathrm{A}$
- *Bias_buffer_b*: $25 \div 75\,\mu\mathrm{A}$
- *Bias_buffer_3v3_top*: $250 \div 1500\,\mu\mathrm{A}$
- *Bias_buffer_3v3_bot*: $250 \div 1500\,\mu\mathrm{A}$
- *Bias_conv_3v3_top*: $1 \div 5\,\mu\mathrm{A}$

- *Bias_conv_3v3_bot*: $1 \div 5\,\mu$A

The input transistor types are summarised in Sec. 4.4 and establish the ground connection (PMOS) and or to the 1.2 V/3.3 V (NMOS). 100 kΩ digital potentiometers (AD8403ARUZ100) are used for the *Bias_conv_3v3* and for the *Bias_amp*, while 10 kΩ potentiometers (AD8403ARUZ10) are adopted for the *Bias_buffer* and for the *Bias_buffer_3v3*.

Test Board input The IC and the ASIC are programmed with an FPGA board connected to the TB with two IDC50 connectors. The LVDS signals generated from the FPGA are then converted on the TB to single-ended 3.3 V signals using 24 IC (SN65LVDT390PWR). The ASIC signals are then shifted to 1.2 V levels with four IC (TXU0104QPWRQ1) level shifters.

Test Board output The four exit lines of the top matrices are connected to four analog buffers with a gain of two which are employed to drive four 50Ω impedance lines exiting the test board with SMA connectors (MAX4214EUK).

The four exit lines of the bottom matrices on the PCB are instead wired to four LVDS buffers utilised as discriminators (SN65LVDS100D) connected to four pins of the second IDC50 connector mounted on the TB. The discriminator threshold could be adjusted through two DAC channels *Disc_level_A* and *Disc_level_B*.

Test-Pulse Circuits No test pulse circuit was implemented in the ASIC. To test the pixels operation, a test pulse circuit was implemented on the TB.

Two identical circuits shown in Fig. 5.2 are implemented on the test-board: one for flavour *a* matrices, the other for flavour *b*. HV_ASIC is connected to the PAD with flavour *a* or *b*, HV 1 is connected to the high voltage supply. TP_IN is used to inject the test pulse; it is usually at 0 V and when the TP signal is sent, it goes to 3.3 V. The pulse width can be adjusted via software, but should be above 100 ns. The BJT transistor is turned on when the TP arrives and produces a voltage step at the HV_ASIC node. This step is propagated to all the pixels. The RC network of the collection electrodes (sensor capacitance plus the 1 MΩ resistor) slows down the signal propagation and its rising time. Therefore, even with a pulse of a few tens of ns, the output signal has a characteristic time of tens of μs.

Bonding diagrams An example of a bonding diagram used for the full matrix read-out is shown in Fig. 5.3. This configuration allows the use of the quadruplet readout. Instead, Fig. 5.4 underlines the connections made for testing just four pixels. The first bonding diagram was used only in the early stage of the tests

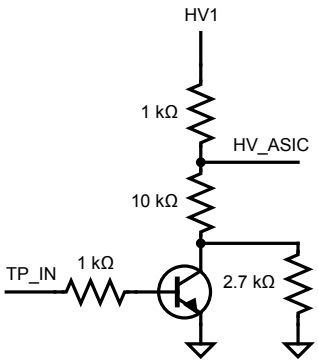


Figure 5.2: Test pulse circuit implemented on the TB.

to check the correct response of the sensor to the external test pulse. However, for the characterisation, it was not employed due to its excessively high parasitic inductance/capacitance. Indeed, if 16 pixels are linked to the same shared line, the parasitic capacitance of the pads and the wire bond inductance change the signal shape, worsening the timing performance. Thus, the second bonding configuration, of Fig. 5.4, was utilised in all beam tests.

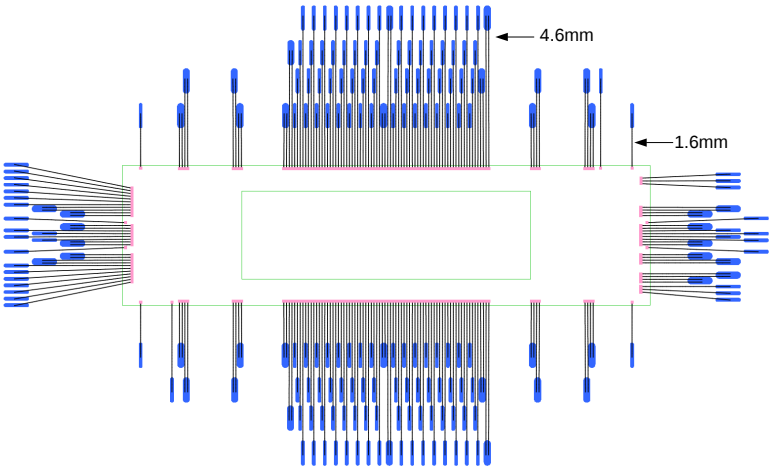


Figure 5.3: Wire bond schematic of all the 512 pixels.

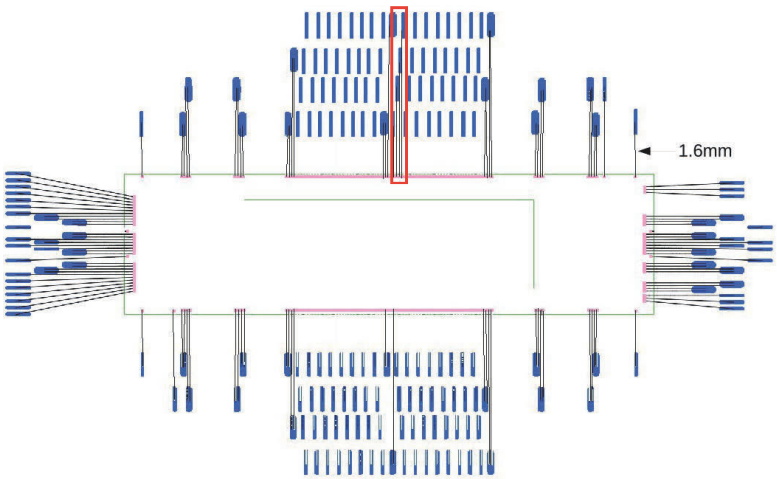


Figure 5.4: Minimum bonding configuration with just four pixels bonded (32, 33, 34 and 35). The red box encloses the four bondings connecting the pixels to the PCB.

5.1.2 Laboratory instrumentation

The main goal of the laboratory tests was the validation of the electronics and the response to the HV bias. First, the HV scan was performed in a probe station where only the guard ring, backside, collection electrode and deep p-well were biased. Each electrode was connected through the TB to a probe station, which could measure currents of the fA order. A first sweep on substrate bias was performed, and then a sweep on the topside voltage. From the first measurement, the punch-through point could be extracted, and from the second one, the breakdown voltage (Sec. 5.2.1).

Then, the board was connected to an FPGA and to a low-voltage power supply to test the power consumption of the electronics. The TB was then placed under a ^{55}Fe source to investigate the proper working of the bonded pixels. Figure 5.5a shows the setup used for MadPIX characterisation. The results are reported in Sec. 5.2.2.

The following instruments were used:

- 4 channels oscilloscope
- 2 channels power supply
- 2 × HV power supply (0-200 V)
- FPGA

(a) (b)

Figure 5.5: Setup used to measure MadPIX static characteristic (a) and laser setup utilised to extract the jitter performances (b).

- Computer

The same setup was used in combination with an IR picosecond laser for the jitter evaluation. Indeed, the Transient Current Technique (TCT) permits a measurement of time resolution by exploiting the signal induced in the sensor by a laser. The TCT setup used for MadPIX was equipped with micro-metrical x-y step motors and a fast pulsed IR laser ($\approx 100\,\text{ps}$, 1060 nm wavelength). The spot size could be focused up to a FWHM $\simeq 10\,\mu\text{m}$. The output signals were acquired using a Tektronix MDO3102 digital oscilloscope with a bandwidth of 1 GHz. A neutral density filter was used to decrease the total number of photons produced by the laser. MadPIX was front-side illuminated. The laser setup is shown in Fig. 5.5b and the results are reported in Sec. 5.2.2.

5.1.3 CERN beam test setup

In the CERN Beam Tests, the sensor response to impinging radiation was studied to extrapolate the chip time resolution.
Different Beam Test (BT) campaigns were carried out at the T10 beam line of CERN Proton Synchrotron (PS): October 2023, April, July and October 2024, April and June 2025.

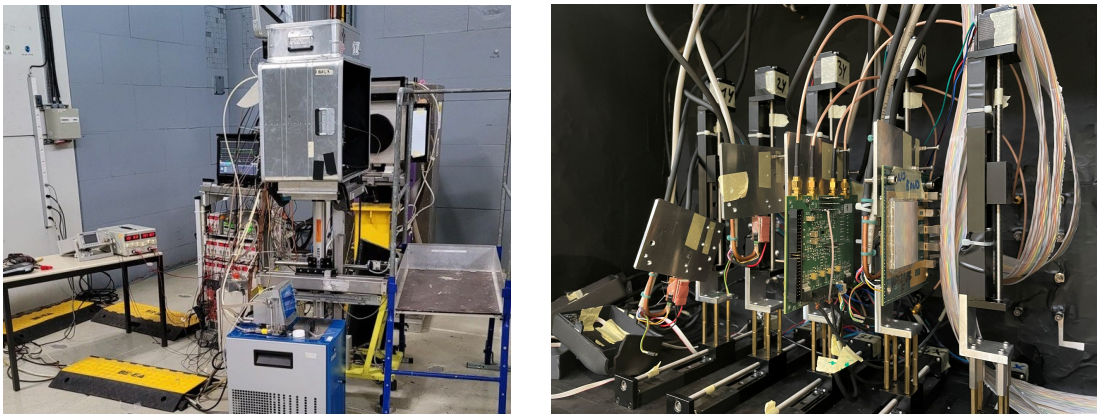
The T10 beam line is a secondary beam facility located in CERN East Area [127]. It is supplied by 24 GeV/c protons that are extracted from the Proton Synchrotron (PS). The spill duration is about $400\,\mu\text{s}$. The primary proton beam strikes a multi-target assembly, in which one of five available targets can be chosen. The standard target is made of beryllium/tungsten alloy. Downstream, the T10 beam line employs a sequence of magnets to guide the generated secondary

particles towards the T10 beam area.

The secondary beam line can operate across a wide momentum range, from 0.5 GeV/c to 11.5 GeV/c. Adjustable collimators provide control over both beam intensity and momentum spread relative to the central momentum set by the magnets. The intensity can vary from 10^3 up to 10^7 particles per spill, depending on the momentum. The polarity, positive or negative, can be selected. For the tests presented in this work, the beam energy was set to 10 GeV/c. This value is the maximum energy reachable at PS, which also provides the highest intensity. As measured in [128], the beam at this energy is mainly composed of protons (68 %) and pions (26 %).

The test setup was based on an aluminium box in which up to 6 planes could be mounted. Each plane had 2-axis motors (x, y) that allowed the sensor alignment. The moving stages were controlled utilising an ARDUINO which communicated with the control room via a *LabVIEW* interface. The box provided a dark environment and was placed at room temperature (Fig. 5.6).

The time reference was given by an LGAD mounted on the nearest plane to the beam source. It was read out with a Santa Cruz (V1.4-SCIPP-08/18) board containing a wide bandwidth (2 GHz) and low noise inverting amplifier with a measured amplification factor of 6. Then, a broadband and low-noise current amplifier with a gain between 13 and 14 was used as a second-stage amplifier. The output signals of the LGAD and of MadPIX were sent to a 4-channel LeCroy WaveRunner 9404M-MS oscilloscope, with 20 Gs/s sampling rate, 4 GHz analog



(a) (b)

Figure 5.6: CERN setup with the closed box containing the DUT and LGAD sensors, oscilloscope and power supplies in the back (a). Inside the box: MadPIX with attached the IDC50 flat cable (left) and LGAD (right), both mounted on moving stages (b).

bandwidth and 8-bit vertical resolution. The oscilloscope contribution to the total time resolution was negligible; indeed, the quantisation error is extracted as the time binning given by the sampling rate divided by $\sqrt{12}$, i.e. 14 ps and then reduced even more by interpolating two consecutive sampling points to extract the time information. One out of the four oscilloscope channels was reserved for the time reference signal (LGAD), while the other three are connected to the DUT (MadPIX).

The beam centre is composed of about $1.5 \cdot 10^4$ particles per mm^2 per spill, and usually 2 or 3 spills per minute are supplied to the T10 area. To maximise the acquisition rate, the oscilloscope was set in sequence mode ($1.5 \cdot 10^4$ maximum triggers per sequence) with a variable time-out set as a function of the spill distribution in time. The trigger was set as the OR of three DUT pixels. The same threshold was set for all the 3 DUT channels. The active area of the 3 DUT pixels is $250\,\mu\text{m} \times 300\,\mu\text{m}^2$ and hence a trigger rate of about 1100 events per spill was expected and measured. The number of particles that crossed both DUT and time reference was between 80 % and 85 % of the triggers.

The following instruments were used:

- 4 channel oscilloscope Lecroy WaveRunner 9404M-MS [1]
- 4 × single channel low power supply (TTI PL303[2])
- 3 × Medium voltage power supply (TDK Z100-4[3])
- High voltage power supply (CAEN N410[4])

The low-voltage power supply was used to bias the electronics (LGAD and MadPIX), the medium-voltage one for the sensor part of MadPIX and the high-voltage one for the LGAD.

5.1.4 DESY beam test setup

In the DESY Beam Tests, the sensor response to radiation as a function of the impinging position was studied to extrapolate the in-pixel efficiency and time resolution.
Two BT campaigns were carried out at DESY in March and November 2025.

[1] Lecroy WaveRunner 9000 Manuals

[2] PL Manual

[3] Z100 Data Sheet

[4] N410 User Manual

DESY provides three dedicated beam test lines: TB21, TB22 and TB24. These lines deliver electron or positron beams originating from bremsstrahlung photons produced in the DESY II electron-positron synchrotron. This bremsstrahlung-based beam is produced by inserting a carbon fibre into the DESY II synchrotron. The resulting photons are then converted into electron–positron pairs using a copper target. After production, a dipole magnet disperses the particles, and a collimator forms the final beam. To have the highest rate, the collimator was set to the maximum aperture (± 10, ± 10). The dipole magnet current was set to select only electrons.

The bremsstrahlung photon energy spectrum follows the $1/E$ law, while the energy distribution from pair production is almost uniform. The current in the dipole magnet sets the momentum of the beam, which can reach up to 6 GeV.
The final beam can reach particle densities up to approximately 1000 particles per cm^2, with selectable energies between 1 and 6 GeV, an energy spread on the order of 5%, and a typical angular divergence of around 1 mRad [129].
The control hut for the TB areas stands near its respective experimental area. Each control room contains the infrastructure for its beam and the installed telescope. A wired point-to-point connection (1 Gbit Ethernet) was used for the communication between the control room and the test setup. During November 2025 BT, the ADENIUM telescope [130] was used in TB22, while in March 2025, the EUDET [131] was used (TB24).

The DESY beam test was organised to test MadPIX using a tracking telescope, which is designed for precise particle track reconstruction. The system was originally developed as part of the EUDET project [132, 133] whose goal was to create a telescope with simple integration of DUT and precise spatial resolution.

Each telescope consists of two moving arms, with three tracking planes per arm. The DUT was positioned between the two arms, and three sensor planes were placed upstream and three downstream. The DUT was mounted on a precision motion stage that provides micron-level positioning in x, y, and rotation (Fig. 5.7). Every telescope plane can be shifted along the beam direction, and it contains MIMOSA26 or ALPIDE, both of which are monolithic CMOS pixel sensors [134, 74].

The MIMOSA26 features a pixel pitch of 18.4 μm and a matrix of 1152×576 pixels, resulting in an active area of approximately $21.2 \times 10.6\,\mathrm{mm}^2$. The sensor operates with a rolling-shutter readout scheme that digitises data directly on chip, producing binary hit information and applying zero suppression. The full frame integration time is 115.2 μs. However, the Trigger Logic Unit (TLU) readout frame contains two consecutive frames, hence the total dead time is 230.4 μs. The sensor thickness is 50 μm and both sides are protected from light with 25 μm Kapton foils. A low material budget is crucial for maintaining high pointing resolution for

(a) (b)

Figure 5.7: EUDET (a) and ADENIUM (b) telescopes. The beam crosses the setup from right to left. The grey box in the middle of the planes contained MadPIX.

the low beam energy supplied by DESY II. The intrinsic spatial resolution of each MIMOSA26 has been measured to be $(3.24 \pm 0.09)\,\mu m$ with a threshold set to be 6 times the RMS noise, for which an average noise occupancy per pixel is about $6 \cdot 10^{-5}$ per readout frame. The best tracking reconstruction accuracy that can be achieved on the DUT is $(1.83 \pm 0.03)\,\mu$m with a 20 mm spacing between the two MIMOSA26 from the DUT, a beam energy of 5 GeV and a DUT material budget X/X_0 of 0.001 % [131]. The MIMOSA26 characteristics are summarised in table 5.1.

The ALPIDE chip [74] is instead fabricated in an 180 nm CIS process on wafers with a 25 μm thick high resistivity p-epitaxial layer on a substrate of the same type. ALPIDE has a larger pixel size, i.e. $26.88 \times 29.24\,\mu\text{m}^2$, but offers a

Table 5.1: MIMOSA26 specifications.

	MIMOSA26
Technology	AMS-C35B4/OPTO
Pixel pitch [μm]	18.4
Number of pixels	1152×576
Active area [mm^2]	21.2×10.6
Readout time [μs]	230.4
Thickness [μm]	50
Spatial resolution [μm]	(3.24 ± 0.09)

Table 5.2: ALPIDE specifications.

	ALPIDE
Technology	TowerJazz 180nm
Pixel size [μm^2]	26.88×29.24
Number of pixels	512×1024
Active area [mm^2]	13.8×29.9
Readout time [μs]	10
Thickness [μm]	50
Spatial resolution [μm]	≈ 4.5

larger active area ($13.8 \times 29.9\,\mathrm{mm}^2$) as well as significantly shorter readout time ($\approx 10\,\mu$s) due to its low peak time (around $2\,\mu$s). The fake-hit rate is 100 times lower than MIMOSA26 with a comparable detection efficiency. Additionally, the power-efficient design results in negligible heat generation, allowing for passive cooling compared to the existing MIMOSA26 planes. The material budget is very similar to MIMOSA26 due to the $50\,\mu$m substrate. The ALPIDE characteristics are summarised in table 5.2.

The tracking resolution on the DUT has a strong dependence on beam energy, spacing between planes, and the DUT material budget. For instance, the beam energy selected for the MadPIX tests was 4.6 GeV, which is the maximum value before the particle rate drop [129]. The minimum spacings between MadPIX and the two nearest MIMOSA26 planes that could be achieved were 64 mm and 51 mm due to the DUT support. The MadPIX material budget X/X_0 is estimated to be 0.32 %. The distance between MIMOSA26 planes is reported in table 5.3. From [131], the expected track resolution on the DUT should be in the $3 \div 4\,\mu$m range. A better estimation was extracted using the telescope analyser tool [135], where all the parameters in table 5.3 were inserted and a track resolution of $3.4\,\mu$m was predicted.

Instead, the positions of ALPIDEs are reported in table 5.4. From [130], the expected track resolution on the DUT should be $3 \div 6\,\mu$m (depending on the plane separation). From the telescope analyser tool, a track resolution of $5.2\,\mu$m was predicted. EUDET offers a better tracking resolution, but it is slower compared to the ADENIUM, and it will be removed from beam lines in the next few years due to insufficient availability of MIMOSA26. For these reasons, the second beam test was conducted using a different telescope from the first one. For MadPIX, a resolution on the DUT between $5\,\mu$m and $6\,\mu$m is sufficient for the proposed studies due to its large pixel size ($250 \times 100\,\mu$m^2).

Both telescopes are controlled by the AIDA TLU [133], which is responsible

Table 5.3: Position and material budget of DUT and MIMOSA26 planes in the EUDET telescope. Plane 0 is the first hit by the beam, and the relative positions were measured starting from this plane after the setup assembly. The material budget includes the thickness of the monolithic chip and Kapton tape used to shield the sensor from light.

	Type	**Position [**cm**]**	**Material budget [%** χ/χ_0**]**
Plane 0	MIMOSA26	0.0	0.07
Plane 1	MIMOSA26	15.1	0.07
Plane 2	MIMOSA26	29.9	0.07
Plane 3	MadPIX	35.0	0.32
Plane 4	MIMOSA26	41.4	0.07
Plane 5	MIMOSA26	50.1	0.07
Plane 6	MIMOSA26	58.4	0.07

for managing all the telescope planes. The TLU provides time stamping and coincidence/trigger logic (Fig. 5.8a). Indeed, when a trigger is issued, the TLU exchanges handshake signals with MIMOSA26 or ALPIDE. Then, the telescope records a full frame for the triggered event. External devices can also be synchronised similarly or run without a handshake if desired.

All components are controlled through the EUDAQ data-acquisition software, which merges the detectors data streams. EUDAQ operates synchronously, meaning the global event rate is limited by the slowest readout device involved. When

Table 5.4: Position and material budget of DUT and ALPIDE planes in ADENIUM telescope. Plane 0 is the first hit by the beam, and the relative positions were measured starting from this plane after the setup assembly. The material budget includes the thickness of the monolithic chip and Kapton tape used to shield the sensor.

	Type	**Position [**cm**]**	**Material budget [%** χ/χ_0**]**
Plane 0	ALPIDE	0.0	0.08
Plane 1	ALPIDE	7.9	0.08
Plane 2	ALPIDE	16.0	0.08
Plane 3	MadPIX	21.1	0.32
Plane 4	ALPIDE	27.3	0.08
Plane 5	ALPIDE	35.4	0.08
Plane 6	ALPIDE	43.3	0.08

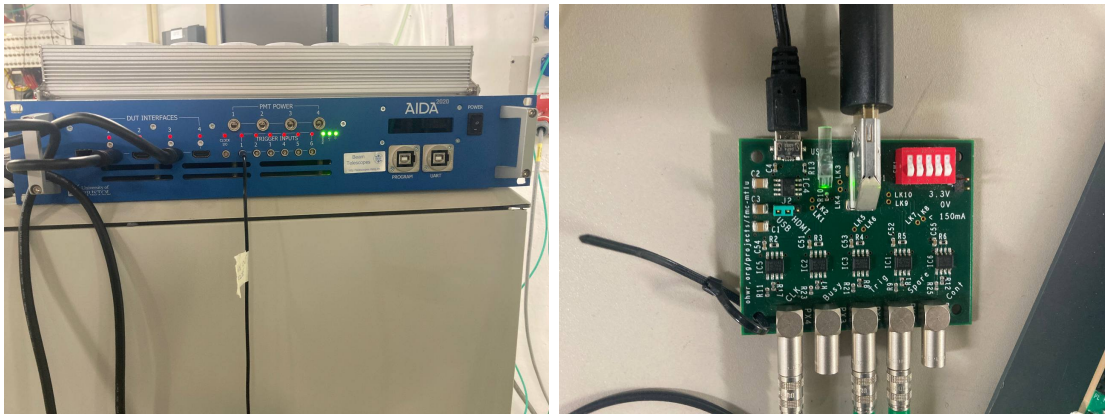
only the telescope is used, the measured event rate reaches around 2 kHz for a particle flux of roughly 10 kHz [131]. Indeed, the dead time is given by the readout of two consecutive frames of the MIMOSA26, i.e. 230 μs, plus the time needed by the TLU operations. The ADENIUM telescope can reach 100 kHz due to its lower dead time, a value not reached at DESY.

The DESY telescopes allow the extraction of the impinging position on the DUT. However, the time information assigned to each trigger has a resolution of 1/8 of the clock period of the TLU. For the standard 40 MHz clock, the LSB is hence 3.125 ns, while the predicted time resolution is 781 ps, which is not adequate to measure sub-ns performances. Hence, in addition to the TLU, an oscilloscope was used to acquire the DUT and the time reference signals. The same readout mode used for the CERN beam tests was used. An oscilloscope was connected to three DUT pixels and to the time reference (LGAD). In DESY BTs, unlike at CERN, the LGAD was mounted as the last plane hit by the beam to minimize material budget and hence multiple scattering.

The oscilloscope and DESY telescope collected data in parallel without communicating with each other. Unlike the CERN beam test, the LGAD sensor triggered the oscilloscope because of its larger area compared to MadPIX. To properly scan the DUT pixels, the trigger area should be greater than the MadPIX active region; otherwise, the efficiency cannot be studied.

To synchronise the two systems and to associate the waveforms collected by the oscilloscope to the trace reconstructed by the telescope, the trigger output port of the oscilloscope was employed (BNC - 1.5 V into a 50 Ω load to ground). This signal was sent to the TLU analog input port 1 (LEMO-50 Ω), which can discriminate signals in the $\pm$1.3 V range (Fig. 5.8a). A threshold of 0.5 V was set for the TLU input controlling MIMOSA26. For the ALPIDE, a higher threshold of 1.2 V was set due to a problem in the TLU input channel. In this telescope, the lower thresholds revealed a ringing effect that produced multiple TLU triggers during the ALPIDE readout frame.

To minimise the oscilloscope dead time needed to save each waveform, as in CERN BT, the sequence mode was used. In particular, the time out was set to maximum, and the number of waveforms per sequence was set to 1000. Sequences were filled in less than 20 seconds due to the LGAD trigger rate of 50 Hz. Indeed, a particle rate of 10 kHz is expected on the MIMOSA26 area ($\simeq 1 \times 2\,\mathrm{cm}^2$), but the LGAD is 225 times smaller than MIMOSA26 and 413 times smaller than ALPIDE. A higher number of events per sequence could have been chosen; however, if synchronisation was lost, as will be described briefly, all the sequences should have been discarded. Hence, 1000 was a good trade-off between oscilloscope dead time and synchronisation error probability.



(a) (b)

Figure 5.8: AIDA TLU connected to six MIMOSA26 planes with the first HDMI cable and to ZCU with the second one (a). The DESY board used for converting the LVDS signal from the TLU to the TTL standard used by the FPGA (b).

Additionally, the oscilloscope was set with a hold-off greater than the TLU; otherwise, if two events were acquired in a 230 μs window (or 10 μs for the ALPIDE), the TLU would have registered only one event and the synchronisation would have been lost. A hold-off of 300 μs was chosen to be conservative for the EUDET telescope (30 μs for the ADENIUM).

To simplify the association of oscilloscope sequences with the event number generated by the telescope, one of the four different TLU handshake modes was used: synchronous with trigger number. In synchronous mode, the TLU sends a clock (40 MHz) to the DUT (*Clock* line). When the TLU is triggered, the *Trigger* line is asserted for one clock cycle, and immediately afterwards the TLU clocks out the trigger number (LSB first) on the *Sync/T0* line. This mode of operation was enabled by setting the *DUTMaskMode* parameter in the configuration file to $0b01$. The three lines (*clock*, *trigger*, and *Sync/T0/Spare*) pass through a HDMI connector using the 3.3 V LVDS standard. HDMI port 3 was used for both telescopes due to a problem in port 2 (port 1 is used for controlling MIMOSA26 or ALPIDE), as shown in Fig. 5.8b. A custom board provided by DESY was used to convert the HDMI lines from LVDS to 1.2 V TTL lines with LEMO connectors. The red switch on this board was set to the value of Fig. 5.8b for using it as a sole output signal. Other configurations allow bidirectional communication between DUT and TLU. The lines between the DESY board and FPGA was as short as possible to avoid interference (i.e. 4 ns coaxial cable). A very long HDMI cable, which is more resistant to jamming, was used between the TLU and the board. The TTL lines were then connected to an FMC to LEMO breakout board

and terminated with a 50 Ω load to ground and connected to an Xilinx ZCU102 FPGA. The *Sync/T0/Spare* was delayed 4 ns more than the other 2 to centre the word transition inside the clock first half period. In this way, the FPGA was better sampling the transition edge.
In table 5.5, the ports used for communicating between the FPGA and TLU are summarised.

The firmware loaded in the FPGA allowed the AXI memory to store the current event number generated by the TLU. AXI bus could then be accessed by Ubuntu OS running on the SoC of the ZCU.

Figure 5.9 shows all the connections and the main components used in the DESY beam test.

Python scripts running in the Jupyter Notebook service controlled the global DAQ system. They managed and tracked the power supplies, oscilloscope and TLU synchronisation. A subprocess constantly read the oscilloscope status to check if the sequence was completed. If 1000 events were recorded, the trigger was disabled. Then, the last TLU number written in the AXI memory bus was read by the Python script. If the synchronisation was still in place, the subprocess enabled the oscilloscope trigger once again and set the oscilloscope file name in which the waveforms were saved to be the next TLU trigger number. If synchronisation was lost, the same procedure occurred, but with an additional error report. With this mechanism, the synchronisation was restored every 1000 events, allowing for a long data acquisition campaign.

Figure 5.10 shows a flowchart of the DESY test beam readout.

A separate PC controlled the EUDET and ADENIUM telescopes. First, the EUDAQ acquisition was initiated to initialise the telescopes, then the oscilloscope acquisition was launched via the Jupyter Notebook. The subsequent acquisitions were triggered by the online synchronisation control described above.

Table 5.5: Connections between TLU and ZCU breakout board.

Breakout Pin Name	**TLU signal**	**DESCRIPTION**
LA21_P	Trigger	Trigger input from TLU
LA28_P	Sync/T0/spare	Data line for event id
LA11_P	Clock	Output clock 40 MHz

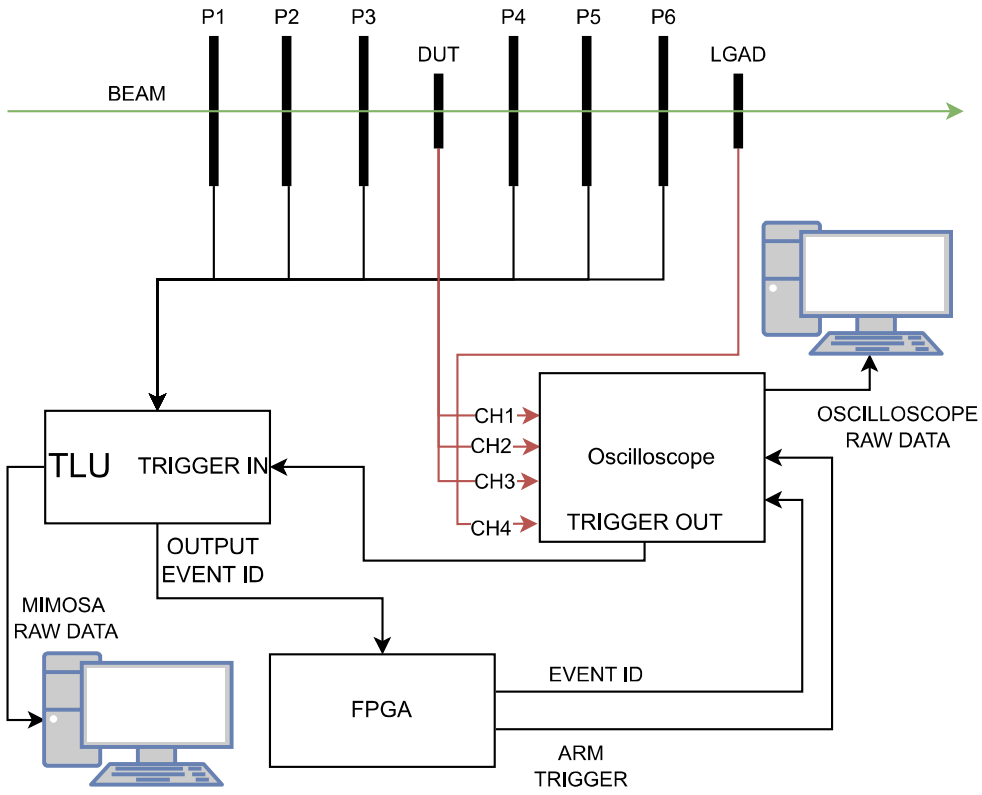


Figure 5.9: Connection used in the DESY beam test to synchronise the oscilloscope and the TLU acquisition. P1, P2, P3, P4, P5 and P6 are the telescope planes (MIMOSA26 or ALPIDE). The DUT is MadPIX, while the LGAD is the time reference and the trigger channel; they are both connected to the oscilloscope. The oscilloscope trigger output is connected to TLU as an input trigger. The TLU send the event ID to the FPGA through a bus. The FPGA controls the oscilloscope via Ethernet (trigger enable and file name). The data are saved on two different PCs.

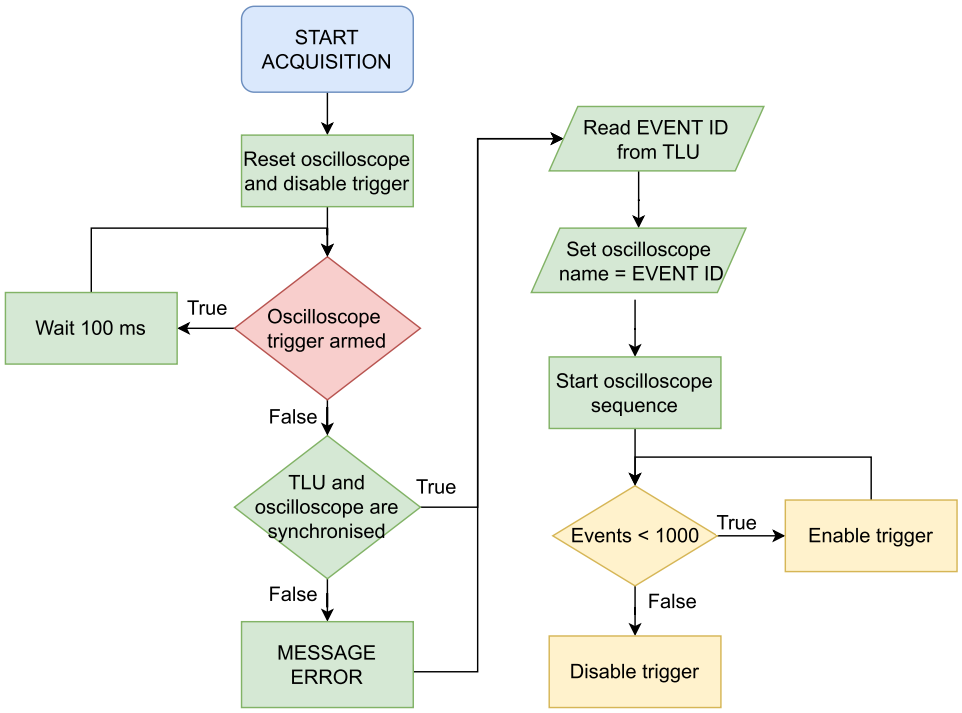


Figure 5.10: Flowchart of the DESY test beam readout. In blue, the start operation is controlled by the user. The red box is a subprocess continuously running in background. In green, the operation executed by the FPGA, while in red, the one controlled by the oscilloscope.

The instrumentation used for the DESY BT was:

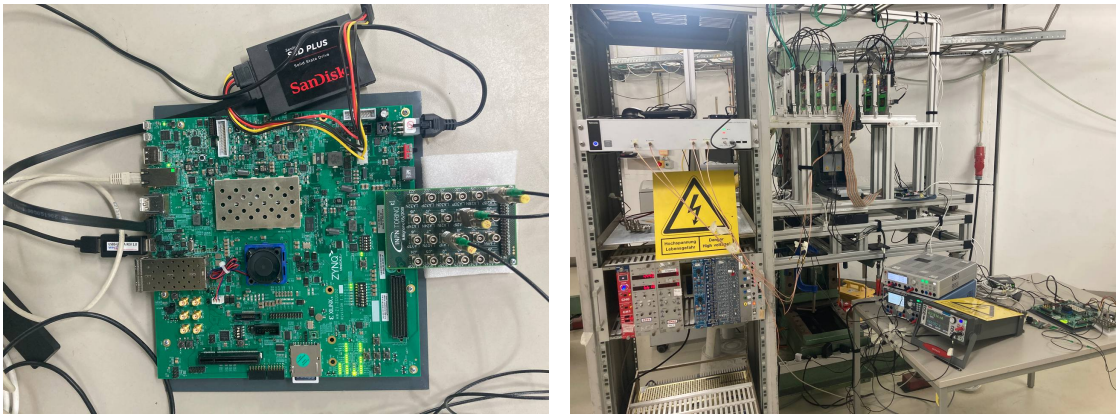
- 4 channel digitizer Tektronix LPD64 6-BW-8000[5]
- 3 × Medium voltage power supply (HMP4040, HMP 2030, and Keithley 2450 [6])
- High voltage power supply (CAEN N410[7])
- Xilinx ZCU102[8]

[5]LPD64 User Manual

[6]HMP4000 Data Sheet, HMP2000 Data Sheet,Keithley 2450 Data Sheet

[7]N410 User Manual

[8]ZCU102 User Manual



(a) (b)

Figure 5.11: ZCU close-up with the LEMO breakout board connected to the DESY board (a). DESY setup with the telescope, oscilloscope, FPGA and power supplies on the right (b).

The digitizer can achieve 8 GHz and 25 GS/s, however the bandwidth was limited to 4 GHz to match the LGAD one. A picture of the setup is shown in Fig. 5.11.

5.2 ARCADIA *Run 3*

In this section, the results obtained with the first production of MadPIX are reported, i.e. the chip produced during the third engineering run of the ARCADIA submission. Wafers were manufactured in July 2023 and diced in August. The first tests started immediately afterwards. Several dose splits were fabricated; however, only the split with the highest implantation dose was tested, and its results are described in this section.

Four TB were manufactured, and different MadPIX were bonded on them; they are summarised in table 5.6. The reticle positions are shown in Fig. 5.12a, while Fig. 5.12b displays the position of MadPIX inside the reticle.

5.2.1 Sensor characterisation

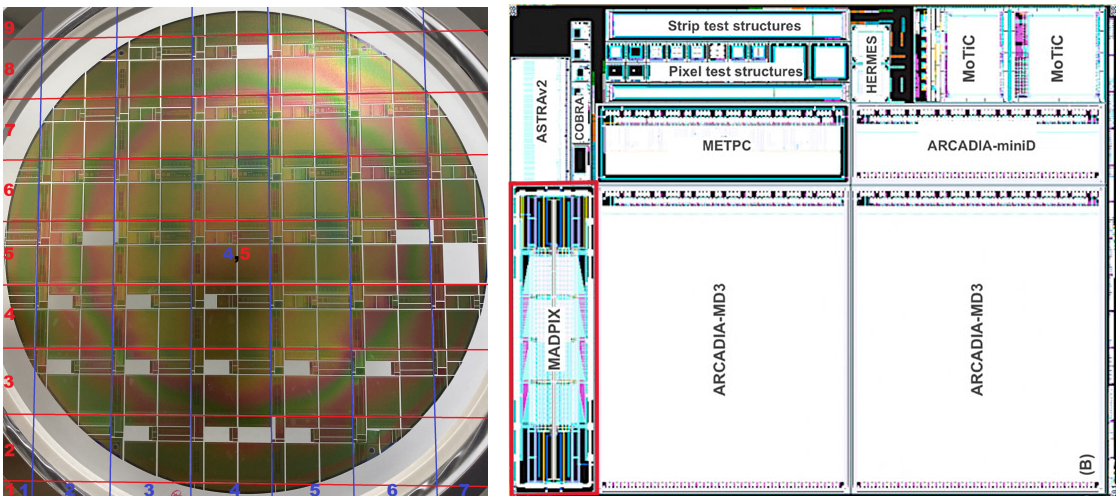
The MadPIX ASIC was wire-bonded to the PCB described in the previous section. The split was chosen based on measurements taken on passive test structures, where there is no front-end electronics and on which sensor capacitance measurements could be performed. The intrinsic gain of the sensor was measured by illuminating these structures with the laser setup described in the previous

Table 5.6: List of ASICs tested for *Run 3* production with extraction wafer, reticle position, bonded test board and number of pixels bonded.

Identifier (ID)	**Wafer**	**Position (x,y)**	**TB**	**Pixels**
0	3	(3,5)	2	8
1	3	(2,2)	3	64
2	6	(3,5)	1	64
3	3	(3,6)	4	64
4	3	(4,2)	2	64
5	3	(3,3)	1	4 (0,1,2,3)
6	3	(4,3)	2	4 (24,25,26,27)

section, as reported in [97]. The expected gain from simulations (Sec. 3.2.1) was between 10 and 20. However, a value of 3 was found in the experimental study.

To validate the gain value extracted with laser readings, lateral sensor capacity measurements were performed [96]. After adjusting TCAD and MC simulations using these values (Sec. 3.2.2), a new expected gain of 3 was estimated, which is compatible with the measured value in the passive structures. For a low gain of 3, the dose variations implemented in the splits (reference, +3 %, +6 %) did not result in a significant change in gain value because the variations in the electric



(a) (b)

Figure 5.12: Wafer picture with the reticle positions. In blue, the y-axis, while in red, the x-axis (a). Reticle structure of the 3rd engineering run of ARCADIA, MadPIX is outlined in red (b). Image (b) is taken from [6].

field maximum were not sufficient to change the gain range. For this reason, only MadPIX belonging to wafers with the highest implanted dose were tested. The simulations covered only the two most promising dose splits corresponding to the target gain values. However, to cope with the foundry process variations, a total of 7 splits were produced (-12 %, -6 %, -3 %, reference, +3 %, +6 %).

MadPIX current-voltage measurements

As for the passive structure, the static characterisation of the sensor itself was performed on bonded MadPIX. Similar to LGAD sensors [136, 137, 138, 3] and to CMOS LGAD passive structures [97, 96], current-voltage (IV) measurements are needed to find out the devices working regions. As previously described in Chapter 3, the CMOS LGAD needs four biases: V_{top} , V_{back}, V_{dp}, V_{gr}. The optimal operating point for V_{top} and V_{back} was extracted from laboratory tests; the other two biases were fixed. V_{dp} must be 0 V otherwise the NMOS and PMOS transistors inside the deep p-well behave improperly because the bulk contacts would be subjected to a voltage different from the nominal one. V_{gr} was set to the maximum achievable value, i.e. 9 V (edge breakdown at 9.3 V). The guard ring implant should be redesigned with greater spacing from other implants to achieve a higher bias. The maximum value was set because the V_{top} breakdown point depends slightly on V_{gr}. Moving from 0 V to 9 V, the collector electrode breakdown was shifted by a few volts, thus providing an improvement in sensor gain. Additionally, it facilitated the full depletion of the sensor.

The V_{top} scan was used for assessing the breakdown voltage, while the V_{back} scan was needed for the punch-through. In particular, the collection electrode current i_{top} significantly grows when V_{top} reaches the breakdown point as in standard LGAD, while the substrate current i_{back} increases considerably when V_{back} is sufficiently large to generate a conductive channel between the deep p-well and the p^+-substrate contact. In addition, i_{top} was employed to extract the substrate depletion; indeed, when V_{back} is not applied, a current flows from the collection electrode to the guard ring (both n-type implants). When V_{back} is high enough, the channel between these two implants disappears and hence i_{top} drops.

Figure 5.13a shows the i_{back} as a function of V_{back} for different ASICs. ID 4 was the only non-working device, and so it is not presented in the following plots. All the prototypes show a similar behaviour, apart from ID 2, which was extracted from a different wafer; its behaviour is comparable to wafer 3, but the current sunk is more than double. i_{back} shows a substantial increase at 10 V (4 V for W6) and another change above 25 V. These values can be compared to passive structures behaviour where the punch-through was measured around 28 V (compatible with the second increase point). However, in passive structures i_{back} was constant below punch-through, while in MadPIX a steep increase is present at 10 V. The

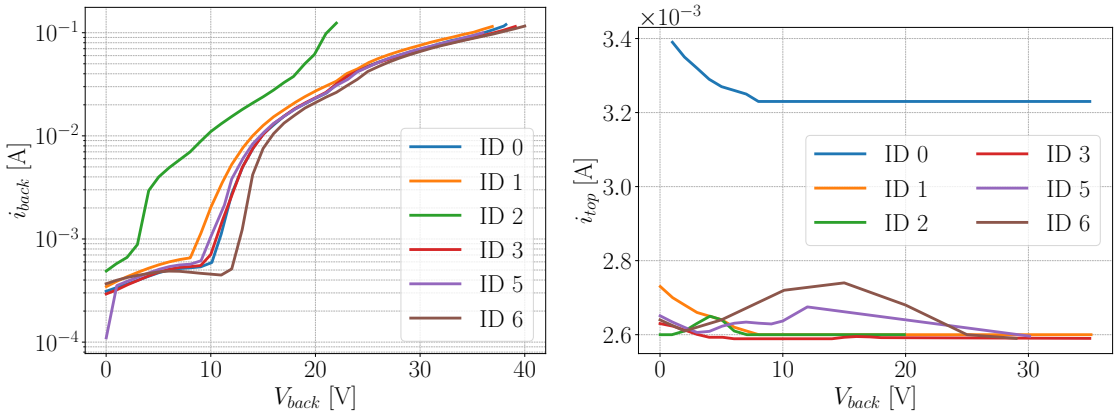


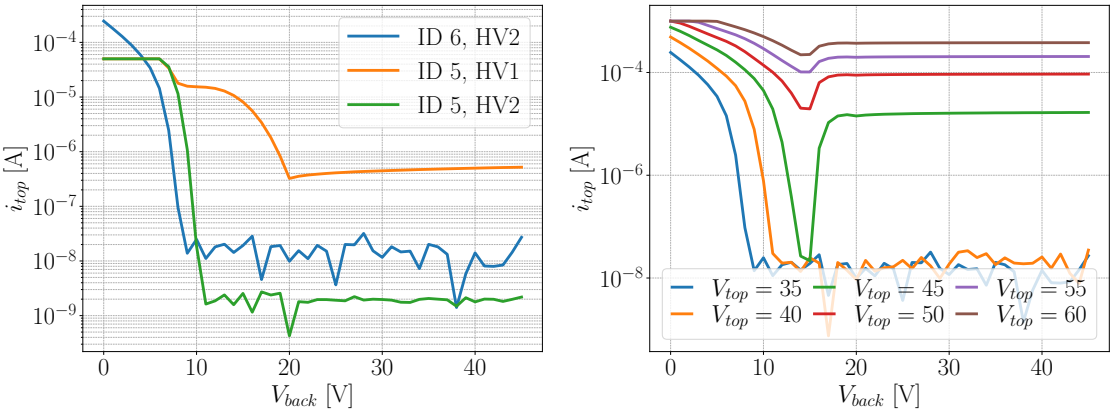
Figure 5.13: i_{back} (a) and i_{top} (b) as a function of the substrate negative voltage.

substrate current measured by MadPIX was three orders of magnitude more than that measured in passive structures. This mismatch was explained by a floating guard ring placed very close to the silicon border, which was left unconnected in MadPIX. This element is outside the pad frame, i.e. where the chip is diced. If biased, it should have been collecting the border current due to the low-resistive path created in the dicing process.

Figure 5.13b shows instead i_{top} plotted as a function of V_{back}. The current values behave differently, and the absolute value does not follow the true behaviour of the collection electrode current. All the above measurements were performed with $V_{top} = 30\,\text{V}$. From Fig. 5.2, it is trivial that the major contribution of the measured current is represented by the one sunk by the test pulse circuit.

Only for IDs 5 and 6, the $10\,\text{k}\Omega$ resistance was removed to obtain a proper i_{top} measurement as a function of V_{top}. Figure 5.14a shows i_{top} as a function of V_{back} for the two different sensor layouts, i.e. *1* and *2*. As predicted, the depletion strongly depends on the layout. The depletion is reached when the i_{top} reaches a minimum, i.e. *layout 1* is depleted at $-20\,\text{V}$ while 2 is depleted at $-10\,\text{V}$. The measurements were performed biasing the collection electrode voltage at 30 V, the point at which passive structures showed intrinsic gain [97].

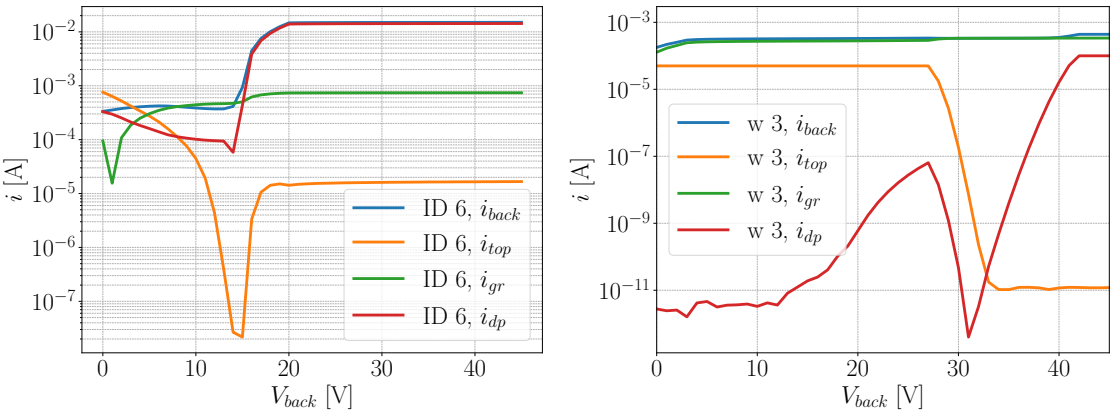
Figure 5.14b displays the collection electrode current as a function of V_{back} for different V_{top}. Below 45 V, the leakage current is stable after depletion, while for higher voltages, there is a significant increase. In addition, this plot reveals that the depletion shifts to higher voltages due to the greater potential difference between the top and guard rings, i.e. the conductive channel between them is stronger. Furthermore, at 15 V the top current increases up to a plateau due to a limitation of the substrate current (10 mA).



(a) (b)

Figure 5.14: i_{top} measured for two ASICs with a probe station after removing the 10 kΩ resistor in the test pulse circuit (a). While in (b) i_{top} of ID 6 was taken at different collection electrode voltages.

The sudden growth of i_{top} and the relative plateaux can be better explained by Fig. 5.15a, where the currents of various implants are shown as a function of the substrate voltage. At 15 V, a conductive channel between deep p-well and substrate is formed, and even i_{top} is affected by this trend. The MadPIX currents can be compared to passive structures. Figure 5.15b reports i_{top}, i_{back}, i_{gr}, and i_{dp} measured in a passive structure with the collection electrode biased at 35 V. The device belongs to W3 extracted in position (2,2). Differently from MadPIX, the



(a) (b)

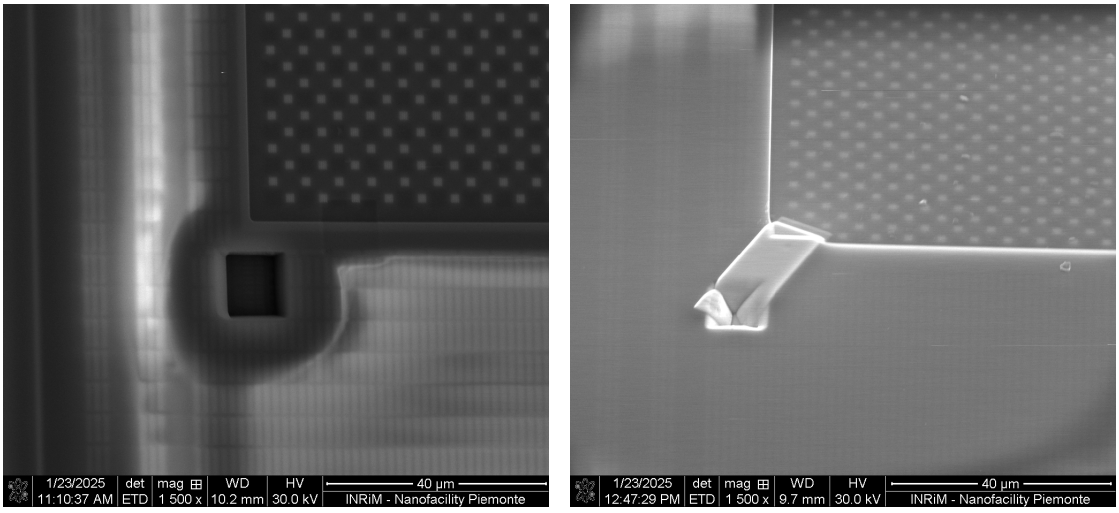
Figure 5.15: i_{top}, i_{back}, i_{gr}, and i_{dp}, for ID 6 (a) and for a passive structure (b) as a function of the substrate bias. V_{top} is fixed at 45 V.

i_{back} is steady up to 45 V and below 1 mA, there is no increase at 15 V. The i_{dp} growth begins when the structure goes in punch-through, i.e. 35 V. The depletion comes later due to a different border structure and due to the floating guard ring.

As described above, high substrate current represented a problem for timing measurements. The high current contributed to chip overheating and incorrect depletion. The proposed solution was to employ the Focused Ion Beam (FIB).

Focused Ion Beam intervention

FIB instruments function similarly to Scanning Electron Microscopes (SEMs) but, instead of electrons, they employ a highly focused beam of gallium ions. Depending on the ion current, the beam can be used either for high-resolution imaging or for localised sputtering and milling if high currents are set. Therefore, with high ^{55}Ga beam currents, some material from the surface is removed in the form of secondary ions (positive or negative), neutral atoms or secondary electrons. By scanning the ion beam across the surface and detecting the secondary electrons, the instrument creates an image of the sample. At low ion currents, only a minimal amount of material is removed, allowing modern systems to reach imaging resolutions of around 5 nm. This limit is largely determined by the sputtering effects of the ions and by the sensing elements. The used instrument was a dual-beam system, which combine both SEM and FIB columns in the same chamber. SEM was employed to locate the position and acquire images of the samples, while FIB



(a) (b)

Figure 5.16: Hole dug with the ion beam near the guard ring pad (a) and platinum connection (b).

Table 5.7: FIB parameter used for etching the material and for depositing the Platinum.

Step / Item	**Details**
Ion beam current	5 nA
Ion beam energy	30 kV
Area to etch	$10 \times 20\,\mu m^2$
Material	(Si_3N_4)
Platinum deposition current	1 nA
Platinum deposition energy	30 kV
Platinum deposition time	15 minutes
Etch time in minutes	**Details**
00:00	Start etching (Start beam)
01:10	Metal F start
03:30	Metal 5 start
05:20	Metal 4 start
07:00	Metal 3 start
08:50	Metal 2 start
09:30	Metal 2 finish
10:40	Metal 1 opening (Stop beam)

was used to dig a hole in silicon dioxide and to deposit platinum.

A high ion current was utilised to enable extremely accurate material removal to mill a $200\,\mu m^2$ hole until the metal above the floating guard ring was exposed. Then, the FIB locally deposited conductive material through Ion Beam Induced Chemical vapour deposition (IBIC). During this step, a gas containing platinum is introduced into the chamber, and it goes onto the sample surface. When the ion beam scans over the region, it decomposes the gas molecules, producing volatile fragments that are pumped away. Instead, the platinum remains on the surface, forming a solid deposit. This method enables a direct connection between the guard ring metal and an adjacent pad.

Figure 5.16a shows the hole milled for one ASIC prototype, the dimension is $10 \times 20\,\mu m^2$, while Fig. 5.16b display the platinum deposition connecting the guard ring to the pad used to bias the same structures which enclose the pixel matrices.

In table 5.7, the parameters used for operating the FIB are reported, together with the time needed for reaching the different metal layers. The etching times depend on the metal lines and the silicon dioxide thicknesses.

The FIB was performed on two samples; the characteristics are shown in table

Table 5.8: List of ASICs on which the FIB was performed for *Run 3* production with extraction wafer, reticle position, bonded test board, number of pixels bonded, and pad used for the floating guard ring bias.

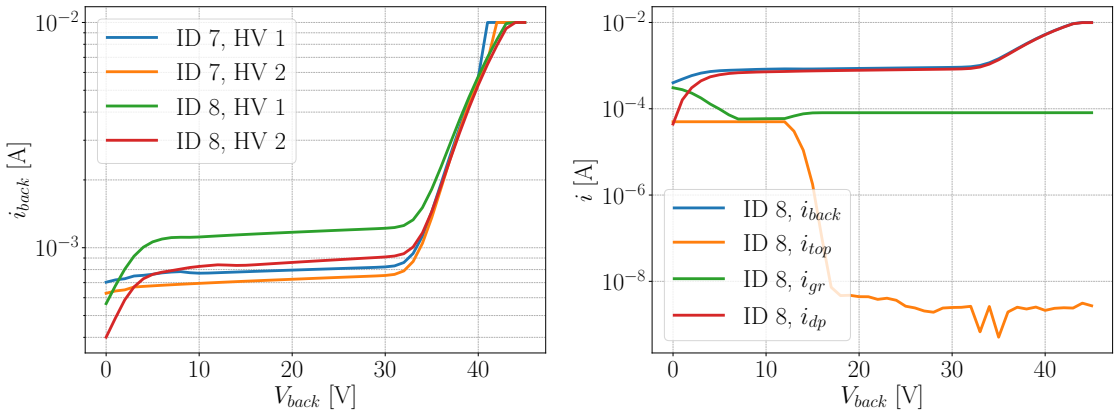
ID	Wafer	Position (x,y)	TB	Pixels	Bias
7	3	(3,4)	1	4 (0,1,2,3)	Power - 3.3 V
8	3	(2,4)	4	4 (6,7,8,9)	Guard ring ≈ 9 V

5.8. To understand the optimal bias, the floating guard ring was connected to the 3.3 V power pad in one sample and to the guard ring pad in the other (9 V).

MadPIX current-voltage measurements after FIB

After bonding, IV measurements were performed on the FIB samples. The same parameter analyser (HP4156A) was used to measure the currents. i_{back} is plotted in Fig. 5.17a, where all the structures show a punch-through around 35 V, the HV 1 bias creates a higher current in the substrate due to the termination, which can be depleted faster. The plot also shows that the chip with a floating guard ring connected to 3.3 V has a slightly lower current.

Figure 5.17b shows all the currents for the ID 8 chip. i_{top} does not have an increase before the punch-through, exactly as the passive structures and the absolute values are compatible. Indeed, the passive structure is composed of 10 pixels, while the HV line of MadPIX is connected to 128 pixels. As for the structures



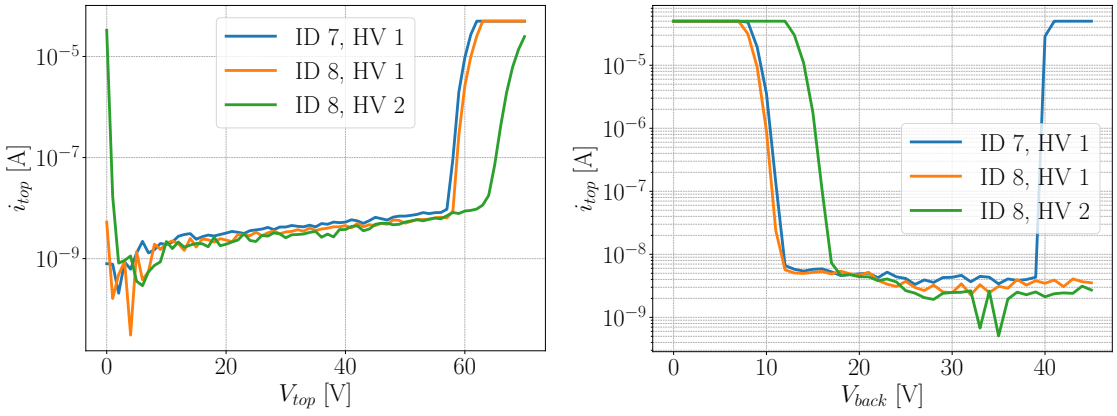
(a) (b)

Figure 5.17: MadPIX i_{back} as a function of the substrate bias measured after FIB (a). i_{back}, i_{gr}, and i_{dp}, for ID 8 as a function of V_{back}. The measurements are performed with $V_{top} = 45$ V.

with FIB correction, depletion starts 15 V before the passive structure due to the different implants. Indeed, in MadPIX, the deep p-wells cover a much larger area due to the electronics, which is not present in passive structures.

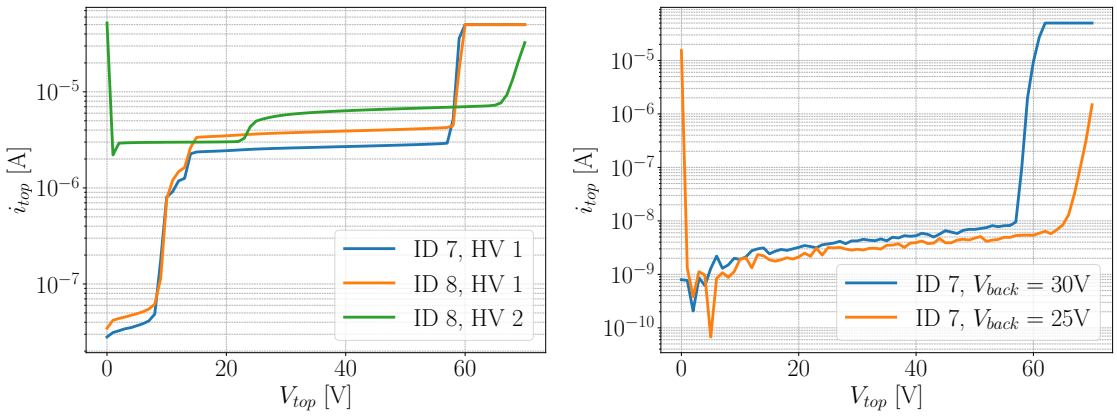
After the FIB operation, the i_{top} was studied as a function of the collection electrode bias (Fig. 5.18a). As expected, the breakdown voltage depends on the termination layout, *1* or *2*. *Layout 1* (HV 1) has no gap between p-gain and n-implant at the pixel border and hence reaches breakdown earlier (60 V) than *layout 2* (HV 2, 65 V). In the device working region, the currents are equal. Figure 5.18b displays i_{top} as a function of the substrate bias. *Layout 1* reaches the full depletion at $V_{back} = 10$ V while *layout 2* at $V_{back} = 15$ V. This difference is attributed to the different termination as well. In addition, HV 1 of ID 7 shows an increase in the top current voltage due to the lower bias (3.3 V) applied to the guard ring connected with the FIB. HV 2 of ID 7 is not shown because the sensor was not working.

After the extraction of the breakdown voltage, it was possible to evaluate the minimum bias for which the multiplication starts. An infra-red LED was placed on top of MadPIX. The diode shines photons on the sample, inducing an increase in the leakage current. In Fig. 5.19a, i_{top} is reported as a function of V_{top} when the IR was on. The absolute values cannot be compared due to a misalignment between the test board and the LED; however, the behaviour does not depend on the setup. HV 2 shows an increase at roughly 25 V, where the multiplication starts, while in HV 1, the current grows at 15 V. This difference can always be traced to the distinct edge terminations characterising the two layouts.



(a) (b)

Figure 5.18: MadPIX i_{top} as a function of the collection electrode bias measured after FIB (a) and as a function of V_{back} (b). In (a), the substrate voltage was fixed at 30 V, while in (b), V_{top} was biased at 45 V.



(a) (b)

Figure 5.19: MadPIX i_{top} as a function of the collection electrode bias measured after FIB under an infra-red diode (a). In (b), the breakdown voltage dependence on the substrate bias is proposed.

Lastly, the effect of substrate bias on breakdown voltage is depicted in Fig. 5.19b. The breakdown shifts to a lower voltage if the substrate bias increases, due to a boost in the electric field. Hence, the breakdown voltage is reached for a lower V_{top}.

5.2.2 Electronics characterisation

For each device, the power consumption of the ASIC was measured. In particular, the power drawn from the front-end and from the 3.3 V buffers. ID 4 was not measured because it was always in compliance due to an error in the bonding, while ID 7 was not characterised because the sensor was not functioning, as shown in the previous section.

In table 5.9, the current values absorbed by the 3.3 V buffers are reported. To obtain the single buffer consumption, the currents should be divided by 64.
All the matrices worked and had a similar power consumption; in particular, Matrix_2a and Matrix_1b sank a higher current. This was due to the power rail of the 3.3 V domain, nearer to the central matrices 2a and 1b.

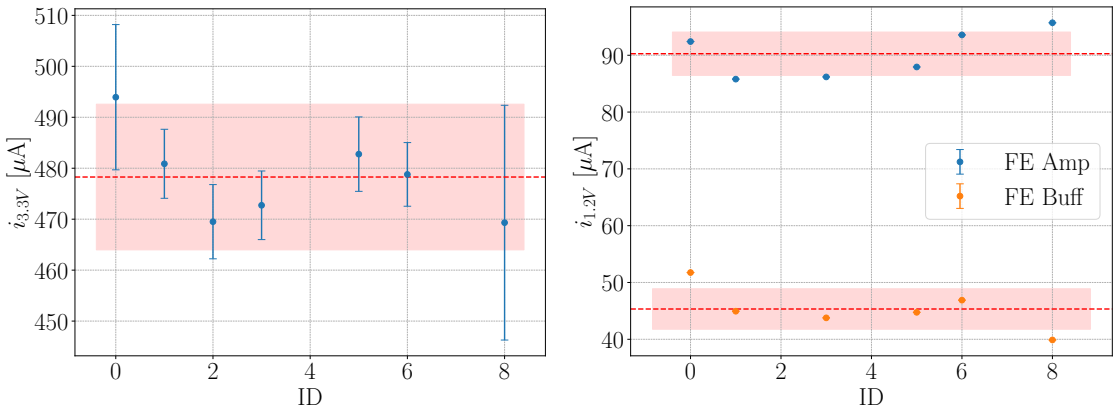
Figure 5.20a shows the mean current value drawn by a single 3.3 V buffer. The red line represents the mean value evaluated using all the samples (standard deviation shown by the light red fill), while points correspond to the mean of different IDs. The error bar represents the standard deviation. Fluctuations below 3 % were measured.

For the 1.2 V cells, it was not possible to directly measure the current drawn by each front end (A and B). Nevertheless, by modifying the transistors biases,

Table 5.9: Total current drawn from the 64 3.3 V analog buffer present inside a matrix measured in mA.

ID	0	1	2	3	4	5	6	7	8
Matrix_1a_top	31.5	31.2	30.3	30.7	-	31.1	31.0	-	32.1
Matrix_2a_top	33.2	32.2	31.4	31.5	-	32.2	32.0	-	32.8
Matrix_1b_top	33.5	32.1	31.4	31.6	-	32.1	32.0	-	32.8
Matrix_2b_top	31.6	31.3	30.7	30.6	-	31.3	31.2	-	32.2
Matrix_1a_bot	31.8	31.2	30.4	31.0	-	31.6	31.2	-	29.6
Matrix_2a_bot	33.7	32.2	31.5	31.6	-	32.5	32.0	-	29.4
Matrix_1b_bot	33.7	32.2	31.5	31.8	-	32.4	32.0	-	29.3
Matrix_2b_bot	31.8	31.5	30.7	30.8	-	31.7	31.4	-	29.6

some general considerations could be drawn. For example, it was possible to verify the proper operation of the system.
The cascode transistor of the split bias was turned off by setting V_casp to 1.2 V and the current flowing in this branch was thus evaluated as the difference between the total and $V\_casp = 1.2\,\text{V}$ current. To obtain the mean value per pixel, this value should then be divided by 256. Instead, by setting $V\_casp = 1.2\,\text{V}$ and $V\_casn = 0\,\text{V}$ the amplifier was turned off. Just the 1.2 V buffers were still active. Concerning the split bias, by subtracting the measured value from the total one,



(a) (b)

Figure 5.20: Mean current absorbed by a 3.3 V buffer (a) and a 1.2 V front end (b). In (b), the contributions from the buffer and amplifier are reported separately. The red dotted line is the mean, while the transparent red area underlines the $\pm 1\sigma$ region.

Table 5.10: Current drawn by the 1.2 V bias, the results are in mA.

ID	0	1	2	3	4	5	6	7	8
Current 1.2 V	74.1	67.3	52.0	66.8	-	68.3	72.3	-	69.8
Split bias A	9.1	8.9	0.2	9.2	-	9.2	9.6	-	9.3
Split bias B	9.1	8.7	9.2	9.2	-	9.3	9.6	-	9.2
Amp A + Amp B	47.5	44.1	37.2	44.3	-	45.2	48.1	-	49.2
Buff A + Buff B	26.6	23.1	14.6	22.5	-	23.0	24.1	-	23.5
FE A + Buff B	23.5	22.0	15.1	22.1	-	22.5	23.9	-	24.7
FE B + Buff A	24.0	22.2	22.3	22.2	-	22.8	24.3	-	24.6

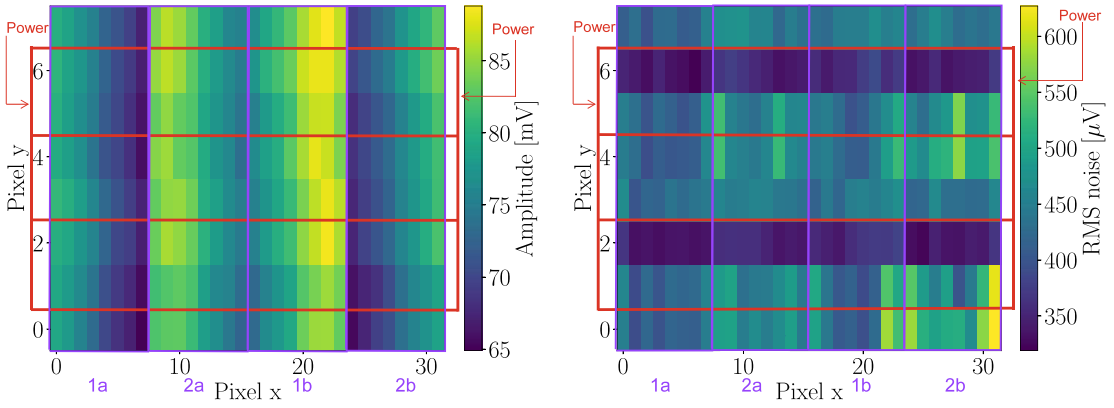
the amplifier current was estimated. For the single cell, the results should be divided by 512. Lastly, by switching off only one amplifier, i.e. A or B, some insights into the working matrix were obtained.

In table 5.10, the values extracted for different IDs are reported. The value corresponds to total currents; no pixel division was performed. The A part of ID 2 was not functioning properly; the current difference, which gives FE A + Buff B and the split bias A shows values not compatible with the others. The split bias currents are stable, while some fluctuations can be observed in the other measurements. However, if the current for a single cell is extracted, the fluctuations are minimal, i.e., below 5 % (Fig. 5.20b).
The front-end measured current ($\approx 135\,\mu$A) is lower than what was expected from simulations ($\approx 160\,\mu$A) due to the voltage drop inside the matrices.

After the static characterisation, ID 1 was characterised with the test pulse. In table 5.11, the bias voltages used for the TP characterisation are reported. Figure 5.21a displays the mean signal amplitude of each pixel, while Fig. 5.21b shows the noise. The amplitude map shows a pattern due to the 1.2 V power distribution grid. The signal decreases by going from each matrix border to the chip centre. Indeed, the 1.2 V power rail is provided from left and right. The power grid is

Table 5.11: Test pulse settings used to test ID 1 chip.

Parameter	**Value**
Number of TP	1000
V_{top}	32.5 V
V_{back}	18.0 V
TP width	5 ns
TP period	1 ms



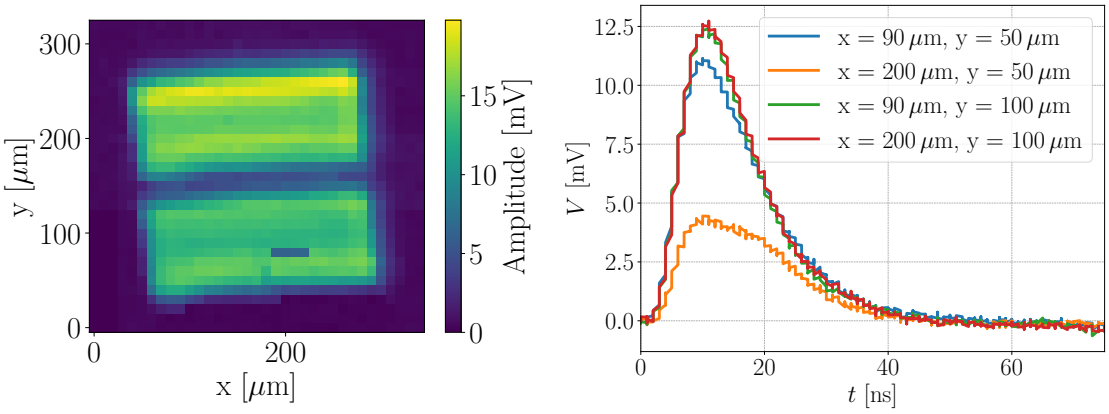
(a) (b)

Figure 5.21: Maximum amplitude measured with the test pulse (a) and RMS noise (b) for each pixel. The purple squares represent the matrices, whilst the red lines show the power grid.

shown in red in Fig. 5.21a and 5.21b; no connecting vertical line is present inside the matrices. The furthest point from the input power line is the bottom right corner of each matrix, where the amplitude reaches the minimum.
The difference between lateral (*1a* and *2b*) and central matrices (*2a* and *1b*) is given by the output buffers power. The external matrices are further away from the pads that supply the 3.3V power, so the signal is lower due to the line resistive drop. Although the noise map shows greater relative variation compared to the amplitude map, it does not exhibit a clearly defined gradient Furthermore, it can be noted that columns 2 and 6 exhibit a lower noise.

Unfortunately, the TP could not be used for estimating the jitter due to the RC network generated in the chip. Indeed, even if just 4 pixels are read at the same time, the TP circuit of Fig. 5.2 supplies the voltage step to all pixels. Each pixel has a 1 MΩ resistor between HV line and collection electrode, which can be represented as a capacitance to ground. The TP circuit sees a parallel of 256 resistors placed in series with the detector capacitance. The time constant is in the order of μs, not suitable for timing.

ID 5 chip was also characterised with the IR laser setup. Figure 5.22a shows the amplitude map as a function of the laser impinging position for the two pixels studied, 2 and 3. The laser was not focused, and thus the spot had a $\approx 10\,\mu$m radius. The chip was front-side illuminated, hence the amplitude increased where any metal lines are present. In the centre, the coupling capacitance partially shields the photons, while in between pixels, no signal is present due to a drop in efficiency. The signal shape does not change considerably inside the pixels; indeed,

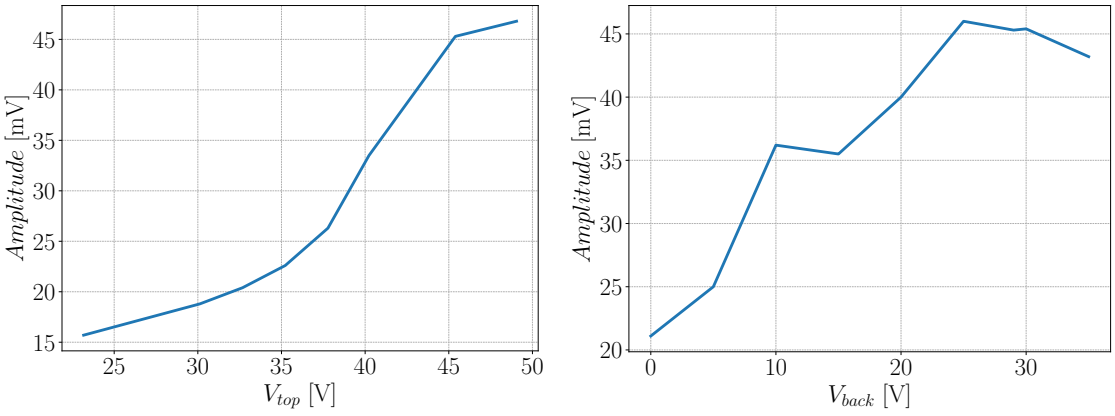


(a) (b)

Figure 5.22: Signal amplitude map obtained using an IR laser (a). Mean signals evaluated by averaging 1000 waveforms taken at different pixel positions (b).

from Fig. 5.22b, just the signal beneath the deep *p*-well has a different tail due to the long collection time of the charges generated far away from the electrode. The map and signals were acquired with $V_{top} = 45\,\text{V}$ and $V_{back} = 25\,\text{V}$.

By fixing the laser power, a scan on V_{top} (Fig. 5.23a) and V_{back} (Fig. 5.23b) was performed. The pixel under study belongs to HV 1 and, as shown in Fig. 5.14a, it reaches the full depletion above 20 V, where the signal amplitude is constant. For V_{back} above 30 V, the signal decreases due to the very high substrate current that was observed before FIB. As for V_{top}, going from 30 to 45 V, the signal increases



(a) (b)

Figure 5.23: Signal amplitude as a function of V_{top} (a) and V_{back} (b). In (a), V_{back} is fixed at 29 V, while in (b) V_{top} is constant at 45 V.

by a factor of 2.25, which is in line with the expected gain. i_{top} was measured for this non-FIB device and showed a steep increase (from 100 pA to 1 nA) at 45 V, which is consistent with laser measurements.

Lastly, the jitter was evaluated by focusing the laser on a fixed spot and changing its intensity. The signal amplitude was then increasing. The σ_t of the time difference between the TTL laser trigger and the MadPIX signal represented the total time resolution. The laser does not have the Landau contribution or distortion terms. The former because photons interact with matter following an exponential decrease, and hence the amount of released energy is always the same (fixing the active thickness of the material). The latter is due to a fixed impinging position of the laser.

Figure 5.24 shows the jitter contribution as a function of the signal amplitude. 50 ps is the intrinsic limit to jitter with this power consumption due to a slew rate limitation. Indeed, the 1.2 V buffer did not sink enough current to drive the RC network generated by the metal lines which connected the pixel front end to the 3.3 V buffer placed outside matrices.

Further measurements showed that this limitation was due to an incorrect parameter set on the TB, which limited the slew rate, and that a resolution below 30 ps could be achieved as predicted by the simulations presented in Sec 4.4.

5.2.3 Data analysis of CERN beam test

Two beam tests were conducted at CERN. The first, in October 2023, validated the readout system and evaluated the baseline performance of MadPIX. The second test, carried out in June 2024, focused on a systematic scan of MadPIX operating

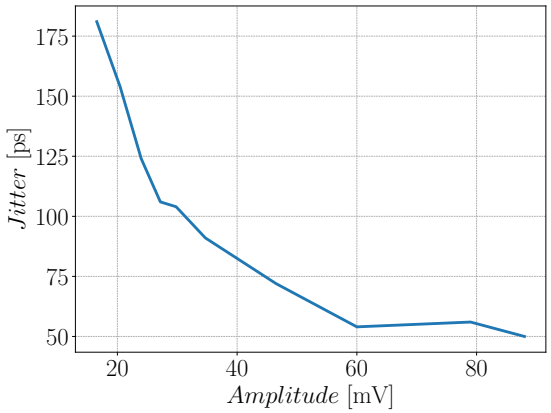


Figure 5.24: MadPIX jitter as a function of the output signal amplitude measured using an IR laser. The measurement was performed with $V_{back} = 25$ V and $V_{top} = 45$ V.

parameters. The results of both BTs are presented in the following paragraphs.

October 2023 BT Using the setup described in 5.1.3, it was possible to test two chips during the October 2023 beam test at CERN.

The chips under study were IDs 6 and 1. In table 5.6, ID 1 is reported with 64 bonded pixels; however, before the BT, all bonds were removed except for 4 corresponding to pixels 8, 9, 10, 11 (2 columns more on the edge compared to ID 6).

A list of the runs is reported in table 5.12, which describes the bonded pixels and the AND logic trigger with the LGAD. The substrate and collection electrode voltages were based on the working point extracted by passive structures, i.e. substrate voltage fixed at 35 V, while altering V_{top}. Runs 10 and 11 were acquired with a higher front-end current to see if some improvement could have been achieved.

Table 5.12: Runs list and pixel chosen for the AND trigger logic with LGAD during the October 2023 beam test.

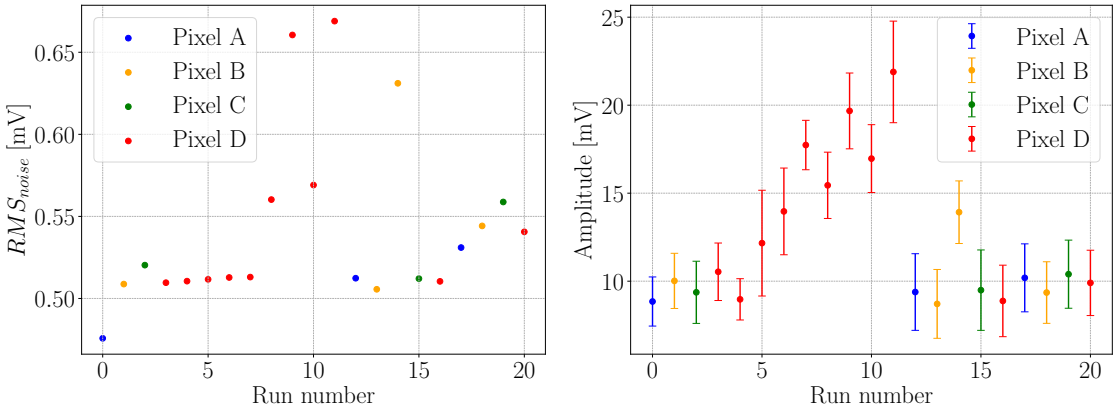
Run	**ID**	**A**	**B**	**C**	**D**	V_{top}[V]	**Sensor layout**	**Boost**
0	6	x				32.5	A2	
1	6		x			32.5	A2	
2	6			x		32.5	A2	
3	6				x	32.5	A2	
4	6				x	30.0	A2	
5	6				x	35.0	A2	
6	6				x	37.5	A2	
7	6				x	40.0	A2	
8	6				x	45.0	A1	
9	6				x	45.0	A2	
10	6				x	45.0	A1	x
11	6				x	45.0	A2	x
12	1	x				32.5	A1	
13	1		x			32.5	A1	
14	1		x			40.0	A1	
15	1			x		32.5	A1	
16	1				x	32.5	A1	
17	1	x				32.5	A2	
18	1		x			32.5	A2	
19	1			x		32.5	A2	
20	1				x	32.5	A2	

The waveforms acquired in each run were analysed and the noise extracted. One point was taken before the signal region from all the waveforms in different runs, always at a fixed time. Figure 5.25a shows the RMS_{noise} in each run for the pixel under study, while Fig. 5.25b reports the most probable value extracted by fitting the signal amplitude distribution.

As can be observed, the noise is stable in all runs apart from 8, 9, 10, and 11. This was due to the increase of V_{top} to 45 V, where from IV the intrinsic gain starts. From Fig. 5.25a, sensor *layout 1* had a lower noise compared to sensor *layout 2*, due to the different sensor capacitance. The ID 1 chip exhibited slightly higher noise compared to ID 6, and it showed the same noise increase in pixel B going from $V_{top} = 32.5$ V to 40 V. The noise was around 0.66 mV when the sensor gain was in place and 0.52 ± 0.03 mV (*layout 2*) or 0.51 ± 0.03 mV (*layout 1*) with $V_{top} = 32.5$ V. These results, measured without gain, are compatible with the predictions presented in Sec. 4.4.

The maximum amplitude for $V_{top} = 32.5$ V was 9.1 ± 0.4 mV in *layout 1* and 9.8 ± 0.6 mV in 2. The 1 was lower than 2 as observed for the test pulse due to a distinct sensor capacitance. At $V_{top} = 45$ V the maximum amplitude reaches 15.4 mV (1) and 19.7 mV (2), which translates to a sensor gain a little bit higher than 2 as observed from laser measurements. By increasing the FE current, the signal amplitude was increased by 10 %.

The Landau distributions for sensor *layouts 1* and *2* are shown in Fig. 5.26. *Layout 2* presents a population at low amplitude, i.e. between 5 mV and 15 mV, which is not present in the other structure. As explained in [96] and Sec. 2.3,



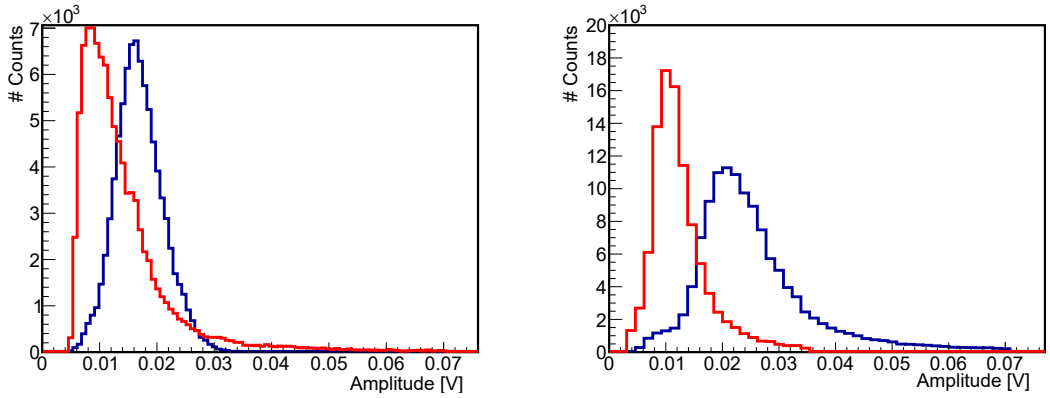
(a) (b)

Figure 5.25: Noise (a) and amplitude MPV (b) extracted by analysing the results of October 2023 TB as a function of the run number.

layout 1 has a different termination compared to *layout 2*. The first one allows the multiplication of deposited charge at borders, while in *layout 2*, at low V_{top} such as 45 V, the electric field is not strong enough to trigger the avalanche. This behavior can also be observed in Monte Carlo simulations presented in Chapter 3, where the gain was studied as a function of the in-pixel position for *layout 2* (Sec. 3.2.3). In particular, as shown in Fig. 3.24b, particles impinging near the pixel borders generate signals with significantly lower gain, contributing to the low-amplitude population ($< 10, \text{mV}$) observed in the Landau distribution.

After the amplitude study, the time resolution was evaluated. The time stamp given by a sensor might be extracted using different algorithms, such as Constant Fraction Discriminator (CFD), Constant Fraction (CF), and Leading Edge (LE). The LE is based on a fixed threshold applied to the input signal, and the time stamp is the time at which the signal crosses this threshold. The LE is one of the easiest ways to extract the time stamp in a hardware implementation; it is affected by time walk, i.e. signals with different amplitudes cross the threshold at various times (Eq. 1.1). The other two are similar; the first one may be implemented in hardware [139, 140, 141], while the second is a software algorithm, both of which extract the time at a certain percentage of the maximum signal amplitude to remove the time walk contribution. If the LE is applied, the time walk must be corrected for the amplitude or a proportional quantity, for example, the Time Over Threshold or the rising time of the signal.

In the beam tests, the full waveform was sampled using an oscilloscope-based readout. The time walk effect was corrected with the signal amplitude. The time



(a) (b)

Figure 5.26: Landau distribution for sensor *layout 1* (a) and *2* (b) measured by pixel D. In red the amplitude histogram at $V_{top} = 30\,\text{V}$ (run 4) and $V_{top} = 32.5\,\text{V}$ (run 16), while in blue at $V_{top} = 45\,\text{V}$ (runs 8 and 9).

resolution dependence is shown in Figure 5.27a.

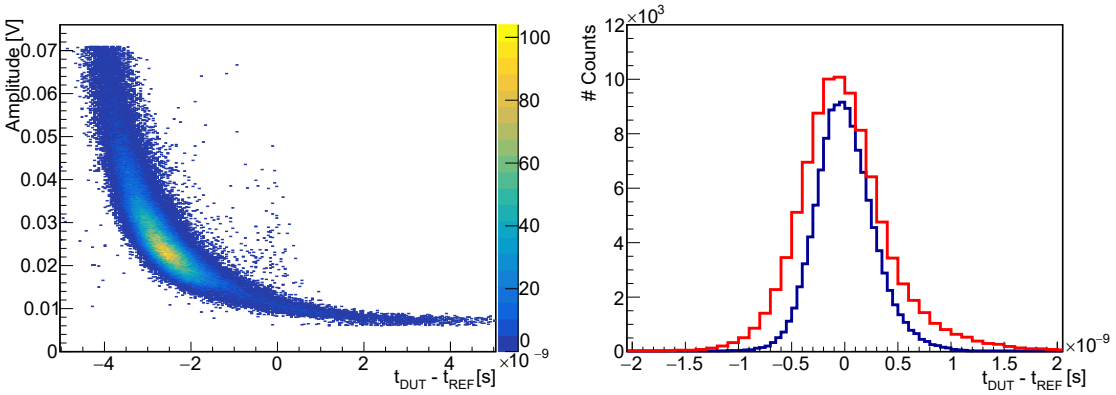
The function used to correct for the undesired effect on the time difference is the following:

$$\text{Amplitude} = a + \frac{b}{\text{t}_{\text{DUT}} - \text{t}_{\text{REF}}} + \frac{c}{(\text{t}_{\text{DUT}} - \text{t}_{\text{REF}})^2}; \tag{5.1}$$

For *Run 3*, the LE type was chosen due to a systematic time resolution worsening for CFD above 40 %. This effect is visible in the Monte Carlo simulation, when V_{top} is not enough to eliminate the potential minimum beneath the gain layer. Indeed, at high CF, the time difference reveals 2 peaks, due to two signal components, i.e. fast and slow (electrons and holes). By choosing the LE, this effect is minimised because the threshold is set well below 50 % of the measured MPV.

The time difference between DUT (MadPIX) and reference (LGAD) was evaluated, and it is plotted in Fig. 5.27b for two collection electrode voltages. As expected, the distribution shrinks, raising V_{top}.

To get the time resolution, the histograms are fitted with a q-Gaussian function (Eq. 5.2) to account for the non-Gaussian tail. This effect is due to the position-dependent delay in the pixel, as demonstrated in DESY BT results. In the q-Gaussian fit, A is a normalisation factor, μ is the mean value of the distribution, σ is the time resolution, i.e. the Gaussian standard deviation. q_R and q_L are the parameter that describes the non-Gaussian tail (right and left tails). For $q \to 1$, the fit is a standard normal distribution. In MadPIX, one of the two tails is Gaussian,



(a) (b)

Figure 5.27: Time difference dependence on amplitude for run 9 with $V_{top} = 45\,\text{V}$ (a) and time resolution after time walk correction for run 9 in red and 4 in blue for $V_{top} = 30\,\text{V}$ (b).

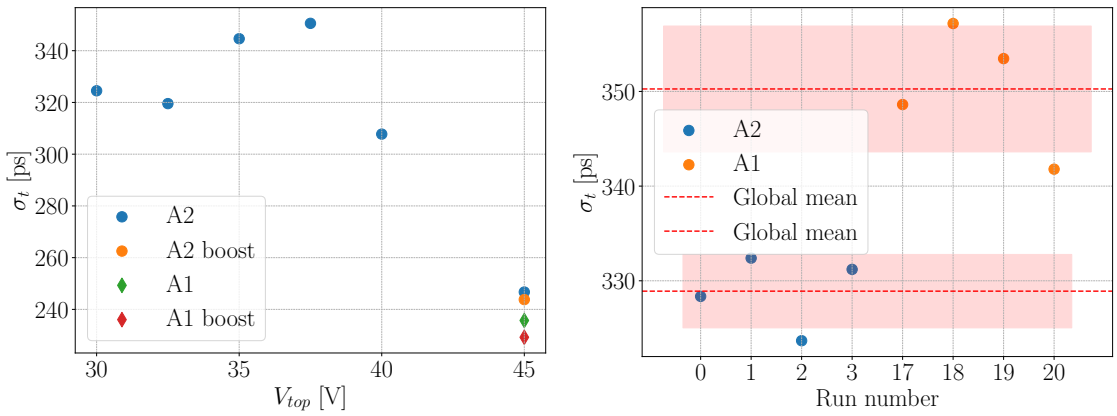
while the other contains higher statistics due to the signal delay observed at pixel edges.

$$f(x) = \begin{cases} A \cdot \left[1 - \frac{(1-q_L)}{3-q_L} \cdot \frac{(x-\mu)^2}{\sigma^2}\right]^{\frac{1}{1-q_L}}, & \text{if } x \leq \mu \\ A \cdot \left[1 - \frac{(1-q_R)}{3-q_R} \cdot \frac{(x-\mu)^2}{\sigma^2}\right]^{\frac{1}{1-q_R}}, & \text{if } x > \mu \end{cases} \tag{5.2}$$

The time resolution for the ID 6 chip as a function of the applied LE threshold is reported in figure 5.28a. *Layout 1* is performing better than *layout 2*, due to a more uniform electric field between edges and centre. From 32.5 to 37.5 V of V_{top}, the time resolution is worsening due to the start of the avalanche process. Then the resolution improves up to 45 V. By increasing the front-end power, the time resolution is lower due to the slight amplitude increase (lower jitter).

Figure 5.28b reports the time resolution measured at 32.5 V for different pixels using a LE threshold of 3 mV for *layout 1* and 4 mV for 2, for which the best time resolution was extracted. The best performance was achieved with a different threshold due to a higher signal amplitude observed in *layout 2*. The reported values do not include the LGAD contribution; this term was subtracted in quadrature. Its value is negligible, because measurements carried out in previous BT showed that its time resolution was below 30 ps [60].

The measures below 40 V were dominated by the jitter, while at 45 V the



(a) (b)

Figure 5.28: Time resolution as a function of V_{top} for *layouts 1* and *2* (a) and for different pixels with $V_{top} = 32.5$ V (b). In subfigure (b), the mean for *layouts 1* and *2* is shown in the red dotted lines, while the pink area represents the $\pm\sigma$ area. In (a), the *boost* label denotes the configuration with increased FE power consumption ($1100, \mathrm{mW/cm^2}$ instead of $660, \mathrm{mW/cm^2}$).

major contribution was the intrinsic sensor time resolution. During the BT, the maximum collection electrode voltage was chosen based on the passive structure behaviour. Indeed, at 45 V with laser, the signal stopped increasing. By studying the MadPIX IV curves shown before, during the beam test in July 2024, the collection electrode and substrate biases were adjusted to measure the effects on MadPIX time resolution.

June 2024 BT With the expertise acquired in the first beam test of October 2023, the trigger logic of the oscilloscope was set to OR to maximise the acquired data. Scans on V_{top} and V_{back} were performed to completely characterise the sensor.

The same TB used in October 2023 were put under beam (TB 2 and 3) with the same device ID in standard configuration.

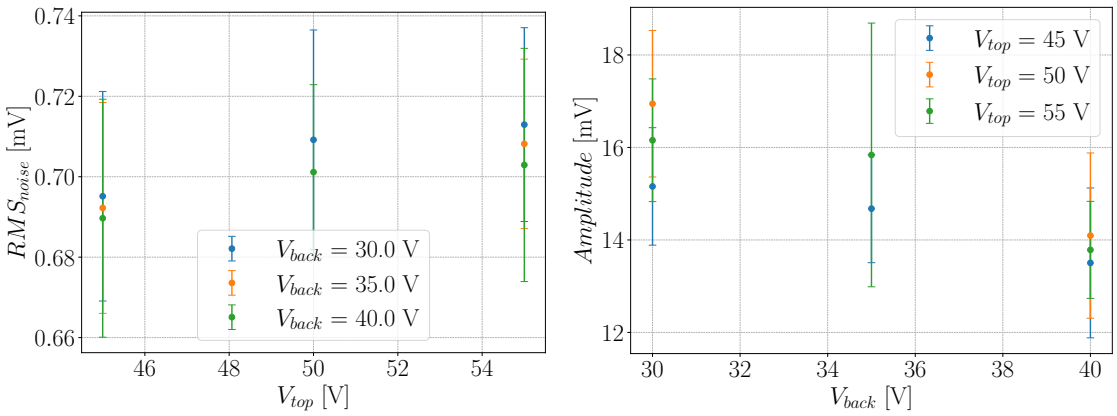
In table 5.13, the runs acquired in June TB are reported.

Table 5.13: Runs list and pixel chosen in the OR trigger logic during the June 2024 beam test.

TB	**Run**	**ID**	**A**	**B**	**C**	**D**	V_{top}	V_{back}	**Matrix**
3	0	1	x	x	x		45.0	30.0	A2
3	1	1	x	x	x		50.0	30.0	A2
3	2	1	x	x	x		55.0	30.0	A2
3	3	1	x	x	x		45.0	40.0	A2
3	4	1	x	x	x		55.0	40.0	A2
3	5	1	x	x	x		45.0	35.0	A2
3	6	1	x	x	x		55.0	35.0	A2
3	7	1	x	x	x		50.0	40.0	A2
3	8	1	x	x	x		50.0	40.0	A2
3	9	1	x	x	x		50.0	35.0	A2
3	10	1	x	x	x		58.0	40.0	A2
3	11	1	x	x	x		58.0	30.0	A2
3	12	1	x	x	x		58.0	35.0	A2
3	13	1	x	x	x		58.0	25.0	A2
3	14	1	x	x	x		58.0	45.0	A2
3	15	1	x	x	x		62.0	45.0	A2
3	16	1	x	x	x		45.0	30.0	A1
3	17	1	x	x	x		50.0	30.0	A1
3	18	1	x	x	x		55.0	30.0	A1
3	19	1	x	x	x		45.0	40.0	A1
3	20	1	x	x	x		55.0	40.0	A1
3	21	1	x	x	x		45.0	35.0	A1

3	22	1	x	x	x		55.0	35.0	A1
3	23	1	x	x	x		40.0	40.0	A1
2	24	6	x	x	x		45.0	30.0	A2
2	25	6	x	x	x		50.0	30.0	A2
2	26	6	x	x	x		55.0	30.0	A2
2	27	6	x	x	x		45.0	40.0	A2
2	28	6	x	x	x		50.0	40.0	A2
2	29	6	x	x	x		55.0	40.0	A2
2	30	6	x	x	x		45.0	35.0	A2
2	31	6	x	x	x		50.0	35.0	A2
2	32	6	x	x	x		55.0	35.0	A2
2	33	6	x	x	x		58.0	45.0	A2
2	34	6		x	x	x	58.0	27.5	A2
2	35	6		x	x	x	60.0	27.5	A2
2	36	6		x	x	x	58.0	25.0	A2
2	37	6		x	x	x	60.0	25.0	A2
2	38	6		x	x	x	58.0	22.5	A2
2	39	6		x	x	x	60.0	22.5	A2
2	40	6		x	x	x	61.0	25.0	A2
2	41	6		x	x	x	61.0	20.0	A2
2	42	6		x	x	x	61.0	17.5	A2
2	43	6		x	x	x	61.0	15.0	A2
2	44	6	x	x	x		45.0	30.0	A1
2	45	6	x	x	x		50.0	30.0	A1
2	46	6	x	x	x		55.0	30.0	A1
2	47	6	x	x	x		45.0	40.0	A1
2	48	6	x	x	x		55.0	40.0	A1
2	49	6	x	x	x		45.0	35.0	A1
2	50	6	x	x	x		55.0	35.0	A1

The noise extracted as a function of the collection electrode voltage in *layout 1* for different V_{back} is reported in Fig. 5.29a. The MPV value of the amplitude distribution is shown in Fig. 5.29b. The plots show a six-pixel average combining IDs 6 and 1 chips with the three pixels tested. The associated error is the standard deviation. The noise slightly increases if the collection electrode is raised, while it decreases if it goes from $V_{back} = 30\,\text{V}$ to $V_{back} = 40\,\text{V}$. This behaviour can be explained with Fig. 5.29b. Indeed, by increasing V_{back}, the signal amplitude shrinks. The plot reports that rising V_{top} from 45 V to 50 V the signal amplitude increases while from 50 V to 65 V decreases again. This behaviour was due to the

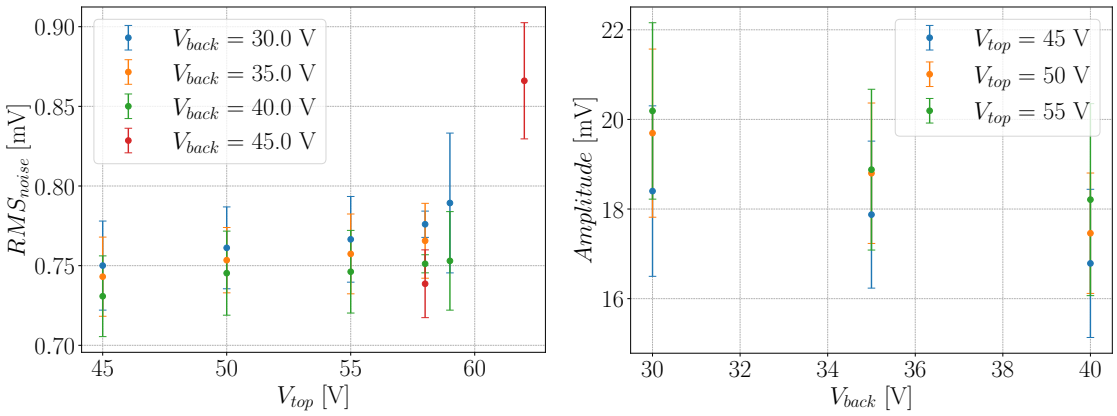


(a) (b)

Figure 5.29: Noise (a) and MPV extracted with a fit on the amplitude histogram (b) for sensor *layout 1* during the July 2024 BT. The dot represents the mean obtained by averaging the values measured for different pixels of IDs 6 and 1.

high substrate current, which was in part collected by the collection electrode. Since V_{back} is responsible for the full substrate depletion, the signal attenuation could not be explained.

A similar behaviour was observed for *layout 2*, reported in Fig. 5.30a and 5.30b. The noise increases as the collection electrode rises, reaching a maximum value at $V_{top} = 65\,\text{V}$, where the sensor is near the breakdown point. For *layout 2*,



(a) (b)

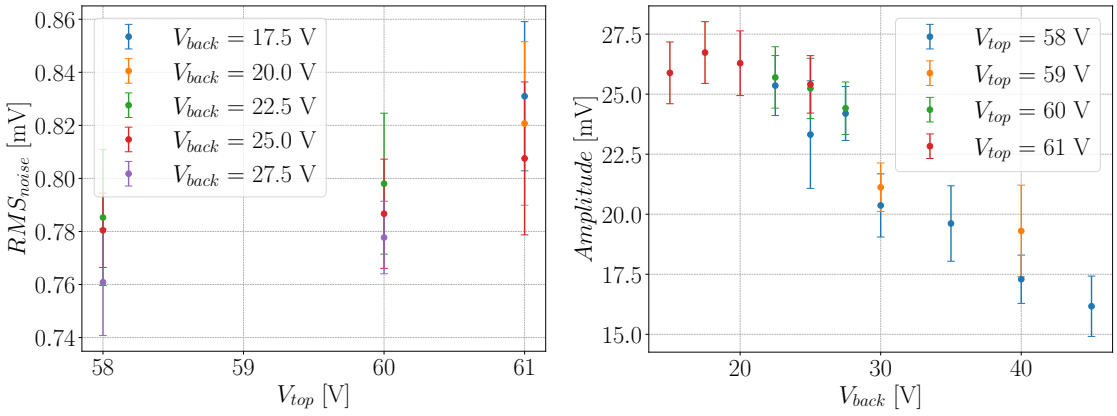
Figure 5.30: Noise (a) and MPV extracted with a fit on the amplitude histogram (b) for sensor *layout 2* during the July 2024 BT. The dot represents the mean obtained by averaging the values measured for different pixels of IDs 6 and 1.

Fig. 5.30b shows that at higher V_{top} the signal is greater. This difference compared to *layout 1* can be attributed to the diverse breakdown voltages: $\simeq 65\,\text{V}$ for *layout 2* and $\simeq 55\,\text{V}$ for *layout 1*. The unexpected signal shrinking, while V_{back} increases, can be observed in both layouts.

To better understand this behaviour, *layout 2* was studied near his breakdown point as a function of V_{back} using the ID 6 chip. Figure 5.31b underlines the unexpected trend. Indeed, going from 45 V applied to the substrate to 17.5 V, the signal is almost doubled, then it starts to decrease again for lower voltages. Comparing these results with IV curves of Fig. 5.14b, the explanation could be inferred. Above $V_{back} = 15\,\text{V}$, the substrate was depleted; however, the high bulk current was also collected from the collection electrode, altering its proper operation.

In Fig. 5.31a, the noise is plotted as a function of V_{top}, it grows with the collection electrode voltage, and it decreases with the substrate bias, as for the signal amplitude. This behavior was attributed to a shrinking of the depletion region, which leads to an increase in sensor capacitance and a reduction in the collected charge. As a result, the signal amplitude decreases, leading to a degradation of both time resolution and signal-to-noise ratio (SNR).

The time resolution was evaluated using a leading-edge algorithm. The values reported in the following plots are the average of pixels from multiple TB. Given a bias condition (V_{top}, V_{back}) a threshold scan was performed between 3 mV and 16 mV and the best result was used for the mean. In appendix A, the optimal



(a) (b)

Figure 5.31: Noise measured on sensor *layout 2* during the July 2024 BT with V_{back} lower than 28 V (a). MPV extracted with a fit on the amplitude histogram (b). The dot represents the mean obtained by averaging the values measured for three ID 6 pixels.

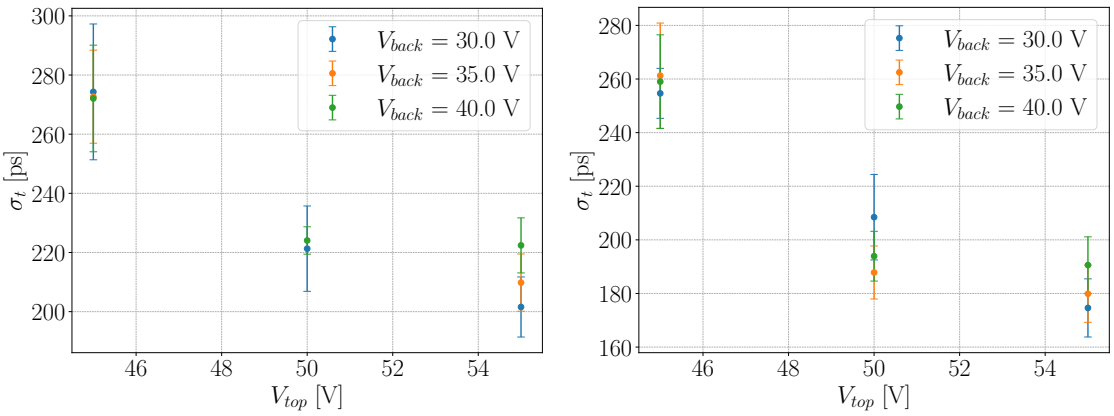


Figure 5.32: Time resolution of sensor *layouts 1* (a) and *2* (b) measured during July 2024 BT. MPV extracted with a fit on the amplitude histogram (b). The dot represents the mean obtained by averaging the values measured for three pixels of IDs 6 and 1.

threshold is reported for each channel of the two chip IDs given V_{top} and V_{back}.

Figure 5.32a shows the time resolution as a function of V_{top} for different V_{back}. The decrease cannot be explained simply by a lower jitter because the signal amplitude increase does not allow for such improvement. Additionally, at $V_{top} = 55\,\text{V}$, the time resolution decreases by lowering V_{back} due to a lower jitter. The same behaviour can be observed in Fig. 5.32b. *Layout 2* performs better than the other one thanks to the different edge termination implants. *Layout 1* collects and multiplies the charge deposited at borders, thus increasing the time resolution. Indeed, at edges, the charge needs to travel a longer path, which means that the arrival time has a deterministic delay, i.e. the time difference distribution is wider as it was predicted from MC simulations (Sec. 3.2.2).

The *layout 2* was also tested at lower V_{back}, and the results are reported in Fig. 5.33. The lowest value that was achieved is $137 \pm 2\,\text{ps}$ measured for $V_{back} = 15\,\text{V}$ and $V_{top} = 61\,\text{V}$. The measured trend can be attributed to the jitter reduction due to the amplitude increase. From laser measurement, the expected jitter for a signal with an amplitude of 25 mV is around 110 ps. The sensor contribution to the total time resolution can be extracted as the quadrature difference between the two terms. The extrapolated sensor resolution is 80 ps. MC simulations with similar bias conditions predict a time resolution evaluated at 50 % CF between 60 ps and 100 ps depending on the map (Sec. 3.2.2).

After the first beam test, the FIB procedure described in Sec. 5.2.1 was performed.

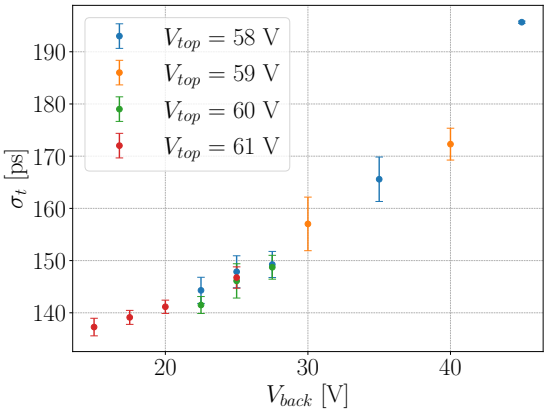


Figure 5.33: Time resolution measured on sensor *layout 2* during the July 2024 BT with V_{top} higher than 58 V. The dot represents the mean obtained by averaging the values measured for three pixels of ID 6.

October 2024 BT During this beam test, the ID 8 chip was characterised. The list of biasing points is shown in table 5.14.

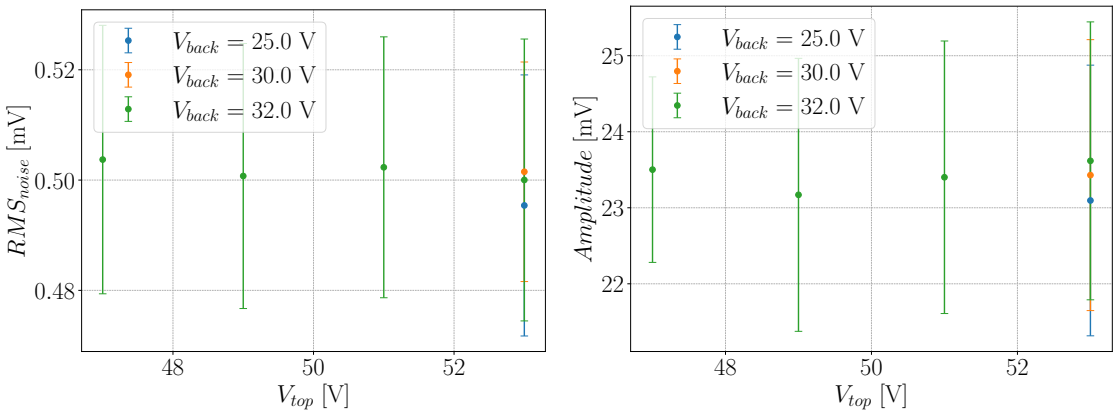
Table 5.14: Runs list and pixel chosen in the OR trigger logic during the October 2024 beam test.

Run	**ID**	**A**	**B**	**C**	**D**	V_{top}	V_{back}	**Matrix**	**Boost**
0	8	x	x	x		47.0	32.0	A1	
1	8	x	x	x		49.0	32.0	A1	
2	8	x	x	x		51.0	32.0	A1	
3	8	x	x	x		51.0	32.0	A1	
4	8	x	x	x		53.0	25.0	A1	
5	8	x	x	x		53.0	30.0	A1	
6	8	x	x	x		53.0	30.0	A1	*
7	8	x	x	x		53.0	32.0	A1	
8	8	x	x	x		53.0	32.0	A1	*
9	8	x	x	x		56.0	32.0	A2	
10	8	x	x	x		58.0	32.0	A2	
11	8	x	x	x		58.0	32.0	A2	*
12	8	x	x	x		60.0	32.0	A2	
13	8	x	x	x		60.0	32.0	A2	*
14	8	x	x	x		62.0	32.0	A2	
15	8	x	x	x		62.0	32.0	A2	*
16	8	x	x	x		64.0	25.0	A2	
17	8	x	x	x		64.0	30.0	A2	

18	8	x	x	x	64.0	32.0	A2	
19	8	x	x	x	64.0	32.0	A2	*
20	8	x	x	x	66.0	25.0	A2	*
21	8	x	x	x	66.0	28.0	A2	*
22	8	x	x	x	66.0	30.0	A2	*
23	8	x	x	x	66.0	32.0	A2	
24	8	x	x	x	66.0	32.0	A2	*
25	8	x	x	x	68.0	32.0	A2	*

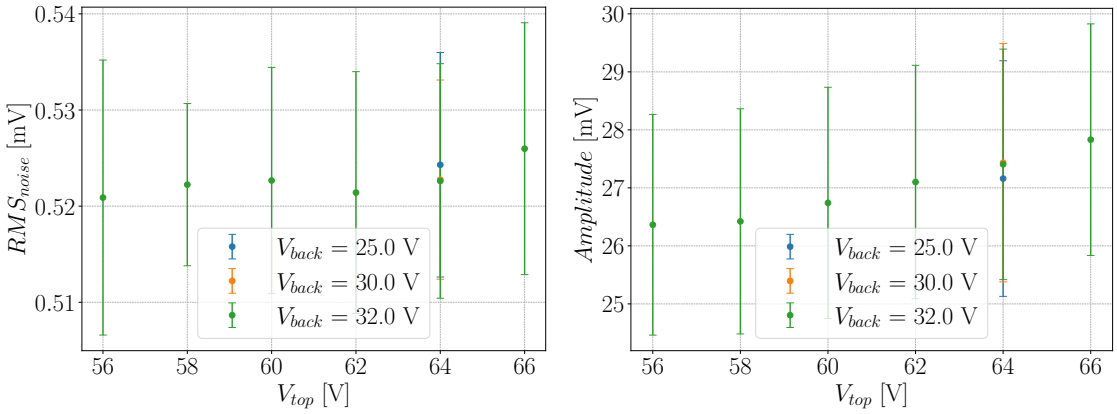
The noise and signal amplitude of *layout 1* are shown in Fig. 5.34a and 5.34b, respectively. Compared to non-FIB structures, the noise is decreased by about 35 % thanks to the lowering of the current. No dependence on V_{back} and V_{top} is observed. The amplitude shows a 30 % increase, and no strong dependence on V_{back} and V_{top}. The signal should not increase after the full depletion ($V_{back} > 15\,\text{V}$). Instead, V_{top} manages the gain and has a strong effect on the gain value; however, for such a low gain, i.e. ≈ 2.5, its contribution is negligible. TCAD simulations presented in [96] show that this behaviour is well predicted in simulations matched with the profiles extracted from experimental data.

The same noise and signal amplitude measurements were performed on *layout 2*. The noise is lower (Fig. 5.35a) and the amplitude (Fig. 5.35b) is greater compared to the same structure before FIB. A slight increase in amplitude is observed by increasing V_{top}, while no changes are present for different V_{back}. Thanks to the



(a) (b)

Figure 5.34: Noise (a) and MPV extracted with a fit on the amplitude histogram (b) for sensor *layout 1* during the October 2024 BT. The dot represents the mean obtained by averaging the values measured for three different pixels of ID 8 on which the FIB was performed.



(a) (b)

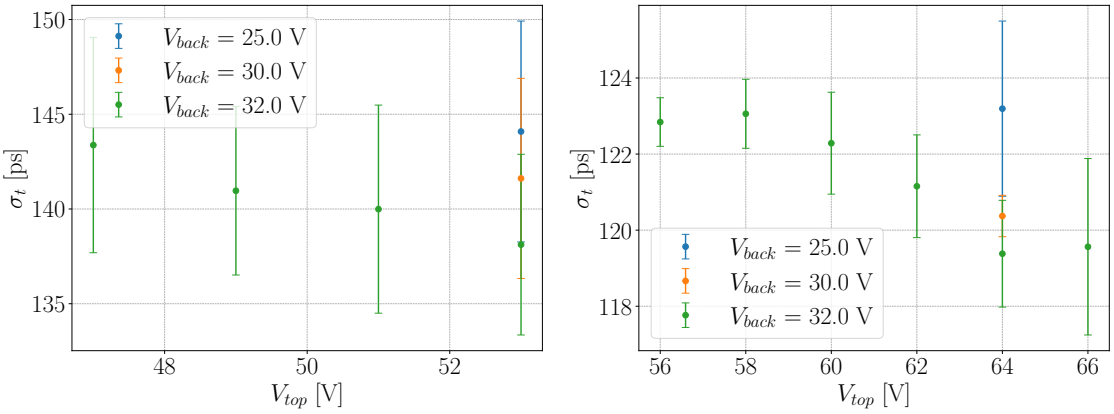
Figure 5.35: Noise (a) and MPV extracted with a fit on the amplitude histogram (b) for sensor *layout 2* during the October 2024 BT. The dot represents the mean obtained by averaging the values measured for three different pixels of ID 8 on which the FIB was performed.

substrate current reduction, both the noise spike present at 65 V and the wrong amplitude behaviour as a function of V_{back} were corrected.

As will be shown by analysing *Run 3.2* data, the amplitude of a MadPIX without a gain layer is around 10 mV, hence the gain extracted for the *Run 3* production was between 2.6 and 2.8, depending on the bias voltage of V_{top}. This result is in good agreement with MC simulations (Sec. 3.2.2), which predict a gain of 3. Also the FE electronics gain is compatible with post-layout simulations presented in Sec. 4.4 (20 mV/fC).

The time resolution is reported in Fig. 5.36a and 5.36b (*layouts 1* and *2*). Increasing V_{top}, the time resolution improves due to higher signal amplitude, which means lower jitter. Instead, if V_{back} grows, the resolution is lowered because the carriers are reaching their saturation velocity, but also because the electric field minimum present beneath the collection electrode increases (Sec. 3.2.2). The best time resolution is 119.4 ± 1.4 ps measured for $V_{top} = 64$ V and $V_{back} = 32$ V. For laser measurement, a jitter of 100 ps was found for an output signal amplitude of 27 mV, which is compatible with BT results. The sensor time resolution, i.e. 65 ps is similar to the 62 ps evaluated for CF 50 % in a Monte Carlo simulation (Sec. 3.2.2). The sensor time resolution is estimated by subtracting the jitter from the total resolution in quadrature.

By increasing the front end power from 165 μW to 280 μW, the jitter was lowered and hence the total time resolution achieved 122.8 ± 0.6 ps for *layout 1* and 100 ± 2 ps for *layout 2*.



(a) (b)

Figure 5.36: Time resolution of sensor *layouts 1* (a) and *2* (b) measured during October 2024 BT. The dot represents the mean obtained by averaging the values measured for three different pixels of ID 8 on which the FIB was performed

Appendix A reports all time resolution values with the mean leading edge used for each configuration, with the associated standard deviation.

Table 5.15 summarises the results achieved with *Run 3* MadPIX after FIB.

Table 5.15: Summary of the MadPIX results - *Run 3*. In brackets, the results obtained with a higher FE power consumption.

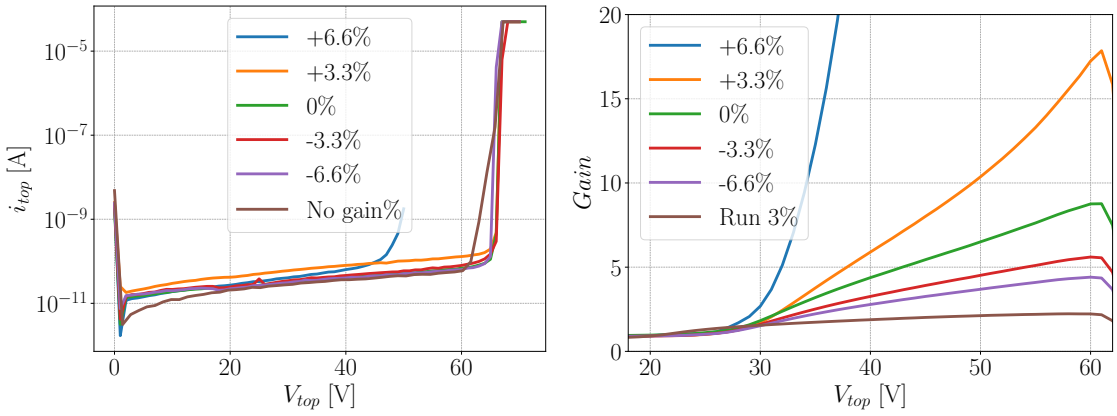
	MadPIX *Run 3*	
Technology	LFoundry 110 nm	
Pixel size [μm^2]	250×100	
Thickness [μm]	48	
Sensor gain	$2.6 \div 2.8$	
FE power consumption [mW/cm^2]	660 (1100)	
Punch-through [V]	35	
Jitter [ps]	≈ 100 (75)	
Layout	1	2
Breakdown [V]	58	67
Time resolution [ps]	138 ± 5 (99 ± 4)	119 ± 1 (117 ± 3)

5.3 ARCADIA *Run 3.2*

After the first production, a short loop was submitted in which the gain layer doping was tuned to match the gain requirement. The gain target, as predicted from the simulation, was between 10 and 20. Different splits were produced alongside the reference dose to cope with process variations: -6.6 %, -3.3 %, +3.3 %, 6.6 %, and one wafer without a gain layer. This last split was crucial to measure the exact gain of MadPIX.

5.3.1 Sensor characterisation

The characterised chip belonged to the three most promising dose splits: -3.3 %, reference and 3.3 % ones. From IV curves obtained testing passive structures, the -6.6 % was in line with *Run 3* gain, i.e. gain below 5. The +6.6 % showed a too early breakdown due to a very high electric field. In Fig. 5.37a, the i_{top} for different splits as a function of V_{top} is plotted. The +6.6 % split reaches breakdown before 50 V while all the others can be biased above 60 V. This effect was explained by an edge breakdown, which does not depend on the gain layer doping. The early breakdown of the +6.6 % split was due to the high electric field beneath the collection electrode. If the device was then illuminated with the IR led, as was done for *Run 3*, a preliminary gain value can be obtained by dividing the measured i_{top} leakage current by the same i_{top} value extracted using the same structure without gain.



(a) (b)

Figure 5.37: i_{top} as a function of V_{top} for the splits of *Run 3.2* (a) and gain extracted using the ratio of leakage current beneath an IR led (b). (a) and (b) are measures carried on the passive structures on the sensor flavour 2 with $V_{back} = 35$ V. (b) reports also the gain of a *Run 3* passive structure.

Table 5.16: List of ASICs tested for *Run 3.2* production with extraction wafer, reticle direction, used test board, number of pixels bonded, and dose split.

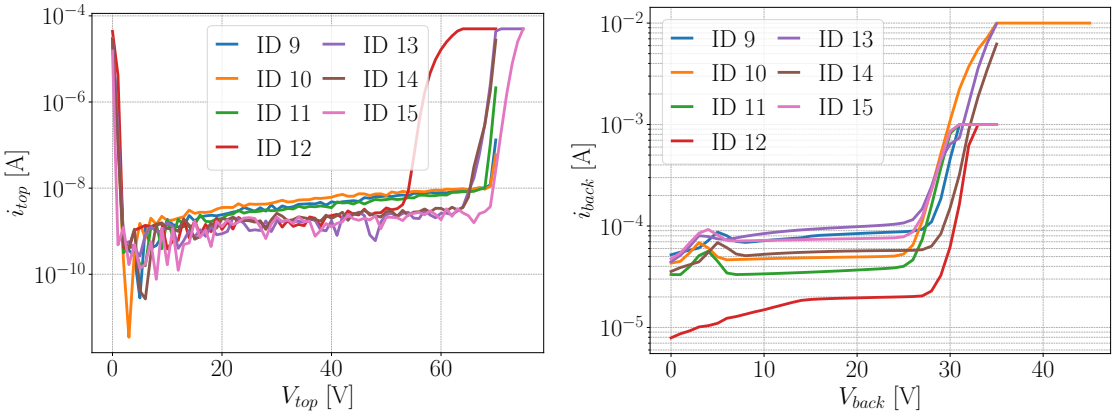
Identifier (ID)	Wafer	Position	TB	Pixels	Dose split
9	15	W	1	4 (0,1,2,3)	Reference
10	15	W	3	4 (0,1,2,3)	Reference
11	6	W	2	4 (0,1,2,3)	-3.3%
12	3		4	4 (0,1,2,3)	No gain
13	8	W	6	4 (0,1,2,3)	+3.3%
14	8	C	4	4 (0,1,2,3)	+3.3 %
15	-	-	5	4 (0,1,2,3)	Reference

The measured values are shown in Fig. 5.37b. The most promising splits are +3.3 %, the reference dose, and the -3.3 %, where the gain stands in the range between 5 and 17. The drop after 60 V is due to the breakdown of the no-gain structure, which starts earlier than the other splits (Fig. 5.37a). Unlike *Run 3*, sensor *layout 1* was not tested due to the premature border breakdown, which did not allow the bias of these types of structures. The absence of the gap of *layout 1* did not allow pushing the collection electrode above 40 V, where the multiplication starts inside the gain layer.

The MadPIX bonded, and their characteristics are summarised in table 5.16. For this run, only the direction inside wafers was annotated: North, South, East, West. All the *Run 3.2* chips that were tested were prototypes on which the FIB operation was performed.

The IV characteristic was extracted only for HV 2 structures due to an early breakdown of *layout 1*. Figure 5.38a shows i_{top} as a function of V_{top}. The current is stable below 10 nA up to the breakdown point at ≈ 65 V. ID 12 shows an increase in the current 10 V before other structures because no gain was implanted. i_{top} is the sum of 128 pixels; hence, the value per pixel is in the order of 100 pA, which is in line with passive structures. The breakdown point is shifted compared to passive structures due to the 1MΩ resistor connected between the bias line and the collection electrode. This circuit element behaves like a quenching resistor for SiPM, allowing for an HV bias increase of $1 \div 2$ V more than passive structures.

Figure 5.38b shows the i_{back} dependence on V_{back}. The substrate current is below 0.1 mA up to punch-through voltage ($\simeq 28$ V). i_{back} cannot be compared with passive structures due to the different area occupied by deep p-wells and the total chip area. From the plot, ID 12 has a lower substrate current due to the absence of a gain layer. The punch-through point is 5 V lower compared to *Run 3*, probably due to a slightly different value of the epitaxial layer resistivity.



(a) (b)

Figure 5.38: i_{top} as a function of V_{top} (a), and i_{back} as a function of V_{back} (b) for MadPIX of *Run 3.2*. In (a) V_{back} is fixed at 25 V, while in (b) $V_{top} = 45$ V.

i_{top} was studied as a function of the substrate bias, in order to find the depletion voltage (Fig. 5.39). At 10 V, the conductive channel between guard ring and collection electrode is closed and i_{top} drops below 10 nA. ID 12 is depleted at higher voltages due to the stronger conduction channel, which is created in the absence of the gain implant.

5.3.2 Electronics characterisation

The current sunk by the 3.3 V buffers is summarised in table 5.17 for each ID. The bottom matrices of ID 10 were not bonded, and hence they were not tested.

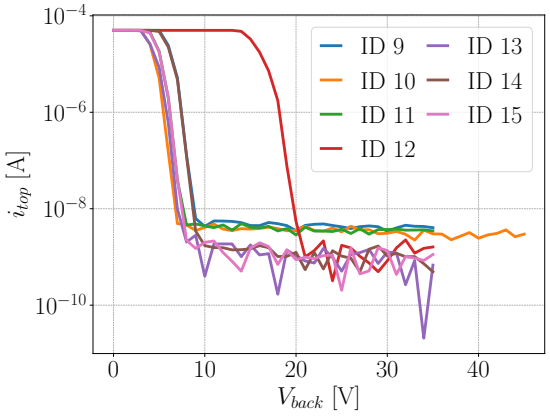


Figure 5.39: i_{top} as a function of V_{back} for the splits of *Run 3.2*, V_{top} is fixed at 45 V.

Table 5.17: Total current drawn from the 64 3.3 V analog buffer present inside a matrix measured in mA for *Run 3.2* production.

ID	9	10	11	12	13	14	15
Matrix_1a_top	31.1	31.7	31.0	30.8	30.0	-	-
Matrix_2a_top	32.0	32.9	31.9	32.0	30.0	-	-
Matrix_1b_top	32.1	32.9	31.8	32.0	31.0	-	-
Matrix_2b_top	31.3	31.9	31.1	31.1	31.0	-	-
Matrix_1a_bot	30.8	-	30.8	30.8	30.8	-	-
Matrix_2a_bot	31.7	-	31.7	31.7	31.7	-	-
Matrix_1b_bot	31.9	-	31.6	31.6	31.8	-	-
Matrix_2b_bot	31.2	-	31.0	31.0	31.2	-	-

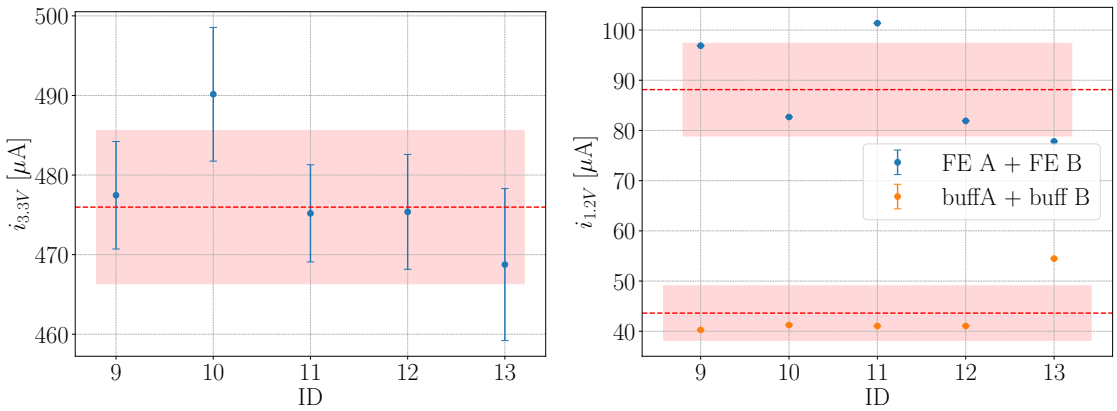
Neither ID 14 nor ID 15 were characterised, the first due to time constraints before beam tests and the second due to problems with the test board.

All the matrices draw compatible currents; as for *Run 3*, the central matrices (2a and 1b) are more power hungry due to power lines. Figure 5.40a shows the mean current value of one 3.3 V buffer for each chip with the light read filling for $\pm\sigma$ area. The obtained value is compatible with the one measured for *Run 3*. The variations are in the 2 % range. Table 5.18 reports the measured current for 1.2 V analog power. IDs 9 and 11 have slightly higher currents in the front end due to a different setting in the potentiometer changed to fix the slew rate loss observed when testing *Run 3* chips.

Figure 5.40b reports the current spreads between chips. ID 13 shows a very high buffer current; this is due to different assembly errors in TB 6, the potentiometer biasing 1.2 V buffers were assembled with a double value compared to what was

Table 5.18: Current drawn by the 1.2 V bias in chips produced in *Run 3.2*, the results are in mA.

ID	9	10	11	12	13	14	15
Current 1.2 V	70.6	63.7	73.2	63.2	67.0	-	-
Split bias a	11.8	8.7	13.2	9.4	9.0	-	-
Split bias b	12.3	9.2	12.7	9.4	9.0	-	-
FE A + FE B	49.8	42.5	52.1	42.1	40.0	-	-
buff A + buff B	20.7	21.2	21.1	21.1	28.0	-	-
FE A + buff B	25.4	20.3	26.2	21.0	18.0	-	-
FE B + buff A	24.5	22.2	25.9	21.1	21.0	-	-



(a) (b)

Figure 5.40: Mean current absorbed by a 3.3 V buffer (a) and a 1.2 V front end (b). In (b), the contribution from the buffer and amplifier is reported separately. The red dotted line is the mean, while the fill area underlines the $\pm 1\sigma$ region.

given by design. Also, 2 other SMD resistors were soldered on the test board with different values from the specification by the PCB vendor.

To lower the jitter, for IDs 9, 10 and 11, the power supply voltage of 1.2 V and 3.3 V was increased to 1.5 V and 3.7 V respectively to increase gain and dynamic range of the front end. Table 5.19 summarises the new 3.7 V currents only for the top matrices, i.e. the tested one during the beam tests. For simplicity, the new configuration will be named *boost*.

Table 5.20 reports the 1.5 V currents. A 35 % increase in the 1.5 V gives a 68 % total power growth due to a higher bias voltage. The highest current increase is observed in the 1.2 V buffer, which mirrors a higher current and is biased at a greater voltage.

The increase in power was useless for *Run 3.2* due to the high amount of charge deposited in the sensor, i.e. the jitter term was negligible compared to the intrinsic

Table 5.19: Total current drawn from the 64 3.7 V analog buffer present inside a matrix measured in mA for *Run 3.2* production in the *boost* configuration.

ID	9	10	11
Matrix_1a_top	79	78.5	78.3
Matrix_2a_top	84	82.5	82.1
Matrix_1b_top	84	82.6	82.1
Matrix_2b_top	81	79.4	79.0

Table 5.20: Current drawn by the 1.2 V bias increased to 1.5 V for the chip produced in *Run 3.2*. The results are reported in mA.

ID	9	10	11
Current 1.2 V	95.0	91.2	92.8
Split bias a	12.0	11.3	11.9
Split bias b	12.0	12.1	11.8
FE A + FE B	49.0	48.2	49.5
buff A + buff B	46.0	42.9	43.3
FE A + buff B	25.0	23.0	24.3
FE B + buff A	24.0	25.3	25.2

sensor time resolution. For the next short loop (planned in mid 2025), it will be crucial due to the substrate thickness reduction to 15 μm. Thinner sensors should reach an intrinsic time resolution below 30 ps (Sec. 3.2.4) but with a higher sensor capacitance and lower charge, i.e. the jitter contribution increases (Sec. 4.4). By increasing the front-end power, it will be possible to lower the jitter term.

5.3.3 Data analysis of CERN beam test

The first beam test performed with *Run 3.2* production was the October 2024 beam test. A second beam test was carried out in July 2025, when a MadPIX without gain was also measured. IDs 9 and 10 were the reference dose, while ID 11 was the -3.3 %.

October 2024 BT Just the sensor flavour *layout 2* was measured due to the early breakdown of the other layout. With a higher implantation dose, the termination without a gap, i.e. *layout 1*, creates a higher field and hence the device experiences premature border breakdown.

In the next plots, results from IDs 9 and 10 are reported. Figures 5.41a and 5.41b show the noise for IDs 9 and 10, respectively. The noise is compatible between the two IDs. Different colours represent the front-end power consumption. Boost 0 is the standard configuration for which the power is reported in the previous section. Boost 1 is the configuration in which the FE current was increased while maintaining the same bias voltages (1.2 V and 3.3 V). In the last one, i.e. boost 2, the power supply provided 1.5 V and 3.7 V to the ASIC.
Table 5.21 reports the FE power for each configuration.

The noise remained constant with the power increase, and it increased compared to the *Run 3* chip, where the sensor gain was ≈ 2.8. This mismatch might

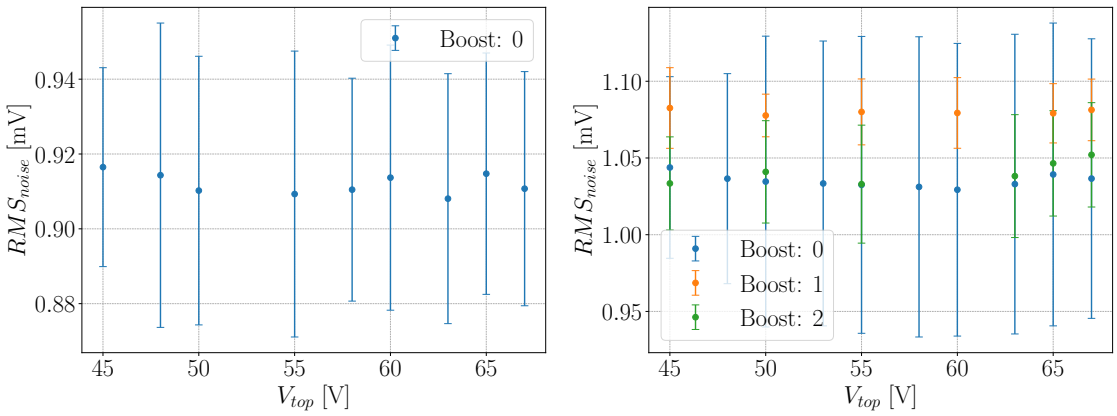


Figure 5.41: RMS noise of IDs 9 (a) and 10 (b) of *Run 3.2* measured during October 2024 BT. The dot represents the mean obtained by averaging the values measured for three different pixels on which the FIB was performed. The measured layout is the 2 with V_{back} fixed at 25 V.

be attributed to the increased gain, which produced a greater sensor noise in the FE input.

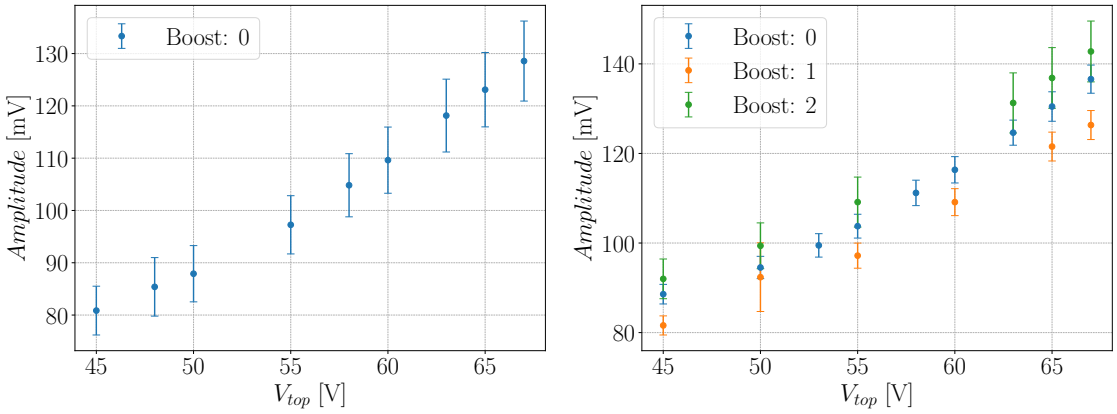
The MPV for ID 9 and 10 as a function of V_{top} is reported in Fig 5.42a and 5.42b. With the same power consumption, the two devices had the same amplitude, as expected. Indeed, they both were extracted from wafers with the same implantation dose. As for noise, the ID 9 MPV is slightly lower than ID 10, probably due to a lower FE gain. The boost 1 configuration shows a lower MPV in ID 10. Increasing the FE current, the operating points of the transistors change, showing a gain reduction. In boost 2, the transistor dynamic range and current increase. Hence, a larger signal was measured.

From 45 V to 67 V of V_{top}, the signal increases more than 60%. By comparing these values with the ones obtained for a MadPIX without a gain implant ($\approx$ 10 mV), a sensor gain value between 8 and 13 is found.

To inspect whether the FIB procedure succeeded, the MPV as a function of

Table 5.21: FE power consumption for *Run 3.2* in October BT.

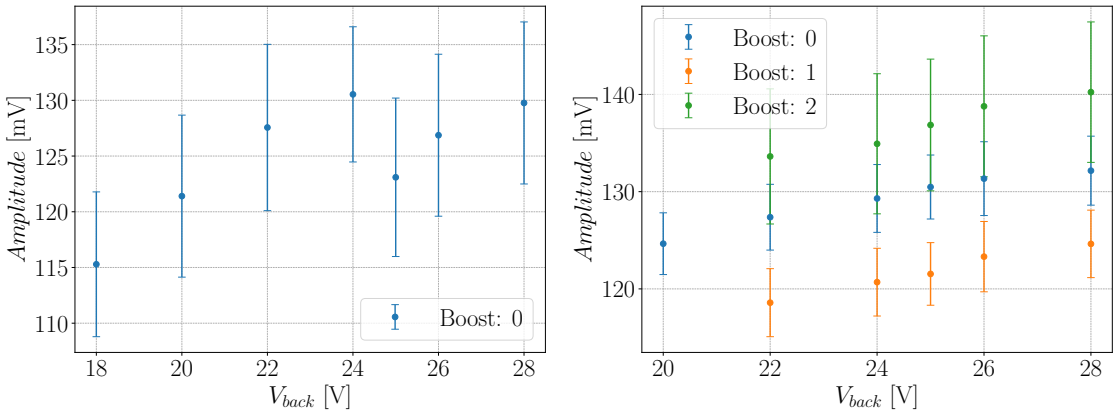
Boost	Power consumption [mW/*ch*]
0	0,16
1	0,20
2	0,28



(a) (b)

Figure 5.42: MPV obtained by fitting the amplitude distributions of IDs 9 (a) and 10 (b) of *Run 3.2* as a function of V_{top} measured during October 2024 BT. The dot represents the mean obtained by averaging the values measured for three different pixels on which the FIB was performed. The measured layout is the *2* with V_{back} fixed at 25 V.

V_{back} was checked. Figures 5.43a and 5.43b show the expected behaviour. By increasing V_{back} above the full depletion, the signal did not change substantially.



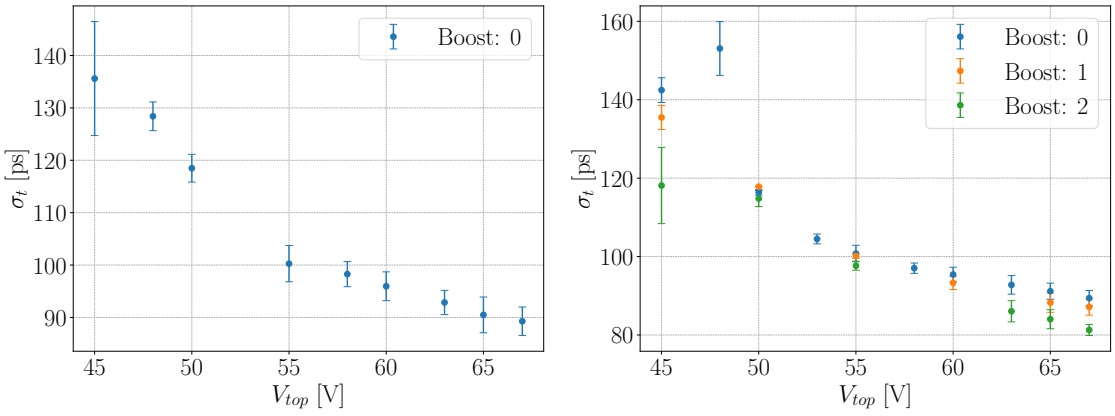
(a) (b)

Figure 5.43: MPV obtained by fitting the amplitude distributions of IDs 9 (a) and 10 (b) of *Run 3.2* measured during October 2024 BT as a function of V_{back}. The dot represents the mean obtained by averaging the values measured for three different pixels on which the FIB was performed. Layout *2* is the one measured and V_{top} is fixed at 65 V.

The strange behaviour observed for *Run 3* structures before FIB was not present here. As observed for V_{top}, the boost condition 2 produced the greatest signals. The time resolution was extracted using the leading edge threshold algorithm.

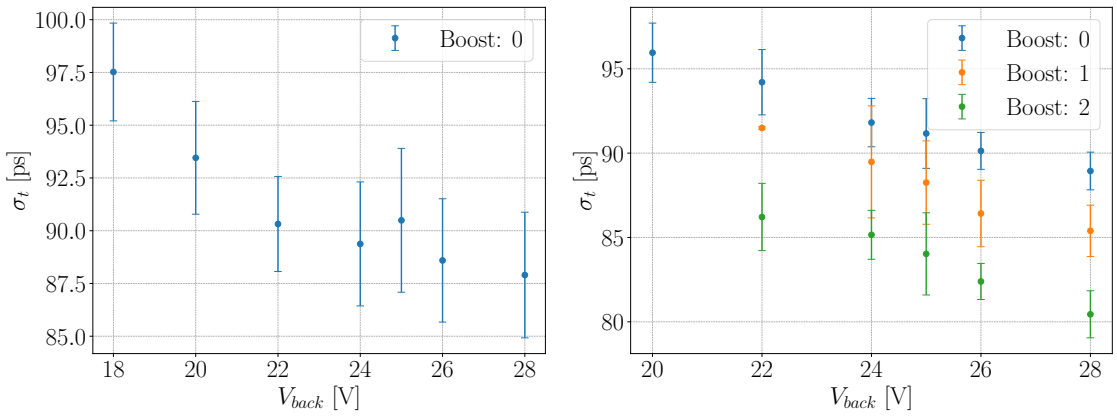
Figures 5.44a and 5.44b report the time resolution of ID 9 and 10 as a function of the collection electrode bias. The two samples reach 90 ps in standard configuration, which is equal to the sum of the sensor resolution and the FE jitter with this power consumption. The expected time resolution for *Run 3.2* extracted from the MC simulation in Sec. 3.2.3 is around 100 ps RMS evaluated with a difference between V_{top} and V_{back} of 85 V. If a q-Gaussian fit is used in a Monte Carlo simulation to give less weight to non-Gaussian tails, a time resolution of 75 ps can be achieved in the best simulation conditions. By subtracting in quadrature the jitter of 50 ps from the measured 90 ps obtained during the BT, a sensor time resolution of 75 ps is found. Hence, simulations and data are in good agreement. In the boost configuration 2, the jitter was lowered by an increase in signal amplitude and in the rise time. Thus, the total time resolution decreased. From preliminary laser measurements in boost 2 configuration, a jitter $\approx$ 25 ps was measured (for the BT MPV), which was compatible with the BT improvement.

The V_{back} dependence is shown in Fig. 5.45a and 5.45b. V_{back} has a lower effect on the total time resolution because it does not change the signal amplitude, i.e. the jitter contribution is almost always the same, changing V_{back}. A minor improvement might be observed due to the minimum electric field increasing beneath the top electrode. This allows for a faster charge carrier collection.



(a) (b)

Figure 5.44: Time resolution of IDs 9 (a) and 10 (b) of *Run 3.2* measured during October 2024 BT as a function of V_{top}. The dot represents the mean obtained by averaging the values measured for three different pixels on which the FIB was performed. *Layout 2* is the one measured and V_{back} is fixed at 25 V.



(a) (b)

Figure 5.45: Time resolution of IDs 9 (a) and 10 (b) of *Run 3.2* measured during October 2024 BT as a function of V_{back}. The dot represents the mean obtained by averaging the values measured for three different pixels on which the FIB was performed. *Layout 2* is the one measured and V_{top} is fixed at 65 V.

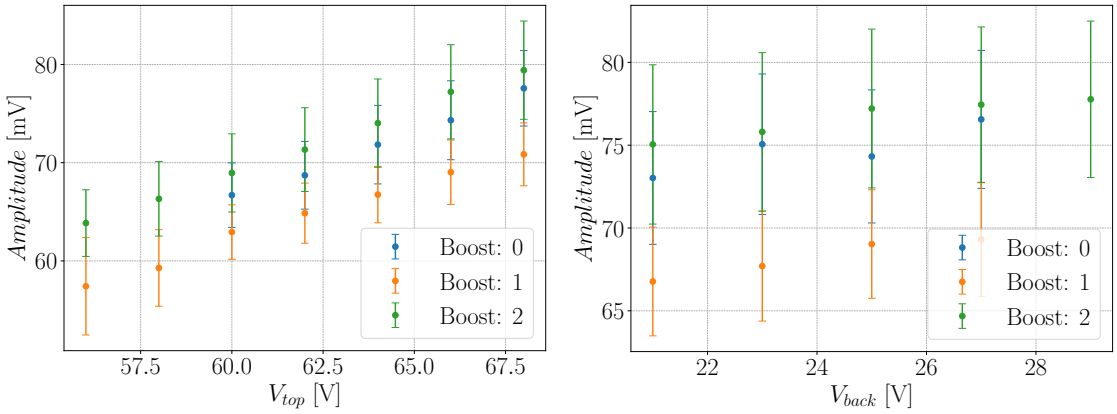
The best time resolution measured for a MadPIX with a reference implantation dose was 80.4 ± 1.4 ps obtained with $V_{top} = 65$ V and $V_{back} = 28V$. The leading edge threshold was set to 55 mV.

During this BT, a sample with the -3.3 % implantation dose was also tested, the ID 11 chip. Its noise was ≈ 0.85 mV, which corresponds to an intermediate value between *Run 3* and *Run 3.2* MadPIX (with the reference dose).

Figures 5.46a and 5.46b report the MPV extracted for this MadPIX as a function of V_{top} and V_{back}. A sensor gain between 6 and 8 was extracted by comparing the signals with a MadPIX without gain. As can be observed from Fig. 5.46b, the FIB was successful. As for IDs 9 and 10, the boost 1 configuration has a lower amplitude compared to the standard one, while boost 2 has a slightly higher FE gain.

Figures 5.47a and 5.47b depict the time resolution as a function of V_{top} and V_{back}. 95 ps were achieved by biasing the substrate with a voltage higher than 26 V and a collection electrode bias above 65 V. The sensor time resolution should be lower than the reference dose structures due to a higher electric field minimum beneath the collection electrode. However, the lower gain increases the jitter term due to a smaller collected charge.

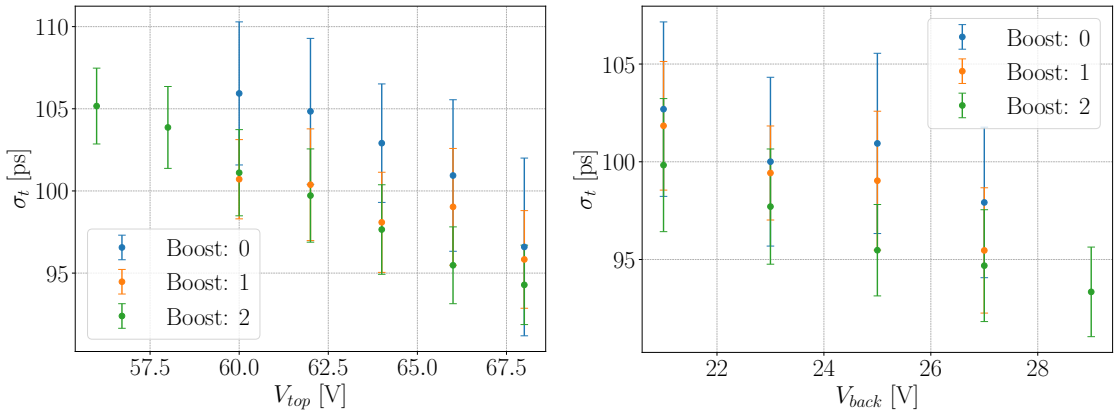
The CMOS LGAD development goal can be highlighted by comparing the reference and -3.3 % doses. Indeed, for the same power consumption (*boost 2* configuration), a higher-gain structure (ID 10 in Fig. 5.45b: $\simeq 80,$ ps) achieves a time resolution improved by $15,$ ps compared to a lower-gain structure (ID 11 in



(a) (b)

Figure 5.46: MPV measured on sensor *layout 2* during the October 2024 BT as a function of V_{top} (a) and V_{back} (b). The MPV was extracted by fitting the amplitude histogram. The dot represents the mean obtained by averaging the values measured for three ID 11 pixels (reference dose) with (a) $V_{back} = 25\,\text{V}$ and (b) $V_{top} = 66\,\text{V}$.

Fig. 5.47a: $\simeq 95,\text{ps}$), corresponding to an improvement of over 15%.



(a) (b)

Figure 5.47: Time resolution of IDs 11 of *Run 3.2* measured during October 2024 BT (reference dose). The dot represents the mean obtained by averaging the values measured for three different pixels of *layout 2* on which the FIB was performed. V_{back} is fixed at 25 V in (a), while in (b) V_{top} if constant at 66 V.

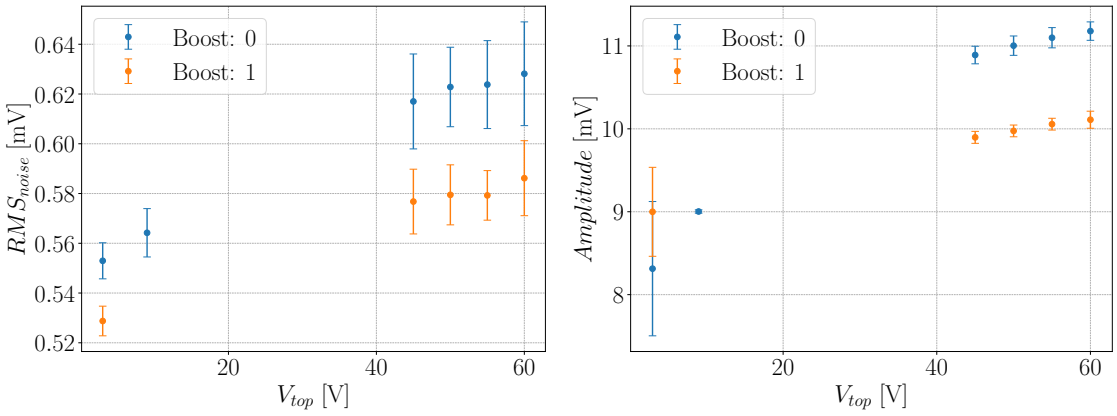
July 2025 BT During this BT, a MadPIX without gain was tested to extract the sensor gain. The measured noise is reported in Fig. 5.48a. As observed for the other samples, in boost 1 configuration, the noise is slightly lower than the standard one due to a gain reduction observed also in 5.48b. An MPV of 11 mV was measured with V_{top} higher than 40 V. The MPV increase was attributed to the extension of the depletion to the border and the increase in the signals rising edge.

The time resolution was dominated by jitter as observed in Fig. 5.49a. Instead, Fig. 5.49b shows that FIB succeeded. The worsening of the time resolution measured for boost condition 1, unlike previous devices, may be attributed to a problem on the test board that was corrected during the following beam tests. It was found that the PCB manufacturer mounted an SMD resistor with a smaller value (0.1 kΩ instead of 10 kΩ) in the 1.2 V buffer current source of the TB.

The front-end gain and noise are compatible with post-layout measurements presented in 4.4.

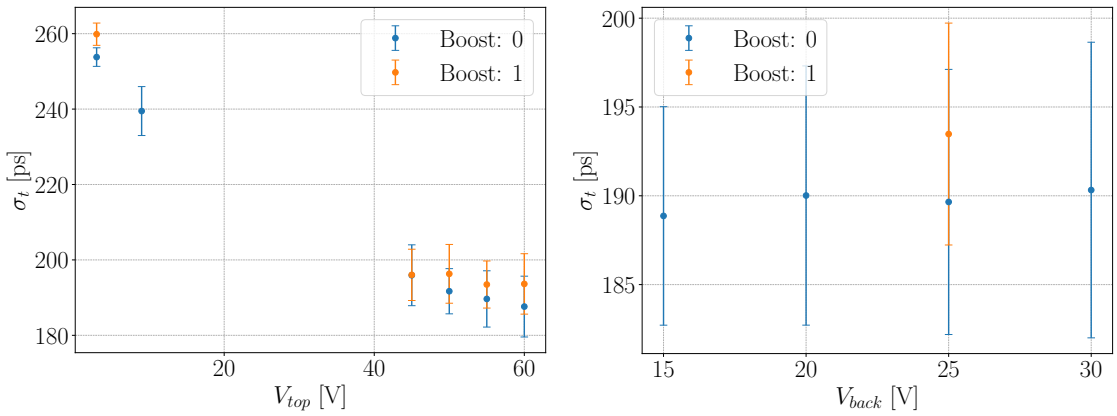
5.3.4 Data analysis of DESY beam test

The DESY beam test facility provides users with tracking telescopes used for efficiency and in-pixel studies. As described before, two telescopes were used to reconstruct the particle trajectories and the impingement position on MadPIX. Due to the low rate (10 Hz), one week of data acquisition was sufficient for just a V_{top} scan. Two BTs, the first one in March 2025 and the second in November 2025,



(a) (b)

Figure 5.48: Noise (a) and MPV (b) measured on sensor *layout 2* during the October 2024 BT as a function of V_{top}. The MPV was extracted using a fit on the amplitude histogram. The dot represents the mean obtained by averaging the values measured for three ID 12 chips (no gain) with $V_{back} = 25$ V.



(a) (b)

Figure 5.49: Time resolution of ID 12 of *Run 3.2* measured during October 2024 BT (no gain). The dot represents the mean obtained by averaging the values measured for three different pixels of *layout 2* on which the FIB was performed. V_{back} is fixed at 25 V in (a), while in (b) V_{top} if constant at 55 V.

were successfully carried out. The data were analysed with *Corrywreckan* [142, 143], a reconstruction framework that allows users to align all the planes and, by minimising the residual (difference between the reconstructed point by the sensor and the reconstructed track using all planes), to predict the crossing point on the DUT with a certain error.

March 2025 BT The ID 9 chip, measured in October 2024 at CERN BT, was also characterised at DESY. The run list is reported in table 5.22. The study was conducted on pixels A, B and D because pixel C stopped working.

To better measure the sensor time resolution, the chip was set in the boost configuration.

For the time resolution analysis, the CF algorithm was used for simplicity;

Table 5.22: Runs list and pixel chosen during March 2025 beam test at DESY.

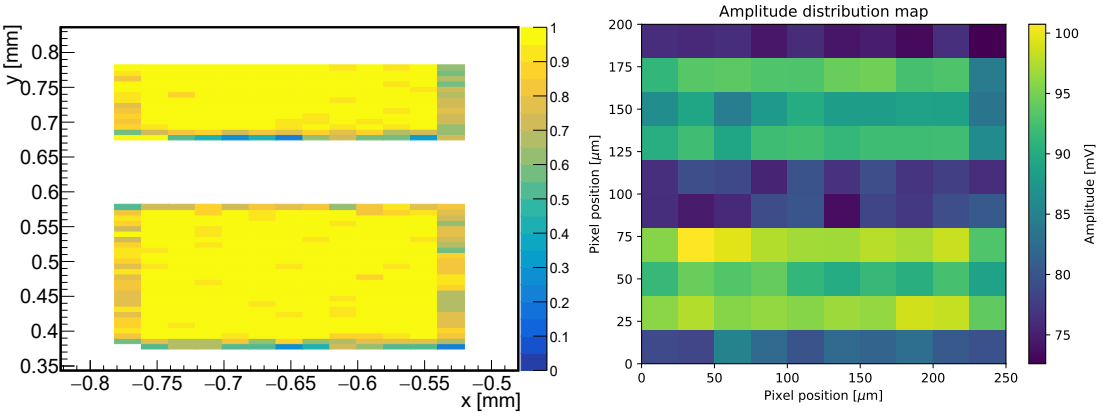
Run	**ID**	**A**	**B**	**C**	**D**	V_{top}	V_{back}	**Matrix**	**Boost**
0	9	x	x		x	45.0	25.0	A2	x
1	9	x	x		x	55.0	25.0	A2	x
2	9	x	x		x	65.0	25.0	A2	x
3	9	x	x		x	65.0	28.0	A2	x

indeed, the performances obtained are compatible with that extracted with the LE, but no time walk correction was performed. To extract the resolution as a function of the impinging position inside pixels, any cut on the amplitude does not need to be performed, and without a threshold, it is not possible to perform time walk correction as a function of the amplitude. For the TOA and time resolution maps, a 40 % CF threshold was used.

The reconstructed tracks on MadPIX are shown in Fig. 5.50a, where the three pixels connected to the oscilloscope are reconstructed. As introduced before, the C pixel was not characterised.
For the analysis, just two adjacent pixels were studied to avoid track reconstruction errors. Indeed, the edges of non-adjacent pixels have some smearing due to the finite track reconstruction error, i.e. $< 5\,\mu$m.

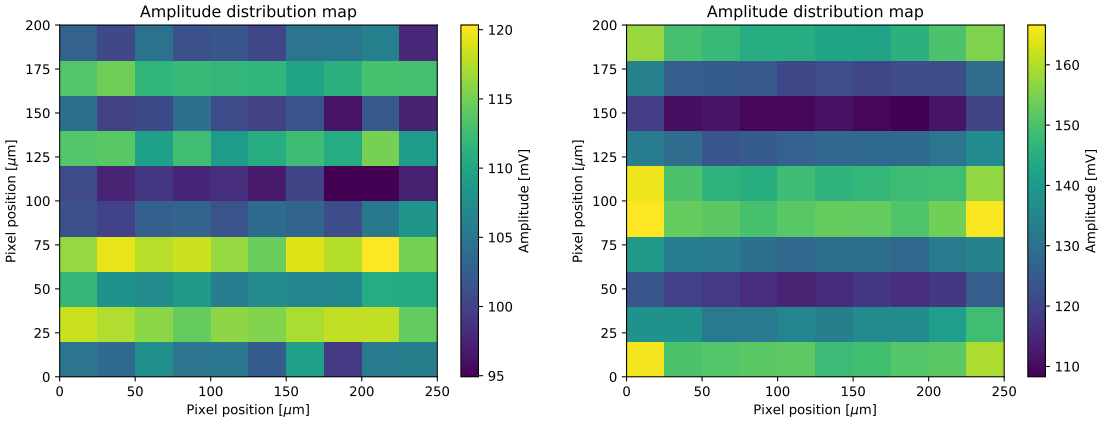
The amplitude map, created by biasing V_{top} at 45 V, is shown in Fig.5.50b. The map represents two binned pixels (25 μm, 20 μm), and each bin value is the MPV found by performing a fit on amplitude histograms. The MPV reaches a minimum at pixel edges, i.e. $y = 0, 100$ and $200\,\mu$m. The pixel centre is not the region with the highest gain with $V_{top} = 45$ V due to the minimum of the electric field present beneath the collection electrode, as shown in the MC simulation of Sec. 3.2.3.

Figures 5.51a and 5.51b show the same map with V_{top} equal to 55 V and 65 V. For $V_{top} = 55$ V, the MPVs globally increase, i.e. the amplitude range is shifted to greater values $\approx +20$ %. If V_{top} reaches voltages near the breakdown point, i.e. 65 V, the MPVs map changes the structure. Indeed, in Fig. 5.51b, the maximum is found at pixel edges. While moving from borders to centres, the MPV is lowered,



(a) (b)

Figure 5.50: Reconstructed tracks on MadPIX with $V_{top} = 65$ V and a 50 mV threshold (a). (b): MPV map of two adjacent pixels (A, B) extracted for $V_{top} = 45$ V. The substrate was biased at -25 V.



(a) (b)

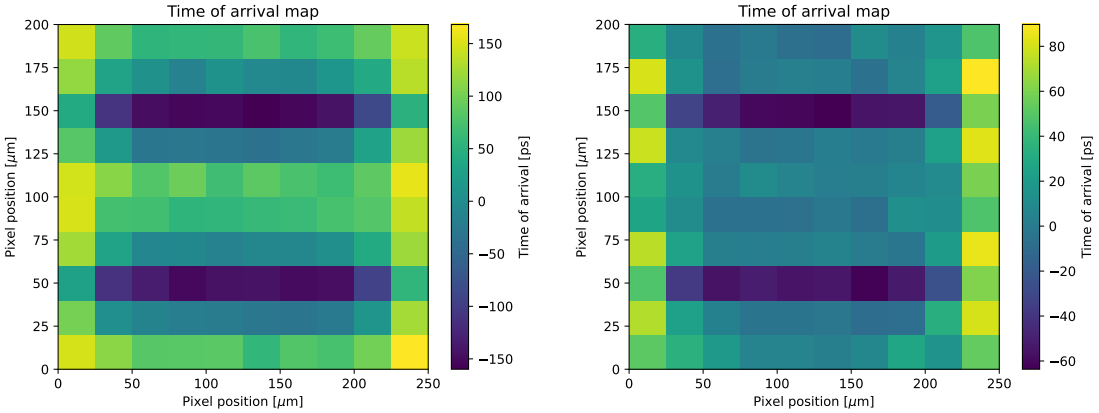
Figure 5.51: MPV map of two adjacent pixels (A, B) extracted for $V_{top} = 55\,\mathrm{V}$ (a) and $V_{top} = 65\,\mathrm{V}$ (b). The substrate was biased at $-25\,\mathrm{V}$.

reaching a minimum in the centre. This behaviour is due to the high electric field present between pixels along the long edge, where the guard ring is biased at 9 V. The potential difference between the collection electrode and the guard ring generated a higher field compared to the one present in the centre. Indeed, these structures experienced an edge breakdown instead of a gain one beneath the electrode as in standard LGAD. All the considerations are valid for the long edge (250 μm) where the guard ring is present. Alongside the short border, no n^+-implant is present, and hence the electric field is not strong enough.

In addition to the MPV dependence on the impinging position, the time resolution was studied. The two major observables are the time resolution and the time of arrival; they might be extracted from the time difference distribution between MadPIX and LGAD reference as the Gaussian sigma or as the mean value of the distributions. For the DESY analysis, the CF algorithm was used to avoid time walk correction.

Figure 5.52a shows the time of arrival map evaluated at $V_{top} = 45\,\mathrm{V}$. A huge delay, i.e. 300 ps, was measured between signals generated from particles impinging in the centre or at borders. This difference may be lowered by increasing V_{top} to 55 V as shown in Fig. 5.52b. With this collection electrode bias, the spread between centre and edges was reduced to 140 ps. The absolute values are not compatible between maps because 0 ps delay is the mean TOA value, averaging all the data together, given a fixed bias voltage (using the same analysis used for CERN BT).

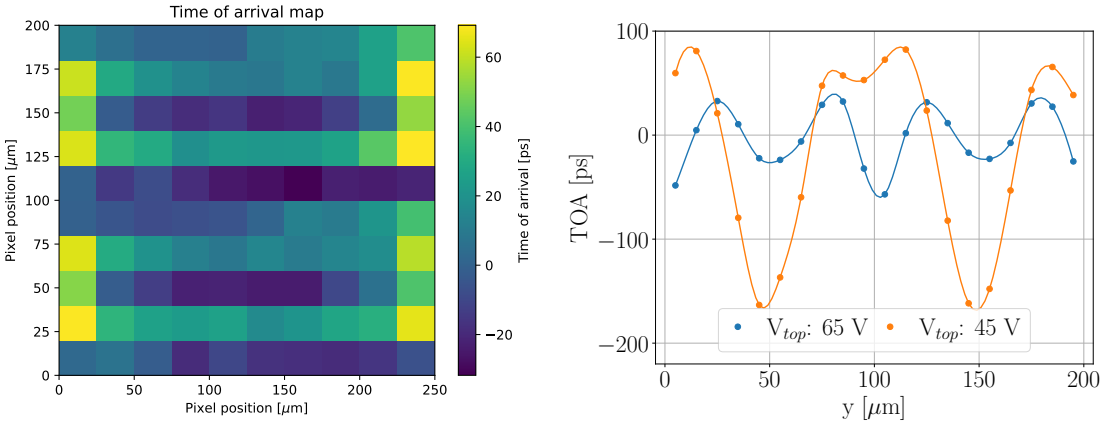
Figure 5.53a shows the TOA map at $V_{top} = 65\,\mathrm{V}$. The TOA spread was lowered



(a) (b)

Figure 5.52: TOA map inside two adjacent pixels (A, B) extracted for $V_{top} = 45\,\text{V}$ (a) and $V_{top} = 55\,\text{V}$ (b). The substrate was biased at $-25\,\text{V}$. The TOA is the mean value of time difference distributions.

again and was below 100 ps; however, the TOA behaviour inside pixels was changing. Indeed, in the previous maps, the slowest signals were generated by particles impinging in the centre, i.e. negative values ($t_{LGAD} - t_{DUT}$), due to the electric field minimum beneath the collection electrode. Instead, at the edges, the electric



(a) (b)

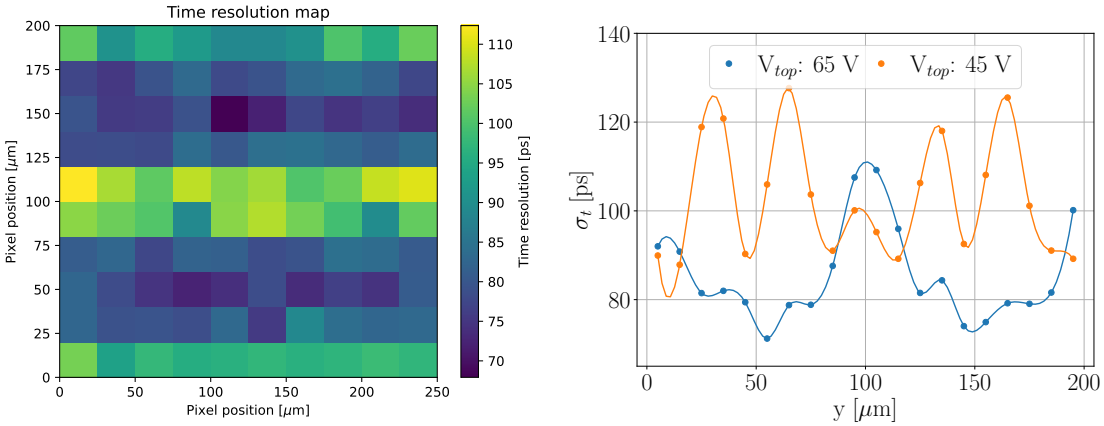
Figure 5.53: TOA map inside two adjacent pixels (A, B) extracted for $V_{top} = 65\,\text{V}$ (a). In (b), its comparison between $V_{top} = 65\,\text{V}$ and $45\,\text{V}$ scanning the pixel from $y = 0\,\mu\text{m}$ to $y = 200\,\mu\text{m}$ while selecting the tracks impinging between $x = 100\,\mu\text{m}$ and $x = 150\,\mu\text{m}$. The substrate was biased at $-25\,\text{V}$.

field was very high, hence compensating for the longer collection time present at the borders. For $V_{top} = 65\,\text{V}$, the fastest signals were generated between the centre and the borders. This effect arose due to the increase in efficiency at edges, thus signals very far from the pixel centre started to weigh more and delayed the TOA.

In Fig. 5.53b, the TOA as a function of the position is plotted for $V_{top} = 45\,\text{V}$ and 65 V. The TOA value was evaluated by considering all tracks impinging between $x = 100\,\mu\text{m}$ and $x = 150\,\mu\text{m}$, which provided higher statistics. The distribution as a function of y was more uniform for higher V_{top}. The fastest signals were present at pixel borders, i.e. $y = 0, 100$ and $200\,\mu\text{m}$, while the maximum delay was in the centre ($y = 50$ and $150\,\mu\text{m}$) at low V_{top}. For 65 V applied to the collection electrode, the fastest signals were generated between centre and edge ($y = 25, 75, 125$ and $175\,\mu\text{m}$), where the collection electrode ends and the electric field is at its maximum.

The results obtained so far have been compared with MC simulations. The measured and predicted behaviour of the TOA as a function of the impinging position is compatible (Fig. 3.23a, where the TOA is inverted compared to experimenal results). The maximum delay between border and centre measured during the BT is smaller than the one extracted from simulations (250 ps), probably due to a non-perfect match of the substrate doping used in TCAD simulations.

The time resolution map evaluated at 65 V is reported in Fig. 5.54a, and it is more uniform than the TOA one. The best time resolution was achieved in the pixel centre, i.e. $\approx 70\,\text{ps}$. This value still contains the time reference timing



(a) (b)

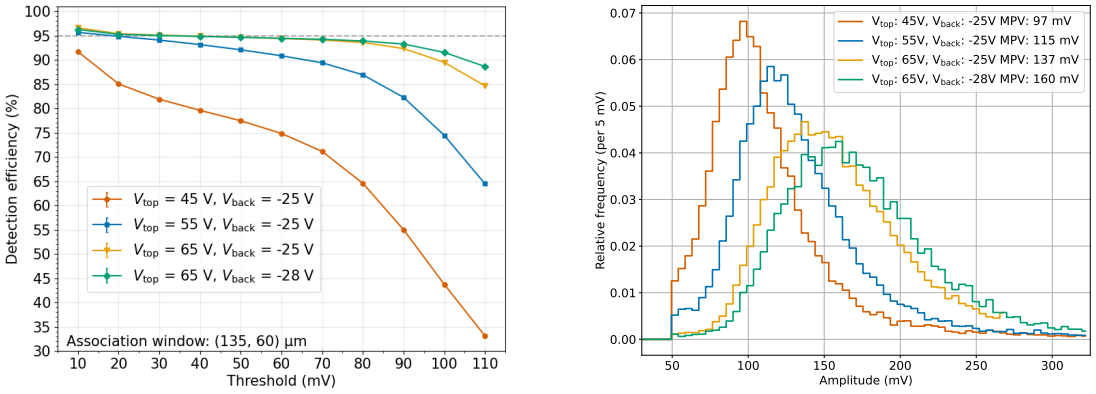
Figure 5.54: Time resolution map inside two adjacent pixels (A, B) extracted for $V_{top} = 65\,\text{V}$ (a). In (b), its comparison between $V_{top} = 65\,\text{V}$ and 45 V scanning the pixel from $y = 0\,\mu\text{m}$ and $y = 200\,\mu\text{m}$ while selecting the tracks impinging between $x = 100\,\mu\text{m}$ and $x = 150\,\mu\text{m}$. The substrate was biased at $-25\,\text{V}$.

resolution, and hence, if the LGAD error is subtracted in quadrature, a total time resolution $\approx 65\,\text{ps}$ is found. The value contains both sensor and electronics contributions and thus includes the jitter term, which was estimated to be about 25 ps in the boost 1 configuration. The Landau contribution to the total time resolution was 60 ps (without jitter), which is in line with the MC and theoretical predictions of the Landau term.

Figure 5.54b shows the time resolution for $V_{top} = 45\,\text{V}$ and 65 V as a function of the impingement position along side the y axis. The best time resolution was achieved for both voltages in the centre ($y = 50$ and $150\,\mu\text{m}$). The worst one was found in the transition area ($y = 25, 7, 125$ and $175\,\mu\text{m}$) due to the highest electric field variation in the $V_{top} = 45\,\text{V}$ configuration. For $V_{top} = 65\,\text{V}$ the time resolution was stable beneath the collection electrode ($25 < y < 75\,\mu\text{m}$ and $125 < y < 175\,\mu\text{m}$) while it reached a maximum below the edges ($y = 0, 100$ and $200\,\mu\text{m}$).

A first measure of efficiency as a function of the LE threshold can be performed (Fig. 5.55a), considering the two adjacent pixels. By increasing V_{top}, the global efficiency can reach 95 % for a threshold below 50 mV. The efficiency increase below 20 mV is due to bipolar signals generated when a neighbouring pixel is hit. In Fig. 5.55b, the amplitude distribution for the bias voltages acquired at DESY. The 50 mV threshold allows for a complete Landau distribution.

November 2025 TB During the November TB at DESY, a L-shaped pixel configuration was tested using a +3.3 % dose chip. The run list is reported in table



(a) (b)

Figure 5.55: Efficiency as a function of the threshold considering two adjacent pixels (A, B) in (a). Landau distributions obtained in the DESY TB of March 2025 in (b).

Table 5.23: Runs list and pixel chosen during November 2025 beam test at DESY.

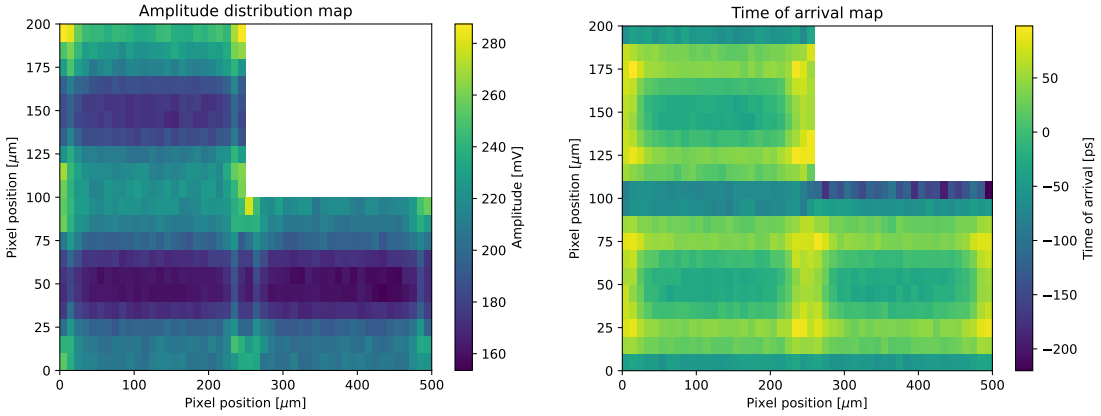
Run	**ID**	**A**	**B**	**C**	**D**	V_{top}	V_{back}	**Matrix**	**Boost**
0	13	x,x	x			55.0	25.0	A2	x
1	13	x,x	x			60.0	25.0	A2	x
2	13	x,x	x			65.0	25.0	A2	x

5.23. Two pixels A of two adjacent semi-columns were bonded to the outputs.

Using the ADENIUM telescope and treasuring the experience gained during the first beam test at DESY (March 2025), in the November BT, it was possible to acquire the three configurations with a 4 times higher statistic.

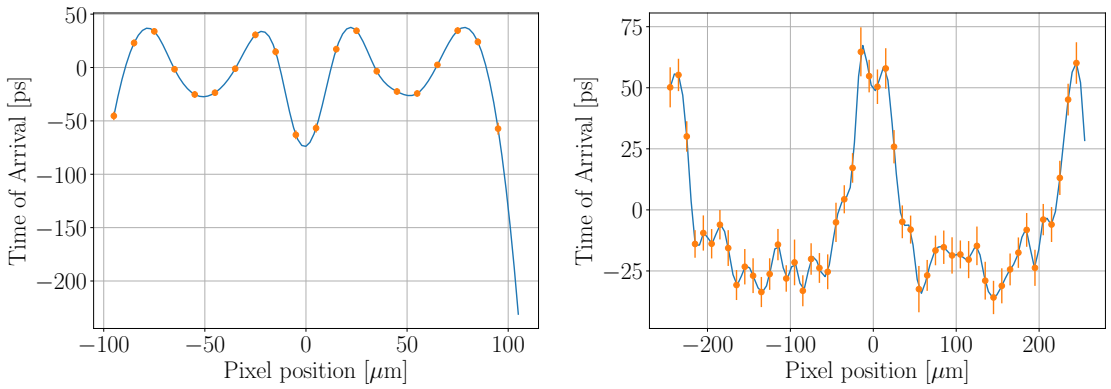
The amplitude map measured at $V_{top} = 65\,\text{V}$ and the corresponding TOA map are shown in Fig 5.56a and 5.56b. The behaviour is similar to the one measured in the first BT at DESY; however, the higher statistic permitted binning the pixel with $10 \times 10\,\mu\text{m}^2$ bins. As observed previously, the TOA was delayed beneath the collection electrode and below the deep $p-$well present in the long edges. The signal amplitude was higher compared to the previous beam test due to the $+3.3\,\%$ dose.

The TOA evaluated at $V_{top} = 65\,\text{V}$ is plot in Fig. 5.57b as a function of the impinging position along side the long edge selecting the particles crossing the pixels between $y = 40\,\mu\text{m}$ and $60\,\mu\text{m}$. While Fig. 5.57a shows the TOA behaviour in the other direction, only the tracks impinging with $100 < x < 150\,\mu\text{m}$ are selected. The TOA is faster at borders ($t_{LGAD} - t_{DUT}$) where the electrode end,



(a) (b)

Figure 5.56: Amplitude (a) and TOA (b) maps inside three adjacent pixels (A, A, B) extracted for $V_{top} = 65\,\text{V}$ and $V_{back} = -25\,\text{V}$.

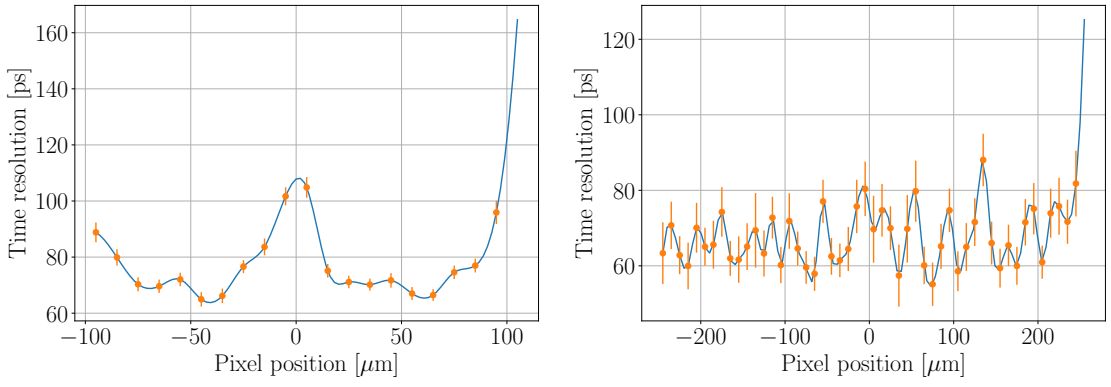


(a) (b)

Figure 5.57: TOA dependence along side the short (a) or long (b) edge extracted for $V_{top} = 65\,\mathrm{V}$ and $V_{back} = -25\,\mathrm{V}$.

and slower in the centre, however, in the short edge (Fig. 5.57b) the delay grows when moving from the collection electrode to the deep p-well due to a greater collection path. No major variations in the TOA were observed between reference and +3.3 % doses.

The same study was performed for the time resolution. No major variations were present alongside the long edge (Fig. 5.58b) while a worsening of the total time resolution was observed beneath the deep p-well in the short edge (Fig. 5.58a) due to the higher electric field and drift path. A mean time resolution of 65 ps



(a) (b)

Figure 5.58: Time resolution dependence along side the short (a) or long (b) edge extracted for $V_{top} = 65\,\mathrm{V}$ and $V_{back} = -25\,\mathrm{V}$.

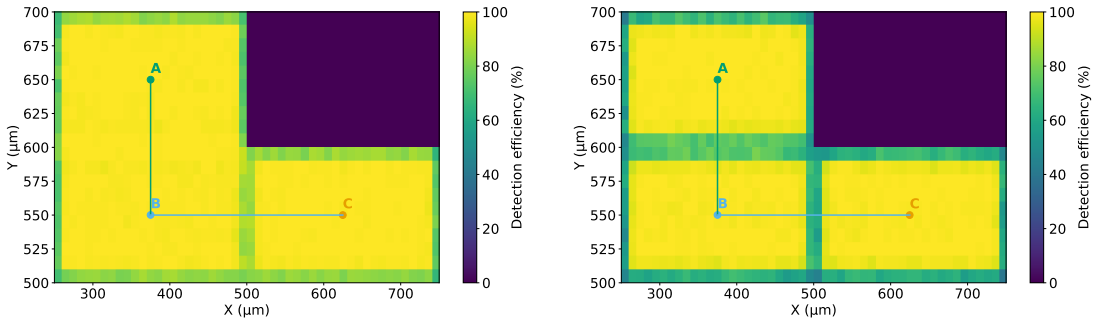
was measured in the centre (5.58b), which corresponds to ≈ 58 ps if the LGAD contribution is subtracted (≈30 ps).

The three pixels bonded in an L-shape allow for a more precise efficiency measure. Indeed, in March BT, the pixel borders were contained in the efficiency evaluation; however, due to the finite track resolution, the top and bottom borders showed a drop in efficiency. Indeed, the bias of track reconstruction is removed by selecting an ROI in which only four triangles are created with the vertices in the pixel centres and with the sides matching the edges of two adjacent pixels.

Figures 5.59a and 5.59b plot the in-pixel efficiency for the 3 pixels measured at $V_{top} = 65\,\text{V}$ and $V_{top} = 55\,\text{V}$. An efficiency drop was observed at the edges for the lower collection electrode voltage. Alongside the long edge, the efficiency reached 100 % for the highest V_{top}, while for the short edge, a minimum was always present.

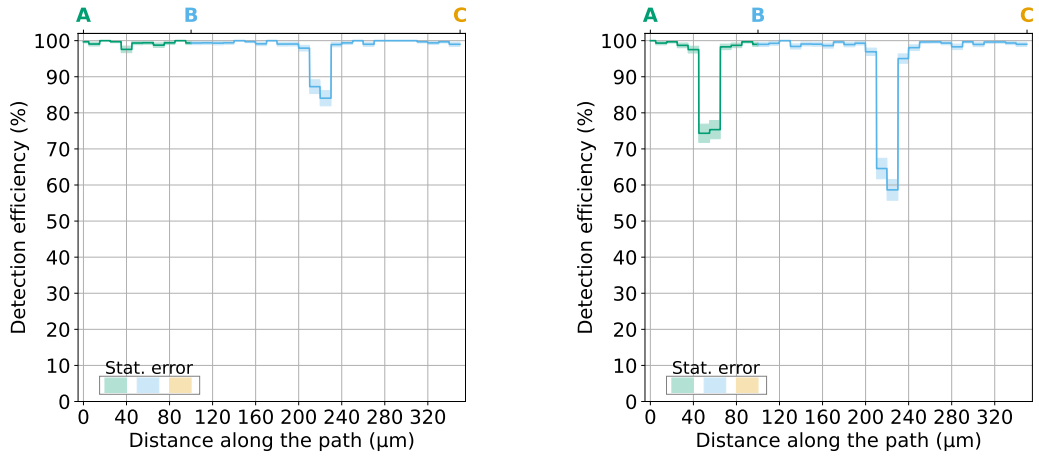
Figures 5.60a and 5.60b report the efficiency moving following the path displayed in Fig. 5.59a and 5.59b. Between A and B, the long edge is crossed, and the efficiency goes from 75 % to 100%, increasing V_{top} from 55 V to 65 V. While from B to C, the minimum is reached beneath the edge, where 60 % of efficiency is measured at $V_{top} = 55\,\text{V}$ and 85 % at $V_{top} = 65\,\text{V}$.

The mismatch between long and short edges is due to the different terminations of implants. Indeed, inside the long edge, between two pixels, an n-type guard ring is followed by a deep p-well (where the FE electronics is) and another n-guard ring, while the short edge has only a deep p-well implant in between pixels. The electric field in the long side is stronger due to the potential difference between the collection electrode and guard ring (biased at 9 V). This allows the efficiency increase because the charge deposited below the edge is also multiplied, as shown in the MC simulations of Sec. 3.2.3. The short edge does not have the guard ring, and hence the electric field is similar to the one in the pixel centre. In addition,



(a) (b)

Figure 5.59: In-pixel efficiency map where the path used for the efficiency - position plot is highlighted. V_{top} was biased at 65 V in (a) and at 55 V in (b), while V_{back} at −25 V.



(a) (b)

Figure 5.60: Efficiency moving from A to B to C. The path is highlighted in Fig. 5.59a and 5.59b. V_{top} was biased at 65 V in (a) and at 55 V in (b), while V_{back} at −25 V.

due to *layout 2* termination, the charges collected below the deep *p*-well are not multiplied, thus the drop in efficiency.

The total pixel efficiency averaging on the three pixels is shown in Fig. 5.61 as a function of the LE threshold applied. As presented for March BT in DESY, the efficiency is higher than 95 %. The threshold values are greater than the previous BT due to bigger amplitudes corresponding to +3.3 % dose.

The efficiency is higher than what was predicted in MC simulations (88 %) due to the different bias conditions and doping profiles (reference dose and +3.3 %). In TCAD simulations, the collection electrode could not be biased at 65 V due to convergence limits. The efficiency measured with $V_{top} = 55$ V reaches 90 % if a threshold of 100 mV is applied with 3.3 % dose. In March BT, where the reference dose was tested, the $V_{top} = 55$ V case showed a similar efficiency (Fig. 5.55a) given the same bias conditions and doping profiles of MC simulations; however, applying 45 V to the collection electrode, the efficiency dropped to 75 %. Thus, variation of V_{top} below 55 V generates substantial changes in the total efficiency, allowing us to explain the 5 % mismatch.

Table 5.24 summarises the results achieved with *Run 3.2* MadPIX after FIB. The jitter values are extracted from preliminary laser measurements.

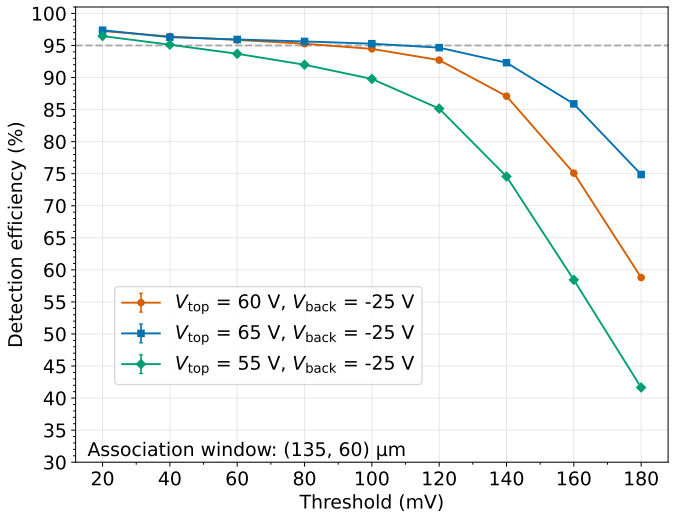


Figure 5.61: Efficiency as a function of the LE threshold applied for different V_{top}. The substrate is biased at -25 V.

Table 5.24: Summary of the MadPIX results - *Run 3.2*. In brackets, the results obtained with a higher FE power consumption.

	MadPIX *Run 3.2*		
Technology	LFoundry 110 nm		
Pixel size [μm^2]	250×100		
Thickness [μm]	48		
FE power [mW/cm^2]	660 (1100)		
Punch-through [V]	25		
Layout	2		
Gain dose	-3.3 %	0 %	3.3 %
Sensor gain	$6 \div 8$	$8 \div 14$	$8 \div 14$
Breakdown [V]	66	68	69
Jitter [ps]	≈ 50 (40)	≈ 40 (25)	≈ 30 (22)
Time resolution [ps]	96.6 ± 4 (93 ± 3)	89 ± 1 (80 ± 1)	83 ± 1 (72 ± 1)
Efficiency	-	≈ 95 %	≈ 95 %

5.4 Limits and perspectives of the CMOS LGAD

The simulation studies and experimental measurements presented in Chapters 3, 4 and 5 highlight that the current time resolution of the CMOS LGAD prototype is mainly constrained by a combination of sensor thickness, pixel geometry, and gain uniformity, primarily due to position-dependent charge collection effects.

One of the main limitations originates from the 48 μm active thickness. This thickness provides a sufficiently high signal-to-noise ratio (SNR) to minimise the electronics jitter, as shown in Sec. 4.3; however, it limits the intrinsic sensor time resolution to $\approx$ 60 ps, as discussed in Secs. 3.2.3 and 5.3. Monte Carlo simulations presented in this work indicate that reducing the active thickness to $\approx$ 15 μm could significantly improve the timing performance, potentially reaching values close to 20 ps, reducing the Landau fluctuations.

Another important contribution to the performance limitations is associated with the pixel geometry. In the current design, the electric field and weighting field are not fully uniform across the pixel area, producing a position-dependent sensor response due to a sub-optimal ratio between pixel pitch and sensor thickness. Consequently, particles crossing different regions of the pixel generate signals with different amplitudes and timing characteristics, resulting in additional contributions to timing jitter and time walk. Monte Carlo simulations and theoretical evaluations have shown that increasing the pixel pitch can improve the time resolution. Moreover, the use of thinner substrates naturally increases the pitch-to-thickness ratio, further enhancing the timing performance.

The gain layer also plays a critical role in determining the detector response. Simulations and experimental measurements suggest that non-uniformities in the multiplication region can affect the local gain, producing variations in signal amplitude and degrading the timing resolution across the sensor area. Additional optimisation of the pixel termination layout is expected to improve the uniformity of the avalanche multiplication process while maintaining stable operation at high electric fields.

Furthermore, the output buffer and the long analog routing lines reduce both the bandwidth and signal amplitude, thereby degrading the front-end performance. Future optimisation of the pixel front-end channel, including the implementation of a fast discriminator, is therefore expected to further reduce the electronics jitter.

Overall, the current CMOS LGAD prototype, namely MadPIX, represents a valuable proof of concept demonstrating the feasibility of implementing a gain layer within a standard CMOS CIS process. At the same time, the studies presented in this thesis identify a clear development roadmap based on three main directions: reduction of the active thickness, optimisation of the pixel geometry, and reduction of the front-end electronics jitter. The combination of these improvements is expected to significantly enhance the timing performance of the CMOS LGAD

toward the 20 ps target.

Conclusions

This work presented MadPIX, the first monolithic CMOS LGAD prototype used as a proof-of-concept for the ALICE 3 time-of-flight detector. The chip was designed in the 110 nm technology node, and its production was included in the last ARCADIA submission. The monolithic chip features large collection electrodes (pixel size of $250 \times 100\,\mu m^2$), gain layer, in-pixel electronics and a 48 μm sensor active thickness. Two different productions were submitted, *Run 3* and *Run 3.2*, using the same mask set but with different doping concentrations of the gain layer.

The chip dimensions are 16.4 mm $\times$ 4.4 mm, and it is composed of 8 matrices, each containing 64 pixels. The in-pixel front-end is AC-coupled to the collection electrode, and it is based on a cascoded common source amplifier followed by a differential buffer. Output buffers placed off-pixel and working with higher voltages are introduced in the periphery to drive the output pad and test board lines. The front-end electronics was designed to match the input capacitance of a 48 μm sensor with MadPIX pixel pitch. Post-layout simulations showed a front-end jitter below 10 ps for an intrinsic sensor gain above 15. Considering also the output buffer and the connections, a jitter between 20 and 15 ps was achieved for a sensor gain $10 \div 20$ and a power consumption of 760 mW/cm^2.

Monte Carlo simulations were used instead to predict the intrinsic sensor gain (≈ 15) and time resolution ($\approx 65\,$ps). The simulations were performed with nominal doping doses and profiles tuned to experimental data. The predicted gain from MC simulations for *Run 3* was about 3; this behaviour was attributed to a shallower gain-layer implantation inferred from CV measurements and reproduced by TCAD simulations tuned to the experimental data. The subsequent short loop (*Run 3.2*), in which the gain layer doping was selected based on the results of *Run 3*, showed a gain between 10 and 15 for the reference dose and around 5 for the -3.3 % dose. Simulations performed on *Run 3.2* profiles predicted a pixel efficiency above 87%, strongly dependent on the collection electrode bias. In-pixel position studies showed a deep correlation between the particle impinging position and the time of arrival of the signal.
The simulations also showed that the pixel pitch implemented in this prototype

could not have reached a time resolution below 90 ps RMS_t ($\sigma_t = 75$ ps) due to the disadvantageous pitch-to-thickness ratio; nevertheless, 55 ps were extracted considering only particles impinging in the pixel centre. Further simulations showed that the 20 ps resolution required by ALICE 3 can be achieved for a thickness of 15 μm and the same pitch.

The chip was statically characterised to extract its operating point. The collection electrode bias was biased up to 70 V, demonstrating that the AC coupling between the collection electrode and front end can sustain voltages high enough to trigger charge multiplication inside the sensor. The chips of *Run 3* showed a maximum gain of 2.8 and a very high substrate current. The low gain was increased in the following short-loop, *Run 3.2*, while the current was reduced by connecting a floating guard ring in the chip. Due to the low gain, the time resolution was dominated by the electronics jitter; 120 ps were achieved at CERN with a power consumption of 650 mW/cm^2.

The *Run 3.2* production showed a strong dependence between dose and sensor gain: $7 \div 8$ (-3.3 %), $9 \div 14$ (0 %) and $16 \div 20$ (+3.3 %). A time resolution below 90 ps was measured at CERN in a test beam. By increasing the FE currents and the biasing voltage to 1.5 V, the jitter term was lowered, and 72 ± 1 ps were achieved. The time resolution is limited by the distortion term arising from the sub-optimal pixel pitch. MadPIX was also characterised at DESY with a tracking telescope for in-pixel studies. The time resolution measured in the device centre was 58 ps for a 3.3 % dose split (65 ps in the reference dose), considering an area of $20 \times 10 \mu$m^2 in the pixel centre. A position-dependent delay, similar to MC simulations, was also extracted. Using the telescope, an efficiency of 95 % was found for V_{top} higher than 60 V. In addition, the efficiency showed a strong dependence on the collection electrode voltage as predicted in MC simulations.

The experimental results obtained by testing *Run 3* and *Run 3.2* proved the robustness of the simulation chain and the manufacturability of a monolithic CMOS sensor with an integrated gain layer. A second short loop was submitted in summer 2025, with a substrate active thickness of 15 μm.
The results presented in this work and the future measurements that will be obtained by testing the 15 μm-thick chips will provide the basis for the design of the CMOS LGAD that will be employed in the ALICE 3 experiment.

Appendix A

Beam Test data

The time resolution obtained in different beam tests and the threshold used are reported in the following tables.

Table A.1: Mean and standard deviation for each Layout and TB configuration for *Run 3*.

V_{top} **[V]**	$V_{back}[V]$	**Layout**	**TB**	σ_t **[ps]**	σ_{σ_t} **[ps]**
45	30.0	A1	TB2	254	4
45	30.0	A1	TB3	295	3
45	30.0	A2	TB2	255	3
45	30.0	A2	TB3	255	14
45	35.0	A1	TB2	259	4
45	35.0	A1	TB3	286	5
45	35.0	A2	TB2	244	5
45	35.0	A2	TB3	279	6
45	40.0	A1	TB2	257	6
45	40.0	A1	TB3	287	9
45	40.0	A2	TB2	244	5
45	40.0	A2	TB3	274	6
50	30.0	A1	TB2	209	4
50	30.0	A1	TB3	234	5
50	30.0	A2	TB2	194	4
50	30.0	A2	TB3	223	1
50	35.0	A2	TB2	193	4
50	35.0	A2	TB3	183	12
50	40.0	A1	TB3	224	5
50	40.0	A2	TB2	199	4

50	40.0	A2	TB3	189	11
55	30.0	A1	TB2	193	4
55	30.0	A1	TB3	210	3
55	30.0	A2	TB2	165	4
55	30.0	A2	TB3	184	5
55	35.0	A1	TB2	202	3
55	35.0	A1	TB3	218	4
55	35.0	A2	TB2	171	6
55	35.0	A2	TB3	189	5
55	40.0	A1	TB2	215	5
55	40.0	A1	TB3	230	3
55	40.0	A2	TB2	182	5
55	40.0	A2	TB3	200	4
58	22.5	A2	TB2	144	3
58	25.0	A2	TB2	148	3
58	25.0	A2	TB3	142	8
58	27.5	A2	TB2	149	2
58	30.0	A2	TB3	137	11
58	35.0	A2	TB2	166	4
58	35.0	A2	TB3	144	4
58	40.0	A2	TB3	163	8
58	45.0	A2	TB2	196	1
58	45.0	A2	TB3	183	11
59	30.0	A2	TB2	157	5
59	40.0	A2	TB2	172	3
60	22.5	A2	TB2	141	2
60	25.0	A2	TB2	146	3
60	27.5	A2	TB2	149	2
61	15.0	A2	TB2	137	2
61	17.5	A2	TB2	139	1
61	20.0	A2	TB2	141	1
61	25.0	A2	TB2	147	2
62	45.0	A2	TB3	201	6

Table A.2: Time resolution *Run 3* after FIB with and without boost.

V_{top} **[V]**	V_{back} **[V]**	**Layout**	**TB**	σ_t **[ps]**	σ_{σ_t} **[ps]**	**Boost**
47	32	A1	TB4	143	6	
49	32	A1	TB4	141	4	

51	32	A1	TB4	140	5	
53	25	A1	TB4	144	6	
53	30	A1	TB4	142	5	
53	32	A1	TB4	138	5	
56	32	A2	TB4	123	1	
58	32	A2	TB4	123	1	
60	32	A2	TB4	122	1	
62	32	A2	TB4	121	1	
64	25	A2	TB4	123	2	
64	30	A2	TB4	120	1	
64	32	A2	TB4	119	1	
66	32	A2	TB4	120	2	
53	30	A1	TB4	120	3	*
53	32	A1	TB4	117	3	*
58	32	A2	TB4	102	3	*
60	32	A2	TB4	101	3	*
62	32	A2	TB4	101	2	*
64	32	A2	TB4	99	2	*
66	25	A2	TB4	102	2	*
66	28	A2	TB4	100	2	*
66	30	A2	TB4	100	2	*
66	32	A2	TB4	99	4	*
68	32	A2	TB4	100	2	*

Table A.3: Leading edge threshold used for extracting the time resolution *Run 3* after FIB.

V_{top} **[V]**	V_{back} **[V]**	**Layout**	**TB**	**LE**$_{thr}$ **[mV]**	$\sigma_{LE_{thr}}[mV]$	**Boost**
47	32	A1	TB4	12	0	
49	32	A1	TB4	12	0	
51	32	A1	TB4	12	0	
53	25	A1	TB4	13	1	
53	30	A1	TB4	13	1	
53	32	A1	TB4	13	1	
56	32	A2	TB4	13	1	
58	32	A2	TB4	13	1	
60	32	A2	TB4	13	1	
62	32	A2	TB4	15	1	

64	25	A2	TB4	14	2	
64	30	A2	TB4	13	1	
64	32	A2	TB4	13	1	
66	32	A2	TB4	15	1	
53	30	A1	TB4	13	1	*
53	32	A1	TB4	13	1	*
58	32	A2	TB4	19	1	*
60	32	A2	TB4	17	3	*
62	32	A2	TB4	18	0	*
64	32	A2	TB4	18	0	*
66	25	A2	TB4	18	2	*
66	28	A2	TB4	19	1	*
66	30	A2	TB4	17	1	*
66	32	A2	TB4	17	1	*
68	32	A2	TB4	17	2	*

Appendix B

Pad frame

In the following table, the list of MadPIX pads is reported with their name and a brief description, the power domain to which they belong, and the voltage or current rating. The pad 0 is placed in the top right corner, and the numbering is clockwise. The external pads needed for sensor biasing are summarised at the end of the table and are named Ext<i>.

To separate the pads belonging to each power domain, matrices and layouts, the following notation is used:

- $\{\ \}_{i\alpha}$: i=[1,2], α=[a, b]. The subscripts are related to the matrices that the quantity in the brackets drives.
- Vcc and Vss: the former is the power, while the latter is the ground voltage.

Pad n°	Pad name	Domain	Function	Value
Top side				
Pad<0>	Gnd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Pad<1>	Gnd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Pad<2>	Vdd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Pad<3>	Vdd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Breaker				
Pad<4>	Vdd_1v2_a	Analog 1.2V	Top/bottom front-end $\{\text{Vcc}\}_{ia}$	1.2V
Pad<5>	Vdd_1v2_a	Analog 1.2V	Top/bottom front-end $\{\text{Vcc}\}_{ia}$	1.2V
Pad<6>	Gnd_1v2_a	Analog 1.2V	Top/bottom front-end $\{\text{Vss}\}_{ia}$	0V
Pad<7>	Gnd_1v2_a	Analog 1.2V	Top/bottom front-end $\{\text{Vss}\}_{ia}$	0V
Breaker				
Pad<8>	Vdd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Pad<9>	Vdd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Pad<10>	Gnd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Pad<11>	Gnd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Pad<12>	Analog_out_top_0	Analog 3.3V	Top analog output $\{00\}_{i\alpha}$	[0, 3.3]V
Pad<13>	Analog_out_top_1	Analog 3.3V	Top analog output $\{01\}_{i\alpha}$	[0, 3.3]V
Pad<14>	Analog_out_top_2	Analog 3.3V	Top analog output $\{02\}_{i\alpha}$	[0, 3.3]V
Pad<15>	Analog_out_top_3	Analog 3.3V	Top analog output $\{03\}_{i\alpha}$	[0, 3.3]V
Pad<16>	Analog_out_top_4	Analog 3.3V	Top analog output $\{04\}_{i\alpha}$	[0, 3.3]V
Pad<17>	Analog_out_top_5	Analog 3.3V	Top analog output $\{05\}_{i\alpha}$	[0, 3.3]V
Pad<18>	Analog_out_top_6	Analog 3.3V	Top analog output $\{06\}_{i\alpha}$	[0, 3.3]V
Pad<19>	Analog_out_top_7	Analog 3.3V	Top analog output $\{07\}_{i\alpha}$	[0, 3.3]V
Pad<20>	Analog_out_top_8	Analog 3.3V	Top analog output $\{08\}_{i\alpha}$	[0, 3.3]V
Pad<21>	Analog_out_top_9	Analog 3.3V	Top analog output $\{09\}_{i\alpha}$	[0, 3.3]V

Pad<22>	Analog_out_top_10	Analog 3.3V	Top analog output $\{10\}_{i\alpha}$	[0, 3.3]V
Pad<23>	Analog_out_top_11	Analog 3.3V	Top analog output $\{11\}_{i\alpha}$	[0, 3.3]V
Pad<24>	Analog_out_top_12	Analog 3.3V	Top analog output $\{12\}_{i\alpha}$	[0, 3.3]V
Pad<25>	Analog_out_top_13	Analog 3.3V	Top analog output $\{13\}_{i\alpha}$	[0, 3.3]V
Pad<26>	Analog_out_top_14	Analog 3.3V	Top analog output $\{14\}_{i\alpha}$	[0, 3.3]V
Pad<27>	Analog_out_top_15	Analog 3.3V	Top analog output $\{15\}_{i\alpha}$	[0, 3.3]V
Pad<28>	Analog_out_top_16	Analog 3.3V	Top analog output $\{16\}_{i\alpha}$	[0, 3.3]V
Pad<29>	Analog_out_top_17	Analog 3.3V	Top analog output $\{17\}_{i\alpha}$	[0, 3.3]V
Pad<30>	Analog_out_top_18	Analog 3.3V	Top analog output $\{18\}_{i\alpha}$	[0, 3.3]V
Pad<31>	Analog_out_top_19	Analog 3.3V	Top analog output $\{19\}_{i\alpha}$	[0, 3.3]V
Pad<32>	Analog_out_top_20	Analog 3.3V	Top analog output $\{20\}_{i\alpha}$	[0, 3.3]V
Pad<33>	Analog_out_top_21	Analog 3.3V	Top analog output $\{21\}_{i\alpha}$	[0, 3.3]V
Pad<34>	Analog_out_top_22	Analog 3.3V	Top analog output $\{22\}_{i\alpha}$	[0, 3.3]V
Pad<35>	Analog_out_top_23	Analog 3.3V	Top analog output $\{23\}_{i\alpha}$	[0, 3.3]V
Pad<36>	Analog_out_top_24	Analog 3.3V	Top analog output $\{24\}_{i\alpha}$	[0, 3.3]V
Pad<37>	Analog_out_top_25	Analog 3.3V	Top analog output $\{25\}_{i\alpha}$	[0, 3.3]V
Pad<38>	Analog_out_top_26	Analog 3.3V	Top analog output $\{26\}_{i\alpha}$	[0, 3.3]V
Pad<39>	Analog_out_top_27	Analog 3.3V	Top analog output $\{27\}_{i\alpha}$	[0, 3.3]V
Pad<40>	Analog_out_top_28	Analog 3.3V	Top analog output $\{28\}_{i\alpha}$	[0, 3.3]V
Pad<41>	Analog_out_top_29	Analog 3.3V	Top analog output $\{29\}_{i\alpha}$	[0, 3.3]V
Pad<42>	Analog_out_top_30	Analog 3.3V	Top analog output $\{30\}_{i\alpha}$	[0, 3.3]V
Pad<43>	Analog_out_top_31	Analog 3.3V	Top analog output $\{31\}_{i\alpha}$	[0, 3.3]V
Pad<44>	Gnd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Pad<45>	Gnd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Pad<46>	Vdd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Pad<47>	Vdd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Pad<48>	Analog_out_top_32	Analog 3.3V	Top analog output $\{32\}_{i\alpha}$	[0, 3.3]V

Pad<49>	Analog_out_top_33	Analog 3.3V	Top analog output {33}$_{ia}$	[0, 3.3]V
Pad<50>	Analog_out_top_34	Analog 3.3V	Top analog output {34}$_{ia}$	[0, 3.3]V
Pad<51>	Analog_out_top_35	Analog 3.3V	Top analog output {35}$_{ia}$	[0, 3.3]V
Pad<52>	Analog_out_top_36	Analog 3.3V	Top analog output {36}$_{ia}$	[0, 3.3]V
Pad<53>	Analog_out_top_37	Analog 3.3V	Top analog output {37}$_{ia}$	[0, 3.3]V
Pad<54>	Analog_out_top_38	Analog 3.3V	Top analog output {38}$_{ia}$	[0, 3.3]V
Pad<55>	Analog_out_top_39	Analog 3.3V	Top analog output {39}$_{ia}$	[0, 3.3]V
Pad<56>	Analog_out_top_40	Analog 3.3V	Top analog output {40}$_{ia}$	[0, 3.3]V
Pad<57>	Analog_out_top_41	Analog 3.3V	Top analog output {41}$_{ia}$	[0, 3.3]V
Pad<58>	Analog_out_top_42	Analog 3.3V	Top analog output {42}$_{ia}$	[0, 3.3]V
Pad<59>	Analog_out_top_43	Analog 3.3V	Top analog output {43}$_{ia}$	[0, 3.3]V
Pad<60>	Analog_out_top_44	Analog 3.3V	Top analog output {44}$_{ia}$	[0, 3.3]V
Pad<61>	Analog_out_top_45	Analog 3.3V	Top analog output {45}$_{ia}$	[0, 3.3]V
Pad<62>	Analog_out_top_46	Analog 3.3V	Top analog output {46}$_{ia}$	[0, 3.3]V
Pad<63>	Analog_out_top_47	Analog 3.3V	Top analog output {47}$_{ia}$	[0, 3.3]V
Pad<64>	Analog_out_top_48	Analog 3.3V	Top analog output {48}$_{ia}$	[0, 3.3]V
Pad<65>	Analog_out_top_49	Analog 3.3V	Top analog output {49}$_{ia}$	[0, 3.3]V
Pad<66>	Analog_out_top_50	Analog 3.3V	Top analog output {50}$_{ia}$	[0, 3.3]V
Pad<67>	Analog_out_top_51	Analog 3.3V	Top analog output {51}$_{ia}$	[0, 3.3]V
Pad<68>	Analog_out_top_52	Analog 3.3V	Top analog output {52}$_{ia}$	[0, 3.3]V
Pad<69>	Analog_out_top_53	Analog 3.3V	Top analog output {53}$_{ia}$	[0, 3.3]V
Pad<70>	Analog_out_top_54	Analog 3.3V	Top analog output {54}$_{ia}$	[0, 3.3]V
Pad<71>	Analog_out_top_55	Analog 3.3V	Top analog output {55}$_{ia}$	[0, 3.3]V
Pad<72>	Analog_out_top_56	Analog 3.3V	Top analog output {56}$_{ia}$	[0, 3.3]V
Pad<73>	Analog_out_top_57	Analog 3.3V	Top analog output {57}$_{ia}$	[0, 3.3]V
Pad<74>	Analog_out_top_58	Analog 3.3V	Top analog output {58}$_{ia}$	[0, 3.3]V
Pad<75>	Analog_out_top_59	Analog 3.3V	Top analog output {59}$_{ia}$	[0, 3.3]V

Pad<76>	Analog_out_top_60	Analog 3.3V	Top analog output $\{60\}_{i\alpha}$	[0, 3.3]V
Pad<77>	Analog_out_top_61	Analog 3.3V	Top analog output $\{61\}_{i\alpha}$	[0, 3.3]V
Pad<78>	Analog_out_top_62	Analog 3.3V	Top analog output $\{62\}_{i\alpha}$	[0, 3.3]V
Pad<79>	Analog_out_top_63	Analog 3.3V	Top analog output $\{63\}_{i\alpha}$	[0, 3.3]V
Pad<80>	Gnd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Pad<81>	Gnd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Pad<82>	Vdd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Pad<83>	Vdd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Breaker				
Pad<84>	Gnd_1v2_b	Analog 1.2V	Top/bottom front-end $\{\text{Vss}\}_{ib}$	0V
Pad<85>	Gnd_1v2_b	Analog 1.2V	Top/bottom front-end $\{\text{Vss}\}_{ib}$	0V
Pad<86>	Vdd_1v2_b	Analog 1.2V	Top/bottom front-end $\{\text{Vcc}\}_{ib}$	1.2V
Pad<87>	Vdd_1v2_b	Analog 1.2V	Top/bottom front-end $\{\text{Vcc}\}_{ib}$	1.2V
Breaker				
Pad<88>	Vdd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Pad<89>	Vdd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Pad<90>	Gnd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Pad<91>	Gnd_3v3_top	Analog 3.3V	Top *out_ buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Right side				
Pad<92>	Bline_buffer_3v3_top	Analog 3.3V	Top *out_ buffers* baseline $\{\text{V}\}_{i\alpha}$	[1, 2.5]V
Pad<93>	Bias_buffer_3v3_top	Analog 3.3V	Top *out_ buffers* bias current $\{\text{A}\}_{i\alpha}$	[250, 1500]μA
Pad<94>	Bias_conv_3v3_top	Analog 3.3V	Top 1.2-3.3V converter bias current $\{\text{A}\}_{i\alpha}$	1μA
Breaker				
Pad<95>	Vdd_dig_top	Digital 1.2V	Top digital $\{\text{Vcc}\}_{i\alpha}$	1.2V
Pad<96>	Vdd_dig_top	Digital 1.2V	Top digital $\{\text{Vcc}\}_{i\alpha}$	1.2V

Pad<97>	Gnd_dig_top	Digital 1.2V	Top digital $\{Vss\}_{i\alpha}$	0V
Pad<98>	Gnd_dig_top	Digital 1.2V	Top digital $\{Vss\}_{i\alpha}$	0V
Breaker				
Pad<99>	Vdd_1v2_b	Analog 1.2V	Top/bottom front-end $\{Vcc\}_{ib}$	1.2V
Pad<100>	Vdd_1v2_b	Analog 1.2V	Top/bottom front-end $\{Vcc\}_{ib}$	1.2V
Pad<101>	Bias_amp_casn_b	Analog 1.2V	Top/bottom front-end amplifiers cascode N $\{V\}_{ib}$	[0.5, 1.2]V
Pad<102>	Bias_buffer_b	Analog 1.2V	Top/bottom front-end buffers bias current $\{A\}_{ib}$	[25, 75]μA
Pad<103>	Bias_amp_b	Analog 1.2V	Top/bottom front-end amplifiers bias current $\{A\}_{ib}$	[10, 200]μA
Pad<104>	Bias_amp_casp_b	Analog 1.2V	Top/bottom front-end amplifiers cascode P $\{V\}_{ib}$	[0, 0.7]V
Pad<105>	Gnd_1v2_b	Analog 1.2V	Top/bottom front-end $\{Vss\}_{ib}$	0V
Pad<106>	Gnd_1v2_b	Analog 1.2V	Top/bottom front-end $\{Vss\}_{ib}$	0V
Breaker				
Pad<107>	Gnd_dig_bot	Digital 1.2V	Bottom digital $\{Vss\}_{i\alpha}$	0V
Pad<108>	Gnd_dig_bot	Digital 1.2V	Bottom digital $\{Vss\}_{i\alpha}$	0V
Pad<109>	Vdd_dig_bot	Digital 1.2V	Bottom digital $\{Vcc\}_{i\alpha}$	1.2V
Pad<110>	Vdd_dig_bot	Digital 1.2V	Bottom digital $\{Vcc\}_{i\alpha}$	1.2V
Pad<111>	Vdd_core_padframe	Core 1.2V	Padframe Vcc	1.2V
Pad<112>	Vdd_core_padframe	Core 1.2V	Padframe Vcc	1.2V
Pad<113>	Gnd_core_padframe	Core 1.2V	Padframe Vss	0V
Pad<114>	Gnd_core_padframe	Core 1.2V	Padframe Vss	0V
Breaker				
Pad<115>	Bias_conv_3v3_bot	Analog 3.3V	Bottom 1.2-3.3V converter bias current $\{A\}_{i\alpha}$	1μA
Pad<116>	Bias_buffer_3v3_bot	Analog 3.3V	Bottom *out_ buffers* bias current $\{A\}_{i\alpha}$	[250, 1500]μA
Pad<117>	Bline_buffer_3v3_bot	Analog 3.3V	Bottom *out_ buffers* baseline $\{V\}_{i\alpha}$	[1, 2.5]V
Bottom side				

Pad<118>	Gnd_3v3_bot	Analog 3.3V	Bottom *out_buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Pad<119>	Gnd_3v3_bot	Analog 3.3V	Bottom *out_buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Pad<120>	Vdd_3v3_bot	Analog 3.3V	Bottom *out_buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Pad<121>	Vdd_3v3_bot	Analog 3.3V	Bottom *out_buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Breaker				
Pad<122>	Vdd_1v2_b	Analog 1.2V	Top/bottom front-end $\{\text{Vcc}\}_{ib}$	1.2V
Pad<123>	Vdd_1v2_b	Analog 1.2V	Top/bottom front-end $\{\text{Vcc}\}_{ib}$	1.2V
Pad<124>	Gnd_1v2_b	Analog 1.2V	Top/bottom front-end $\{\text{Vss}\}_{ib}$	0V
Pad<125>	Gnd_1v2_b	Analog 1.2V	Top/bottom front-end $\{\text{Vss}\}_{ib}$	0V
Breaker				
Pad<126>	Vdd_3v3_bot	Analog 3.3V	Bottom *out_buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Pad<127>	Vdd_3v3_bot	Analog 3.3V	Bottom *out_buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Pad<128>	Gnd_3v3_bot	Analog 3.3V	Bottom *out_buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Pad<129>	Gnd_3v3_bot	Analog 3.3V	Bottom *out_buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Pad<130>	Analog_out_bot_63	Analog 3.3V	Bottom analog output $\{63\}_{i\alpha}$	[0, 3.3]V
Pad<131>	Analog_out_bot_62	Analog 3.3V	Bottom analog output $\{62\}_{i\alpha}$	[0, 3.3]V
Pad<132>	Analog_out_bot_61	Analog 3.3V	Bottom analog output $\{61\}_{i\alpha}$	[0, 3.3]V
Pad<133>	Analog_out_bot_60	Analog 3.3V	Bottom analog output $\{60\}_{i\alpha}$	[0, 3.3]V
Pad<134>	Analog_out_bot_59	Analog 3.3V	Bottom analog output $\{59\}_{i\alpha}$	[0, 3.3]V
Pad<135>	Analog_out_bot_58	Analog 3.3V	Bottom analog output $\{58\}_{i\alpha}$	[0, 3.3]V
Pad<136>	Analog_out_bot_57	Analog 3.3V	Bottom analog output $\{57\}_{i\alpha}$	[0, 3.3]V
Pad<137>	Analog_out_bot_56	Analog 3.3V	Bottom analog output $\{56\}_{i\alpha}$	[0, 3.3]V
Pad<138>	Analog_out_bot_55	Analog 3.3V	Bottom analog output $\{55\}_{i\alpha}$	[0, 3.3]V
Pad<139>	Analog_out_bot_54	Analog 3.3V	Bottom analog output $\{54\}_{i\alpha}$	[0, 3.3]V
Pad<140>	Analog_out_bot_53	Analog 3.3V	Bottom analog output $\{53\}_{i\alpha}$	[0, 3.3]V
Pad<141>	Analog_out_bot_52	Analog 3.3V	Bottom analog output $\{52\}_{i\alpha}$	[0, 3.3]V
Pad<142>	Analog_out_bot_51	Analog 3.3V	Bottom analog output $\{51\}_{i\alpha}$	[0, 3.3]V

Pad<143>	Analog_out_bot_50	Analog 3.3V	Bottom analog output $\{50\}_{ia}$	[0, 3.3]V
Pad<144>	Analog_out_bot_49	Analog 3.3V	Bottom analog output $\{49\}_{ia}$	[0, 3.3]V
Pad<145>	Analog_out_bot_48	Analog 3.3V	Bottom analog output $\{48\}_{ia}$	[0, 3.3]V
Pad<146>	Analog_out_bot_47	Analog 3.3V	Bottom analog output $\{47\}_{ia}$	[0, 3.3]V
Pad<147>	Analog_out_bot_46	Analog 3.3V	Bottom analog output $\{46\}_{ia}$	[0, 3.3]V
Pad<148>	Analog_out_bot_45	Analog 3.3V	Bottom analog output $\{45\}_{ia}$	[0, 3.3]V
Pad<149>	Analog_out_bot_44	Analog 3.3V	Bottom analog output $\{44\}_{ia}$	[0, 3.3]V
Pad<150>	Analog_out_bot_43	Analog 3.3V	Bottom analog output $\{43\}_{ia}$	[0, 3.3]V
Pad<151>	Analog_out_bot_42	Analog 3.3V	Bottom analog output $\{42\}_{ia}$	[0, 3.3]V
Pad<152>	Analog_out_bot_41	Analog 3.3V	Bottom analog output $\{41\}_{ia}$	[0, 3.3]V
Pad<153>	Analog_out_bot_40	Analog 3.3V	Bottom analog output $\{40\}_{ia}$	[0, 3.3]V
Pad<154>	Analog_out_bot_39	Analog 3.3V	Bottom analog output $\{39\}_{ia}$	[0, 3.3]V
Pad<155>	Analog_out_bot_38	Analog 3.3V	Bottom analog output $\{38\}_{ia}$	[0, 3.3]V
Pad<156>	Analog_out_bot_37	Analog 3.3V	Bottom analog output $\{37\}_{ia}$	[0, 3.3]V
Pad<157>	Analog_out_bot_36	Analog 3.3V	Bottom analog output $\{36\}_{ia}$	[0, 3.3]V
Pad<158>	Analog_out_bot_35	Analog 3.3V	Bottom analog output $\{35\}_{ia}$	[0, 3.3]V
Pad<159>	Analog_out_bot_34	Analog 3.3V	Bottom analog output $\{34\}_{ia}$	[0, 3.3]V
Pad<160>	Analog_out_bot_33	Analog 3.3V	Bottom analog output $\{33\}_{ia}$	[0, 3.3]V
Pad<161>	Analog_out_bot_32	Analog 3.3V	Bottom analog output $\{32\}_{ia}$	[0, 3.3]V
Pad<162>	Vdd_3v3_bot	Analog 3.3V	Bottom *out_ buffers* $\{\text{Vcc}\}_{ia}$	3.3V
Pad<163>	Vdd_3v3_bot	Analog 3.3V	Bottom *out_ buffers* $\{\text{Vcc}\}_{ia}$	3.3V
Pad<164>	Gnd_3v3_bot	Analog 3.3V	Bottom *out_ buffers* $\{\text{Vss}\}_{ia}$	0V
Pad<165>	Gnd_3v3_bot	Analog 3.3V	Bottom *out_ buffers* $\{\text{Vss}\}_{ia}$	0V
Pad<166>	Analog_out_bot_31	Analog 3.3V	Bottom analog output $\{31\}_{ia}$	[0, 3.3]V
Pad<167>	Analog_out_bot_30	Analog 3.3V	Bottom analog output $\{30\}_{ia}$	[0, 3.3]V
Pad<168>	Analog_out_bot_29	Analog 3.3V	Bottom analog output $\{29\}_{ia}$	[0, 3.3]V
Pad<169>	Analog_out_bot_28	Analog 3.3V	Bottom analog output $\{28\}_{ia}$	[0, 3.3]V

Pad<170>	Analog_out_bot_27	Analog 3.3V	Bottom analog output $\{27\}_{ia}$	[0, 3.3]V
Pad<171>	Analog_out_bot_26	Analog 3.3V	Bottom analog output $\{26\}_{ia}$	[0, 3.3]V
Pad<172>	Analog_out_bot_25	Analog 3.3V	Bottom analog output $\{25\}_{ia}$	[0, 3.3]V
Pad<173>	Analog_out_bot_24	Analog 3.3V	Bottom analog output $\{24\}_{ia}$	[0, 3.3]V
Pad<174>	Analog_out_bot_23	Analog 3.3V	Bottom analog output $\{23\}_{ia}$	[0, 3.3]V
Pad<175>	Analog_out_bot_22	Analog 3.3V	Bottom analog output $\{22\}_{ia}$	[0, 3.3]V
Pad<176>	Analog_out_bot_21	Analog 3.3V	Bottom analog output $\{21\}_{ia}$	[0, 3.3]V
Pad<177>	Analog_out_bot_20	Analog 3.3V	Bottom analog output $\{20\}_{ia}$	[0, 3.3]V
Pad<178>	Analog_out_bot_19	Analog 3.3V	Bottom analog output $\{19\}_{ia}$	[0, 3.3]V
Pad<179>	Analog_out_bot_18	Analog 3.3V	Bottom analog output $\{18\}_{ia}$	[0, 3.3]V
Pad<180>	Analog_out_bot_17	Analog 3.3V	Bottom analog output $\{17\}_{ia}$	[0, 3.3]V
Pad<181>	Analog_out_bot_16	Analog 3.3V	Bottom analog output $\{16\}_{ia}$	[0, 3.3]V
Pad<182>	Analog_out_bot_15	Analog 3.3V	Bottom analog output $\{15\}_{ia}$	[0, 3.3]V
Pad<183>	Analog_out_bot_14	Analog 3.3V	Bottom analog output $\{14\}_{ia}$	[0, 3.3]V
Pad<184>	Analog_out_bot_13	Analog 3.3V	Bottom analog output $\{13\}_{ia}$	[0, 3.3]V
Pad<185>	Analog_out_bot_12	Analog 3.3V	Bottom analog output $\{12\}_{ia}$	[0, 3.3]V
Pad<186>	Analog_out_bot_11	Analog 3.3V	Bottom analog output $\{11\}_{ia}$	[0, 3.3]V
Pad<187>	Analog_out_bot_10	Analog 3.3V	Bottom analog output $\{10\}_{ia}$	[0, 3.3]V
Pad<188>	Analog_out_bot_9	Analog 3.3V	Bottom analog output $\{9\}_{ia}$	[0, 3.3]V
Pad<189>	Analog_out_bot_8	Analog 3.3V	Bottom analog output $\{8\}_{ia}$	[0, 3.3]V
Pad<190>	Analog_out_bot_7	Analog 3.3V	Bottom analog output $\{7\}_{ia}$	[0, 3.3]V
Pad<191>	Analog_out_bot_6	Analog 3.3V	Bottom analog output $\{6\}_{ia}$	[0, 3.3]V
Pad<192>	Analog_out_bot_5	Analog 3.3V	Bottom analog output $\{5\}_{ia}$	[0, 3.3]V
Pad<193>	Analog_out_bot_4	Analog 3.3V	Bottom analog output $\{4\}_{ia}$	[0, 3.3]V
Pad<194>	Analog_out_bot_3	Analog 3.3V	Bottom analog output $\{3\}_{ia}$	[0, 3.3]V
Pad<195>	Analog_out_bot_2	Analog 3.3V	Bottom analog output $\{2\}_{ia}$	[0, 3.3]V
Pad<196>	Analog_out_bot_1	Analog 3.3V	Bottom analog output $\{1\}_{ia}$	[0, 3.3]V

Pad<197>	Analog_out_bot_0	Analog 3.3V	Bottom analog output $\{0\}_{i\alpha}$	[0, 3.3]V
Pad<198>	Gnd_3v3_bot	Analog 3.3V	Bottom *out_buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Pad<199>	Gnd_3v3_bot	Analog 3.3V	Bottom *out_buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Pad<200>	Vdd_3v3_bot	Analog 3.3V	Bottom *out_buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Pad<201>	Vdd_3v3_bot	Analog 3.3V	Bottom *out_buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Breaker				
Pad<202>	Gnd_1v2_a	Analog 1.2V	Top/bottom front-end $\{\text{Vss}\}_{ia}$	0V
Pad<203>	Gnd_1v2_a	Analog 1.2V	Top/bottom front-end $\{\text{Vss}\}_{ia}$	0V
Pad<204>	Vdd_1v2_a	Analog 1.2V	Top/bottom front-end $\{\text{Vcc}\}_{ia}$	1.2V
Pad<205>	Vdd_1v2_a	Analog 1.2V	Top/bottom front-end $\{\text{Vcc}\}_{ia}$	1.2V
Breaker				
Pad<206>	Vdd_3v3_bot	Analog 3.3V	Bottom *out_buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Pad<207>	Vdd_3v3_bot	Analog 3.3V	Bottom *out_buffers* $\{\text{Vcc}\}_{i\alpha}$	3.3V
Pad<208>	Gnd_3v3_bot	Analog 3.3V	Bottom *out_buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Pad<209>	Gnd_3v3_bot	Analog 3.3V	Bottom *out_buffers* $\{\text{Vss}\}_{i\alpha}$	0V
Left side				
Breaker				
Pad<210>	Enable_2b_bot	Digital 1.2V	Bottom enable matrix *2b*	0-1.2V
Pad<211>	Enable_1b_bot	Digital 1.2V	Bottom enable matrix *1b*	0-1.2V
Pad<212>	Enable_2a_bot	Digital 1.2V	Bottom enable matrix *2a*	0-1.2V
Pad<213>	Enable_1a_bot	Digital 1.2V	Bottom enable matrix *1a*	0-1.2V
Pad<214>	D_in_bot	Digital 1.2V	Bottom start shift-register $\{\text{V}\}_{i\alpha}$	0-1.2V
Pad<215>	Set_in_bot	Digital 1.2V	Bottom set rolling shutter $\{\text{V}\}_{i\alpha}$	0-1.2V
Pad<216>	Clk_in_bot	Digital 1.2V	Bottom clock $\{\text{V}\}_{i\alpha}$	0-1.2V
Pad<217>	Vdd_dig_bot	Digital 1.2V	Bottom digital $\{\text{Vcc}\}_{i\alpha}$	1.2V
Pad<218>	Vdd_dig_bot	Digital 1.2V	Bottom digital $\{\text{Vcc}\}_{i\alpha}$	1.2V

Pad<219>	Gnd_dig_bot	Digital 1.2V	Bottom digital $\{Vss\}_{i\alpha}$	0V
Pad<220>	Gnd_dig_bot	Digital 1.2V	Bottom digital $\{Vss\}_{i\alpha}$	0V
Breaker				
Pad<221>	Gnd_1v2_a	Analog 1.2V	Top/bottom front-end $\{Vss\}_{ia}$	0V
Pad<222>	Gnd_1v2_a	Analog 1.2V	Top/bottom front-end $\{Vss\}_{ia}$	0V
Pad<223>	Bias_amp_casp_a	Analog 1.2V	Top/bottom front-end amplifiers cascode P $\{V\}_{ia}$	[0, 0.7]V
Pad<224>	Bias_amp_a	Analog 1.2V	Top/bottom front-end amplifiers bias current $\{A\}_{ia}$	[10, 200]μA
Pad<225>	Bias_buffer_a	Analog 1.2V	Top/bottom front-end buffers bias current $\{A\}_{ia}$	[25, 75]μA
Pad<226>	Bias_amp_casn_a	Analog 1.2V	Top/bottom front-end amplifiers cascode N $\{V\}_{ia}$	[0.5, 1.2]V
Pad<227>	Vdd_1v2_a	Analog 1.2V	Top/bottom front-end $\{Vcc\}_{ia}$	1.2V
Pad<228>	Vdd_1v2_a	Analog 1.2V	Top/bottom front-end $\{Vcc\}_{ia}$	1.2V
Breaker				
Pad<229>	Gnd_dig_top	Digital 1.2V	Top digital $\{Vss\}_{i\alpha}$	0V
Pad<230>	Gnd_dig_top	Digital 1.2V	Top digital $\{Vss\}_{i\alpha}$	0V
Pad<231>	Vdd_dig_top	Digital 1.2V	Top digital $\{Vcc\}_{i\alpha}$	1.2V
Pad<232>	Vdd_dig_top	Digital 1.2V	Top digital $\{Vcc\}_{i\alpha}$	1.2V
Pad<233>	Clk_in_top	Digital 1.2V	Top clock $\{V\}_{i\alpha}$	0-1.2V
Pad<234>	Set_in_top	Digital 1.2V	Top set rolling shutter $\{V\}_{i\alpha}$	0-1.2V
Pad<235>	D_in_top	Digital 1.2V	Top start shift-register $\{V\}_{i\alpha}$	0-1.2V
Pad<236>	Enable_1a_top	Digital 1.2V	Top enable matrix *1a*	0-1.2V
Pad<237>	Enable_2a_top	Digital 1.2V	Top enable matrix *2a*	0-1.2V
Pad<238>	Enable_1b_top	Digital 1.2V	Top enable matrix *1b*	0-1.2V
Pad<239>	Enable_2b_top	Digital 1.2V	Top enable matrix *2b*	0-1.2V
Breaker				
External pad				
Ext<0>	Edge_term_ring	Analog	Backside bias	[-100, 0]V

Ext<1>	Guard_ring	Analog	Guard ring bias	[0, 100]V
Ext<2>	Edge_term_ring	Analog	Backside bias	[-100, 0]V
Ext<3>	Bias_hv_2b	Analog	Topside bias *2b*	[0, 100]V
Ext<4>	Bias_hv_1b	Analog	Topside bias *1b*	[0, 100]V
Ext<5>	Edge_term_ring	Analog	Backside bias	[0, 100]V
Ext<6>	Guard_ring	Analog	Guard ring bias	[0, 100]V
Ext<7>	Edge_term_ring	Analog	Backside bias	[-100, 0]V
Ext<8>	Bias_hv_2a	Analog	Topside bias *2a*	[0, 100]V
Ext<9>	Bias_hv_1a	Analog	Topside bias *1a*	[0, 100]V

Nomenclature

Roman letters

η	Pseudorapidity	
ρ	Charge density	$[\mathrm{C\,cm^{-3}}]$
σ_J	Electronics jitter	[ps]
σ_t	Time resolution	[ps]
B	Magnetic field	[T]
E	Electric field	$[\mathrm{V\,cm^{-1}}]$
E_W	Weighting field	$[\mathrm{V\,cm^{-1}}]$
p_T	Transverse momentum	$[\mathrm{GeV\,c^{-1}}]$
T	Temperature	[K]
V	Electric potential	[V]
V_W	Weighting potential	

Constants

ε_0	Electric constant $8.854 \cdot 10^{-12}\,\mathrm{C\,V^{-1}\,m^{-1}}$
ε_{Si}	Silicon relative permittivity 11.68
k_b	Boltzamn constant $1.38 \cdot 10^{-23}\,\mathrm{m^2\,kg\,s^{-2}\,K^{-1}}$
T_0	Reference temperature 300 K

Abbreviations and acronyms

AdS/CFT	Anti-de Sitter/Conformal field theory

ALICE A Large Ion Collider Experiment

ASIC Application-Specific Integrated Circuit

ATLAS A Toroidal LHC Apparatus

AXI Advanced eXtensible Interface

BJT Bipolar Junction Transistor

BNC Bayonet Neill Concelman connector

BT Beam Test

CDN Clock Distribution Network

CERN Conseil européen pour la recherche nucléaire

CF Constant Fraction algorithm

CF Constant Fraction

CIS CMOS Image Sensor

CMOS Complementary Metal-Oxide-Semiconductor

CMS Compact Muon Solenoid

CSA Charge Sensitive Amplifier

DAC Digital to Analog Converter

DESY Deutsches Elektronen-Synchrotron

DMAPS Depleted Monolithic Active Pixel Sensor

DUT Device Under Test

ePIC Electron-Proton/Ion Collider

FBK Fondazione Bruno Kessler

FCC Future Circular Collider

FE Front End

FIB Focused Ion Beam

FOM Figure Of Merit

FPGA Field Programmable Gate Array

FWHM Full Width at Half Maximum

HDMI High-Definition Multimedia Interface

HEED High-Energy ElectroDynamics

HEP High Energy Physics

IBIC Ion Beam Induced Chemical vapor deposition

IC Integrated Circuit

IR Infra Red

ITS2 Inner Tracking System 2

ITS3 Inner Tracking System 3

LE Leading Edge algorithm

LGAD Low Gain Avalanche Diode

LHC Large Hadron Collider

LOI Letter Of Intent

LSB Least Significant Bit

LVDS Low-Voltage Differential Signaling

MAPS Monolithic Active Pixel Sensor

MFT Muon Forward Tracker

MIP Minimum Ionizing Particle

MPV Most Probable Value

PAI Photo-Absorption Ionization

QCD Quantum ChromoDynamics

QGP Ring-Imaging Cherenkov detector

R&D Research and Development

RICH Ring-Imaging Cherenkov detector

RSD Resistive Silicon Detector

SEM Scanning Electron Microscope

SiPM Silicon Photomultiplier

SiPM Silicon Photon Multiplier

SNR Signal-to-Noise Ratio

SoC System on Chip

TB Test Board

TCAD Technology Computer-Aided design

TCT Transient Current Technique

TDC Time to Digital Converter

TLU Trigger Logic Unit

TOA Time Of Arrival

TOF Time-of-Flight

TOT Timo Over Threshold

TP Test Pulse

TPSCo Tower Partners Semiconductor Co. Ltd.

ZCU Zynq UltraScale+

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