Design and implementation of a transresistance amplifier for accurate current measurements in the microampere range

Design and implementation of a transresistance amplifier for accurate current measurements in the microampere range

Marta Musso, Massimo Ortolano

***Abstract*—This article presents the design, implementation and preliminary verification of a transresistance amplifier suitable for the operation with calibrated external resistance standards, allowing traceable and accurate current measurements in the microampere range. Traditionally, the traceability of current measurements is ensured by calibration through the injection into a transresistance amplifier of one or more calibrated currents. The transresistance amplifier presented in this work allows for an alternative traceability path, in which the calibration is ensured by an external calibrated resistance standard and the accuracy of the transresistance gain. The transresistance amplifier has been designed for an accuracy of the transresistance gain at the level of $0.1\,\mu\Omega/\Omega$ with respect to the external transresistance value. The transresistance gain error has been experimentally verified with an uncertainty at the level of $0.3\,\mu\Omega/\Omega$ (coverage factor of 2). The current measurement uncertainty introduced by this transresistance amplifier is thus at the $0.1\,\mu\mathrm{A/A}$ level.**

***Index Terms*—Current measurement, electrical resistance measurement, low-noise amplifiers, calibration, measurement uncertainty**

I. Introduction

THE measurement of small-medium direct (DC) electric currents, from the sub-femtoampere range to the milliampere range, is commonly performed with *transresistance amplifiers* (TRAs, *current-to-voltage converters*, *IV converters*) [1, Chap. 4x.3], [2, Sec. 2.1], [3, Sec. 4.2.1]. Like *shunt resistors* (*current shunts*), TRAs convert current into voltage, with a conversion factor or gain called *transresistance* or *mutual resistance*. With respect to shunt resistors, TRAs provide lower input and output resistances [2, Sec. 2.1], [3, Sec. 4.2.1], thus minimizing the errors due to the input burden voltage and the output loading at small currents, where high conversion factors are needed. For small-medium alternating (AC) currents or generally variable currents, *transimpedance amplifiers* (TIAs) are commonly used. These are very similar to TRAs, but with a bandwidth optimized for the current signals of interest.

TRAs and TIAs are employed in a wide variety of applications and can be purpose-designed, available on the market as standalone devices or embedded in instruments such as electrometers and source-measure units.

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Accurate TRA current measurements require the traceability of the transresistance to the International System of Units (SI) and the removal of offset and drift errors by means of polarity reversals or other offset and drift cancellation schemes [4, Sec. 3.3.2], [5].

The traceability of the transresistance to the SI can be ensured by two alternative techniques: i) transresistance calibration by injection of one or more calibrated currents and measurement of the corresponding output voltages with a calibrated voltmeter; or ii) definition of the TRA transresistance by a calibrated external resistance standard and design of the TRA so that its contribution to the transresistance uncertainty is at a specified level.

Technique i) is commonplace and is routinely employed by National Metrology Institutes (NMIs) and calibration laboratories to calibrate commercial electrometers and TRAs. Methods for the traceable generation of currents are reviewed in [6], [7], [8], [9]. State-of-the-art systems emerged in the last decade are the *ultrastable low-noise current amplifier* (ULCA) [10], [11], [12], [13], [14], [15], [16], [17], the *programmable quantum current generator* (PQCG) [18], [19], [20], [21] and the direct combination of a programmable Josephson voltage standard with either a quantized Hall array resistance standard (QHARS) [22] or a quantized anomalous Hall resistance standard [23]. In the ULCA, thanks to its special architecture, current gain and transresistance can be directly calibrated from a quantized Hall resistance standard (QHRS) by means of a cryogenic current comparator. The other systems exploit Ohm's law to directly generate quantized currents from the Josephson and the quantum Hall effects (a "quantum Ohm's law").

Technique ii) requires a bespoke TRA design. To date, to the authors' knowledge, it was concretely applied only in [24], where the TRA was implemented by cascading a commercial TRA with the second stage of an ULCA configured as integrator. In [12] it was first suggested to use a QHRS to define the transresistance of the second stage of an ULCA for a quantum triangle experiment.

The present work pursues technique ii) and describes the design, implementation and preliminary verification of a TRA for the traceable measurement of currents in the microampere range with a target accuracy at the $0.1\,\mu\mathrm{A/A}$ level. The TRA has been designed to operate with calibrated external four-terminal room-temperature artifact resistance standards with nominal values of $10\,\mathrm{k}\Omega$ and $1\,\mathrm{M}\Omega$, single-element QHRSs with nominal value $R_\mathrm{H} = R_\mathrm{K}/2$ ($\approx 12\,906\,\Omega$) and

one-hundred-element QHARSs with nominal value $100R_{\mathrm{H}}$ ($\approx 1.2906\,\mathrm{M\Omega}$), ensuring a transresistance gain accuracy at the level of $0.1\,\mu\Omega/\Omega$ with respect to the external resistance value. The useful measuring ranges in which the expected order of uncertainty can be obtained with feasible integration times, without considering the current source noise, are about $(10\text{–}1000)\,\mu\mathrm{A}$ for a $10\,\mathrm{k\Omega}$ transresistance and about $(0.1\text{–}10)\,\mu\mathrm{A}$ for a $1\,\mathrm{M\Omega}$ transresistance. With QHRS and QHARS, the maximum current is indeed limited by the device breakdown current. The design also takes into account the possible need for long interconnecting cables to the external resistance standards, allowing input and output capacitive loads of up to $3\,\mathrm{nF}$, and the need to protect QHRSs and QHARSs from overvoltages. The TRA has been conceived as a composite amplifier to meet the stated specifications and be flexible enough for future adaptations to higher transresistance values. Two prototypes have been assembled and labeled QuTRA 1.1 and 1.2.

The structure of this paper is as follows. Section II presents a simple model for the DC gain error in TRAs and derives the constraints on the stray parameters for a specified target error. Section III discusses the constraints on TRAs offset, drift and noise for specified target error and resolution. Sections IV and V present the design and implementation of the QuTRA prototypes, with the solutions adopted to meet the required constraints. Section VI presents the characterization of the QuTRA prototypes and the first tests performed with four-terminal resistance standards to verify the gain accuracy. Some perspectives on potential applications of the QuTRA to the primary metrology of small electrical currents are offered in section VII.

In this work, according to a long-established convention in electronics [25], [26], [27], instantaneous values of currents and voltages are denoted by lowercase letters with uppercase subscripts (e.g. v_{O}); constant or average values by uppercase letters with uppercase subscripts (e.g. V_{O}); variations with respect to constant values by lowercase letters with lowercase subscripts (e.g. $v_{\mathrm{o}} = v_{\mathrm{O}} - V_{\mathrm{O}}$). Furthermore, AC phasors, Fourier or Laplace transforms of variations are denoted by uppercase letters with lowercase subscripts (e.g. V_{o} for a transform of v_{o}). Main circuit parameters like resistance, capacitance and inductance are denoted by uppercase letters with lowercase subscripts (e.g. R_{f}), whereas stray parameters are denoted by lowercase letters with lowercase subscripts (e.g. r_{o}).

In the following, some details of the implementation are omitted for simplicity, but the full schematic, bill of materials and the printed circuit board (PCB) layout are available at [28] as open source hardware project.

II. Transresistance Amplifier DC Gain Errors

A TRA is a circuit which multiplies an input current i_{S} by a transresistance R_{m} producing an output voltage $v_{\mathrm{O}} = R_{\mathrm{m}} i_{\mathrm{S}}$. Fig. 1 shows the schematic of a basic operational amplifier (op amp) TRA [2, Sec. 2.1], with source, load and main stray elements. The circuit is composed of an op amp, a feedback resistance R_{f}, a feedback capacitor C_{f}, a current source

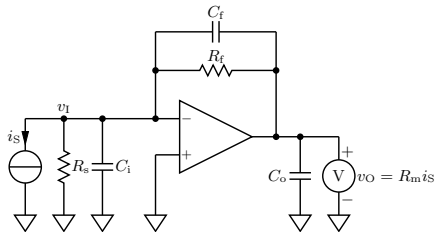

Fig. 1. Schematic of a basic op amp TRA: i_{S} is the source current, R_{S} is the source resistance, R_{f} is the feedback resistance, C_{f} is the feedback capacitor, C_{i} is the input stray capacitance, C_{o} is the output stray capacitance, v_{O} is the output voltage, and v_{I} is the input burden voltage.

with output current i_{S} and source resistance R_{S}, an input capacitance C_{i} and an output capacitance C_{o}. The capacitor C_{f} provides the frequency compensation needed to ensure stability and avoid self-oscillatory behavior [2, Chap. 8], [1, Chap. 4x.3], [29, Chap. 3]; C_{i} and C_{o} represent stray capacitances from op amp, printed circuit board, cables, connectors, etc. The output voltage v_{O} is measured by a voltmeter; v_{I} is the input burden voltage. The reference direction of i_{S} is chosen such that $R_{\mathrm{m}} > 0$.

In DC, if the devices are ideal, $R_{\mathrm{m}} = R_{\mathrm{f}}$ exactly and $v_{\mathrm{I}} = 0$. For a real circuit, $R_{\mathrm{m}} \neq R_{\mathrm{f}}$ and $v_{\mathrm{I}} \neq 0$. The DC gain error ϵ_{G} can be defined as

$$\epsilon_{\mathrm{G}} = \frac{R_{\mathrm{m}}}{R_{\mathrm{f}}} - 1. \tag{1}$$

An expression for ϵ_{G} can be derived from the equivalent schematic in Fig. 2. The op amp has been represented by an equivalent model with finite open-loop gain a, differential resistance r_{d} and output resistance r_{o}, and C_{f} has been replaced by its leakage resistance r_{l}. The leakage resistance of C_{o} does not significantly affect the gain, and that of C_{i} can be included in R_{s}. For the R_{f} values of interest in this work, $r_{\mathrm{o}} \ll R_{\mathrm{f}} \ll r_{\mathrm{d}}$, $R_{\mathrm{f}} \ll r_{\mathrm{l}}$ and $R_{\mathrm{f}} \ll aR_{\mathrm{s}}$, such that, at first order in the stray parameters, R_{m} can be expressed as

$$R_{\mathrm{m}} \approx R_{\mathrm{f}}\left[1 - \frac{1}{a} - \frac{R_{\mathrm{f}}}{r_{\mathrm{l}}} - \frac{R_{\mathrm{f}}}{aR_{\mathrm{s}}}\right]. \tag{2}$$

The gain error can then be expressed as

$$\epsilon_{\mathrm{G}} = -\frac{1}{a} - \frac{R_{\mathrm{f}}}{r_{\mathrm{l}}} - \frac{R_{\mathrm{f}}}{aR_{\mathrm{s}}} = -\frac{1}{a} - \frac{R_{\mathrm{f}}}{r_{\mathrm{l}}} - \frac{r_{\mathrm{i}}}{R_{\mathrm{s}}}, \tag{3}$$

where $-1/a$ is the error component due to the finite open-loop gain, $-R_{\mathrm{f}}/r_{\mathrm{l}}$ is the error component due to the feedback capacitor leakage and $-R_{\mathrm{f}}/(aR_{\mathrm{s}})$ is the error component due to the input burden voltage caused by the non-zero TRA input resistance $r_{\mathrm{i}} \approx R_{\mathrm{f}}/a$. Given R_{f}, R_{s} and a maximum admissible error $|\epsilon_{\mathrm{G}}|_{\max}$, the TRA can be designed by imposing the constraints $r_{\mathrm{l}} \gtrsim R_{\mathrm{f}}/|\epsilon_{\mathrm{G}}|(\max)$ and $a \gtrsim (1 + R_{\mathrm{f}}/R_{\mathrm{s}})/|\epsilon_{\mathrm{G}}|(\max)$.

III. Offset, Drift and Noise

Fig. 3 shows the DC equivalent model of Fig. 2 with added input bias current I_{B} and offset voltage V_{OS}. The output voltage can be written as

$$v_{\mathrm{O}} = R_{\mathrm{m}}\left(i_{\mathrm{S}} + I_{\mathrm{B}} + \frac{V_{\mathrm{OS}}}{R_{\mathrm{s}} \parallel R_{\mathrm{f}}}\right) = R_{\mathrm{m}}(i_{\mathrm{S}} + I_{\mathrm{OS}}), \tag{4}$$

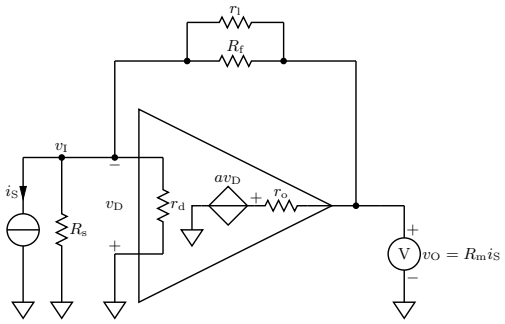

Fig. 2. TRA DC model for gain error evaluation. C_f has been substituted by the leakage resistance r_l and the op amp by an equivalent model with open-loop gain a, differential resistance r_d and output resistance r_o.

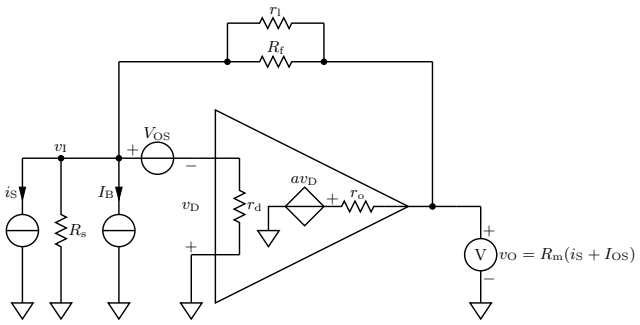

Fig. 3. TRA DC model for offset error evaluation.

with the symbol $\parallel$ denoting parallel connection and with the input-referred equivalent offset current

$$I_\mathrm{OS} = I_\mathrm{B} + \frac{V_\mathrm{OS}}{R_\mathrm{s} \parallel R_\mathrm{f}}. \tag{5}$$

For the R_f and R_S values of interest in this work, the term $V_\mathrm{OS}/(R_\mathrm{s} \parallel R_\mathrm{f})$ predominates over I_B.

If I_OS is constant, its effect can be canceled by periodically reversing the polarity of i_S ("$+-$" measurement scheme) or by periodically zeroing it ("$+0$" measurement scheme). However, if I_OS drifts by ΔI_OS between two subsequent phases in the aforementioned schemes, the reconstructed i_S is affected by a systematic error, equal to $\Delta I_\mathrm{OS}/2$ for a "$+-$" scheme and ΔI_OS for a "$+0$" scheme. Therefore, for the error to be less than $0.1\,\mu\mathrm{A/A}$, the maximum acceptable $|\Delta I_\mathrm{OS}|$ is $2\times10^{-7} i_\mathrm{S}$ for a "$+-$" scheme and $10^{-7} i_\mathrm{S}$ for a "$+0$" scheme. A linear drift on I_OS can be instead canceled by a "$+--+$" measurement scheme. Other measurement schemes can be employed for higher order polynomial drifts [5], [30].

In many measuring systems, noise can be suitably characterized by the Allan deviation as a function of the averaging time, especially when power-law noise processes (e.g. white noise, flicker noise, random walk) are dominant [31], [32], [33]. Flicker noise is frequently the main limiting factor of the type A uncertainty or the resolution of a measuring system. In fact, for a flicker noise process with one-sided spectral density function h_{-1}/f, the Allan deviation is approximately equal to $\sqrt{(2\ln 2)h_{-1}}$ [31], independent of the averaging time (that is, when flicker noise is dominant, increasing the averaging time does not decrease the type A uncertainty). For a TRA, once an uncertainty target is specified, the flicker noise floor sets a constraint on the flicker current noise coefficient $h_{i,-1}$ of the TRA. For the R_f and R_S values of interest in this work, from (5), the flicker current noise is actually mainly determined by the flicker voltage noise, that is, $h_{i,-1} \approx h_{v,-1}/(R_\mathrm{s} \parallel R_\mathrm{f})^2$, where $h_{v,-1}$ is the flicker voltage noise coefficient. For an uncertainty of $0.1\,\mu\mathrm{A/A}$ with $R_\mathrm{f} \approx 1\,\mathrm{M\Omega}$, $R_\mathrm{s} \gg R_\mathrm{f}$ and $i_\mathrm{s} \approx 1\,\mu\mathrm{A}$, the constraint is $h_{v,-1}^{1/2} < 85\,\mathrm{nV}$ (a value in the order of those of typical low-noise op amps). However, differential measurement schemes, like the offset and drift cancellation schemes described in the above, filter the TRA noise in a way that "whitens" flicker noise (see e.g. [34]), allowing measurements with type A uncertainty below the TRA flicker noise floor. For this reason, the specification $h_{v,-1}^{1/2} < 85\,\mathrm{nV}$ is actually not a hard constraint for the TRA design, and front-end op amps with slightly larger noise can be accepted too.

TABLE I
TRA DESIGN PARAMETERS

R_f	$10\,\mathrm{k\Omega}$ or $R_\mathrm{K}/2$	$1\,\mathrm{M\Omega}$ or $50R_\mathrm{K}$
$\lvert\epsilon_\mathrm{G}\rvert(\max)$	$0.1\,\mu\Omega/\Omega$	$0.1\,\mu\Omega/\Omega$
$i_\mathrm{S}(\max)$	$50\,\mu\mathrm{A}$	$1\,\mu\mathrm{A}$
$v_\mathrm{O}(\max)$	$2.1\,\mathrm{V}$	$11\,\mathrm{V}$
$a(\min)$	10^7	10^7
$r_\mathrm{l}(\min)$	$0.1\,\mathrm{T\Omega}$	$10\,\mathrm{T\Omega}$
$C_\mathrm{i}(\max)$	$3\,\mathrm{nF}$	$3\,\mathrm{nF}$
$C_\mathrm{o}(\max)$	$3\,\mathrm{nF}$	$3\,\mathrm{nF}$

IV. THE DESIGN

Table I summarizes the key design parameters for the TRA. The minimum specifications on a and r_l fulfill the constraints derived in Section II for the transresistances and accuracy level stated in Section I, assuming $R_\mathrm{S} \gtrsim R_\mathrm{f}$. In addition, the TRA should have low input bias current, low and stable offset, and low noise (Section III). The listed requirements cannot be met by a single op amp, but with a composite amplifier design [2, Chap. 8].

This work employs a four-stage composite amplifier, whose schematic is shown in Fig. 4, without the external transresistance. The compensation network corresponds to C_f in Fig. 1. Three connectors, labeled as IN, GND and OUT, correspond to the $-$, $+$ and output nodes of the TRA.

The total gain $a = -a_1 a_2 a_3 a_4 > 10^7$ is distributed among the four stages with individual gains $a_1, \ldots, a_4$ (the minus sign in the product derives from $a = v_\mathrm{O}/v_\mathrm{D} = -v_\mathrm{O}/v_\mathrm{I}$). The first stage employs an ultra-low input bias current Texas Instruments LMP7721 [35] precision op amp configured as a non-inverting amplifier with gain $a_1 \approx +31$ and powered by a $\pm 2.5\,\mathrm{V}$ supply. This stage fulfills the input current, offset and noise requirements discussed in Section III and divides the noise from subsequent stages. The second stage is an inverting amplifier with gain $a_2 \approx -5$. The $\pm 15\,\mathrm{V}$ power supply increases the dynamic range with respect to the first stage. The third stage is an inverting integrator with gain $a_3 < -2 \times 10^5$ which shapes the frequency response. The final stage has gain $a_4 \approx -1$ and provides capacitive load isolation [2, Sec. 8.4] and output voltage limitation.

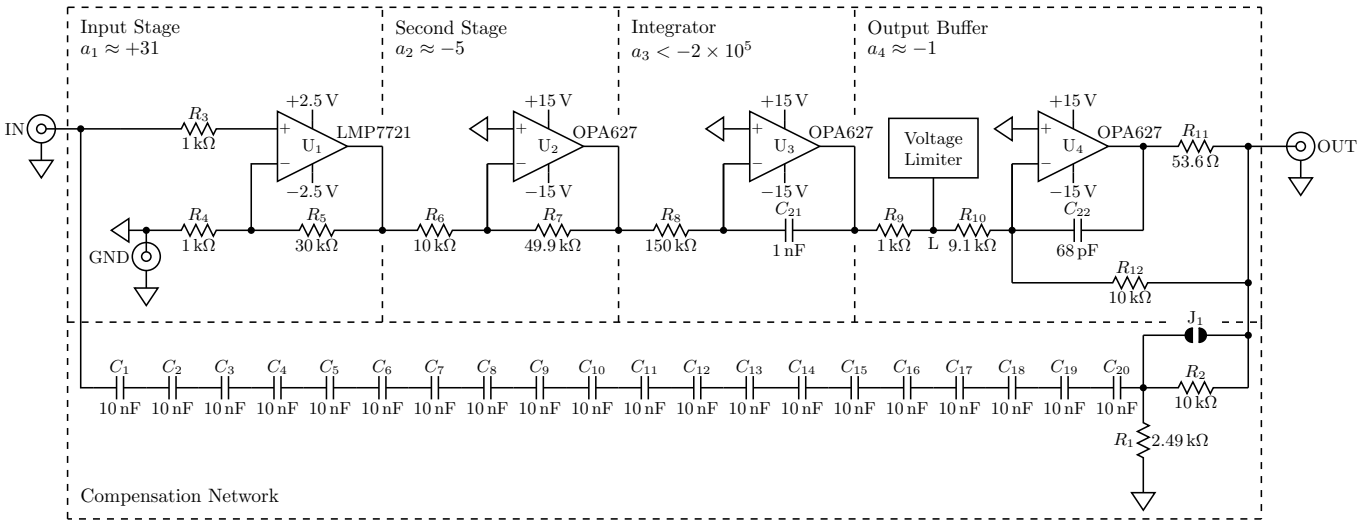

Fig. 4. Schematic of the TRA design. In dashed boxes the four stages of the composite amplifier with the respective gains and the compensation network. Power supplies are not shown for simplicity.

The $\pm 15\,\mathrm{V}$ power supplies are provided by a pair of onboard LM317/337 voltage regulators and the $\pm 2.5\,\mathrm{V}$ power supplies are provided by a pair of onboard LT3045/3094 low-noise voltage regulators, not shown in Fig. 4 for simplicity.

The schematic of Fig. 4 was analyzed with a Spice simulator to determine the loop gain. The stability at the maximum values of C_o and C_i was ensured by adjusting R_{11}, C_{22}, C_f and the integrator time constant $R_8 C_{21}$.

The required C_f and minimum r_l vary with the feedback resistor (Table I): $R_\mathrm{f} = 10\,\mathrm{k\Omega}$ requires $C_\mathrm{f} = 500\,\mathrm{pF}$ and $r_\mathrm{l} \gtrsim 100\,\mathrm{G\Omega}$; $R_\mathrm{f} = 1\,\mathrm{M\Omega}$ requires $C_\mathrm{f} = 100\,\mathrm{pF}$ and $r_\mathrm{l} \gtrsim 10\,\mathrm{T\Omega}$. To accommodate both transresistances in a single amplifier design, the compensation capacitor C_f has been replaced by the compensation T network of Fig. 5(a), where a capacitor C is connected to the center tap of the voltage divider composed of R_1 and R_2. The jumper $\mathrm{J_1}$ allows one to possibly short R_2. The network of Fig. 5(a) is equivalent to the one of Fig. 5(b), which shows that the compensation impedance equals $R_2 + (br) \parallel (b/(sC))$, where $b = (R_1 + R_2)/R_1$ and s represents the complex angular frequency in the Laplace s-domain. The network effectively multiplies the leakage resistance r of the capacitor C by the factor b and divides its capacitance by the same factor, such that

$$C_\mathrm{f} = C/b \qquad \text{and} \qquad r_\mathrm{l} = br. \tag{6}$$

Instead, if $\mathrm{J_1}$ shorts R_2, $C_\mathrm{f} = C$ and $r_\mathrm{l} = r$. Therefore, imposing $b \approx 500\,\mathrm{pF}/100\,\mathrm{pF} \approx 5$ allows to compensate for both transresistances by opening or shorting $\mathrm{J_1}$. The choice of R_1 and R_2 is a compromise between two competing factors. On the one hand, R_2 is in series with the equivalent capacitor $(br) \parallel (b/(sC))$ and should not be too high to avoid excessively altering the compensation behavior; on the other, R_1 loads the TRA output when $\mathrm{J_1}$ is shorted and should not be too low. Therefore, both were chosen at the $\mathrm{k\Omega}$ level.

A minimum r of $2\,\mathrm{T\Omega}$ is required to ensure $r_\mathrm{l} \gtrsim 10\,\mathrm{T\Omega}$ when $R_\mathrm{f} = 1\,\mathrm{M\Omega}$ [cf. (6) with $b \approx 5$]. Since common capacitors do not have such a high leakage resistance[1], this design uses twenty $10\,\mathrm{nF}$ C0G series-connected capacitors ($C_1, \ldots, C_{20}$ in Fig. 4), with individual leakage resistance greater than $100\,\mathrm{G\Omega}$, ensuring $C = 500\,\mathrm{pF}$ with $r > 2\,\mathrm{T\Omega}$.

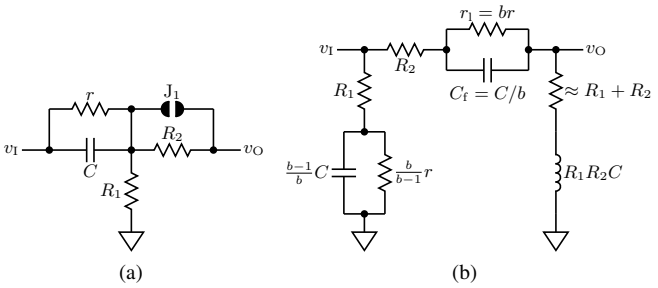

Fig. 5. (a) Principle schematic of the compensation T network: the capacitance C has leakage resistance r; R_1 and R_2 compose a voltage divider; and the jumper $\mathrm{J_1}$ allows to short R_2. (b) Equivalent schematic of the network (a) with equivalent impedances between the input and output nodes and the ground. The compensation impedance between the input and the output of TRA is $R_2 + (br) \parallel (b/(sC))$ with $b = (R_1 + R_2)/R_1$ (when $\mathrm{J_1}$ is shorted, $R_2 = 0$ and $b = 1$).

With the designed compensation network, the simulated bandwidth is around $2\,\mathrm{kHz}$ at the highest transresistance.

To protect possible QHRS or QHARS employed as feedback resistors, the maximum output voltage can be limited by the clipping circuit of Fig. 6, connected at node L in Fig. 4. Either of two voltage limiters, depending on the transresistance, can be selected with a jumper at node L. The clipping voltages are $\pm 10\,\mathrm{V}$ ($\mathrm{U_5}$ and $\mathrm{U_6}$) or $\pm 1.9\,\mathrm{V}$ ($\mathrm{U_7}$ and $\mathrm{U_8}$). Given that the gain from node L to the output is about 1.1 (Fig. 4), the output voltage of the TRA is limited to about $\pm 11\,\mathrm{V}$ or $\pm 2.1\,\mathrm{V}$, respectively.

[1]An alternative option is to use porcelain capacitors, which have leakage resistances in the order of $1\,\mathrm{T\Omega}$, but these are much more expensive with respect to C0G capacitors and less readily available on the market. Porcelain capacitors can be considered to minimize the stray inductance with respect to the long series of capacitors, which can be useful if one wishes to widen the TRA bandwidth, or for higher transresistance.

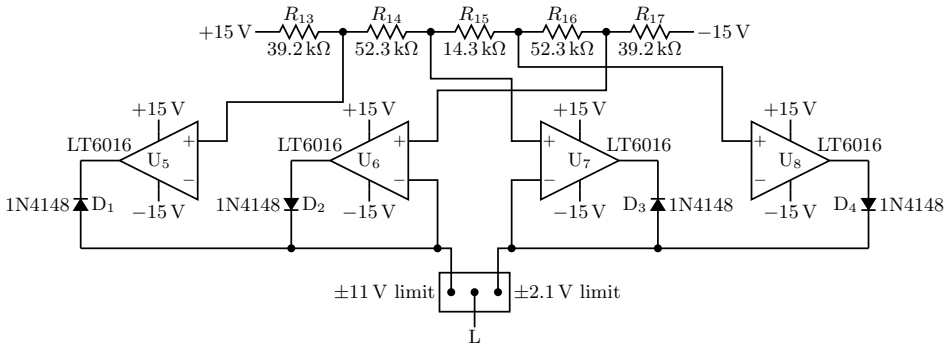

Fig. 6. Schematic of the voltage limiter circuit. Node L can be connected to either U_5 and U_6, limiting the TRA output voltage to ±11 V, or to U_7 and U_8, limiting the TRA output voltage to ±2.1 V.

Fig. 7. Assembled QuTRA 1.1 PCB inside its box with the lid open. The amplifier interfaces via three SMA connectors (IN, OUT, GND) and a 4-pin LEMO connector for external battery supply.

From the specifications of the LMP7721 [35] and from Spice noise simulations, the estimated Allan deviation for the flicker current noise floor is on the order of 120 fA.

V. Implementation and Characterization

Fig. 7 shows a picture of the assembled TRA.

The PCB has four copper layers; from top to bottom: signal layer, ground plane, ±2.5 V power plane and ±15 V power plane. The ground plane also guards the signal plane from the power planes. To increase the surface resistance and the one towards ground, the insulating layer between signal and ground planes is a high resistivity material (Rogers RO4350). The IN, OUT and GND ports of Fig. 4 correspond to the three SMA connectors of Fig. 7. The input is guarded with a grounded ring that encircles the IN center conductor, the inverting and non-inverting inputs of U_1 and C_1–C_9, as shown in Fig. 8.

The TRA is battery powered to reduce power line interferences. The battery pack is composed of four series-connected 12 V 7 A h lead acid batteries generating a ±(24–27) V dual supply voltage which ensures more than one week of operation.

A. Leakage resistance

The measurement of the leakage resistance r of the series of capacitors $C_1, \ldots, C_{20}$ was performed before soldering any other component to the PCB, according to the three-terminal definition of resistance, which is insensitive to the effect of stray resistances [36, Sec. 2.1.2], [4, Sec. 2.3.1]. The setup is represented in Fig. 8: the right pin of J_1 is driven by the high voltage V_H, the ground is connected to the outer conductor of the IN SMA connector, which is also connected to the ground plane and the guard ring, and a femtoammeter is connected to the center conductor of the IN SMA to measure the current I_L. The leakage resistance is defined as

$$r = \left.\frac{V_\mathrm{H}}{I_\mathrm{L}}\right|_{V_\mathrm{L}=0}. \tag{7}$$

A Keysight B2985B high-resistance meter is used as source-measure unit: it applies V_H, measures I_L, and keeps $V_\mathrm{L} \approx 0$. The leakage resistance measurement setup is enclosed in a purpose-built shielded box with a high voltage binding post, a triaxial connector for the femtoammeter and a safety interlock. Both QuTRA 1.1 and 1.2 were characterized and r was determined by linear least squares regression from the measured I_L values obtained at V_H of 0 V, 50 V, 100 V, 150 V and 200 V. The measured values are spread from about 10 TΩ to 30 TΩ, yielding $r_\mathrm{l} = br$ from about 50 TΩ to 150 TΩ when J_1 is open.

B. Input impedance

The input impedance Z_i of the TRA was characterized by injecting a sinusoidal current i_S at frequency f into the TRA input, and by measuring the TRA input voltage v_I with a lock-in amplifier LIA (Zurich Instruments MFLI). The current i_S is generated by the LIA output voltage v_S through an external source resistance R_s, such that $i_\mathrm{S} = v_\mathrm{S}/R_\mathrm{s}$. The input impedance is determined as $Z_\mathrm{i} = R_\mathrm{s}V_\mathrm{i}/V_\mathrm{s}$, V_i and V_s being the complex phasors associated to v_I and v_S, respectively. Fig. 9 reports measurements and Spice simulations of the input impedance modulus $|Z_\mathrm{i}(f)|$ for $R_\mathrm{f} = 10\,\mathrm{k\Omega}$ and $R_\mathrm{f} = 1\,\mathrm{M\Omega}$. In each measurement, $R_\mathrm{s} = R_\mathrm{f}$, and $V_\mathrm{S} \approx 7\,\mathrm{V}$. The required LIA time constant and the resulting settling time increase significantly at low frequency. Therefore, for practical reasons, the chosen minimum measurement frequency is 0.01 Hz. From

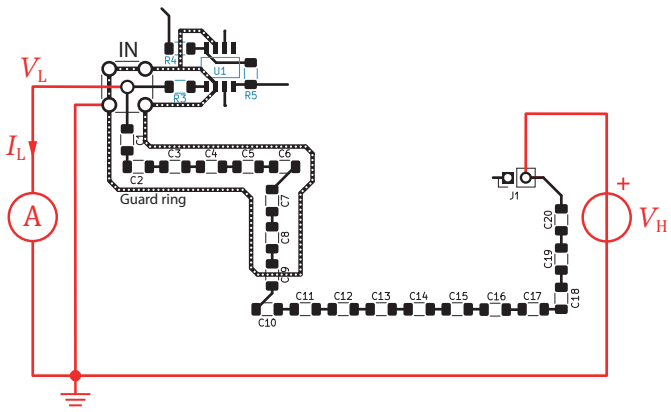

Fig. 8. PCB signal-layer detail of interest for the measurement of r. Interconnections and soldered components are represented in black; unsoldered components, in blue. The red schematic shows the source-measure unit connection: V_H is applied to the right pin of J_1, I_L is measured from the inner conductor of the IN SMA and the outer conductor is connected to ground. The picture also shows the guard ring encircling the IN center conductor, the inverting and non-inverting inputs of U_1 and C_1–C_9.

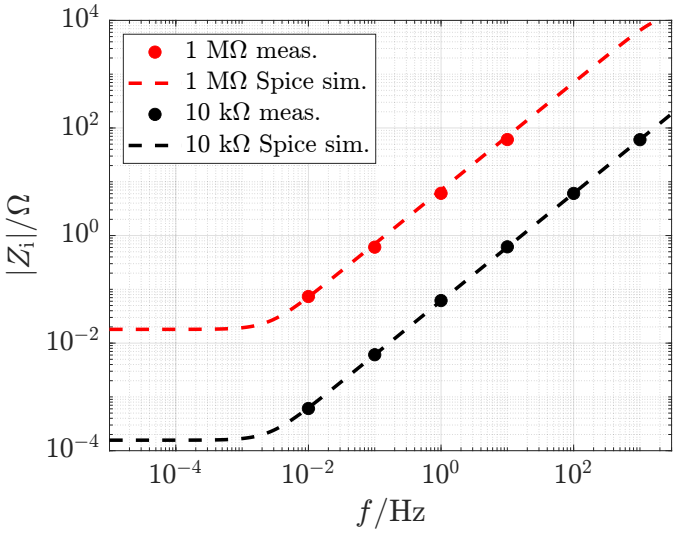

Fig. 9. Measurements of the input impedance modulus $|Z_i|$ as a function of the frequency f for $R_f = 10\,\mathrm{k\Omega}$ (black markers) and $R_f = 1\,\mathrm{M\Omega}$ (red markers), together with the corresponding Spice simulations (dashed lines).

the measured values, it can be inferred that the DC input resistance R_i is less than $1\,\mathrm{m\Omega}$ at $R_f = 10\,\mathrm{k\Omega}$ and $0.1\,\Omega$ at $R_f = 1\,\mathrm{M\Omega}$.

C. Offset voltage

The amplifier's output offset voltage $R_m I_{OS}$ (from (4)) was measured at different temperatures, obtaining values in the $15\,\mu\mathrm{V}$–$20\,\mu\mathrm{V}$ range at about $23\,^\circ\mathrm{C}$, with a temperature coefficient of about $5.5\,\mu\mathrm{V}/^\circ\mathrm{C}$. The considerations in Section III lead to a maximum admissible temperature variation between two subsequent measurement phases of $0.02\,^\circ\mathrm{C}$ for a "+−" scheme and of $0.01\,^\circ\mathrm{C}$ for a "+0" scheme, obtained for the case $R_f = 10\,\mathrm{k\Omega}$, which is more demanding. For a "+−−+" measurement scheme, which rejects the linear offset drift, the temperature stability requirement is more relaxed.

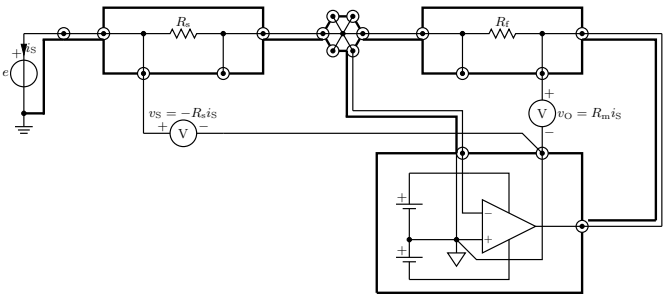

Fig. 10. Voltage ratio measurement configuration: the transresistance $R_m \approx R_f$ of the TRA multiplies the input current i_S, generated by a voltage $e = \pm 1\,\mathrm{V}$ applied through a resistance R_s. The feedback resistance R_f and R_s are two $10\,\mathrm{k\Omega}$ four-terminal resistance standards. The DMM measures the ratio between the output voltage v_O and the voltage v_S across R_s.

VI. Results

The TRA prototypes were tested in order to determine the gain error ϵ_G from (1), $R_m = (1+\epsilon_G)R_f$. This is achieved by comparing a resistance ratio measurement to a voltage ratio measurement.

The setup schematic for the voltage ratio measurement is shown in Fig. 10. The input current i_S is generated by a voltage e applied through a resistance R_s, such that the circuit of Fig. 10 is equivalent to that of Fig. 1 with $i_S = v_S/R_s$. Both R_s and R_f are $10\,\mathrm{k\Omega}$ shielded four-terminal resistance standards. These are based on Vishay Precision Group Z Series foil resistors with a temperature coefficient less than $8 \times 10^{-7}/^\circ\mathrm{C}$ contained in the same shielding box. For the measurements after 16 Jan 2026, the box has been placed on top of a Meerstetter Engineering SKT-1165 temperature control, ensuring a temperature stability of the resistors in the millikelvin range. A measurement of the resistance ratio with the temperature control yielded a relative stability of few parts in the 10^9 over a few hours of averaging time, which is sufficient for this experiment. The voltage e is generated by a Keysight B2961B low-noise power source. The voltages v_O and v_S are alternately measured by the two channels (front/rear terminals) of a Fluke 8588A reference multimeter (DMM). A star junction is used to interconnect the low current terminals of R_s and R_f and the amplifier input.

To reject the TRA offset and drift error, the polarity of e is periodically reversed following a "+−−+" measurement scheme between the values $e = E^+ = 1\,\mathrm{V}$ and $e = E^- = -1\,\mathrm{V}$. The corresponding output measured by the DMM are $V^{\pm}_{O,k}$ and $V^{\pm}_{S,k}$, where the superscripts $+$ or $-$ denote the source polarity and $k = 1, \ldots, 4$ the measurement phase. These voltages determine the voltage ratio

$$Q_V = -\frac{\frac{V^+_{O,1}}{V^+_{S,1}} + \frac{V^-_{O,2}}{V^-_{S,2}} + \frac{V^-_{O,3}}{V^-_{S,3}} + \frac{V^+_{O,4}}{V^+_{S,4}}}{4}. \tag{8}$$

For the resistance ratio measurement, the TRA is disconnected from the circuit and the resistance standards are connected to the DMM according to the schematic of Fig. 11. In this case, the resistance ratio $Q_R = R_f/R_s$ is directly measured by the DMM in the "True ohm" mode as the ratio between the voltage V_{R_f} across R_f and the voltage V_{R_s} across

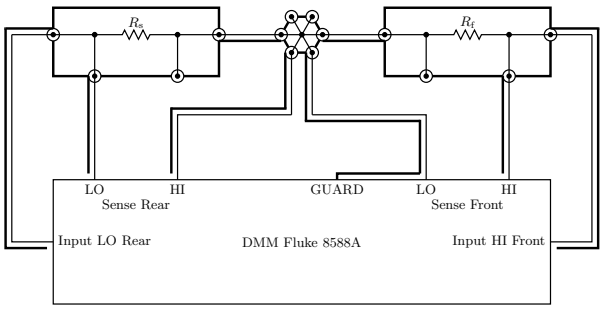

Fig. 11. Resistance ratio measurement schematic; the DMM measures the ratio between two 10 kΩ four-terminal resistance standards R_f and R_s in "True ohm" mode. The DMM injects a 100 µA current between the terminals Input LO Rear and Input HI Front, which is reversed periodically. $R_\mathrm{f}/R_\mathrm{s}$ is measured as the ratio between the voltage V_{R_f} across R_f and the voltage V_{R_s} across R_s.

R_s, when a 100 µA current is driven through both resistors. The DMM is connected to the resistance standards at the star junction to measure both R_s and R_f as in the voltage ratio setup.

From (2) and (4), it can be proved that Q_R and Q_V are related by

$$\frac{R_\mathrm{m}}{R_\mathrm{s}} = (1+\epsilon_\mathrm{G})Q_R = -\frac{Q_V}{1+\epsilon_V}, \tag{9}$$

with $\epsilon_V = -(1/2)\big(1/V_\mathrm{S}^+ + 1/V_\mathrm{S}^-\big)R_\mathrm{s}I_\mathrm{OS}$, with V_S^+ average positive V_S and V_S^- average negative V_S.

To cancel the DMM gain error, the measurements of Q_V and Q_R are repeated after interchanging the front and rear terminals, obtaining two measurements labeled as forward (f) and reverse (r) (see also [37] and [38] for similar applications of this technique). The DMM reading of a generic voltage V is affected by a gain error g that depends on the channel: the voltage measured from the front terminals is here labeled V^A and the error is $g^\mathrm{A}(V^\mathrm{A})$; the voltage measured from the rear terminals is here labeled V^B and the error is $g^\mathrm{B}(V^\mathrm{B})$. Therefore, the same voltage V can be expressed as either $V = (1+g^\mathrm{A}(V^\mathrm{A}))V^\mathrm{A}$ or $V = (1+g^\mathrm{B}(V^\mathrm{B}))V^\mathrm{B}$. In the forward configuration,

$$Q_V^\mathrm{f} = \frac{[1+g^\mathrm{A}(V_\mathrm{O}^\mathrm{A})]V_\mathrm{O}^\mathrm{A}}{[1+g^\mathrm{B}(V_\mathrm{S}^\mathrm{B})]V_\mathrm{S}^\mathrm{B}} = \frac{1+g^\mathrm{A}(V_\mathrm{O}^\mathrm{A})}{1+g^\mathrm{B}(V_\mathrm{S}^\mathrm{B})}Q_V^{\mathrm{f,read}}, \tag{10}$$

where $Q_V^{\mathrm{f,read}} = V_\mathrm{O}^\mathrm{A}/V_\mathrm{S}^\mathrm{B}$ is the forward voltage ratio reading. In the reverse configuration,

$$Q_V^\mathrm{r} = \frac{[1+g^\mathrm{B}(V_\mathrm{O}^\mathrm{B})]V_\mathrm{O}^\mathrm{B}}{[1+g^\mathrm{A}(V_\mathrm{S}^\mathrm{A})]V_\mathrm{S}^\mathrm{A}} = \frac{1+g^\mathrm{B}(V_\mathrm{O}^\mathrm{B})}{1+g^\mathrm{A}(V_\mathrm{S}^\mathrm{A})}Q_V^{\mathrm{r,read}}, \tag{11}$$

where $Q_V^{\mathrm{r,read}} = V_\mathrm{O}^\mathrm{B}/V_\mathrm{S}^\mathrm{A}$ is the reverse voltage ratio reading.

Since R_f and R_s are in $1:1$ ratio, V_O and V_S differ only of tens of microvolts. Therefore, we can assume that the DMM gain error remains approximately the same between the two voltages measured with the same channel, such that $g^\mathrm{A}(V_\mathrm{O}^\mathrm{A}) \approx g^\mathrm{A}(V_\mathrm{S}^\mathrm{A})$ and $g^\mathrm{B}(V_\mathrm{O}^\mathrm{B}) \approx g^\mathrm{B}(V_\mathrm{S}^\mathrm{B})$. From (9), (10) and (11), and taking into account the above approximations, it holds that

$$\begin{aligned}(1+\epsilon_\mathrm{G})^2Q_R^2 &= \frac{1+g^\mathrm{A}(V_\mathrm{O}^\mathrm{A})}{1+g^\mathrm{B}(V_\mathrm{S}^\mathrm{B})}\frac{Q_V^{\mathrm{f,read}}}{1+\epsilon_V^\mathrm{f}}\frac{1+g^\mathrm{B}(V_\mathrm{O}^\mathrm{B})}{1+g^\mathrm{A}(V_\mathrm{S}^\mathrm{A})}\frac{Q_V^{\mathrm{r,read}}}{1+\epsilon_V^\mathrm{r}}, &(12)\\ &\approx \frac{Q_V^{\mathrm{f,read}}}{1+\epsilon_V^\mathrm{f}}\frac{Q_V^{\mathrm{r,read}}}{1+\epsilon_V^\mathrm{r}}, &(13)\end{aligned}$$

where a superscript has been added to ϵ_V to denote either the forward or reverse measurement.

A similar reasoning can be applied also to the measurement of Q_R, such that $g^\mathrm{A}(V_{R_\mathrm{f}}^\mathrm{A}) \approx g^\mathrm{A}(V_{R_\mathrm{s}}^\mathrm{A})$ and $g^\mathrm{B}(V_{R_\mathrm{f}}^\mathrm{B}) \approx g^\mathrm{B}(V_{R_\mathrm{s}}^\mathrm{B})$, and

$$\begin{aligned}Q_R &= \sqrt{Q_R^{\mathrm{f,read}}Q_R^{\mathrm{r,read}}\frac{[1+g^\mathrm{A}(V_{R_\mathrm{f}}^\mathrm{A})][1+g^\mathrm{B}(V_{R_\mathrm{f}}^\mathrm{B})]}{[1+g^\mathrm{B}(V_{R_\mathrm{s}}^\mathrm{B})][1+g^\mathrm{A}(V_{R_\mathrm{s}}^\mathrm{A})]}} &(14)\\ &\approx \sqrt{Q_R^{\mathrm{f,read}}Q_R^{\mathrm{r,read}}}, &(15)\end{aligned}$$

where $Q_R^{\mathrm{f,read}} = V_{R_\mathrm{f}}^\mathrm{A}/V_{R_\mathrm{s}}^\mathrm{B}$ is the forward resistance ratio reading and $Q_R^{\mathrm{r,read}} = V_{R_\mathrm{f}}^\mathrm{B}/V_{R_\mathrm{s}}^\mathrm{A}$ is the reverse resistance ratio reading.

The error ϵ_G can be found from the DMM measurements as

$$\epsilon_\mathrm{G} \approx \frac{\sqrt{\frac{Q_V^{\mathrm{f,read}}}{1+\epsilon_V^\mathrm{f}}\frac{Q_V^{\mathrm{r,read}}}{1+\epsilon_V^\mathrm{r}}}}{\sqrt{Q_R^{\mathrm{f,read}}Q_R^{\mathrm{r,read}}}} - 1. \tag{16}$$

In this work, $Q_V^{\mathrm{f,read}}$ and $Q_V^{\mathrm{r,read}}$ are obtained by combining five $V_{\mathrm{O,k}}^\pm$ DMM readings and five $V_{\mathrm{S,k}}^\pm$ DMM readings with 10 s DMM aperture time and a 4 s delay at each channel switching. A delay of 10 s is added after the source polarity reversal. The averaging time (sum of the aperture times) of a "+−−+" cycle for a single $Q_V^{\mathrm{f,read}}$ or $Q_V^{\mathrm{r,read}}$ measurement is 200 s, and the measurement time for the same cycle is about 10 min. Ten $Q_V^{\mathrm{f,read}}$ and ten $Q_V^{\mathrm{r,read}}$ measurements are taken. The term ϵ_V is estimated from the average positive V_S and the average negative V_S.

Fig. 12 reports the estimated Allan deviations $\sigma_{Q_V}(\tau)$ of $Q_V^{\mathrm{f,read}}$ and $Q_V^{\mathrm{r,read}}$ for an example measurement, as a function of the averaging time τ (integer multiple of 200 s). The Allan deviation and its uncertainty were determined from the estimated values of the *Haar wavelet variance*, taking into account the connection between the wavelet and Allan variances described in [39], [32]. The behavior of $\sigma_{Q_V}(\tau)$ is compatible with white measurement noise, by virtue of the whitening effect of the "+−−+" measurement scheme, as discussed in Section III.

The $Q_R^{\mathrm{f,read}}$ and $Q_R^{\mathrm{r,read}}$ measurements reported in this work are obtained by the DMM "True ohm" function, which already reverses the current periodically. Each point is already the average of two ratios of voltage readings obtained with 10 s DMM aperture time and 4 s delay after the channel switching, for a total averaging time of 40 s and a measurement time of 56 s. Twenty $Q_R^{\mathrm{f,read}}$ and twenty $Q_R^{\mathrm{r,read}}$ measurements are taken.

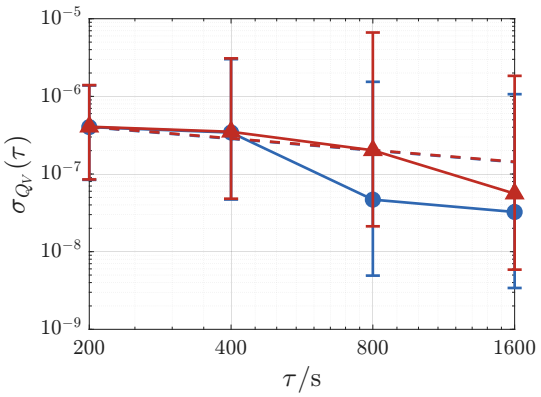

Fig. 12. Allan deviation for an example measurement of the voltage ratio measurements Q_V: the blue filled circles represent the measurements relative to the forward configuration; the red filled triangles represent the measurements relative to the reverse configuration. The dashed lines represent the theoretical Allan deviation of a white noise.

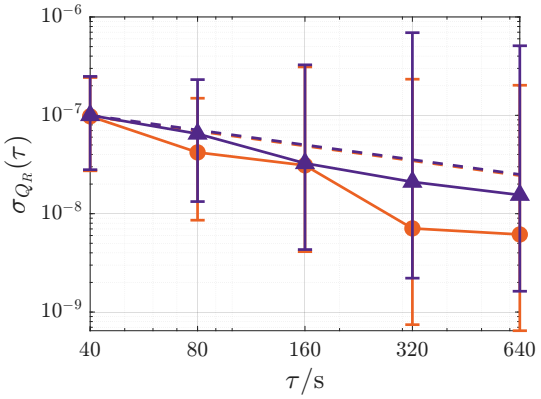

Fig. 13. Allan deviation for an example measurement of the resistance ratio measurements Q_R: the orange filled circles represent the measurements relative to the forward configuration; the purple filled triangles represent the measurements relative to the reverse configuration. The dashed lines represent the theoretical Allan deviation of a white noise.

Fig. 13 reports the Allan deviations of $Q_R^{\mathrm{f,read}}$ and $Q_R^{\mathrm{r,read}}$ for an example measurement, as a function of the averaging time. Also in the case, the Allan deviations are compatible with white measurement noise.

Fig. 14 shows a number of measurements of ϵ_{G} obtained along a period of about one month. The uncertainty bars are reported with a coverage factor of 2. The red filled circles represent data obtained when the resistors were not yet temperature controlled; purple triangles represent data obtained with temperature-controlled resistors. It can be observed that the spread of the measurements is reduced when the resistors are temperature-controlled, due to the improved stability of the resistance ratio.

It was found that the output voltage of the Keysight B2961B power source generating e drifted at each voltage measurement asymmetrically between positive and negative voltages with a ratio of about $1:4$. The drift was likely partly due to the temperature variations in the laboratory, which is not temperature-controlled, with laboratory temperature variations as high as $3\,^{\circ}\mathrm{C}$, but the asymmetry in the drift rate was unexpected. This asymmetrical drift cannot be compensated by the "$+--+$"

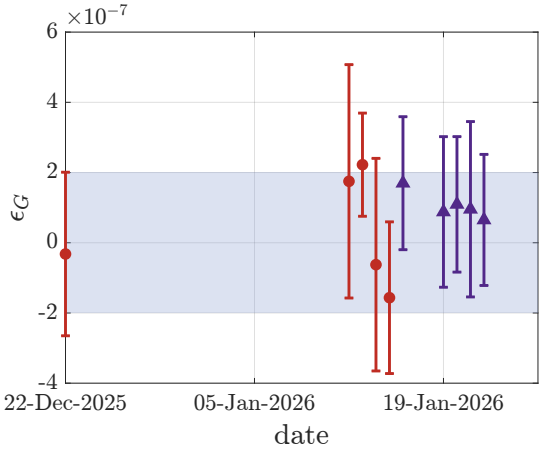

Fig. 14. Gain error ϵ_{G} measurement over time: the red filled circles are measurements taken without temperature control on the four-terminal resistors; the purple triangles are measurements taken with temperature-controlled resistors. The blue shaded region is the target accuracy of the amplifier.

measurement scheme and yields an additional measurement bias. The magnitude of the source drift can be up to $0.5\,\mu\mathrm{V}$ per measurement with positive voltage and $2\,\mu\mathrm{V}$ per measurement with negative voltage. As a consequence, measurements with excessive drift were discarded; the drift was considered excessive when, in the measurements of v_{S}, a steep trend could be clearly identified in either polarity, with a typical slope on the order of $5\,\mu\mathrm{V/min}$. For the measurements considered in this work, on the basis of a rough estimate of the drift observed, the bias on ϵ_{G} can be considered uniformly distributed in the range $\pm 0.17\,\mu\Omega/\Omega$. This was taken into account in the uncertainty budget and in Fig. 14 as an additional component $\Delta\epsilon_{\mathrm{G}}(\mathrm{bias})$ with uncertainty $(0.17\,\mu\Omega/\Omega)/\sqrt{3} \approx 0.1\,\mu\Omega/\Omega$.

Table II reports the uncertainty budget for the measurement ϵ_{G} taken on January 22, 2026, for which $\epsilon_{\mathrm{G}} = (0.065 \pm 0.140)\,\mu\Omega/\Omega$. The type A uncertainty contributions are evaluated taking into account white measurement noise. The reported type B offset contribution is negligible due to the measurement procedure and the small difference between the two polarities of V_{S}. The main uncertainty components are the type A uncertainty of $Q_V^{\mathrm{f,read}}$ and $Q_V^{\mathrm{r,read}}$, and the uncertainty of the source instability $\Delta\epsilon_{\mathrm{G}}$.

Some test measurements were also performed using two $1\,\mathrm{M\Omega}$ resistance standards (based on Caddock USF series 300 film resistors) as R_{f} and R_{s}. In the $1\,\mathrm{M\Omega}$ range, the DMM cannot operate in the "True ohm" function, and the two resistors cannot be connected as in Fig. 11 for the resistance ratio measurement, keeping the same configuration of the voltage ratio measurement. Furthermore, in this case, the DMM injects current in the two resistors alternately and not simultaneously as in the case of the "True ohm" function, and this results in temperature changes in the resistors. As a result, the ϵ_{G} measurements with the $1\,\mathrm{M\Omega}$ resistance standards were compatible with a value of zero, but with an uncertainty in the order of $1\,\mu\Omega/\Omega$. However, for $R_{\mathrm{s}} = R_{\mathrm{f}}$, taking into account (3), the value of ϵ_{G} is affected by R_{f} only through the term $-R_{\mathrm{f}}/r_{\mathrm{l}}$. Since $r_{\mathrm{l}} > 50\,\mathrm{T\Omega}$ for $R_{\mathrm{f}} = 1\,\mathrm{M\Omega}$ (Section V),

TABLE II
UNCERTAINTY BUDGET FOR THE 22 JAN 2026 MEASUREMENT OF FIG. 14

i	Quantity	x_i		$u(x_i)$		Type	c_i	$u_i(x) = \lvert c_i \rvert u(x_i)$	
1	$Q_V^{\mathrm{f,read}}$	$-1.000\,010\,86$	V/V	0.12	µV/V	A	-0.5	62	nΩ/Ω
2	$Q_V^{\mathrm{r,read}}$	$-1.000\,011\,17$	V/V	0.14	µV/V	A	-0.5	68	nΩ/Ω
3	$Q_R^{\mathrm{f,read}}$	$1.000\,011\,062$	Ω/Ω	18	nΩ/Ω	A	-0.5	9	nΩ/Ω
4	$Q_R^{\mathrm{r,read}}$	$1.000\,010\,844$	Ω/Ω	22	nΩ/Ω	A	-0.5	11	nΩ/Ω
5	$(R_{\mathrm{s}} I_{\mathrm{OS}})^{\mathrm{f}}$	18	µV	3	µV	B	$0.15\,\mathrm{MV}^{-1}$	0.46	pΩ/Ω
6	$(R_{\mathrm{s}} I_{\mathrm{OS}})^{\mathrm{r}}$	18	µV	3	µV	B	$-0.3\ \mathrm{MV}^{-1}$	0.90	pΩ/Ω
7	$\Delta\epsilon_{\mathrm{G}}$(bias)	0	nΩ/Ω	100	nΩ/Ω	B	1	100	nΩ/Ω
	ϵ_{G}	65	nΩ/Ω			RSS		140	nΩ/Ω

the effect of R_{f} can be considered negligible on ϵ_{G}, and the measurement with $R_{\mathrm{f}} = 10\,\mathrm{k\Omega}$ can be considered sufficient to estimate ϵ_{G}.

VII. CONCLUSIONS

The TRA presented in this work allows laboratories to perform traceable measurements of currents in the microampere range employing a calibrated external resistance standard, with an uncertainty mainly defined by the resistance calibration uncertainty because the gain error introduced by the amplifier is less than $0.1\,\mu\Omega/\Omega$ (verified with an expanded uncertainty of about $0.3\,\mu\Omega/\Omega$ with coverage factor of 2, limited by the available experimental equipment). The achievable level of uncertainty in a current measurement is therefore competitive with those declared by NMIs (which are typically above $1\,\mu\mathrm{A/A}$) for the same current range in the calibration and measurement capabilities (CMCs), registered in the key comparison database (KCDB) [40].

The TRA has been designed to operate with both room-temperature resistance standards, quantum Hall resistance standards and quantum Hall array resistance standards. Tests have been performed with artifact resistance standards. Tests with quantum devices will be possible in the future in collaboration with some NMIs.

Future developments will also be aimed at modifying the TRA to operate with higher transresistance values, possibly realized by ladder-network quantum Hall array resistance standards as in [41].

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