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# On the Susceptibility to Switching Noise of Operational Amplifiers

Jacopo Serra
*Electronics and Telecommunications Dpt. (DET)*
*Politecnico di Torino*
Torino, Italy
jacopo.serra@polito.it

Franco Fiori
*Electronics and Telecommunications Dpt. (DET)*
*Politecnico di Torino*
Torino, Italy
franco.fiori@polito.it

***Abstract*—This paper investigates the susceptibility of operational amplifiers (OpAmps) to switching noise generated by the commutation of output transistors in power ASICs. Such a switching noise couples to the analog control circuitry through the shared substrate and package parasitic elements. While primarily present at high frequencies, the switching noise is down converted within the analog channel bandwidth by the demodulation carried out by the OpAmp input stage. To better analyze this problem, a reference system comprising of a buck converter and a feedback OpAmp integrated in the same silicon die is considered. The disturbance at the OpAmp input is first evaluated through time-domain simulations and then analyzed in the frequency domain to gain further insight. The resulting noise is then applied to the inputs of three commercial OpAmps with different technologies, architectures, and electrical parameters through a Direct Power Injection (DPI) setup to compare their immunity.**

***Index Terms*—Susceptibility, electromagnetic interference, switching noise, operational amplifiers, power ASIC, ICs**

## I. Introduction

The last decades advances in power ASICs, driven by higher functionality, faster switching, and greater power density, have elevated intra-system compatibility challenges to a new level [1]. However, the trend toward integrating analog, digital, and power devices on the same silicon die has outpaced the development of systematic design methodologies addressing intra-system compatibility, which are still largely based on empirical approaches [2].

A representative case is a power ASIC such as the one shown in Fig. 1, where the switching leg of a buck converter, implemented with high-voltage transistors, is integrated together with the analog circuitry required for its proper operation. Ideally, the power and control sections of the IC should be isolated, however, in practice they are coupled through the shared substrate [3], [4]. As a consequence, the activity of the high-voltage transistors generates switching noise through the parasitic bipolar structures of the substrate, interfering with the operation of the sensitive analog circuitry. This issue becomes even more critical when considering that switching noise not only corrupts the nominal signals at high frequencies but is also demodulated by the input stages of the operational amplifiers that form the analog front-end [5], [6], [7]. As a result, out-of-band RFI is translated into the signal bandwidth, directly affecting the analog channel.

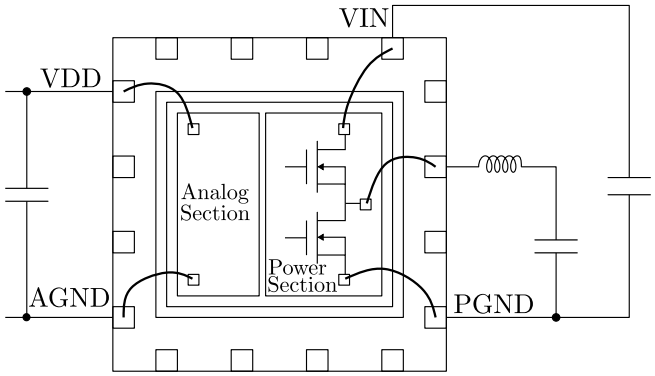


Fig. 1: Block diagram of a power ASIC.

These observations have driven the research on the susceptibility of OpAmps to radio-frequency interference (RFI), resulting in several techniques aimed at improving their immunity [8], [9], [10]. Nevertheless, most of these studies consider only continuous-wave (CW) excitation, thereby assuming that immunity to sinusoidal interference implies immunity to non-sinusoidal disturbances. Consistently, international standards such as IEC 62132 define EMI immunity tests exclusively based on sinusoidal signals [11].

To assess this implicit assumption, this work investigates the susceptibility of operational amplifiers such as those used as analog front-end to switching-noise-based interference. The RF interference is obtained from the time-domain analysis of a realistic power ASIC, such as the one shown in Fig. 1. The resulting interference is then applied to different commercial OpAmps in the Direct Power Injection (DPI) test, in accordance with the IEC-62132-4.

The remainder of this paper is organized as follows. Section II investigates substrate coupling in power ASICs and presents a simplified model, which is validated through time-domain analyses, to characterize the switching noise waveform. Section III describes the DPI test setup and reports the experimental results. Finally, concluding remarks are drawn in Section IV.

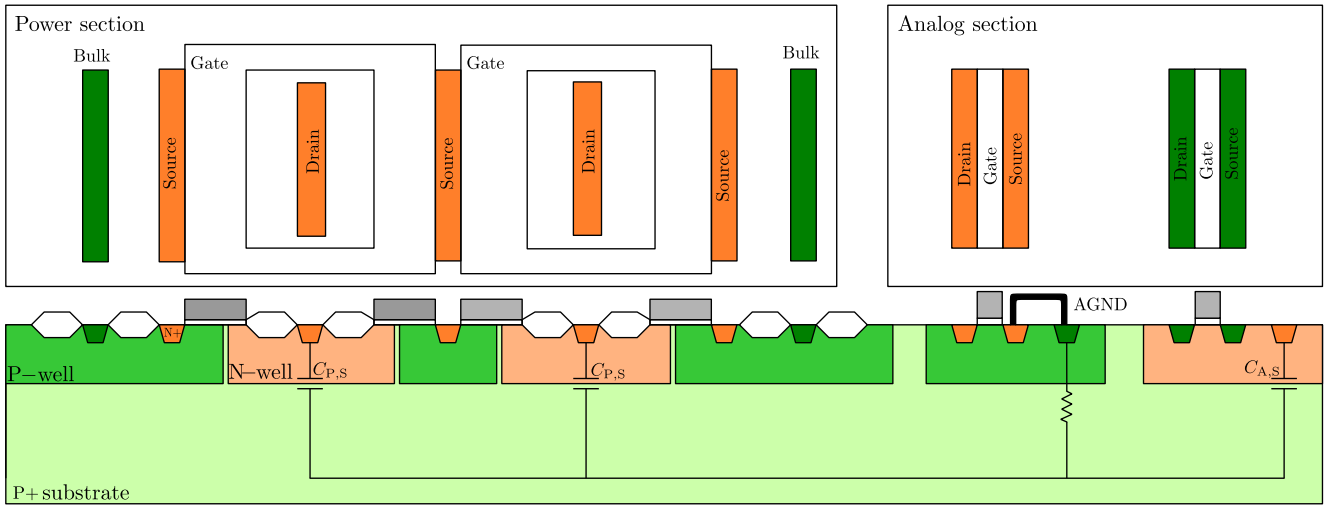


Fig. 2: Cross-section of a CMOS isolated process showing an LDMOS in the power section and low-voltage devices in the analog section.

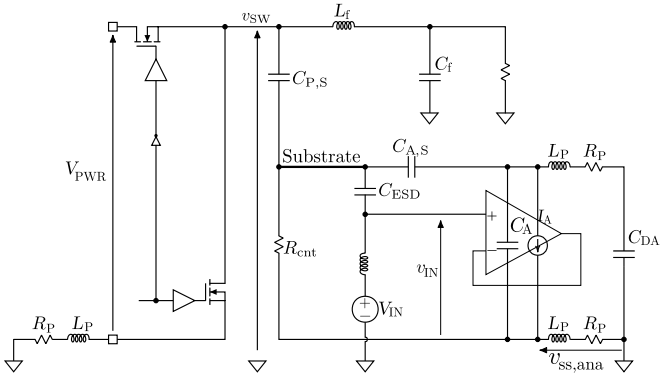


Fig. 3: Equivalent circuit used to study the propagation of the switching noise through the substrate.

## II. Substrate Coupling Driven Interference

The disturbances considered in this study arise from the cross-coupling between the different sections of an ASIC. Indeed, the sections of the IC are ideally isolated but in practice, they are coupled by the substrate they share.

The ASIC considered in this study is an integrated buck converter, in which the switching leg acts as the aggressor while, a feedback OpAmp in the control loop represents the victim. Under nominal conditions, the DC-DC converter operates at $f_{SW}$ = 10 MHz and generates a regulated output voltage ($V_{out}$) from a 5 V supply. Both the converter switching leg and the feedback OpAmp are implemented in a HV 350 nm CMOS technology, with the passive components assumed to be off-chip. The switching leg employs lateral diffused MOS (LDMOS) transistors, whereas conventional low-voltage devices are used in the OpAmp design. A simplified cross-section of an LDMOS in the power section, together with representative NMOS and PMOS devices from the N- and P-wells of the OpAmp, is shown in Fig. 2. In the switching leg, both the high-side (HS) and low-side (LS) transistors are implemented as arrays of unit devices. The drains of the LS transistors are diffused into the N-well and therefore form a reverse-biased pn junction with the substrate. As a result, switching activity injects currents into the substrate through the associated junction capacitances ($C_{P,S}$). Such a switching noise propagates through the substrate and contact resistances, affecting the analog ground of sensitive analog circuits.

A rough model of the substrate coupling between the switching node voltage ($v_{SW}$) and the analog ground voltage ($v_{ss,ana}$) is shown in Fig. 3. Under worst-case conditions, the substrate is assumed to be equipotential. The substrate-coupling network is modeled as a star connection including the parasitic junction capacitance between the power section and the substrate $C_{P,S}$, the capacitance associated with the PN junction between the analog N-well and the substrate ($C_{A,S}$) and the contact resistance $R_{cnt}$. In addition, the circuit of Fig. 3 includes a simple model of the package lead frame, the equivalent capacitance of the input pin ESD protection toward the substrate, and both the off-chip and on-chip decoupling capacitor ($C_{DA}$ and $C_A$, respectively).

The switching noise generated by the DC/DC converter and coupled through the substrate appears at the OpAmp input, effectively superimposed on the nominal input signal $v_{IN}$. In the following frequency-domain analysis, uppercase symbols denote the Fourier-domain counterparts of the corresponding time-domain voltages. Based on the equivalent circuit, the transfer function between the switching voltage and the analog ground voltage can be derived by applying the Extra Element Theorem to the capacitance $C_{ESD}$ [12], as

$$\frac{V_{SS,ANA}}{V_{SW}} = H_{wo,ESD}\frac{1+j\omega C_{ESD}Z_N}{1+j\omega C_{ESD}Z_D}, \qquad (1)$$

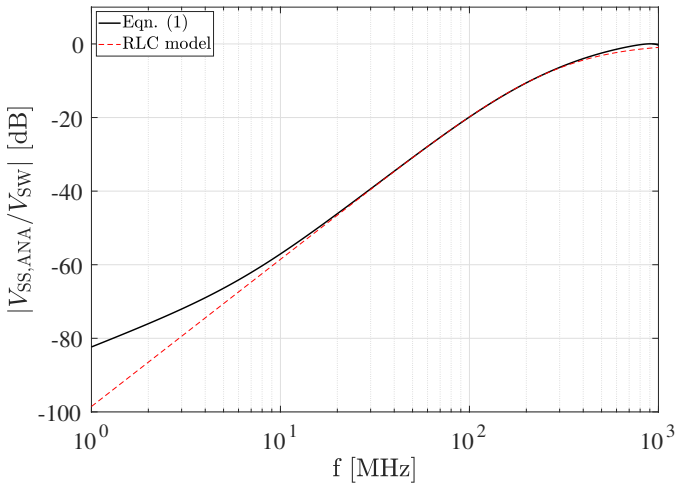


Fig. 4: Magnitude of the transfer function $V_{\mathrm{SS,ANA}}/V_{\mathrm{SW}}$.

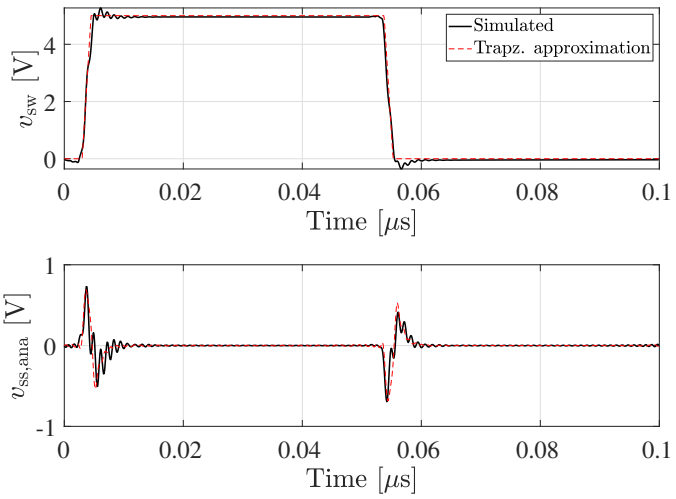


Fig. 5: Time domain analysis results. Switching-node voltage ($v_{\mathrm{sw}}$) and induced analog ground disturbance ($v_{\mathrm{ss,ana}}$).

where $H_{wo,ESD}$ is the transfer function of the network without $C_{\mathrm{ESD}}$. $Z_{\mathrm{D}}$ and $Z_{\mathrm{N}}$ represent the driving-point impedance and the impedance under the null double injection (NDI) condition, respectively.
Defining,

$$\begin{aligned} Z_{\mathrm{PA}} &= j\omega L_{\mathrm{P}} + R_{\mathrm{P}} + \frac{1}{j\omega C_{\mathrm{DA}}} \\ Z_{\mathrm{PB}} &= j\omega L_{\mathrm{P}} + R_{\mathrm{P}} \\ Z_{\mathrm{CA}} &= \frac{1}{j\omega C_{\mathrm{A}}}, \quad Z_{\mathrm{CAS}} = \frac{1}{j\omega C_{\mathrm{A,S}}}, \quad Z_{\mathrm{CPS}} = \frac{1}{j\omega C_{\mathrm{P,S}}} \end{aligned} \tag{2}$$

and referring to the triangle-star transformation,

$$\begin{aligned} Z_{\mathrm{A}} = \frac{\Sigma}{Z_{\mathrm{CA}}}, Z_{\mathrm{B}} = \frac{\Sigma}{Z_{\mathrm{CAS}}}, Z_{\mathrm{C}} = \frac{\Sigma}{Z_{\mathrm{PA}}} \\ \Sigma = Z_{\mathrm{CAS}} Z_{\mathrm{PA}} + Z_{\mathrm{PA}} Z_{\mathrm{CA}} + Z_{\mathrm{CA}} Z_{\mathrm{CAS}} \end{aligned} \tag{3}$$

the transfer function $H_{wo,ESD}$ can be expressed as

$$H_{wo,ESD} = \frac{Z_{\mathrm{F}} || Z_{\mathrm{A}}}{Z_{\mathrm{F}} || Z_{\mathrm{A}} + Z_{C,PS}} \frac{Z_{\mathrm{B}} || Z_{\mathrm{PB}}}{Z_{\mathrm{B}} || Z_{\mathrm{PB}} + Z_{\mathrm{C}} || R_{\mathrm{cnt}}}, \tag{4}$$

where

$$Z_{\mathrm{F}} = Z_{\mathrm{B}} || Z_{\mathrm{PB}} + Z_{\mathrm{C}} || R_{\mathrm{cnt}}. \tag{5}$$

Furthermore, based on these definitions,

$$Z_{\mathrm{D}} = j\omega L_{\mathrm{p}} + \frac{Z_{\mathrm{CPS}} \cdot Z_{\mathrm{F}} || Z_{\mathrm{A}}}{Z_{\mathrm{CPS}} + Z_{\mathrm{F}} || Z_{\mathrm{A}}}, \tag{6}$$

while the impedance in NDI condition is

$$Z_{\mathrm{N}} = j\omega L_{\mathrm{p}} (Z_{\mathrm{C}} || R_{\mathrm{cnt}}) \frac{Z_{\mathrm{PB}} + Z_{\mathrm{B}}}{Z_{\mathrm{PB}} Z_{\mathrm{B}}}. \tag{7}$$

The magnitude of the transfer function $V_{\mathrm{SS,ANA}}/V_{\mathrm{SW}}$, evaluated using the parameters listed in Tab. I, is shown by the black continuous line in Fig. 4. In the frequency range 10 MHz - 1 GHz, the substrate exhibits a high-pass behavior. This behavior can be reproduced by a second-order RLC filter

$$H = \frac{(j\omega)^2 L_{\mathrm{p}} C_{\mathrm{P,S}}}{1 + j\omega R_{\mathrm{cnt}} C_{\mathrm{P,S}} + (j\omega)^2 L_{\mathrm{P}} C_{\mathrm{P,S}}}, \tag{8}$$

TABLE I: CIRCUIT PARAMETERS

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $L_{\mathrm{Pi}}$ | 2.5 nH | $C_{\mathrm{A,S}}$ | 2 pF |
| $R_{\mathrm{Pi}}$ | 100 mΩ | $R_{\mathrm{cnt}}$ | 10 Ω |
| $C_{\mathrm{DA}}$ | 100 nF | $C_{\mathrm{P,S}}$ | 120 pF |
| $C_{\mathrm{A}}$ | 5 pF | $C_{\mathrm{ESD}}$ | 0.700 pF |
| $C_{\mathrm{f}}$ | 5 nF | $L_{\mathrm{f}}$ | 5 µF |

whose response is shown as the red dashed line in Fig. 4. The figure highlights the dominant role of $L_{\mathrm{P}}$ and $C_{\mathrm{P,S}}$ in the substrate coupling.
The noise induced on the analog ground ($v_{ss,ana}$) by the chopping of the converter input voltage ($V_{\mathrm{PWR}}$) was evaluated via a time-domain analysis of the circuit in Fig. 3. The results were then compared with those obtained by applying the transfer function in (1) to a trapezoidal waveform with

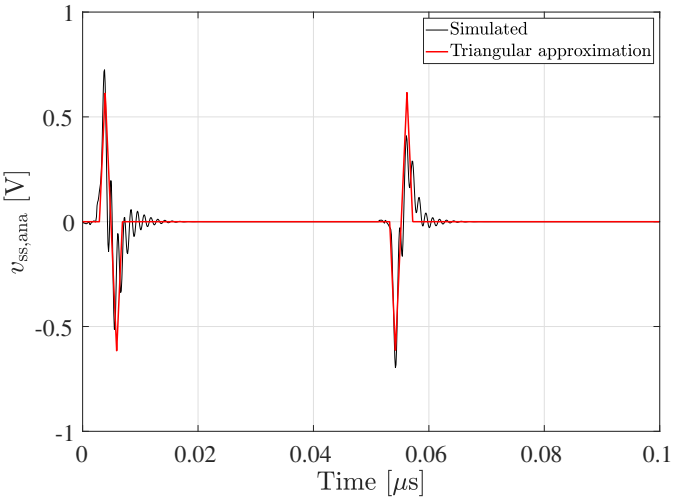


Fig. 6: Triangular approximation of the analog ground disturbance ($v_{\mathrm{ss,ana}}$).

TABLE II: OpAmps Parameters

| | Bipolar | CMOS | CMOS Chopper |
|---|---|---|---|
| $A_d$ | 100 dB | 91 dB | 135 dB |
| SR | 0.6 V/µs | 4.5 V/µs | 0.19 V/µs |
| GBW | 1.1 MHz | 8 MHz | 400 kHz |
| CMRR | 85 dB | 82 dB | 136 dB |
| $V_{off}$ | 1 mV | 0.1 mV | 1 µV |
| $f_{SW}$ | - | - | 400 kHz |

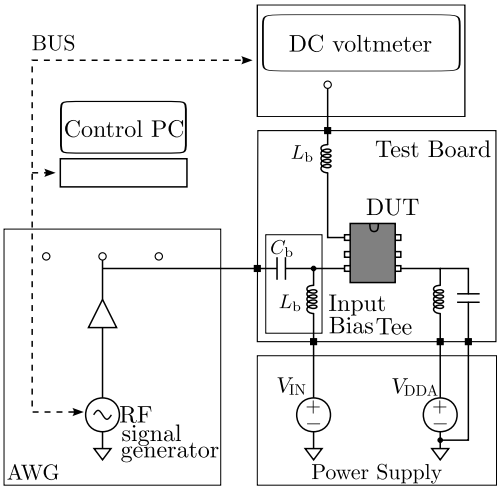


Fig. 7: DPI test bench used to asses the susceptibility to switching-noise interference.

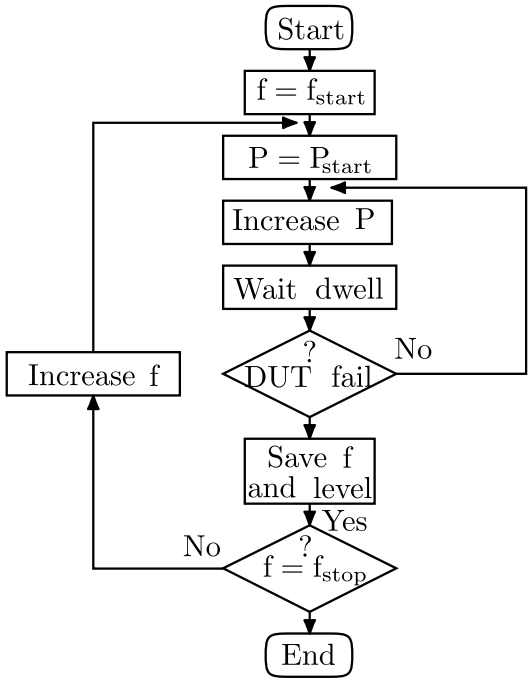


Fig. 8: DPI test procedure flow chart.

amplitude A = 5 V, rise/fall time $t_r$ = 1.5 ns, and 50% duty cycle. The resulting analog-ground voltages are plotted in Fig. 5 as the black continuous line and the red dashed line, respectively. Analysis of the analog ground voltage shows that every transition of $v_{SW}$ produces a bipolar spike at both the rising and falling edges. Each spike has a duration of a few nanoseconds, an amplitude of several hundred millivolts, and repeats at the switching frequency $f_{SW}$.

To facilitate the experimental generation of the switching noise disturbance, each bipolar spike is approximated by a piece-wise linear (PWL) waveform. In this approximation, each spike is represented by two consecutive triangular pulses with equal rise/fall time ($t_r$) and amplitude ($A$). The amplitude is chosen to preserve the spike energy, while the rise time is the same as $v_{SW}$. Mathematically, the waveform is expressed as

$$y(t) = \begin{cases} \frac{A}{t_r} t, & 0 \le t \le t_r, \\ \frac{A}{t_r}(2t_r - t), & t_r \le t \le 2t_r. \end{cases} \quad (9)$$

The resulting approximation with amplitude A = 0.6 V and $t_r$ = 1.25 ns is compared with $v_{ss,ana}$ in Fig. 6. The injected power delivered to a reference resistance R = 50 Ω is

$$P_{in} = \frac{1}{T} \int_0^T \frac{v_{ss,ana}^2}{R} dt, \quad (10)$$

where $T = 1/f_{SW}$ is the switching period. The same noise waveform, hereinafter referred to as triangular interference, will be used in the following DPI experiments with different repetition frequencies and injected power levels, as defined in (10), to assess the susceptibility of selected commercial OpAmps.

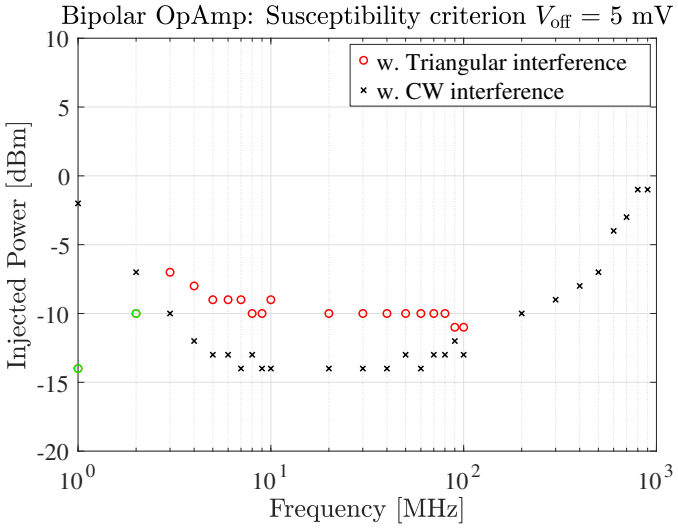


Fig. 9: Immunity levels for the bipolar OpAmp with the CW RFI (black crosses) and the triangular interference (red circles). Green circles indicate the frequencies at which no failure is observed.

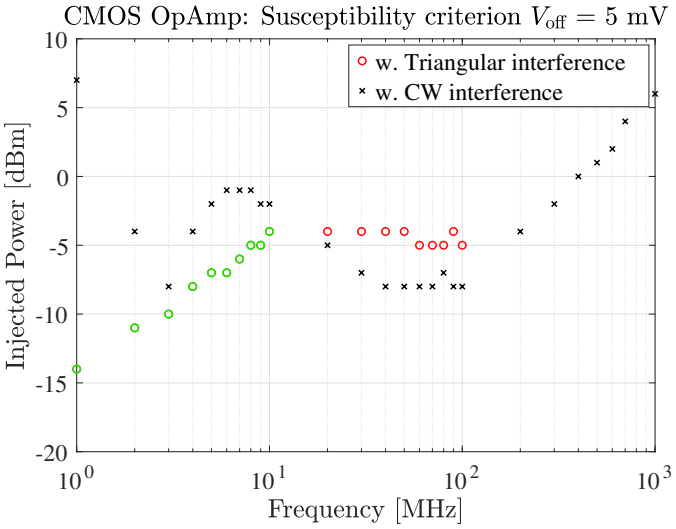


Fig. 10: Immunity levels of the CMOS OpAmp with the CW RFI (black crosses) and the triangular interference (red circles). Green circles indicate the frequencies at which no failure is observed.

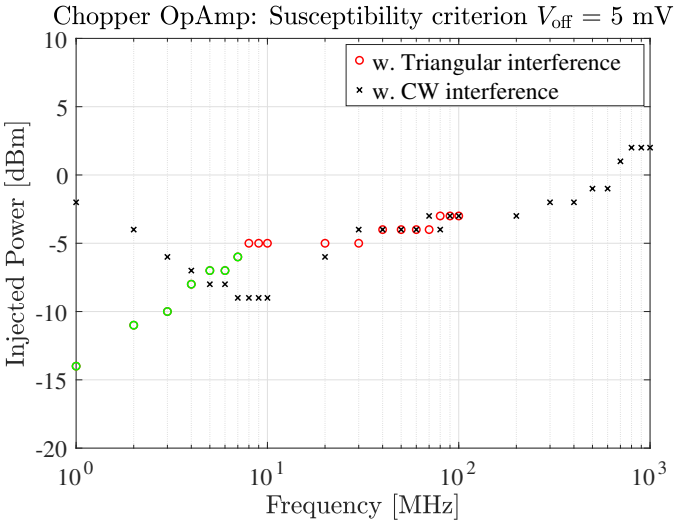


Fig. 11: Immunity levels of the chopper OpAmp with the CW RFI (black crosses) and the triangular interference (red circles). Green circles indicate the frequencies at which no failure is observed.

## III. Experimental results

A measurement campaign was carried out to assess the susceptibility to EMI of three commercial OpAmps, namely a bipolar, a CMOS, and a chopper device, whose main parameters are summarized in Tab. II.

For this purpose, a test board compliant with the IEC 62132 was designed for each Device Under Test (DUT) [11], configured as a voltage follower. Each test board was inserted into the Direct Power Injection (DPI) test bench shown in Fig. 7, which allows an interference signal to be superimposed onto the nominal input pin by means of the decoupling capacitor $C_{\text{b}}$. The DUT bias point is instead set by applying the supply voltage ($V_{\text{DDA}}$) and the nominal DC input ($V_{\text{IN}}$) through the bias tee inductors $L_{\text{b}}$. The voltage follower output is monitored using a DC voltmeter, from which the DUT response to the injected interference is evaluated. Finally, a wide band arbitrary waveform generator (AWG) was employed as the RF source [13], enabling the generation of both sinusoidal and non-sinusoidal disturbances.

In conventional DPI tests, the injected interference is typically a continuous-wave (CW) or amplitude-modulated (AM) RF signal, which induces a DC output offset due to demodulation in the OpAmp input stage. The choice of sinusoidal interference signals implicitly assumes that a DUT immune to such disturbances, substantially different from those experienced in real operating conditions, is also immune to non-sinusoidal disturbances having the same power and frequency.

Figure 8 outlines the DPI test procedure adopted in this work, which is independent of the interference profile. For each test frequency, the nominal DUT output voltage is first recorded. The RF source is then enabled and, after a dwell time of one second, the output voltage is re-acquired to evaluate the interference-induced offset. The interference power is subsequently increased in 1 dB steps until the susceptibility criterion, defined as a 5 mV DC output offset, is reached.

The results for the bipolar, CMOS, and the chopper OpAmps are shown in Figs. 9-11. Black crosses indicate the immunity levels obtained with CW signals, while red circles represent the response to the triangular-based waveform. Green circles markers indicate the frequencies at which the maximum output range of the AWG is reached before a failure occurs. No results are reported above 100 MHz because, above that frequency subsequent pulses would overlap. Overall, the results indicate that the OpAmps exhibit higher susceptibility to CW signals compared to the triangular waveform. The susceptibility of the chopper OpAmp, whose immunity results are reported in Fig. 11, is comparable for both types of interference at frequencies above 20 MHz.

## IV. Conclusion

This work investigated the susceptibility of commercial OpAmps to realistic switching noise, such as that generated by power transistors in power ASICs and coupled through the substrate to sensitive analog circuitry. The interference was first evaluated through time-domain analysis and then analyzed in the frequency domain to gain theoretical insight. The resulting triangular-based interference was applied to assess the immunity of three commercial OpAmps featuring different technologies, architectures, and device parameters. Measurement results show that the three OpAmps are less susceptible to switching-noise interference than to CW interference. These findings suggest that conventional CW-based DPI tests may lead to conservative susceptibility estimates when realistic switching-noise waveforms are considered.

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