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An Active Gate Driver to Mitigate the Overshoot Due to the Fast Switching of HV E-mode GaN HEMTs

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***Abstract*—The paper presents an active gate driver implementing two approaches for mitigating the over (under) voltages caused by the fast switching of WBG power transistors. The first is based on the fact that the overshoot (undershoot) and the oscillations following the turn on (off) of a power transistor deal with the switching speed. This can be limited acting on the magnitude of the gate current sourced (sunk) to (from) the gate terminal. A gate driver having the output transistors partitioned in elementary ones, each one driven independently from the others, so that the current sourced (sunk) to (from) the power transistor gate terminal can be set by the user.**
The second solution proposed in this work is based on the turning off of the gate driver for a short time interval during the Miller plateau. In this case the partitioning of the gate driver output transistors is not needed. A test chip implementing the two solutions was designed, prototyped and experimentally characterized. The effectiveness of the proposed approach is proved by the experimental results.

***Index Terms*—Active gate driver, GaN power transistor, over-voltage, ringing, oscillations, electromagnetic interference.**

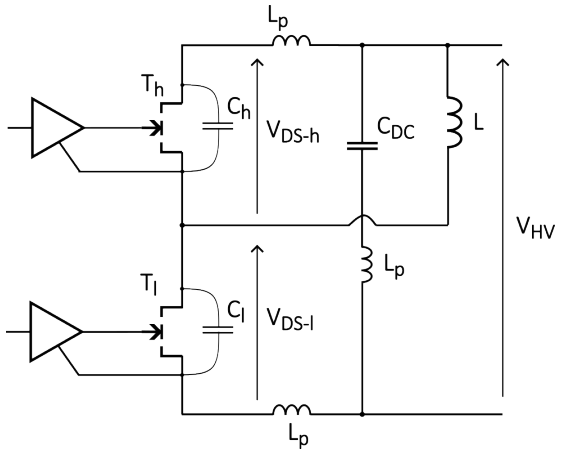

Fig. 1. E-mode GaN switching leg. The parasitic capacitances and inductances that causes over-voltages and ringing in the power loop are highlighted.

I. Introduction

The continuous development of Wide Band Gap (WBG) semiconductor technologies based on Silicon Carbide (SiC) and Gallium Nitrade (GaN) has made possible the design of power modules featuring ever higher switching frequency and conversion efficiency. This has increased the power density of modern modules but it has also introduced unexpected reliability and electromagnetic compatibility issues [1], [2]. Indeed, the fast switching of power transistors makes the stray capacitances of the switching and the non switching transistors to resonate with the stray inductances of the power circuit interconnects. Such resonances are responsible for the over-voltages (under-voltages) resulting at the power transistor drain-source terminals at each commutation, whose amplitude can exceed the maximum voltage of the power device itself. As a consequence, the transistors performance can degrade over time reducing their lifetime or causing unexpected operating failures. Traditionally, such problems are addressed by increasing the rise and fall time of the switching voltages, but this increases switching losses. In recent years, several authors showed that the amplitude of the over-voltage (under-voltage) can be also reduced by shaping the gate current provided to the transistor during commutations [3]. This can be obtained with a gate driver whose output transistors are partitioned in elementary ones and connected in parallel but driven by independent pre-drivers. This allows one to make each transistor switch at different time instants within the switching time of the power transistor [4], [5]. Usually, such gate drivers are referred to as Active Gate Drivers (AGDs). Using this approach, the overshoot (undershoot) affecting the switching voltage can be reduced with a minor increment of switching loss. However, it should be noted that the shape of the gate current that minimizes overshoots (undershoots) as well as the switching losses is obtained by a trial and error approach [4]. Such gate drivers has drawn the interest of designers and practitioners but to date they have not been used in real applications because of their complexity and silicon area overhead. Recently, it has been shown that over-voltages (under-voltages) affecting the output of a switching leg (hard switching) can be reduced significantly by a short

perturbation of the gate current during the Miller plateau. This last approach requires a simple gate driver since it does not need the partitioning of the output transistors. [6] showed the effectiveness of the technique referring to a MOS power transistor driven by a basic gate driver made up of discrete transistors mounted on the same test board hosting the power devices.

In this work, a test chip implementing the above mentioned techniques was developed with the purpose of driving E-mode GaN HEMT transistors. The integrated circuit was prototyped and fully characterized.

The paper is organized as follows. Section II presents the causes of over-voltage (under-voltage) and ringing affecting the power loop voltages, which result from the fast switching of WBG power transistors. The need for active gate drivers is discussed in Section III while the gate driver developed within this work is presented in Section IV. Some measurement results and concluding remarks are provided in Section V and VI, respectively.

II. The Need for Active Gate Drivers

The overshoot (undershoot) and oscillation resulting from the fast switching on power transistor can be explained referring to a half-bridge driving an inductive load like that shown in Fig. 1. Beside the power transistors ($T_{\rm l}$, $T_{\rm h}$), the inductive load (L) and the DC link decoupling capacitor ($C_{\rm DC}$), the circuit highlights the stray inductances modeling the PCB traces connecting the power devices to the DC link ($L_{\rm ph}$, $L_{\rm pl}$) and the drain-source capacitance of the high side transistor ($C_{\rm h}$) that are responsible for the generation for the unwanted oscillations triggered by the fast switching of the low side transistor ($T_{\rm l}$). Indeed, at the end of the dead time, while the the high side is in free wheeling ($T_{\rm h}$ conducts the load current in reverse mode), the turn on of $T_{\rm l}$ at the end of the dead time not only provides a path to the load current but it also sinks current that is needed to charge $C_{\rm h}$, the capacitance of the high side transistor. Depending of the switching speed, the drain-source voltage of $T_{\rm h}$ can exceed temporary the maximum value over which the device is damaged.

A common approach to limit such an unwanted effect is that of slowing down the switching transistor. This is obtained by limiting the current provided (taken) to (from) the gate to turn it on (off). Indeed, at the Miller plateau, the variation of the voltage across the gate-drain capacitance $C_{\rm GD}$ is about that between drain and source, i.e., the output voltage $v_{\rm O}$. Indeed,

$$\frac{dv_{\rm DS-l}}{dt} = -\frac{i_{\rm G}}{C_{\rm GD-eff}}, \tag{1}$$

where $C_{\rm GD-eff}$ is gate drain effective capacitance of the switching transistor.

III. An AGD based on the Gate Current Dip Technique

As mentioned in the introduction, AGDs were introduced with the aim of shaping the current sourced (sunk) to (from) the transistor gate during the switching phase with the purpose of damping the oscillation resulting from fast switching. This can be obtained with a gate driver which output transistors are made up of several transistor connected in parallel but driven independently. This way, the user can configure the gate driver to generate almost any kind of current shape. However, such an approach increases the complexity of the circuit a lot. Each elementary output transistor needs its own pre-driver, an independent PWM and Enable inputs and the complexity of the timing logic increases significantly with the number of elementary transistors to drive. Furthermore, to date the optimal gate current waveform to avoid overshoot and ringing is obtained by a trial-and-error approach [4]. In [6], it was shown that the same result can be obtained by switching off the gate driver for a short time interval during the Miller plateau. The effectiveness of the proposed approach was validated with a basic gate driver made up of discrete transistors mounted on a test board close to the power device. A low voltage MOS power transistor was used because the stray inductances and capacitances of the PCB assembly limited the switching speed of the gate driver.

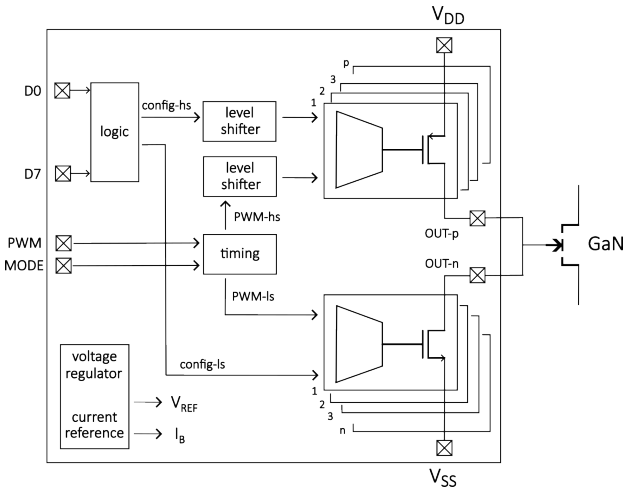

Fig. 2. Gate driver architecture.

In this work, an active gate driver implementing the approach introduced in [6], namely the gate current dip (GCD) technique as well as that based on limiting the gate driver strength by means of segmented output (SO) transistors is presented. The architecture of the developed gate driver is shown in Fig. 2.

The output stage comprises of a pMOS and an nMOS transistor, made up of $p = 16$ and $n = 8$ elementary devices, respectively. Each transistor is driven by an independent pre-driver, which in turn receives the enable signals (*en-h*, *en-l*) from the configuration logic blocks (*config-ls*, *config-hs*) and the switching commands *pwm-ls*, *pwm-hs* from the *timing logic*. This last block generates the dead time needed to avoid the cross conduction of the gate driver output transistors.

The configuration signals (D0-D7 and MODE) as well as the PWM command are provided to the AGD by a microcontroller (not shown in Fig. 2). If the MODE logic input is set LOW, the AGD runs in SO mode, in GCD mode otherwise. In the

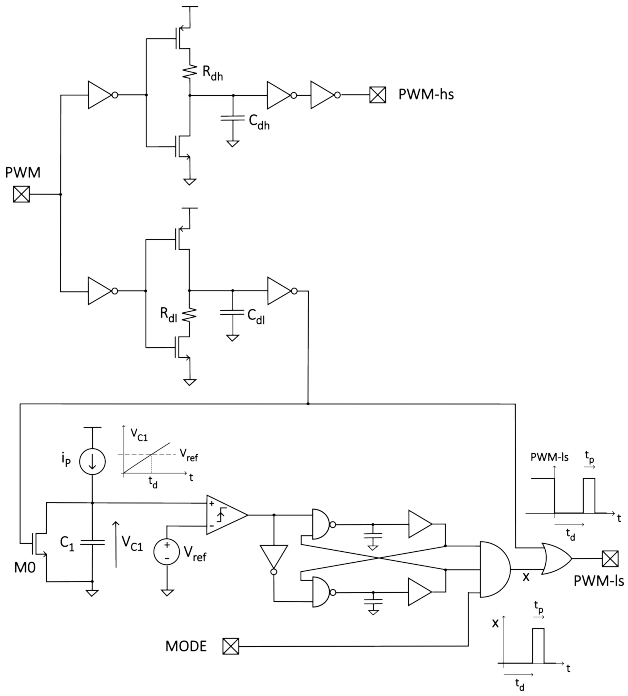

Fig. 3. Schematic view of the *timing logic* block.

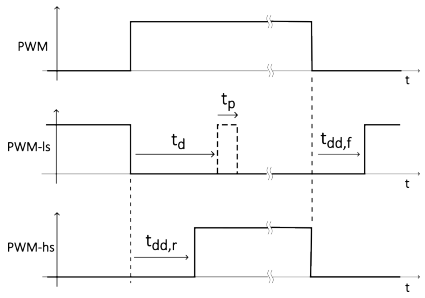

Fig. 4. PWM signals generated by the timing block.

former case, the configuration inputs (D0-D7) set the strength of the gate driver, meaning the overall width of the pMOS and the nMOS transistors, in the latter, the same inputs are used to set the delay (t_{d}) after which the gate driver is turned off for t_{p}, the dip time. In this work the dip time is set to $t_{\mathrm{p}} = 1\ ns$. The schematic view of the *timing logic* is shown in Fig. 3. The circuit is made up of two inverter chains that generate the PWM commands (PWM-hs, PWM-ls) for the high side and the low side output transistors. The second inverter included in each chain is modified to introduce a constant delay whenever the *PWM* input switches from LOW (HIGH) to HIGH (LOW) but not on vice versa. By doing so, the transition LOW-HIGH (HIGH-LOW) of the PWM input signal causes the sudden turn off of the nMOS (pMOS) while the turn on of the pMOS (nMOS) is delayed by $t_{\mathrm{dead,r}}$ ($t_{\mathrm{dead,f}}$). The dead times are set in the design phase by choosing the time constants $\tau_{\mathrm{h}} = R_{\mathrm{dh}}C_{\mathrm{dh}}$, $\tau_{\mathrm{l}} = R_{\mathrm{dl}}C_{\mathrm{dl}}$. In this work $t_{\mathrm{dead,r}} = t_{\mathrm{dead,f}} = 10\ ns$. The PWM signals generated by the timing logic with the device configured in *SO mode* (*MODE = LOW*) are those shown by continuous lines in Fig. 4. In *GCD mode* (*MODE = HIGH*), the transition of the *PWM-ls* from HIGH to LOW enables the propagation to PWM-ls of the short pulse needed to turn off the gate driver for t_{p}. Indeed, PWM-ls switch off M0, so that the dc current source i_{p} charges C_1 at constant rate. When v_{C1} crosses over the reference voltage V_{ref}, the voltage comparator turns on the pulse generator. The delay t_{d} to release the short pulse is set by the code D0-D7, which in turn sets the magnitude of the dc current sourced by i_{p}. The gate driver presented so far was designed referring to a 130nm HV CMOS technology process. A micro photograph of the test chip encapsulated in a QFP package is shown in Fig. 5.

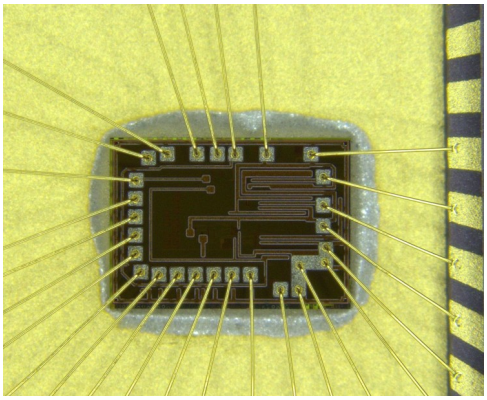

Fig. 5. A micro-photograph of the test chip.

IV. Test Bench and Measurement Results

A test board suitable to perform the double pulse test (DPT) was designed and prototyped. Besides the test chip, it comprises two GaN HEMTs [7] connected as shown in Fig. 6. The low side transistor is driven by the proposed AGD, which in turn is controlled by a microcontroller. The gate of the high side transistor (T_{h}) is shorted to the source to keep it off permanently. Therefore, during the free wheeling the device is driven in reverse conduction mode by the load current. The power supply of the switching leg was set to $V_{\mathrm{HV}} = 150\ V$. The drain-source voltage of the low side as well as the drain voltage of the high side were measured with an oscilloscope connected as shown in Fig. 6. The DPT was carried out driving the gate driver to obtain a current level of $i_{\mathrm{L}} = 5\ A$ at the turn on of the low side. Furthermore, the gate driver was configured to drive the transistor at the maximum switching speed (dashed lines), to damp the oscillation and minimize the switching loss (dash-dotted line), to damp the oscillation with the GCD technique (solid line). The drain-source voltages and the low side and high side transistors obtained from the measurements are shown in Fig. 7 and Fig. 8, respectively.

Furthermore, at a closer look to the plots shown in Fig. 7, it can be found that the fall time of $V_{\mathrm{DS-l}}$ in the different operating modes is $t_{\mathrm{f,maxspeed}} = 6.1\ ns$, $t_{\mathrm{f,SO}} = 14.3\ ns$ and $t_{\mathrm{f,GCD}} = 8.1\ ns$. As expected, the minimum switching

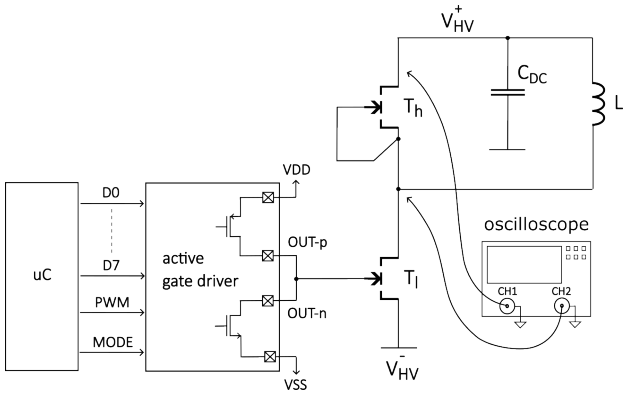

Fig. 6. Schematic view of the test bench.

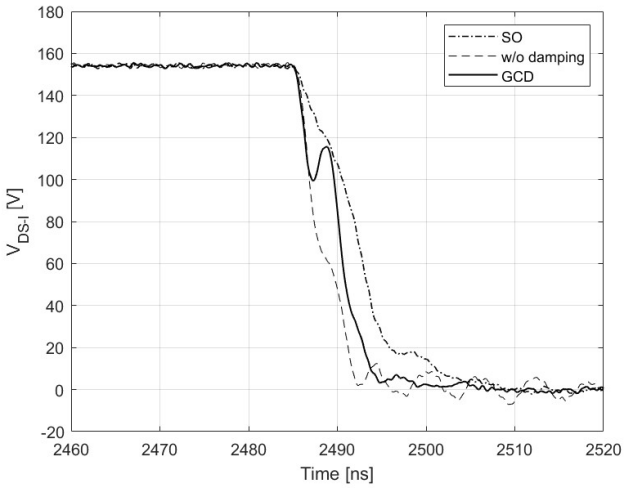

Fig. 7. $V_{\mathrm{DS-l}}$ with dpt: maximum speed, SO control, GCD technique.

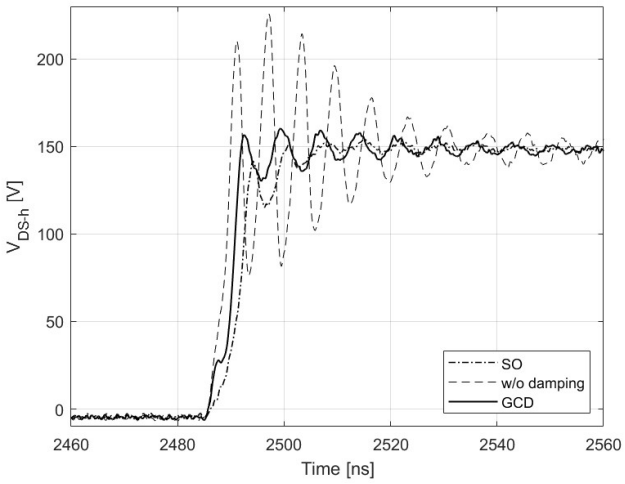

Fig. 8. $V_{\mathrm{DS-h}}$ with dpt: maximum speed, SO control, GCD technique.

time, meaning the minimum switching loss of the low side, is obtained with the low side driven at the maximum speed, but in that case the high side drain-source voltage is affected by an over-voltage of about 70 V (dashed line in Fig. 8). With the gate driver configured in SO mode and programmed to damp the oscillations (dash-dotted line in Fig. 8), the minimum fall time is more than twice the previous one. Finally, with the gate driver configured in GCD mode, the overshoot as well as the oscillations are greatly reduced, the fall time is greater than that obtained driving the low side at the maximum speed but it is much lower than that obtained in SO mode.

V. Conclusions

An active gate driver that mitigates the overshoot (undershoot) caused by the fast switching of GaN HEMT power transistors was designed, prototyped and fully characterized. A solution to limit the slew rate of the output voltage by limiting the current sourced (sunk) by the gate driver at the turn on (off) was implemented at the silicon level. This was obtained with output transistors made up of smaller ones connected in parallel, that can be selected and driven independently with the purpose of modulating the strength of the gate driver.
With the same purpose, a novel approach based on the zeroing of the gate current for a short time interval during the Miller plateau was also implemented. This solution does not require the partitioning of the gate driver output transistors, therefore the complexity of the gate driver and the related silicon area are significantly reduced.
The measurement results showed that both approaches are effective in reducing overshoot and ringing but the gate current dip (GCD) technique makes the power transistor switch faster.

Acknowledgment

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