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DENEB: a 1024-channel cryogenic mixed-signal ASIC for SiPM matrix readout targeting sub-100 ps timing and wide dynamic range

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Abstract: DENEB is a 1024-channel mixed-signal ASIC under development at INFN in 110 nm CMOS technology for the readout of 32 × 32 silicon photomultiplier (SiPM) matrices over a wide temperature range (77–300 K). It is intended for scintillation-light cameras in single-phase noble-liquid detectors, where charged-particle tracks are reconstructed from scintillation light alone.

Each channel comprises a low-impedance input stage, a fast timing branch with dual-threshold discriminators, on-pixel time-to-digital converters, and a charge branch for photon counting based on discrete-time current-to-frequency conversion. The front end targets sub-100 ps single-photon time resolution and a dynamic range exceeding 100 photoelectrons, while supporting per-channel event rates up to a few MHz under stringent power and cryogenic constraints. At the periphery, SRAMs buffer the event words and 32 high-speed SLVS/LVDS transceivers provide an aggregate bandwidth up to ∼ 20 Gbps in double-data-rate mode using time-division multiplexing. Architectural choices are driven by scalability to large channel counts, the need for derandomization to mitigate TDC deadtime, and robustness across the full temperature range.

This work presents the system requirements, design strategy, and key architectural features of the DENEB ASIC, including pixel and end-of-column organization, data-readout scheme, and integration aspects at the package and detector level. Design trade-offs and ongoing challenges related to large-channel-count cryogenic operation are discussed, together with the current development status and outlook.

Keywords: Analogue electronic circuits; Digital electronic circuits; Front-end electronics for detector readout; Cryogenic detectors

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1 Introduction and system-level requirements

Noble-liquid detectors are increasingly employed in rare-event searches and neutrino physics [1, 2], where photodetectors, including silicon photomultipliers (SiPMs), detect the prompt scintillation light produced by charged particles in liquid argon.

LAr TPCs traditionally combine ionization-charge readout with scintillation-light detection for event reconstruction and timing. More recent approaches based solely on scintillation light are being explored [3], imposing stringent requirements on the front-end readout in terms of timing resolution, dynamic range, channel density, data throughput, and operation at cryogenic temperature.

In these camera concepts, each module comprises a SiPM matrix directly coupled to a dedicated readout ASIC. The ASIC must be placed as close as possible to the SiPM matrix, immersed in LAr, in order to minimize interconnect parasitics, which deteriorate the performance of the front-end amplifier, and to reduce the number of cryostat feedthroughs, which increase the thermal load [5]. As a consequence, the readout electronics must operate over the temperature range from 77 K to room temperature to enable laboratory tests and operation in liquid argon.

In the targeted camera configuration, the readout ASIC must handle 1024 SiPM channels in parallel and time-stamp single-photon events with a single-photon time resolution better than 100 ps. Due to the large scintillation yield of liquid argon, reconstructed images may exhibit high photon statistics, with acquisition windows containing isolated single photons as well as bursts with hundreds of photons in time windows of order 10 µs (spill). This leads to multiple single-photon events closely spaced in time (down to $\mathcal{O}$(ns)) across the matrix, under illumination conditions ranging from nearly uniform exposure of the full array to localized hotspots. To enable track reconstruction, bursts separated by ∼100 ns must be individually time-stamped and digitized. These conditions motivate on-pixel time and charge digitization, while constraints on power density, on-chip memory, and off-chip data bandwidth limit the complexity of the per-channel architecture and the amount of data that can be stored and transmitted out of the cryostat.

Motivated by this application, DENEB is a 1024-channel mixed-signal ASIC under development at INFN Torino in 110 nm CMOS technology [4]. This paper presents the main system-level specifications and design strategy, focusing on the pixel and end-of-column architecture, floorplan, and cryogenic packaging concept.

2 ASIC specifications and design trade-offs

Given the wide range of possible signal conditions, from isolated single-photon events to highly piled-up bursts, a waveform-sampling architecture would offer the most flexibility at the single-channel level. However, the combination of sub-100 ps timing, expected hit-rates, photon-counting capability and a kilochannel matrix would require prohibitively high sampling rates and data volumes. Storing full waveforms either on chip or in external memory would exceed the available area and power budget, while continuously streaming them out of the cryostat is incompatible with the limited number of high-speed links that can be routed from a ton-scale liquid-argon detector.

For these reasons, DENEB adopts an event-based architecture with on-pixel time and charge extraction and a compact digital representation of each event.

Table 1 summarizes the main specifications targeted by DENEB, a 1024-channel mixed-signal ASIC developed in a 110 nm CMOS process to meet the requirements outlined in the previous section. The ASIC builds on the experience with ALCOR, a 32-channel mixed-signal SiPM readout ASIC designed in the same technology at INFN Torino [6]. ALCOR has been experimentally characterized both at room temperature and in liquid nitrogen, providing a validated reference for circuit operation down to 77 K.

Table 1. Main features of the DENEB ASIC.

Features	**Value**
Technology	110 nm CMOS
Operating temperature	77–300 K
Channels	1024 (32×32 pixels, 500 µm pitch)
Silicon area	$\sim 18 \times 23.5\,\mathrm{mm}^2$
Measurements/channel	Time-of-arrival, Time-over-threshold, Slew-Rate, Charge (Photon-Counting)
Single-photon time resolution (SPTR)	< 100 ps
Dynamic range (charge)	> 100 photoelectrons
Photon-counting resolution	$\sim$ 3–4 codes/PE (1 PE resolved between 1 and 5 PE)
Maximum event rate on a pixel	~ 3.8 MHz
In-pixel event word	1×64-bit (timing) or 2×64-bit words (timing, charge)
End-of-column memory	2048 (64-bit) or 1024 (2×64-bit) words/column
Output links	32 SLVS/LVDS differential transceivers
Link speed	320 Mbps SDR or 640 Mbps DDR
Aggregate bandwidth	up to $\sim$ 20 Gbps (DDR, Time-Division-Multiplexing)
Average power / channel	$\sim$ 5–15 mW/channel (mode and temperature dependent)
Special features	Power gating, dark-count suppression window

Since no PDK officially qualified for cryogenic operation is available, the DENEB design relies on extrapolated device models, whose validity is supported by the agreement between simulations and ALCOR measurement results over the 77–300 K range. These studies indicate that cryogenic operation has a significant impact on analog circuit performance, with threshold voltage increase (up to ~ 200 mV rise) being one of the dominant effects. This results in reduced voltage headroom and limits the maximum number of stacked transistors that can be used while maintaining proper biasing

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conditions. At the same time, long-term reliability considerations require operation at reduced supply voltage to mitigate hot-carrier degradation effects [7], introducing an additional constraint on the available voltage budget. To mitigate these effects, transistors from the "High-Speed" (HS) device option, characterized by lower threshold voltage ($\sim$ 250 mV at 300 K), have been employed with channel lengths longer than minimum to balance speed, noise, and robustness across temperature [7]. The chip is simulated across process and temperature corners to assess the resulting spread of key parameters, and programmable configuration bits are used to compensate for temperature-induced variations, such as delay and poly-resistance values, enabling adaptation of the circuit operating point across the full temperature range.

3 Floorplan

Figure 1 shows the system-level floorplan of the ASIC, including the padframe and a single-channel block diagram. The chip features a 32×32 pixel matrix read out along 32 columns, with per-pixel analog and digital circuitry. Each pixel has a dedicated analog input pad placed directly above the first front-end stage, thereby minimizing interconnect parasitics between the SiPM and the amplifier and forming an "analog pad island" across the matrix. Clock distribution is implemented using an H-tree network with interpixel delay lines to introduce a controlled skew between pixels. The pixel pitch is $500 \times 500\ \mu m^2$, with approximately two-thirds of the area allocated to analog circuitry and one-third to digital control logic.

Along the bottom of the matrix, the end-of-column periphery hosts the bias generation, digital control, SRAM blocks and 32 SLVS/LVDS transmitters. The transceivers operate at 320 Mbps in SDR or 640 Mbps in DDR mode, providing an aggregate bandwidth up to 32×640 Mbps via time-division multiplexing. Triple modular redundancy (TMR) is implemented in selected periphery blocks to improve radiation robustness, while it is not adopted at the pixel level due to area constraints. The overall chip footprint is about $18 \times 23.5\ mm^2$.

The ASIC operates from a 1.2 V supply and is organized in five main power domains. A programmable power-gating feature that reduces the power of the analog blocks in the channels is introduced to reduce the average power. To mitigate static and dynamic IR drop, supply and ground pads for the channels matrix and the high-speed transmitters are distributed in a ring around the matrix. Where possible, core blocks and analog bias distribution are implemented with architectures that reduce sensitivity to IR drops, and channel performance is being validated for the expected worst-case IR-drop conditions. Power integrity simulations are being performed to validate the chip-level supply network and to refine the pad placement and routing strategy.

High-level mixed-signal simulations are performed in a digital-on-top environment, while detailed AMS and fully SPICE analyses are carried out on selected critical regions, including low-temperature operation, to validate these design choices. Mixed-signal noise is reduced by dedicated power partitioning, with one analog domain for the very front-end, one for the data converters, a digital supply for the pixel and EoC logic, and a separated substrate (p-substrate and n-well guard rings) line. The transceivers have dedicated supply pads, while their physical separation from the core limits substrate noise coupling. In the analog blocks, deep-n-well NMOS devices are used to reduce the impact of substrate noise on performance, at the cost of additional area. A dedicated p-well blocking layer is used to define isolated well regions for mixed-signal integration. In addition, layout techniques have been adopted to further reduce the impact of substrate noise, such as a mirrored layout of alternating

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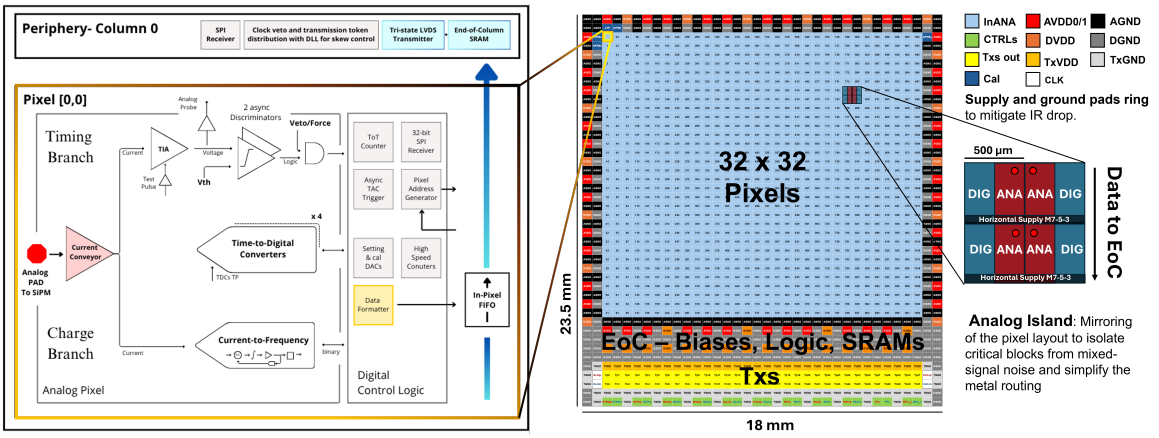

Figure 1. From left to right: pixel-channel block diagram, full-chip floorplan and pad map, and mirrored pixel-column layout for mixed-signal noise reduction and routing optimisation.

pixel columns, which connects the analog areas of neighboring columns into a common island and keeps sensitive analog inputs away from digital switching activity, as illustrated in figure 1.

4 Channel and end-of-column architecture

The DENEB architecture follows an event-based approach in which each pixel extracts a compact set of timing and charge observables, which are then aggregated at the end of each column and transmitted off chip through shared high-speed links.

Each pixel reads a SiPM through a dedicated analog input pad. The sensor current is collected by a low-impedance front-end stage [8] and mirrored into two main branches: a timing branch for time measurement and a charge branch for wide-dynamic-range photon counting, as shown in figure 1.

In the timing branch, the current signal is converted into a voltage by a fast amplifier and compared against two independent thresholds by asynchronous discriminators. This enables the measurement of time of arrival (ToA), time-over-threshold (ToT), and slew rate (SR), which are used for time-walk correction and low-dynamic-range photon counting (up to a few photoelectrons). The timing chain is designed to achieve single-photon time resolution in the sub-100 ps range for the targeted SiPM sizes ($\leq 3 \times 3\,\mathrm{mm}^2$), under the constraints summarized in table 1. At low temperature, a dedicated configuration bit reduces the number of stacked transistors in the input stage and lowers the input current to preserve bias conditions, but overall timing performance is expected to improve at 77 K [9]. SiPM models are parametrized to account for variations due to low-temperature operation.

Previous characterization of ALCOR [6] shows that slew-rate measurements provide more robust time-walk correction than ToT alone, at the cost of two fine time measurements per event. To maintain low deadtime while preserving this information, DENEB implements four on-pixel time-to-digital channels per pixel, thereby derandomizing closely spaced events with separations down to $\mathcal{O}(100\,\mathrm{ns})$. The time digitizers are based on analog interpolation over an effective window of $1.5\,T_{clk}$ with on-pixel analog-to-digital conversion, with a target time bin of the order of 50–20 ps.

During acquisition, an event is defined by the interval between the rising and falling crossings of the thresholds. Programmable extensions of this window by a few tens of clock cycles allow small photon packets close in time to be merged, reducing the occupancy of the time digitizers. High

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dark-count-rate (DCR) conditions can be mitigated by programmable digital veto windows at the pixel level, reducing the impact of uncorrelated noise hits on the event definition and subsequent timing and charge measurements.

In the second branch, the SiPM mirrored current is integrated over the event window to reconstruct the total number of detected photoelectrons. To cope with both isolated single photons and highly piled-up signals while maintaining single-photon sensitivity, DENEB employs a discrete-time current-to-frequency conversion scheme, conceptually similar to the approach in [10], with real-time digital counting, effectively implementing a single-stage sigma-delta converter at the pixel. This approach provides an instantaneous dynamic range of several tens of coincident photoelectrons and a total charge dynamic range exceeding 100 photoelectrons within the acquisition window, using a single block per channel. The architecture is optimized for real-time digitization, with a dead time comparable to the signal duration.

For each event, the pixel produces two independent 64-bit words, carrying timing and charge-related information, respectively. This separation allows the readout to be configured for either full timing and charge reconstruction or for timing-dominated applications, in which charge information can be suppressed to double the effective bandwidth. Event words are transferred along a daisy chain to the end-of-column logic, where they are stored in dedicated SRAM blocks dimensioned to buffer up to about 1024 events per column. The 32 SLVS/LVDS transmitters are placed below the SRAMs at the bottom of the die.

5 Cryogenic packaging and camera integration

The DENEB ASIC features a dense padframe implemented as a 36×44 grid with a pitch of 500 µm, including 1024 analog input pads for the SiPM connections, pads for analog probes, 64 differential pads for the high-speed transmitters, and additional pads for clock, control, power management, calibration and reset signals. The resulting I/O density makes conventional wire-bond packaging impractical, and a fan-out wafer-level packaging (FOWLP) solution has been adopted. In this approach, the ASIC is bump-bonded and embedded in a fan-out structure, where redistribution layers (RDL) route the signals to an array of solder balls (BGA) with 500 µm pitch. The use of silicon-compatible materials is driven by the need to minimize the coefficient-of-thermal-expansion mismatch between the die, package and board, which is critical to avoid mechanical stress and connection failures during cooldown from room temperature to liquid argon.

The packaged ASIC acts as a self-contained readout unit that can be soldered to a custom camera board hosting one or more SiPM matrices. In this configuration, the SiPM electrodes are routed directly to the analog input pads of the package, while only a limited number of high-speed data links, clocks and power lines are brought out of the board through the cryostat feedthroughs. This solution reduces the number of feedthroughs and data cables, enabling the readout of a large number of channels while keeping the thermal load and system complexity under control.

6 Conclusions

DENEB is a 1024-channel mixed-signal ASIC developed for room temperature to cryogenic SiPM camera applications, targeting scintillation-light-based tracking in noble-liquid detectors, and combines sub-100 ps single-photon timing with wide-dynamic-range photon counting in a 32×32 SiPM matrix.

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The architecture adopts on-pixel time and charge extraction, per-column buffering and shared high-speed links to match the available bandwidth and feedthrough budget. The chip floorplan groups the pixel matrix into an analog island surrounded by end-of-column logic, SRAMs and 32 SLVS/LVDS transmitters at the periphery, while a dedicated fan-out wafer-level package provides the I/O density and mechanical robustness required for operation from 77 K to 300 K.

The design is currently in an advanced phase, with the main architectural choices frozen and block-level verification ongoing. Chip validation is being performed over process and temperature corners. Finalization of the mixed-signal blocks and full-chip verification are in progress, to be followed by tape-out in an engineering run and by room-temperature and cryogenic characterization of the performance, resulting in the integration of DENEB in a camera demonstrator setup.

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