Investigation on the Susceptibility to RF Interference of LDO Voltage Regulators

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***Abstract*—The DC output voltage of low dropout (LDO) voltage regulators can be affected by the presence of radio frequency interference (RFI) superimposed onto the DC input terminal. This is due to the rectification of the interference carried out by the building blocks of the voltage regulator. Traditionally the problem has been addressed by adding filters at the printed circuit board level, but this requires additional components, and filters are effective on a limited frequency band. This work discusses the susceptibility to RFI of an LDO based on a traditional architecture, then a novel solution to increase its immunity is proposed. The effectiveness of the proposed approach is validated through simulations.**

***Index Terms*—LDO voltage regulator, Susceptibility to RFI, RFI rectification, Direct Power Injection test**

I. Introduction

LDO voltage regulators are widely used in electronic unit both at the integrated circuit level and at the module level to ensure a stable and clean DC power supply for analog and digital electronic circuits.

Usually, they receive a DC power supply from a DC-DC voltage regulator and generate at their output a DC power supply featuring low sensitivity to the input voltage, load current, and temperature variations. They are preferred to their switching-mode counterparts because they deliver a clean power supply, meaning not affected by switching noise. It can be stated without ambiguity that LDO regulators effectively act as filters for switching noise. However, investigations carried out in the last decades showed that the regulated DC output voltage changes if the DC input voltage is affected by RF interference [1], [2], [3], [4].

Common voltage regulators comprise a pre-regulator, a bandgap voltage reference, and a feedback amplifier driving the output transistor as shown in Fig. 1 [5]. The pre-regulator steps down the DC input voltage to provide the power supply (v_{PRE}) to the other blocks, namely the voltage reference, the amplifier, the bias circuits, and the ancillary circuits, such as current sensors and thermal protections. Previous works have shown that the RFI-induced offset observed at the output of the voltage regulator is due to the rectification of the RFI in the bandgap voltage reference [6], [7], in the amplifier [8], [9] or in the ancillary circuits [10], [11], [12]. Given that all these blocks are supplied by the pre-regulator, and with the aim of addressing the problem in one go, the analysis focused on the pre-regulator and on the way the interference is propagated to the other circuits. To this purpose, a self-biased topology is proposed, and its effectiveness in increasing RFI immunity is evaluated through time-domain analysis following the DPI procedure.

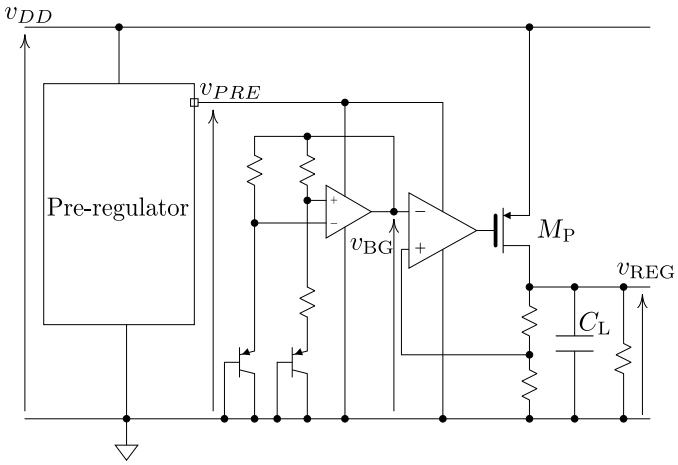

Fig. 1: Block diagram of an LDO voltage regulator including a pre-regulation network, and a bandgap voltage reference.

The remainder of the paper is organized as follows. Section II compares the conventional architecture with its self-biased counterpart, discussing the RFI propagation paths and the approach used to enhance immunity. Section III describes the simulation setup employed to assess LDO RFI immunity and presents the main results. Finally, concluding remarks are provided in Section IV.

II. A Self-Biased Pre-Regulator

The voltage regulator under study is composed of three main building blocks: the LDO, the bandgap reference, and a pre-regulator that provides their supply. A possible transistor-level implementation of the pre-regulation network, adopted in this work as a representative example, is shown in Fig. 2. It consists of a current generator, which establish the current I_2, implemented by R_1, R_2 and M_1, M_2; a current mirror made by M_3 and M_4; two diode connected transistors; and the pass-

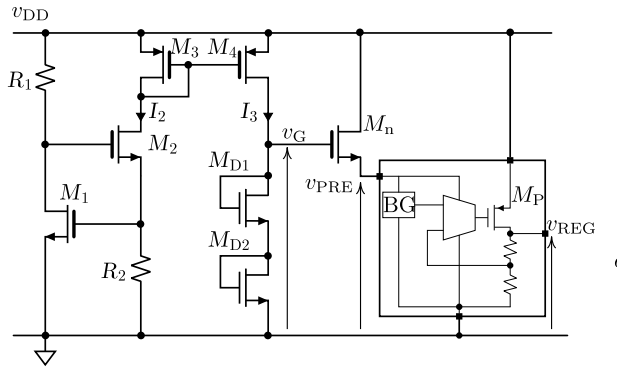

Fig. 2: Transistor-level schematic of the pre-regulator within the LDO voltage regulator.

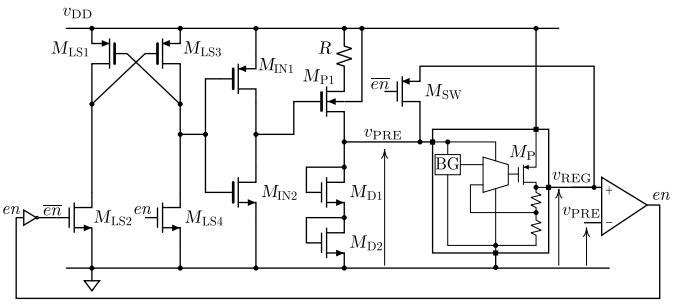

Fig. 3: Transistor-level schematic of the self-biased voltage regulator.

transistor M_{n}. The current I_2 is mirrored and subsequently translated into the voltage V_{G}, which represents the pre-regulated voltage, excluding the gate-source voltage drop of M_{n}.

Taking the entire LDO voltage regulator into account, an RF interference applied at the supply can reach the regulated output (v_{REG}) through two main propagation paths: the first is the direct path through the LDO power transistor M_{p}, while the second is the indirect path through the pre-regulator and the bandgap.

The indirect coupling path can be suppressed by employing a self-biased voltage regulator. The transistor level implementation adopted in this work is shown in Fig. 3. In this architecture, the pre-regulator consists of a level shifter implemented by $M_{\mathrm{LS1}} - M_{\mathrm{LS4}}$, an inverter $M_{IN1} - M_{IN2}$, the switch M_{SW} and two diode-connected transistors. A comparator controls the transition between the start-up and post-start-up phases. During start-up, v_{PRE} is set by M_{D1} and M_{D2}. Once the start-up of the LDO is completed v_{REG} approaches v_{PRE}, the enable signal (en) goes high, and v_{PRE} is directly derived from v_{REG}. With M_{P1} turned off, the indirect path through the pre-regulation network and the bandgap voltage reference is suppressed, leaving only the direct path through M_{P} to convey the RF interference from v_{DD} to v_{REG}.

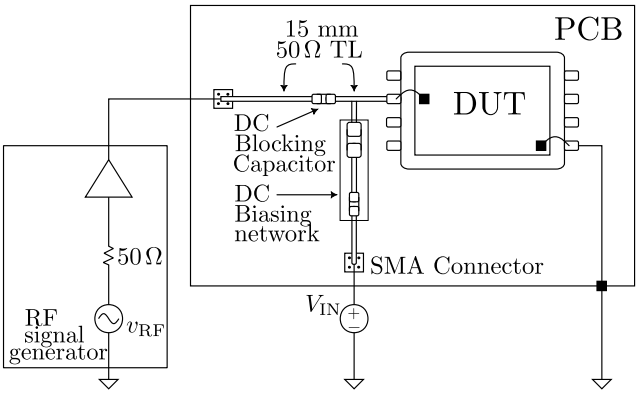

Fig. 4: Block diagram of the DPI test-board.

In the following section, the susceptibility of the two architectures is assessed and compared through time-domain analyses carried out within the DPI setup.

III. Simulation Setup and Results

To access the RFI immunity of an IC, the Direct Power Injection (DPI) procedure is widely employed. In this procedure, an RF disturbance is applied to one of the pins of the Device Under Test (DUT) through an injection network integrated on the same test board as the DUT. The guidelines for the DPI test board are described in the IEC 62132 standard [13], [14], and their main aspects are summarized in Fig. 4.

The injection network comprises a DC-blocking capacitor, and a DC-biasing network which prevents RF energy from coupling back into the power supply. For single-pin injection, the recommended value for the DC-blocking capacitor is 6.8 nF, while the impedance of the DC-biasing network must be greater than 400 Ω over the entire DPI frequency range. Moreover, the PCB trace form the RF injection port to the DC-blocking capacitor must be implemented as a 50 Ω transmission line. The standard also limits the length of the transmission line from the DC-blocking capacitor to the DUT pin to less than 15 mm.

A. DPI simulation setup

Starting from the DPI test-board configuration, an equivalent electrical model was constructed. As shown in Fig. 5, the simulation setup includes the voltage regulator and the injection network. Any decoupling capacitor was removed from the power supply input pin to maximize the coupling of EMI to the voltage regulator input [15].

1) The voltage regulator model includes the pre-regulator, the bandgap voltage reference, and the LDO. It provides a 3 V DC output voltage when supplied with a DC input in the 4 - 15 V range. In this work, the bandgap voltage reference is based on the topology proposed in [16], while the high-voltage output capacitor-less LDO

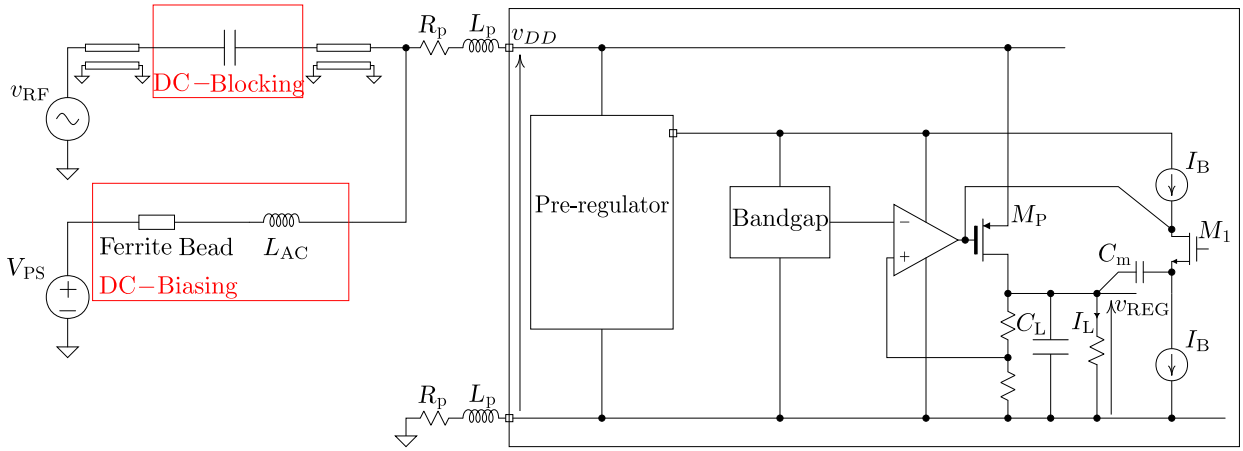

Fig. 5: Electrical model of the DPI test board.

TABLE I: VOLTAGE REGULATOR PARAMETERS

Parameter	Unit
V_{DD}	9 V
V_{PRE}	3 V
I_L^{max}	20 mA
V_{do}	1 V
UGF	1 MHz
PM_{min}	45°

is based on the design presented in [17]. The LDO is made stable by a Current Buffer Miller Compensation network, implemented with C_m and M_1, and an 80 pF on-chip output capacitor. The voltage regulator parameters are listed in Tab. I. Aiming to improve the results accuracy, a complete transistor-level schematic has been designed referring to the 0.35 µm technology [18]. Moreover, a package model accounting for the parasitic resistance R_p and inductance L_p of the bondwires and package pins is included.

2) The injection network model comprises the DC-blocking capacitor which is implemented through a 6.8 nF capacitor modeled by a series RLC equivalent circuit, and the DC-biasing network comprising a 47 µH inductor and a ferrite bead. The measurement-based models adopted for the inductor and the ferrite bead are the same as those characterized in [19]. The PCB traces between the 6.8 nF capacitor, the SMA connector, and the DUT input pin are modeled as two 15 mm-long, 50 Ω transmission lines on a 1.6 mm-thick FR-4 substrate.

B. Simulation Procedure

In the DPI procedure, the injected RF disturbance is applied to one of the DUT input pins and its amplitude is gradually increased until a failure is observed at the monitored output. In this work, a continuous-wave (CW) signal in the 1 MHz - 1 GHz frequency range, with frequency steps defined by IEC62132-1, is used as RF disturbance [13].

The regulated output v_{REG} is recorded under nominal conditions. Then, the CW signal with power gradually increasing from -20 dBm to 37 dBm in 1 dB steps is injected into the power supply pin of the DUT. For each power level, the regulated output v_{REG} is monitored. The failure criterion is defined as a fluctuation of 100 mV in the time-varying component of v_{REG}, which has a nominal DC value of 3 V.

C. Simulation Results

The DPI setup shown in Fig. 5, along with the procedure described above, was used to assess and compare the immunity of two voltage regulator architectures: one with a pre-regulator and the other employing the self-biasing technique.
Time-domain analyses were performed, and an example of the resulting waveforms is shown in Fig. 6. From the top to the bottom, the figure shows the power supply voltage affected by a 1 V, 10 MHz CW RFI disturbance, and the resulting output voltage of the pre-regulated LDO. As illustrated in Fig. 6, the voltage regulator demodulates the injected RFI in two main ways: (1) it introduces a DC offset superimposed on the nominal regulated voltage, and (2) it produces an AC disturbance superimposed onto the nominal output.
A comparison of the immunity levels of the two architectures is given in Fig. 7. The figure shows that the self-biasing technique reduces the susceptibility to RFI in almost the entire DPI frequency range, when compared with the same LDO employing the pre-regulator. As a representative case, the time-domain results for a 6 dBm CW signal at 10 MHz, the injected power level that triggers failure in the pre-regulated LDO, are analyzed. The analysis shows that the indirect path introduces a 60 mV DC offset together with a 65 mV AC disturbance appearing at v_{REG}. The direct path through the LDO power transistor M_p adds a further 3 mV DC offset and an AC disturbance with 22 mV amplitude. When subjected to the same disturbance, the self-biased LDO produces a 1.6 mV DC offset and a 26 mV AC disturbance, primarily due to direct coupling through M_p. Comparable reductions in both DC offset and AC disturbance are observed over the

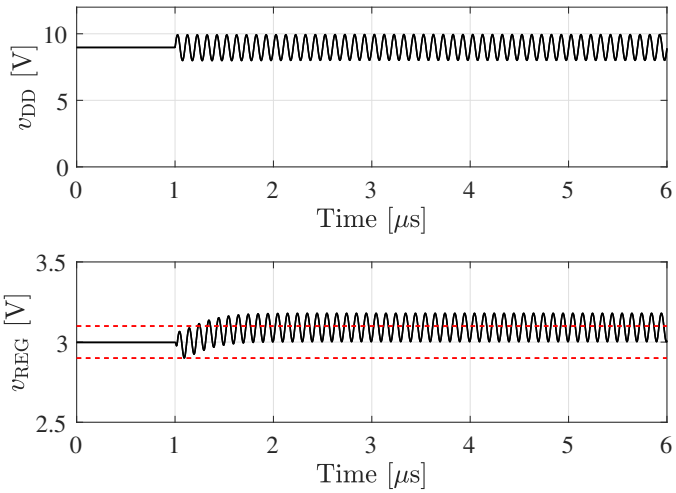

Fig. 6: Waveforms obtained from the time-domain analysis of the voltage regulator employing the pre-regulation network.

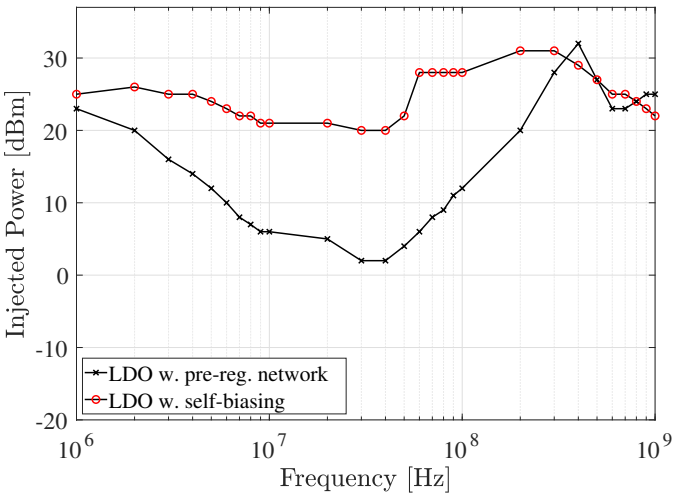

Fig. 7: Immunity results for the LDO voltage regulators. Device failure levels for the LDO with the pre-regulation network (crosses on the solid line) and for the LDO employing the self-bias technique (circles on the solid line).

full frequency range where the self-bias technique operates correctly highlighting the improved immunity of the voltage regulator.

IV. Conclusions

In this paper, the susceptibility of an LDO voltage regulator to RF disturbances injected at the power-supply pins has been analyzed. In particular, the role of the pre-regulator in propagating RFI through the entire LDO was investigated, showing that it conveys interference to the power supplies of the other circuits, thereby reducing the overall immunity. Furthermore, a self-biased LDO architecture was proposed as a solution to improve immunity. Its effectiveness was validated through time-domain analyses implementing the DPI procedure. The results demonstrate that the self-biased LDO withstands higher disturbance levels than the conventional design, confirming its enhanced immunity.

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