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Investigation on the Susceptibility of Operational Amplifiers to Switching Noise / Serra, J., Fiori, F.. - STAMPA. - (2026), pp. 1-4. (2026 Asia-Pacific International Symposium and Exhibition on Electromagnetic Compatibility (APEMC 2026) Kuala Lumpur (Mys) 4 - 7 May 2026) [10.1109/APEMC65388.2026.11593771].

Availability:
This version is available at: 11583/3010799 since: 2026-05-13T13:25:11Z

Publisher:
IEEE

Published
DOI:10.1109/APEMC65388.2026.11593771

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(Article begins on next page)

19 November 2026

Investigation on the Susceptibility of Operational Amplifiers to Switching Noise

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***Abstract*—This work deals with the susceptibility of operational amplifiers to the noise generated by the fast switching of power transistors. The problem is of high importance for any high density electronic circuits comprising power and analog sections, as it is for power ASICs. In such systems, the switching noise generated by the power section couples with the analog one although they are kept isolated. This is due to the parasitic coupling of such circuits through the package and through the silicon substrate they share. Such disturbances, not only affect the nominal signals at high frequency, meaning at the switching frequency and its harmonics, but also within the bandwidth of the analog channel. This is due to the demodulation of such disturbances, which results from the nonlinear characteristics of the device the analog circuits are made of. Specifically, this work focuses on the operational amplifiers, which are widely used in analog design. An integrated system comprising of a buck converter and a feedback operational amplifier, both integrated in the same silicon die is considered with the aim of evaluating the disturbance affecting the operational amplifier at the input, then a DPI test bench comprising a wide band arbitrary waveform generator is used to inject the switching noise resulted from the transient analyses. The results of the DPI immunity tests carried out with such a disturbance are compared with those obtained by injecting CW RFI.**

***Index Terms*—Susceptibility, electromagnetic interference, switching noise, operational amplifier, smart power, ASIC, integrated circuits.**

I. Introduction

In the last decades, advances in semiconductor technology have enhanced the integration of analog, digital, mixed-signal, and power devices on the same silicon die. By integrating multiple functions on a single die, manufacturers have reduced system-level component requirements while achieving continuous improvements in terms of switching frequency, power density and system integration.

On vice versa, the solutions to put in place for ensuring the intra compatibility of such complex systems has not been developed at the same pace. For instance, ICs like that shown in Fig. 1, which comprise a half-bridge, a digital core and an analog section having independent power supply usually suffer from the parasitic coupling of the different circuits through the silicon substrate [1], [2], [3], [4], in the sense that the operation of the analog section is affected by the switching noise generated by the power section because of the parasitic coupling through the substrate they share [5]. Similarly, in printed circuit board (PCB) or in system in a package (SiP), the analog section can be affected by the switching noise generated by the power section, because of the unwanted coupling among system interconnects (grounding and crosstalk issues) or external electromagnetic fields [6], [7], [8].

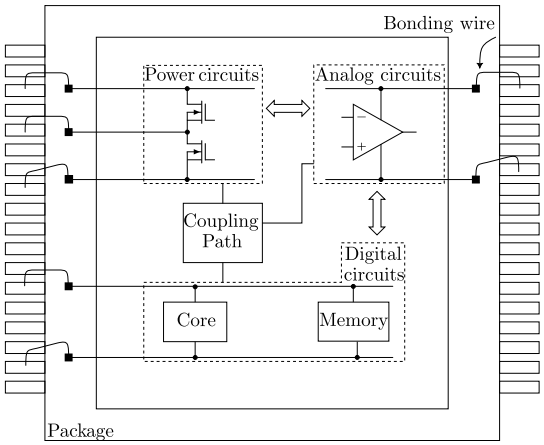


Fig. 1: Block diagram of a smart power IC.

This work presents an investigation aimed at evaluating the effect of pulsed interference on feedback operational amplifiers (OpAmps) such as those used for the conditioning of signals coming from sensors. The waveform of the switching noise affecting the OpAmp is obtained from the time domain analysis of a system like that shown in Fig. 1. Then, direct power injection (DPI) immunity tests are carried out as prescribed by IEC-62132-4, but the RF chain is replaced by a wide band arbitrary waveform generator (AWG), which replicates the waveform obtained from the time domain simulation.

The remainder of this paper is organized as follows. Section II analyzes, through time domain simulations, the substrate-coupled disturbances generated by a buck converter. Section III shows the test setup and the experimental results obtained from the DPI tests carried out on a commercial OpAmp. Concluding remarks are drawn in Section V.

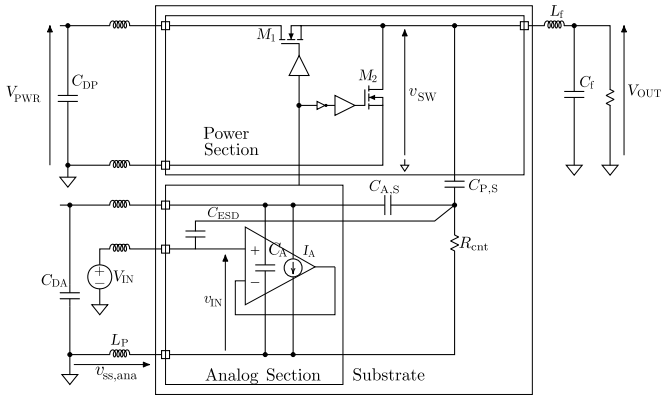


Fig. 2: Equivalent circuit used to obtain the switching waveform affecting the OpAmp.

TABLE I: Buck Converter Nominal Parameters

Parameter	Value
V_{PRW}	5 V
V_{OUT}	2.5 V
I_L	100 mA
f_{SW}	10 MHz
L_f	5 µH
C_f	5 nF

II. Evaluation of the Switching Noise Affecting OpAmps Embedded in ASICs

Wanting to evaluate the switching noise affecting an OpAmp belonging to a power ASIC, a simple system comprising a feedback OpAmp and the active components of a DC-DC converter is considered. Under nominal conditions, the buck converter provides V_{OUT} = 2.5 V from a 5 V power supply (V_{PWR}), with a load current ranging from 100 mA to 200 mA. The corresponding design parameters are summarized in Tab. I. In practice, only the switching leg of the converter is integrated on-chip, while the passive components required for its operation are implemented off-chip. The switching leg is implemented using the 0.35 µm CMOS technology [9]. It consists of two NMOS transistors (M_1 and M_2). As said, the noise generated by the switching leg is propagated to the OpAmp through the substrate. Therefore, the circuit in Fig. 2 comprises a rough model of the substrate, which aims to represents the worst case conditions. Indeed, the switching node is coupled with the substrate through $C_{P,S}$, the substrate is supposed to be equipotential and it is tied to the analog ground through an equivalent resistive contact R_{cnt}. No other shunt elements from the substrate to ground due to other blocks like the digital one are considered. The capacitive coupling of the analog power supply with the substrate is modeled by $C_{A,S}$. Finally, the package model as well as those of the off-chip components are included (stray elements are not shown in Fig. 2 for the sake of clarity).

The time domain analysis of such a circuit showed that the OpAmp is mostly affected by the voltage drop across the stray inductance L_P, which represents the lead-frame and the bonding wire connecting the analog ground to the PCB. The switching noise affecting the analog ground ($v_{ss,ana}$) resulted from the time domain analysis is shown in Fig. 3. In practice, the substrate coupling acts as a high-pass filter, allowing for the propagation of the high-frequency content of v_{SW} to the OpAmp input port. As a consequence, the nominal input signal (V_{IN}) is affected by narrow spikes of magnitude of several hundred millivolts and a duration of a few nanoseconds, at frequency f_{SW}.

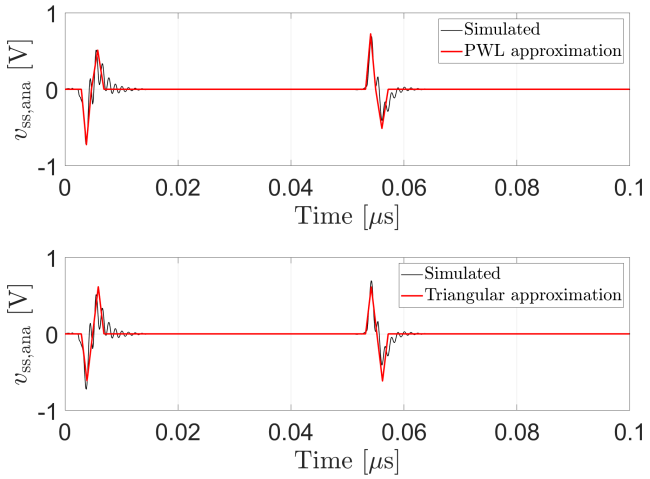


Fig. 3: Time domain analysis results. Induced analog ground disturbance (black solid line) and its PWL (top red solid line) and triangular (bottom red solid line) approximations.

The disturbance affecting the analog ground voltage can be approximated by (1) a piecewise-linear (PWL) waveform or by (2) a triangular-shaped one, as shown in Fig 3. The PWL waveform was defined aiming to preserve the energy, the maximum and the minimum values of each spike obtained from the simulation. In the triangular approximation, the positive and the negative spikes associated with each switching transition are modeled by two consecutive triangular pulses with equal rise/fall time (t_r) and amplitude (A). The parameter t_r is chosen so that each triangular pulse has the same duration as the corresponding spike in the PWL approximation, while A is chosen so that the energy of the triangular pulse matches that of the PWL approximation. Therefore, the triangular waveform can be expressed as

$$y(t) = \begin{cases} \dfrac{A}{t_r} t, & 0 \le t \le t_r, \\ \dfrac{A}{t_r}(2t_r - t), & t_r \le t \le 2t_r, \end{cases} \quad (1)$$

In the triangular approximation shown in Fig. 3, the parameters are A = 0.6 V and t_r = 1.25 ns, resulting in a total pulse duration of t_d = 5 ns.

To sum up, the switching noise generated by the buck converter and propagated through the substrate affects the OpAmp at its input, as if it were superimposed onto the nominal input signal (v_{IN}) directly. This means that, the susceptibility of an

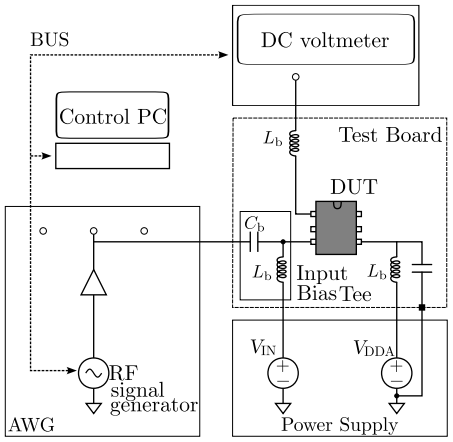


Fig. 4: Schematic view of the DPI setup considered to evaluate the susceptibility to EMI.

TABLE II: OpAmp Parameters

Parameter	Value
A_d	100 dB
SR	0.6 V / µs
GBW	1.1 MHz
CMRR	85 dB
V_{off}	1 mV

OpAmp to the switching noise can be evaluated referring to the direct power injection (DPI) setup, which is commonly used to check the immunity of ICs to RF interference.

III. Susceptibility of OpAmps to pulsed Interference

Usually, the susceptibility to EMI of operational amplifiers is investigated with the device connected in the voltage follower configuration and inserted in a test board like that prescribed by the IEC-62132 [10], which in turn is inserted in a test bench like that shown in Fig. 4. The interference is superimposed onto the nominal signals by means of coupling-decoupling networks (CDNs), known also as bias tees, (see L_b and C_b in Fig. 4). The interference is a CW or AM RF signal, which is injected into one of the DUT terminals through C_b. The nominal input signal (V_{IN}) and the power supply (V_{DDA}) are provided to the DUT through the CDN inductors. If the nominal input signal is a DC voltage V_{IN}, the output voltage is constant as well, therefore a DC voltmeter should be used to monitor the effect of the interference on the operation of the DUT.

It is known that CW RFI injected into the input terminal causes a DC output offset voltage, which amplitude depends on the magnitude and frequency of the RF interference [11], [12]. In [13] it has been shown that the such an offset is due to the demodulation of the RFI in the OpAmp input stage. Over the years, several authors investigated the susceptibility to RFI of OpAmps and proposed solutions aimed at increasing their immunity to EMI taking for granted that an OpAmp immune

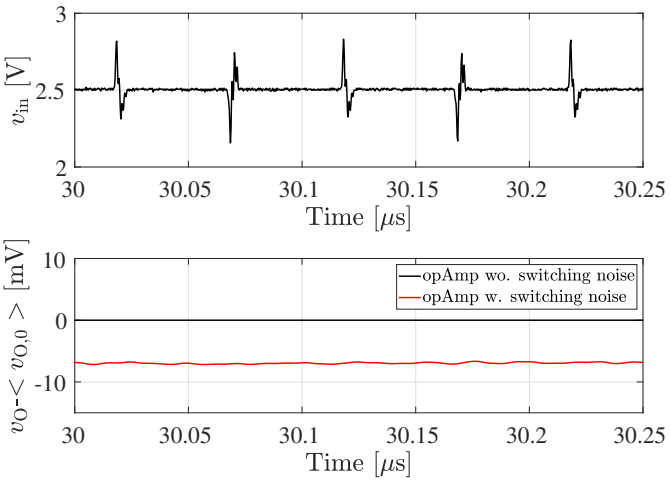


Fig. 5: Input voltage (plot on the top) of the OpAmp under measured with an oscilloscope while injecting the switching noise at the input. The output voltages shown in the bottom plot were obtained with (red) and without (black) interference.

to sinusoidal interference is also immune to a non sinusoidal one featuring the same magnitude and frequency [14], [15]. Wanting to check this implicit assumption, the DPI setup was modified replacing the RF source, meaning the RF generator and the RF amplifier, with an arbitrary waveform generator (AWG) capable of reproducing the noise waveforms presented above [16]. The main parameters of the commercial OpAmp considered in the present investigation are listed in Table II. Furthermore, the DPI tests were carried out referring to the susceptibility criterion

$$| < v_{O,wrf}(t) > - < v_{O,0}(t) > | \leq 5\text{mV} \qquad (2)$$

where, $< v_{O,0}(t) >$ is the average output voltage under nominal conditions, while $< v_{O,wrf}(t) >$ is the average output voltage in the presence of the switching disturbance.

The DPI setup was first used to evaluate the susceptibility of the OpAmp under test to the above shown pulsed interference obtaining time domain waveforms like those shown in Fig. 5. From top to bottom, the input voltage affected by the pulsed interference and the output voltage measured with an oscilloscope are shown. Specifically, the output voltage without interference is shown in black, that measured with the input affected by the pulsed interference is shown in red. Furthermore, Fig. 6 shows the resulting output offset voltage as the switching frequency is swept, highlighting the susceptibility of this amplifier to such disturbances. As the switching frequency increases, the offset rises with an almost quadratic trend. Furthermore, the two proposed approximations yield offset levels consistent with those obtained with the waveform resulted from the simulation. Interestingly, the results are close to one another but the triangular-shaped interference leads to the highest offset voltage across the entire frequency range.

The DPI test was also carried out as prescribed by the IEC 62132-4 standard, using the susceptibility criterion indicated in (2). The results are shown in Fig. 7 by the red circles. No

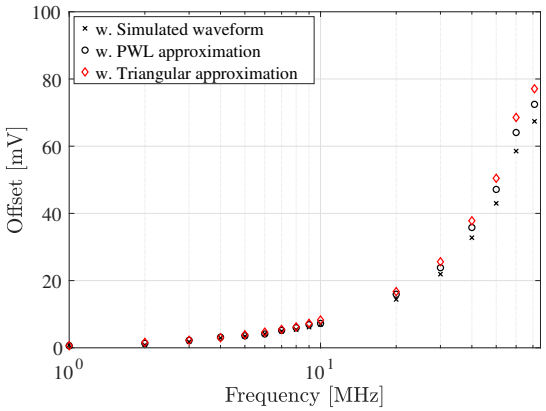


Fig. 6: Output offset voltage vs. frequency obtained while injecting at the OpAmp input the interference resulted from the simulation (black crosses), from the PWL approximation (black circles) and from the triangular-shaped waveform (red diamonds).

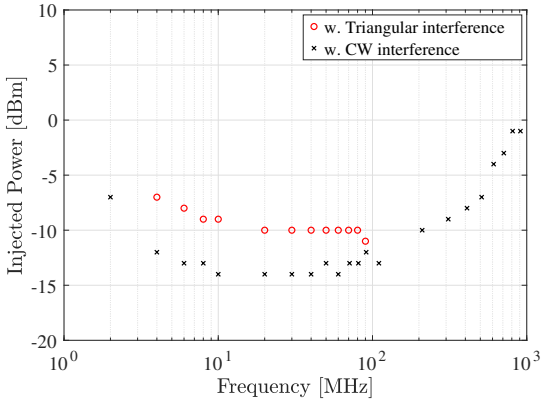


Fig. 7: DPI test results obtained with the CW RFI (black crosses) and the triangular-shaped interference (red circles). The susceptibility criterion is $v_{\text{off}} = 5$ mV.

results are reported above 100 MHz because the time duration of each triangular pulse is $t_{\text{d}} = 5$ ns and above that frequency subsequent pulses would overlap. Finally, the measurement was repeating injecting a CW RFI. The results are reported in the same figure by crosses. Interestingly, the DUT is less susceptible to triangular-shaped interference rather than CW one all over the frequency range of interest. This means that a triangular-shaped interference featuring the same power level and the same frequency of a CW one gives rise to a lower DC offset voltage.

IV. Conclusions

This work presented an investigation on the susceptibility of OpAmps to pulsed interference like that generated by switching power transistors. Time-domain simulations were carried out to obtain the switching waveform to be applied in the experimental tests to the input of a feedback OpAmp to evaluate its immunity. A piecewise-linear approximation and a triangular approximation were derived and used as disturbance to be applied in DPI tests to the input of a commercial OpAmp. The measurement results show that the OpAmp exhibits lower susceptibility to the switching noise interference than to CW interference featuring the same frequency and power level.

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