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08 October 2026

Reduced Output Swing Capacitance Multiplier for Common-Mode EMI Filtering in Traction Inverters

Markeljan Fishta, and Franco Fiori, *Member, IEEE*

***Abstract*—The transition from silicon to WBG-based designs in the automotive field has enabled increased power density, which, in turn, leads to a requirement of smaller and smaller Electromagnetic Interference (EMI) filters. In this context, Active and Hybrid EMI Filters (AEF/HEF) have become increasingly popular. However, when dealing with high-voltage systems, the required amplifier output voltage swing can be significant, requiring a high supply voltage, which leads to demanding design constraints. To tackle this issue, the present paper proposes a novel technique to decrease the amplifier output voltage swing. The technique is based on the suppression of the fundamental switching component, with the aid of a notch filter inserted in the interference sensing branch. The proposed technique is validated through experimental tests, showing that the amplifier output voltage swing is reduced by more than 4 times with respect to the conventional design.**

***Index Terms*—Active filters, Conducted emissions, Hybrid EMI filter, Notch filter, Traction inverter**

I. Introduction

RESEARCH on techniques to mitigate conducted Electromagnetic Interference (EMI) in switching converters has increased rapidly in the last years. The main driver of this development has been the transition from Silicon (Si) to Wide Band Gap (WBG) devices, which enables increased power density, making traditional Passive EMI Filters (PEFs) the bottleneck to system volume optimization [1], [2]. Indeed, in automotive inverters, like that represented in Fig. 1, the EMI filter is one of the bulkiest components, occupying potentially up to one third of the inverter volume [3]. In recent years, efforts have been made to decrease the EMI filter volume by mitigating EMI at the source [4], [5], [6], [7], [8], [9]. Another promising research line is the investigation of Active/Hybrid EMI Filters (AEFs/HEFs) [10]. Such filters perform interference sensing, which is elaborated to generate a suitable cancellation signal. The signal elaboration can take place in the analog [11], [12], [13], [14] or digital domain [15], [16], [17], [18]. AEFs are mainly effective at Low Frequency (LF), meaning that the attenuation required from the passive filter components decreases. As a consequence, the PEF cutoff frequency is relaxed and the resulting components, needed for compliance with regulations [19], are smaller. Depending on the sensed and injected quantity, four topologies can be identified for AEFs [10]. Among these, the topology based on Voltage Sensing Current Cancellation (VSCC) has become popular [20], [21], [22], since it does not require additional magnetic components to perform sensing and injection.

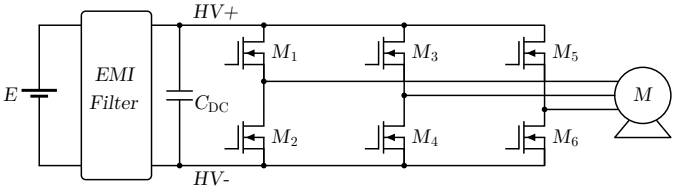

Fig. 1: Schematic representation of two-level power inverter, with input EMI filter.

In a practical implementation, the operation of the AEF is limited by aspects such as bandwidth and stability, which have been investigated in previous works [23], [24], [25]. However, in High-Voltage (HV) applications, the amplifier supply voltage is a critical parameter, as it should be sufficient to accommodate the required output swing. To avoid saturation of the amplifier, the required supply voltage can be significant, such as in [20] where a 60 V supply was used for the HEF in a 400 V converter, in [24] where a 30 V supply was used for the HEF in a 380 V converter, and [26] where a 100 V supply was used in a 380 V application. However, a high supply voltage results in increased design complexity, limited availability of suitable off-the-shelf active components, higher component cost at fixed performance and higher stress on the components. In [27] a technique was presented to improve the amplifier rejection of low-frequency components, mitigating the output voltage saturation, but the proposed circuit was not demonstrated within a real HV application.

The main contribution of the present paper is a novel AEF circuit with reduced amplifier output voltage swing. This, in turn, allows for supply voltage reduction, leading to less demanding design constraints. The remainder of this paper focuses on an overview of the VSCC-based HEF operation, in Sect. II. Then, in Sect. III, the analysis of the amplifier output voltage is performed, followed by the circuit implementation and design of the proposed technique, presented in Sect. IV. Sect. V presents the developed prototype and experimental validation of the proposed circuit. Concluding remarks are given in Sect. VI.

II. Common-Mode Hybrid EMI Filter

A conducted emissions testbench [19] employing a Common-Mode (CM) PEF is shown in Fig. 2(a), where a π topology is considered, while the two blocks to the right and to the left represent the inverter and the Line Impedance Stabilization Network (LISN), respectively. A CM equivalent

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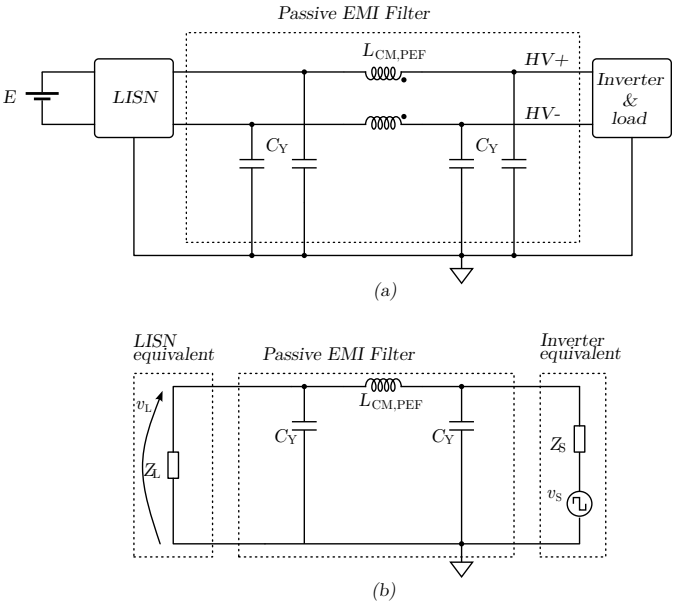

Fig. 2: (a) Conducted emission testbench with π PEF, (b) CM equivalent.

of the setup is given in Fig. 2(b). The CM interference source is represented by the Thévenin equivalent circuit $v_{\mathrm{S}}-Z_{\mathrm{S}}$, while the interference load by Z_{L}. The PEF is designed to provide an Insertion Loss (IL) higher than a target one, resulting from the emission spectrum excess with respect to the limit [19]. The filter IL is defined as

$$IL(s) = \frac{V_{\mathrm{l}}(s)}{V_{\mathrm{l}}'(s)} \tag{1}$$

where $V_{\mathrm{l}}(s)$ represents the voltage across Z_{L} prior to the EMI filter insertion, while $V_{\mathrm{l}}'(s)$ represents that after the EMI filter insertion. Assuming $Z_{\mathrm{L}} = R_{\mathrm{L}}$, $Z_{\mathrm{S}} = \frac{1}{sC_{\mathrm{S}}}$ and $C_{\mathrm{Y}} \gg C_{\mathrm{S}}$, for frequencies higher than the filter poles, it results

$$IL_{\mathrm{PEF}}(s) \simeq \frac{s^3 L_{\mathrm{CM,PEF}} C_{\mathrm{Y}}^2 R_{\mathrm{L}}}{1 + sR_{\mathrm{L}}C_{\mathrm{S}}}, \tag{2}$$

showing that the IL magnitude is proportional to the product $L_{\mathrm{CM}} \cdot C_{\mathrm{Y}}^2$. Since the inductor is the bulkiest component in the EMI filter, its value can be decreased by increasing that of the filter capacitors, at fixed IL. However, due to safety constraints [28] the maximum stored charge is limited to $0.2\,\mathrm{J}$, which limits the maximum CM capacitance, leading to larger inductance values required to comply with emission limits. The maximum allowed capacitance decreases with increasing inverter supply voltage, hence the limitation is critical in high-voltage applications.

To overcome this limitation, AEFs can be employed. The working principle of a VSCC AEF is illustrated in Fig. 3. The high-pass (HP) branch $C_{\mathrm{SEN}} - R_{\mathrm{SEN}}$ senses the interference voltage, v_{F}, which is amplified by an inverting amplifier with voltage gain $-G$. The amplifier drives the capacitor C_{INJ}, injecting the cancellation current. The equivalent impedance

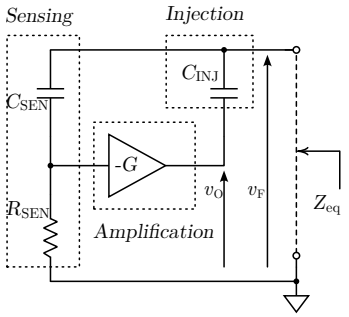

Fig. 3: Working principle of VSCC AEF.

of such a configuration, considering an amplifier with infinite input impedance and bandwidth, is given by

$$Z_{\mathrm{eq}}(s) = \frac{1 + sC_{\mathrm{SEN}}R_{\mathrm{SEN}}}{s(C_{\mathrm{SEN}} + C_{\mathrm{INJ}}) + s^2 R_{\mathrm{SEN}}C_{\mathrm{SEN}}C_{\mathrm{INJ}}(1+G)}. \tag{3}$$

For frequencies above the cutoff of the HP branch, and such that the impedance of C_{INJ} is much lower than R_{SEN}, i.e.,

$$f > \max\left\{\frac{1}{2\pi R_{\mathrm{SEN}}C_{\mathrm{SEN}}}, \frac{1}{2\pi R_{\mathrm{SEN}}C_{\mathrm{INJ}}}\right\}, \tag{4}$$

such an impedance can be approximated as

$$Z_{\mathrm{eq}}(s) \simeq \frac{1}{sC_{\mathrm{INJ}}(1+G)}, \tag{5}$$

which shows that, seen from the input port, the injection capacitance is boosted by a factor $(1+G)$.

The combination of the PEF with the AEF results in an HEF, which enables the filter volume reduction [29], overcoming the maximum CM capacitance limitation. Indeed, the AEF in Fig. 3 can replace some, or all, of the CM capacitors in the PEF. However, due to current stress constrains [25], it is better to employ the AEF at the second filter stage. This results in the schematic of Fig. 4(a). The sensing and injection capacitors are split, so that the circuit senses and compensates the CM interference. Its CM equivalent is shown in Fig. 4(b). The IL of the HEF must be designed so that it is larger or equal to that of the reference PEF, and it can be derived from (2), by letting one $C_{\mathrm{Y}} \to (1+G)C_{\mathrm{INJ}}$,

$$IL_{\mathrm{HEF}}(s) \simeq \frac{s^3 L_{\mathrm{CM,HEF}} C_{\mathrm{Y}}(1+G)C_{\mathrm{INJ}}R_{\mathrm{L}}}{1 + sR_{\mathrm{L}}C_{\mathrm{S}}}. \tag{6}$$

Furthermore, assuming $C_{\mathrm{INJ}} = C_{\mathrm{Y}}$, and imposing that

$$|IL_{\mathrm{HEF}}(\omega)| \geq |IL_{\mathrm{PEF}}(\omega)| \tag{7}$$

one gets

$$L_{\mathrm{CM,HEF}} \geq \frac{L_{\mathrm{CM,PEF}}}{1+G} \tag{8}$$

effectively reducing the required CM inductance by a factor $(1+G)$. The remainder of this paper deals with the amplifier employed in the VSCC AEF, more specifically with the swing of its output voltage v_{O}.

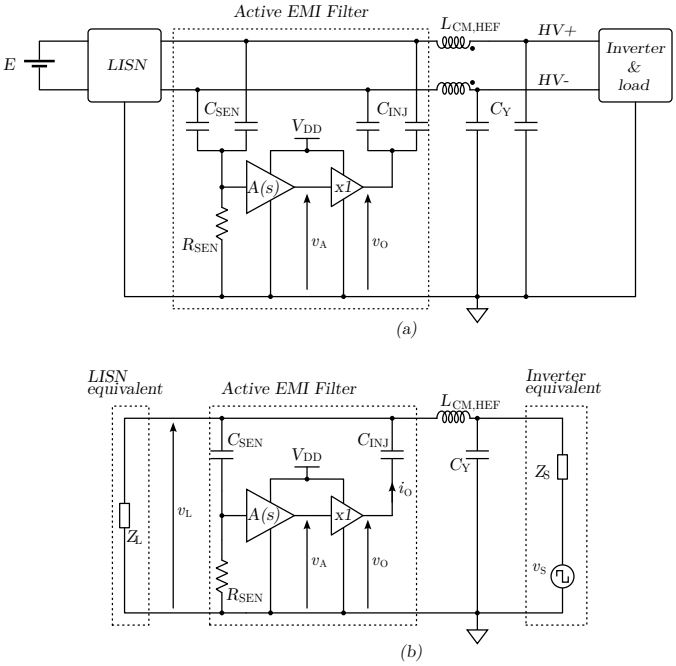

Fig. 4: (a) Conducted emission testbench with π HEF, (b) CM equivalent.

TABLE I: Reference parameters.

Param.	Value	Unit	Param.	Value	Unit
E	400	V	f_{sw}	32	kHz
C_S	10	nF	t_r	100	ns
C_Y	200	nF	L_{CM}	100	µH
C_{INJ}	200	nF	G	10	
T_H	$T_{SW}/2$		f_H	1	MHz

III. Amplifier Output Voltage Analysis

Aiming to evaluate the output voltage swing of the amplifier employed in the capacitance multiplier circuit, the schematic of Fig. 4(b) is considered. The amplifier is modeled with the frequency-dependent gain

$$A(s) = -\frac{G}{1+\frac{s}{2\pi f_H}} \tag{9}$$

where G represents the in-band amplification factor and f_H the dominant pole of the amplifier. The interference source impedance is assumed as capacitive (C_S). The load impedance represents the CM equivalent impedance of the LISN and is considered $Z_L = 25\,\Omega$ in this analysis. It is assumed that the interference voltage $v_S(t)$, which represents the CM voltage at the output of the inverter, has a trapezoidal shape, with amplitude E, period $T_{sw} = \frac{1}{f_{sw}}$, pulse duration T_H, and rise and fall times t_r. Assuming that, in band

$$V_O(s) \simeq A(s)V_L(s), \tag{10}$$

the amplifier output voltage can be written as a function of the disturbance source, as

$$\begin{aligned} V_O(s) &= \frac{A(s)\cdot V_S(s)}{1+\frac{(1+sC'_S Z_{LCM})(1+sC_{INJ}[Z_L(1-A(s))])}{sC'_S Z_L}} \\ &= H(s)\cdot V_S(s) \end{aligned} \tag{11}$$

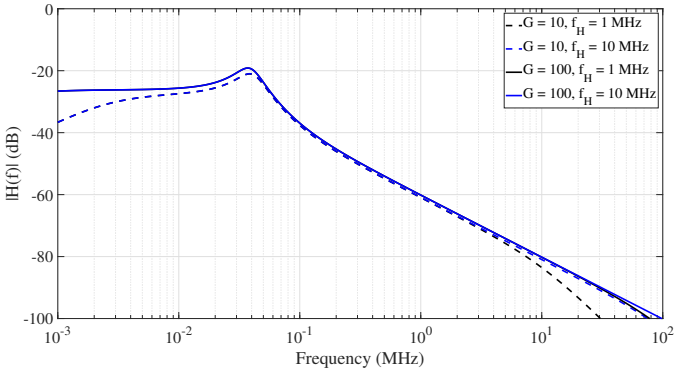

Fig. 5: Magnitude of $H(f)$ for parameters in Table I, as the amplifier gain and bandwidth are modified.

where Z_{LCM} represents the impedance of the CM choke, $C'_S = C_Y + C_S$, and $V_O(s)$, $V_L(s)$, $V_S(s)$ are the Laplace transform of $v_O(t)$, $v_L(t)$, $v_S(t)$, respectively. The magnitude behavior of the transfer function $H(f)$ for the reference parameters of Table I, as the amplifier gain and bandwidth are modified, is given in Fig. 5. The transfer function results in magnitude peaking around 40 kHz, which is nearly independent from the amplifier gain and bandwidth.

Concerning the disturbance voltage, since it is assumed to be trapezoidal, it can be expanded in Fourier series [30] as

$$v_S(t) = c_0 + \sum_{n=1}^{\infty} |c_n^+| \sin\left(2\pi n f_{sw} + \angle c_n\right) \tag{12}$$

where

$$c_0 = E\frac{T_H}{T_{sw}}, \tag{13}$$

$$|c_n^+| = 2E\frac{T_H}{T_{sw}}\left|\frac{\sin\left(n\pi T_H/T_{sw}\right)}{n\pi T_H/T_{sw}}\right|\left|\frac{\sin\left(n\pi t_r/T_{sw}\right)}{n\pi t_r/T_{sw}}\right|, \tag{14}$$

$$\angle c_n = \pm n\pi\frac{T_H + t_r}{T_{sw}} \tag{15}$$

for $n > 0$. From the Fourier coefficients of the source voltage, knowing the transfer function $H(s)$, the amplifier output voltage can be expressed as

$$v_O(t) = \sum_{n=1}^{\infty} A_n \sin\left(2\pi n f_{sw} + B_n\right) \tag{16}$$

with

$$\begin{aligned} A_n &= |c_n^+|\cdot|H(2\pi n f_{sw})| \\ B_n &= \angle c_n + \angle H(2\pi n f_{sw}). \end{aligned} \tag{17}$$

The magnitude of the harmonic components is plotted in Fig. 6, for the disturbance source voltage, $v_S(t)$, and for the amplifier output voltage, $v_O(t)$, considering the parameters of Table I. Due to the assumed symmetry of the waveform, i.e., $T_H = \frac{T_{sw}}{2}$, only the odd harmonics are present. The amplifier output voltage presents a decreasing spectral amplitude, as the frequency increases, meaning that the waveform swing is dominated by the first N_{max} components. Such an observation

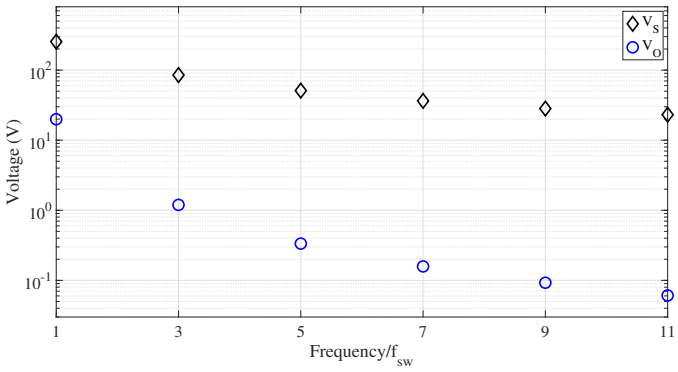

Fig. 6: Harmonic components of $v_{\mathrm{S}}(t)$ and $v_{\mathrm{O}}(t)$, for parameters in Table I.

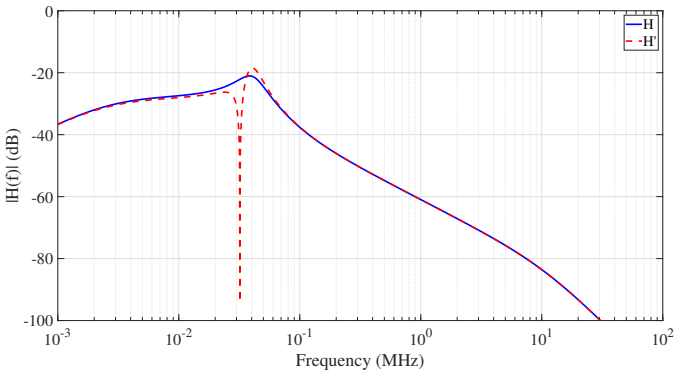

Fig. 7: Magnitude of $H(f)$ and $H'(f)$ for parameters in Table I.

allows for a simplified evaluation of the output voltage in the time domain, using the truncated series

$$v_{\mathrm{O}}(t) \simeq \sum_{n=1}^{N_{\max}} A_{\mathrm{n}} \sin\left(2\pi n f_{\mathrm{sw}} + B_{\mathrm{n}}\right) \tag{18}$$

where $N_{\max}$ is picked such that the contribution of the last harmonic has an arbitrarily small effect on the total waveform. In formulae

$$\frac{A_{\mathrm{n}}}{A_1} < \epsilon, \frac{C_{\mathrm{n}}}{C_1} < \epsilon, \forall n \geq N_{\max}, \tag{19}$$

with ϵ being an arbitrary constant. The output voltage was evaluated by means of (18) for different values of $N_{\max}$, and compared with time-domain simulation results. The voltage swing resulting from the simulation was $v_{\mathrm{o,pp}} = 38.8\,\mathrm{V}$, while the one evaluated by means of (18), with $N_{\max} = 3$, resulted in a relative error of $0.17\,\%$, confirming that the amplifier output voltage swing is dominated by the lower harmonic components of the switching waveform.

However, one can notice that EMC standards [19] require the conducted emissions to be below the limit in a specific frequency range. For current generation traction inverters, for high-efficiency operation, the fundamental switching frequency f_{sw} is usually below the lower limit of the regulated band, i.e. $150\,\mathrm{kHz}$. For this reason, this work proposes to suppress the fundamental switching component, ensuring that the AEF does not compensate it. This reduces the amplifier's output swing and, consequently, the required supply voltage for correct operation. To suppress the fundamental switching component, the frequency response of the amplifier, $A(s)$, is modified by multiplying it with a notch response like

$$H_{\mathrm{N}}(s) = \frac{\omega_0^2 + s^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{20}$$

where ω_0 is the center frequency and Q is the quality factor. In order to obtain the desired operation, it must be $\omega_0 = 2\pi f_{\mathrm{sw}}$. By doing so, a modified frequency response is obtained for the amplifier, as

$$A'(s) = A(s) \cdot H_{\mathrm{N}}(s), \tag{21}$$

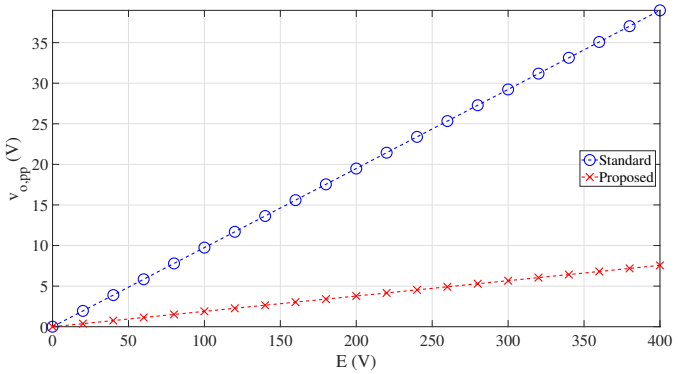

Fig. 8: Output voltage swing, from SPICE simulation, before and after inclusion of the notch filter transfer function in the amplifier transfer function, as the interference amplitude is increased.

which leads to a modified transfer function from the disturbance source to the amplifier output voltage

$$H'(s) = \frac{A'(s)}{1 + \frac{\left(1+sC'_{\mathrm{S}}Z_{\mathrm{LCM}}\right)\left(1+sC_{\mathrm{INJ}}[Z_{\mathrm{L}}(1-A'(s))]\right)}{sC'_{\mathrm{S}}Z_{\mathrm{L}}}}. \tag{22}$$

A comparison of the transfer functions is shown in Fig. 7. The magnitude of the two transfer functions is roughly the same everywhere, except for the frequencies near f_{sw}, where the notch is positioned, indicating the suppression of the switching component in the amplifier output voltage. SPICE simulations of the circuit in Fig. 4(b) were carried out for the reference parameters in Table I, as E was swept, for the cases prior and after the inclusion of the notch response. The two cases are named *standard* and *proposed*, respectively, hereinafter. The simulation results given in Fig. 8 show that the output voltage swing results proportional to the interference amplitude for both cases. The *proposed* case yields a voltage swing nearly five times smaller than the *standard* case.

IV. Circuit Implementation

Following the theoretical analysis presented in the previous section, which derived the improvement achievable through the proposed technique, this section presents the circuit implementation of the AEF for both the *standard* and *proposed*

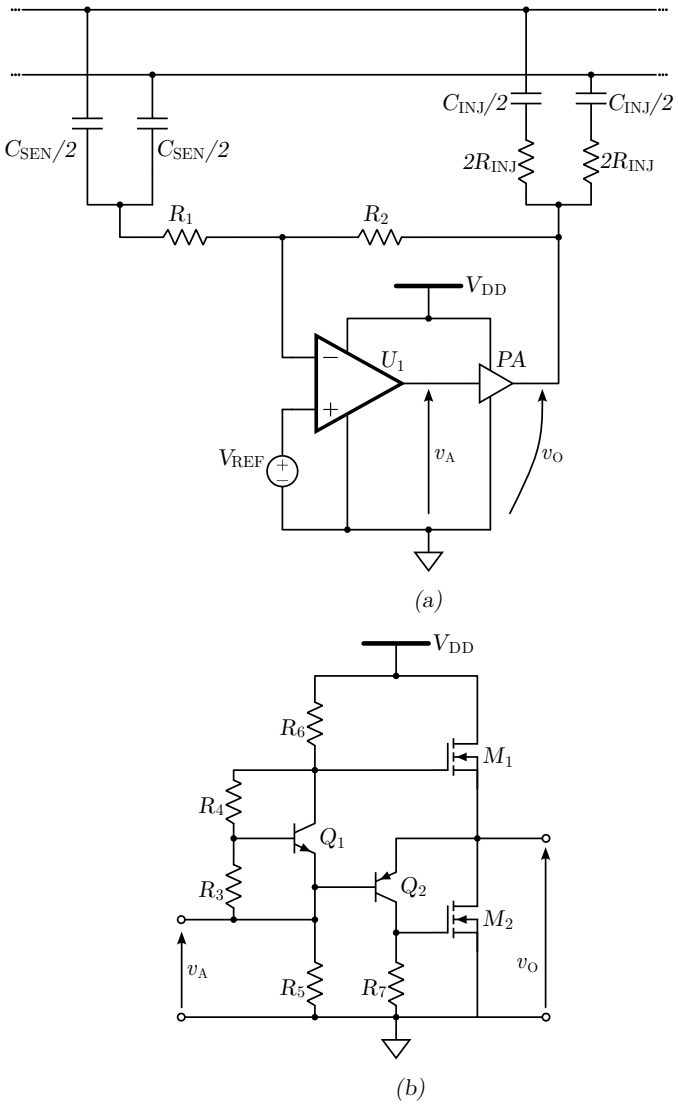

Fig. 9: Circuit implementation of (a) *standard* VSCC AEF and (b) output power stage.

topologies. The circuit schematics are presented and the implementation details are discussed with emphasis on the relation between component values and equivalent impedance and stability.

A. Standard circuit implementation and analysis

The AEF shown in Fig. 4(a) is implemented by means of the circuit represented in Fig. 9(a). The amplifier is realized by using an operational amplifier U_1, followed by an output stage PA, in inverting configuration. The sense resistance is represented by the input resistance of the closed-loop amplifier, i.e., $R_{\rm SEN} = R_1$. The circuit implementation of the output power stage is shown in Fig. 9(b). It is implemented as a push-pull voltage follower, used to boost the output current capability of the OpAmp. The open-loop gain of the complete amplifier, OpAmp and PA, is approximated as a single-pole response

$$A_{\rm d}(s) = \frac{A_{\rm d0}}{\left(1 + \frac{s}{2\pi f_{\rm P1}}\right)} \tag{23}$$

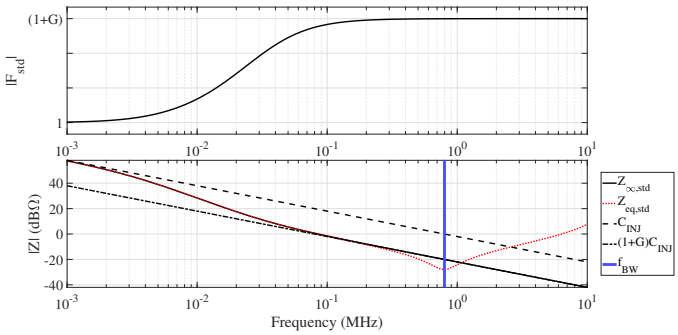

Fig. 10: (Top) Frequency-dependent capacitance multiplication factor and (bottom) equivalent CM input impedance for the *standard* circuit.

where $A_{\rm d0}$ is the DC gain, $f_{\rm P1} = \frac{f_{\rm U}}{A_{\rm d0}}$ is the dominant pole frequency and $f_{\rm U}$ is the unity-gain frequency. Furthermore, it is assumed that the output stage, PA, has an equivalent output resistance r_0. The noninverting input of the amplifier is biased at $V_{\rm REF} = \frac{V_{\rm DD}}{2}$ to maximize the output range. The CM interference sensing is performed by means of two capacitors with value $C_{\rm SEN}/2$ and the injection is performed through two capacitors with value $C_{\rm INJ}/2$, each with a series resistor $2R_{\rm INJ}$. The equivalent CM impedance of the circuit can be evaluated by shorting the two input terminals, and using the Blackman's theorem [31]

$$Z_{\rm eq,std} = Z_{\infty,\rm std}\frac{1 + \frac{1}{T_{\rm SC,std}}}{1 + \frac{1}{T_{\rm OC,std}}}. \tag{24}$$

Such a formula allows one to write the equivalent impedance as an ideal term, $Z_{\infty,\rm std}$ assuming that the gain of the amplifier goes to infinity, multiplied by a corrective factor that accounts for the amplifier nonidealities, i.e, its bandwidth limitation and nonzero output resistance. In particular, $T_{\rm OC,std}$ is the return ratio with the impedance calculation port in open circuit and $T_{\rm SC,std}$ is the return ratio with the impedance calculation port in short circuit. Performing the calculations yields

$$Z_{\infty,\rm std}(s) = \frac{1 + sR_1C_{\rm SEN}}{s(C_{\rm SEN} + C_{\rm INJ}) + s^2C_{\rm SEN}C_{\rm INJ}(R_1 + R_2)} \tag{25}$$

and, assuming $C_{\rm INJ} \gg C_{\rm SEN}$

$$Z_{\infty,\rm std}(s) \simeq \frac{1}{sC_{\rm INJ}F_{\rm std}(s)} \tag{26}$$

where

$$F_{\rm std}(s) = \left[1 + \left(\frac{sR_2C_{\rm SEN}}{1 + sR_1C_{\rm SEN}}\right)\right] \tag{27}$$

is the frequency-dependent capacitance multiplication factor, for an ideal amplifier. The behavior of such a term is represented in Fig. 10 for the parameter values given in Table II. At low frequency, the capacitance multiplication factor tends to 1, since the HP sensing network is below cutoff. At high frequency, the factor tends to $\left(1 + \frac{R_2}{R_1}\right)$, from which $G = \frac{R_2}{R_1}$

TABLE II: Reference parameters.

Param.	Value	Unit	Param.	Value	Unit
R_1	2.4	kΩ	R_2	22	kΩ
$C_{\rm SEN}$	2	nF	$C_{\rm INJ}$	200	nF
$A_{\rm d0}$	1e5		$f_{\rm U}$	16	MHz
r_0	2	Ω	Q	0.68	
f_0	32	kHz	$V_{\rm DD}$	20	V

can be determined. To include the amplifier nonidealities, the two return ratios are evaluated as

$$T_{\rm SC,std} \simeq \frac{R_1 A_{\rm d}(s)}{R_1+R_2+r_0\left(1+\frac{C_{\rm INJ}}{C_{\rm SEN}}\right)+sr_0C_{\rm INJ}\left(R_1+R_2\right)}$$
$$T_{\rm OC,std} = A_{\rm d}(s). \tag{28}$$

The approximation of $T_{\rm SC,std}$ assumes $f > \frac{1}{2\pi R_1 C_{\rm SEN}}$, which is reasonable since the corrective term intervenes at high frequency, where the amplifier open-loop gain decreases. The equivalent impedance has the desired behavior,

$$Z_{\rm eq,std} \simeq Z_{\infty,\rm std} \tag{29}$$

up to a frequency

$$f_{\rm BW} = \sqrt{\frac{f_{\rm U}}{2\pi r_0 C_{\rm INJ}(1+G)}} \tag{30}$$

[25], resulting in equivalent series inductance

$$ESL = \frac{r_0}{2\pi f_{\rm U}}. \tag{31}$$

The impedance behavior is represented in Fig. 10, where a good agreement results between $f_{\rm BW}$ and the resonance point of $Z_{\rm eq,std}$. At low frequency, $Z_{\rm eq,std}$ is close to the impedance of $C_{\rm INJ}$, while at high frequency, up to $f_{\rm BW}$, it is close to that of $(1+G)C_{\rm INJ}$, achieving the desired amplification.

B. Proposed circuit implementation and analysis

To reduce the amplifier output voltage swing, the *proposed* circuit given in Fig. 11(a) is obtained from the *standard* one, by inserting a notch filter in the sensing branch. This way the amplifier does not compensate the frequency component at which the notch filter is tuned. The circuit implementation of the notch filter is given in Fig. 11(b). Such a topology is known as Fliege [32] and the addition of a buffer at its input ensures that the notch circuit presents high input impedance, avoiding central frequency variation due to the upstream impedance. Furthermore, the topology presents low output impedance resulting in good impedance decoupling. The addition of the resistor R_1 towards GND maintains the same cutoff frequency for the HP sensing network and the same nominal gain of the amplifier. To suppress the fundamental switching frequency, the notch must be designed so that its central frequency $f_0 = f_{\rm sw}$. Moreover, the quality factor should be selected so that the notch response does not interfere with the desired impedance behavior in the regulated frequency band. Knowing that the $-3\,{\rm dB}$ frequencies of the notch filter are at

$$f_{-3\,\rm dB} = f_0\left(\sqrt{1+\frac{1}{4Q^2}} \pm \frac{1}{2Q}\right) \tag{32}$$

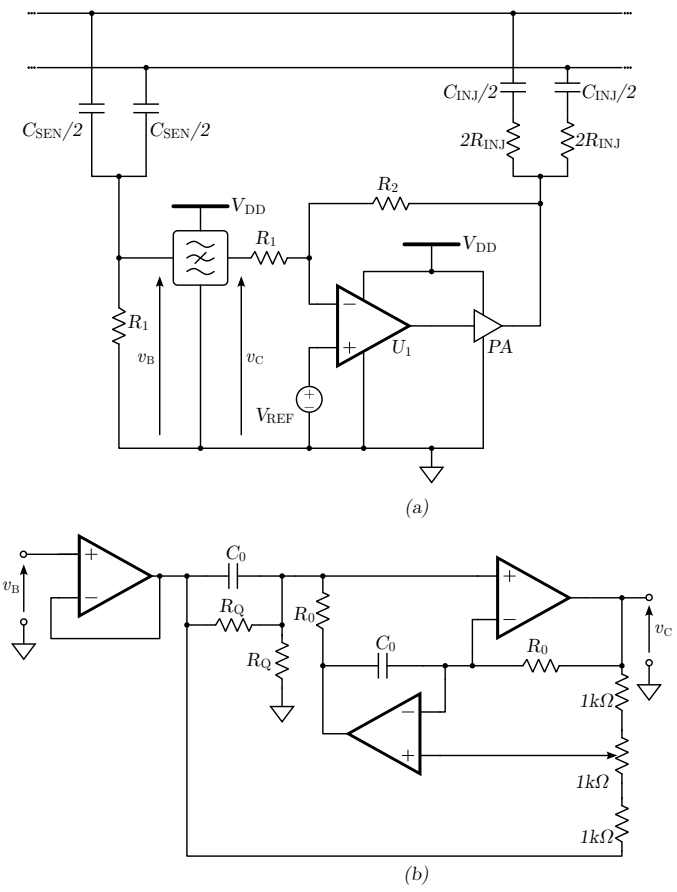

Fig. 11: Circuit implementation of (a) *proposed* VSCC AEF and (b) notch filter.

the quality factor should be designed so that

$$f_0\left(\sqrt{1+\frac{1}{4Q^2}}+\frac{1}{2Q}\right) < 150\,{\rm kHz}. \tag{33}$$

Such a constraint translates to $Q > 0.23$ at $f_0 = 32\,{\rm kHz}$. The parameters can be fixed through the component values according to the following relations

$$f_0 = \frac{1}{2\pi R_0 C_0}$$
$$Q = \frac{R_{\rm Q}}{2R_0}. \tag{34}$$

In automotive traction inverters, the switching frequency might vary with motor speed to optimize dynamic response and efficiency. In such cases the central frequency of the notch filter must track the inverter switching frequency to achieve the desired operation. Central frequency tuning in the application can be obtained by employing programmable resistors [33] in place of R_0. The equivalent CM impedance of the circuit is evaluated by shorting the two inputs and using the Blackman's formula [31]

$$Z_{\rm eq,prd} = Z_{\infty,\rm prd}\frac{1+\frac{1}{T_{\rm SC,prd}}}{1+\frac{1}{T_{\rm OC,prd}}}. \tag{35}$$

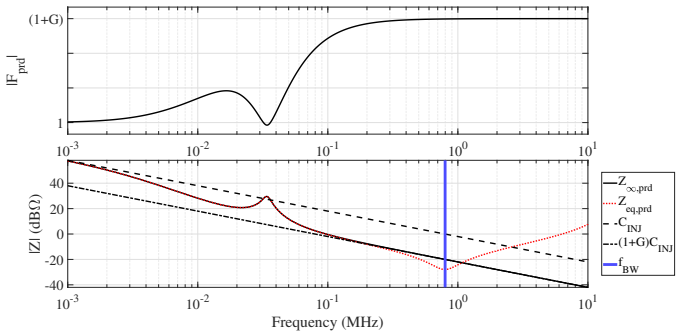

Fig. 12: (Top) Frequency-dependent capacitance multiplication factor and (bottom) equivalent CM input impedance for the *proposed* circuit.

Performing the calculations yields

$$Z_{\infty,\mathrm{prd}}(s) = \frac{1 + sR_1C_{\mathrm{SEN}}}{s(C_{\mathrm{SEN}} + C_{\mathrm{INJ}}) + s^2C_{\mathrm{SEN}}C_{\mathrm{INJ}}(R_1 + H_{\mathrm{N}}R_2)} \tag{36}$$

and, assuming $C_{\mathrm{INJ}} \gg C_{\mathrm{SEN}}$

$$Z_{\infty,\mathrm{prd}}(s) \simeq \frac{1}{sC_{\mathrm{INJ}}F_{\mathrm{prd}}(s)} \tag{37}$$

where

$$F_{\mathrm{prd}}(s) = \left[1 + H_{\mathrm{N}}(s)\left(\frac{sR_2C_{\mathrm{SEN}}}{1 + sR_1C_{\mathrm{SEN}}}\right)\right] \tag{38}$$

is the frequency-dependent capacitance multiplication factor, for an ideal amplifier. The behavior of such a term is represented in Fig. 12. At low frequency, the capacitance multiplication factor tends to 1, since the HP sensing network is below cutoff, while at high frequency the factor tends to $(1+G)$. Differently from the *standard* case, the multiplication factor drops sharply around the notch frequency f_0. To include the amplifier nonidealities, the two return ratios are evaluated as

$$\begin{aligned} T_{\mathrm{SC,prd}} &= \frac{R_1A_{\mathrm{d}}(s)}{R_1 + R_2 + r_0 + sr_0C_{\mathrm{INJ}}\,(R_1 + R_2)} \\ T_{\mathrm{OC,prd}} &\simeq A_{\mathrm{d}}(s). \end{aligned} \tag{39}$$

The approximation of $T_{\mathrm{OC,prd}}$ assumes $f > \frac{1}{2\pi R_1C_{\mathrm{SEN}}}$ and $f > f_0$, which is reasonable since the corrective term intervenes at high frequency, where the amplifier open-loop gain decreases. The impedance behavior is represented in Fig. 12, where it can be observed that it inherits the same behavior as the *standard* case for frequencies far from f_0. Around f_0, the equivalent impedance has a sharp increase, due to the notch filter inserted in the sensing branch.

C. Stability analysis

The stability of the AEF is evaluated, considering the effect of the LISN, inverter and the passive filter components. Considering the *standard* case first, as shown in Fig. 13, the loop gain is calculated by opening the loop at the cross mark. The CM impedance of the LISN, as specified by [19], is denoted by Z_{L}, and it is given by

$$Z_{\mathrm{L}} = \left(R_{\mathrm{LISN}} + \frac{1}{sC_{\mathrm{LISN}}}\right) \parallel \left(sL_{\mathrm{LISN}} + \frac{1}{sC_{\mathrm{LISN}}}\right) \tag{40}$$

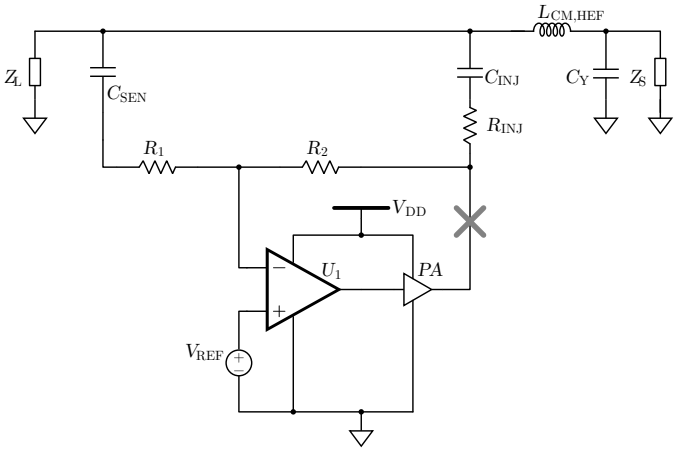

Fig. 13: Equivalent CM circuit for the stability analysis of the *standard* topology.

where the component values are defined by the standard [19]. The CM equivalent impedance of the inverter is denoted by Z_{S}. An equivalent impedance, connected between the input of the AEF and ground, can be evaluated as

$$Z_{\mathrm{SL}} = Z_{\mathrm{L}} \parallel \left[Z_{\mathrm{CM,HEF}} + \left(\frac{1}{sC_{\mathrm{Y}}} \parallel Z_{\mathrm{S}}\right)\right] \tag{41}$$

where $Z_{\mathrm{CM,HEF}}$ represents the equivalent impedance of the CM choke. The loop gain evaluation yields [34]

$$T_{\mathrm{std}} = T_{\mathrm{sc}} \cdot \frac{1 + \frac{Z_{\mathrm{SL}}}{Z_{\mathrm{N,std}}}}{1 + \frac{Z_{\mathrm{SL}}}{Z_{\mathrm{D}}}} \tag{42}$$

with

$$\begin{aligned} T_{\mathrm{sc}} &= A_{\mathrm{d}} \cdot \frac{Z_{\mathrm{SEN}}}{Z_{\mathrm{SEN}} + R_2 + r_0 \parallel Z_{\mathrm{INJ}}} \cdot \frac{Z_{\mathrm{INJ}}}{Z_{\mathrm{INJ}} + r_0} \\ Z_{\mathrm{N,std}} &= Z_{\mathrm{SEN}} \parallel \left(Z_{\mathrm{INJ}} \cdot \frac{Z_{\mathrm{SEN}}}{R_2 + Z_{\mathrm{SEN}}}\right) \\ Z_{\mathrm{D}} &\approx Z_{\mathrm{INJ}} + r_0 \end{aligned} \tag{43}$$

and $Z_{\mathrm{SEN}} = R_1 + \frac{1}{sC_{\mathrm{SEN}}}$, $Z_{\mathrm{INJ}} = R_{\mathrm{INJ}} + \frac{1}{sC_{\mathrm{INJ}}}$. Concerning the *proposed* circuit, the loop gain is evaluated in a similar manner, as

$$T_{\mathrm{prd}} = T_{\mathrm{sc}} \cdot \frac{1 + \frac{Z_{\mathrm{SL}}}{Z_{\mathrm{N,prd}}}}{1 + \frac{Z_{\mathrm{SL}}}{Z_{\mathrm{D}}}} \tag{44}$$

where

$$Z_{\mathrm{N,prd}} = Z_{\mathrm{SEN}} \parallel \left(Z_{\mathrm{INJ}} \cdot \frac{Z_{\mathrm{SEN}}}{H_{\mathrm{N}}R_2 + Z_{\mathrm{SEN}}}\right). \tag{45}$$

Both these expressions were evaluated for the parameters assumed in the present study, and their behavior is shown in Fig. 14. In the case of the *standard* circuit, the presence of Z_{SL} causes the loop gain magnitude to drop near its resonance frequency, leading to two additional crossover frequencies. However, near these frequencies, two complex zeros are followed by two complex poles, leading to a phase boost, which is beneficial for stability. Indeed, the phase margins result $\varphi_{\mathrm{m1,std}} = 115°$ and $\varphi_{\mathrm{m2,std}} = 137°$ at $f_{\mathrm{T1,std}} = 235.6\,\mathrm{kHz}$ and $f_{\mathrm{T2,std}} = 237.4\,\mathrm{kHz}$, respectively. In the case of the *proposed* circuit, a similar behavior can be observed, with

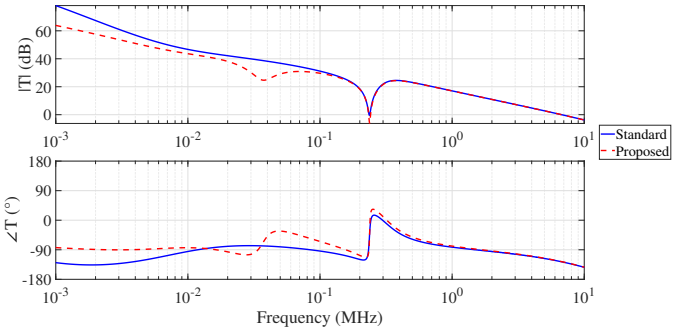

Fig. 14: Loop gain evaluation for the two circuits (a) magnitude and (b) phase.

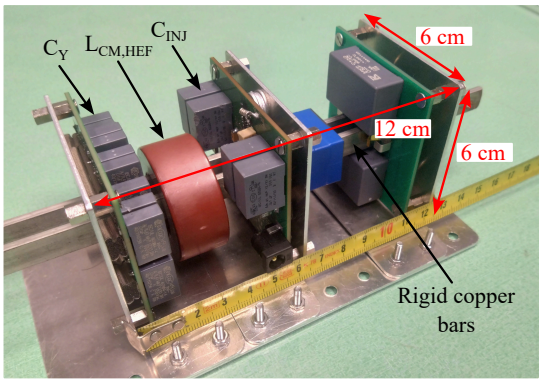

Fig. 15: Hybrid EMI filter prototype. The circuit can be reconfigured to include or exclude the notch filter.

phase margins $\varphi_{\mathrm{m1,prd}} = 83°$ and $\varphi_{\mathrm{m2,prd}} = 165°$ at $f_{\mathrm{T1,prd}} = 233.5\,\mathrm{kHz}$ and $f_{\mathrm{T2,prd}} = 241.4\,\mathrm{kHz}$, respectively. In addition, at lower frequencies, the loop gain magnitude of the *proposed* circuit shows a trough at around f_0 due to the notch filter. However, the loop gain at these frequencies is large so no cross-over occurs. Finally, both curves decrease with frequency, resulting in a cross-over around $f_{\mathrm{T3}} = 6.5\,\mathrm{MHz}$ with $\varphi_{\mathrm{m3}} = 56°$.

V. Experimental Results

A prototype HEF was built for validation purposes, as shown in Fig. 15. The HEF was designed for a rated current of $I = 150\,\mathrm{A}$, resulting in a required wire cross-section area of $30\,\mathrm{mm}^2$, with a maximum current density of $J = 5\,\mathrm{A/mm}^2$. This prevented the use of wound chokes, leading to the adoption of rigid copper bars with cross-section of $3\,\mathrm{mm} \times 10\,\mathrm{mm}$. The target attenuation was similar to that of an equivalent PEF, resulting in a decrease of the volume of the CM chokes by $50\,\%$. The magnetic core is mounted around the bars, while capacitors are placed on dedicated PCBs. The capacitance multiplier board has been designed so that the notch filter can be included or excluded, for comparison. The employed DM filter was a passive one, the same for both cases. First, small-signal measurements were performed for both circuits. The equivalent CM impedance of the AEF was measured by means of an impedance analyzer [35], and the results are given in Fig. 16. For comparison, the curves corresponding to $C_{\mathrm{INJ}} = 200\,\mathrm{nF}$ and to $(1+G)C_{\mathrm{INJ}} = 2\,\mu\mathrm{F}$ are represented. It results

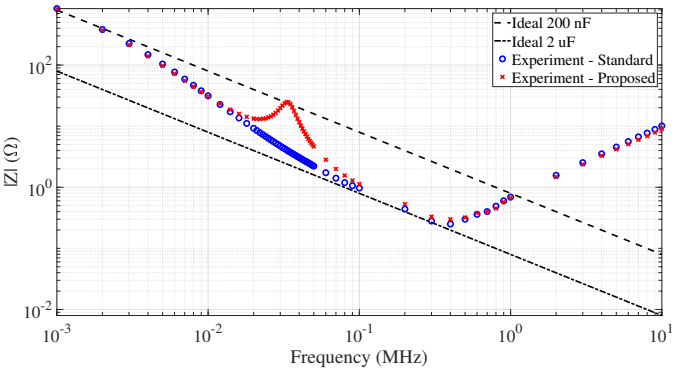

Fig. 16: CM equivalent impedance for both circuits.

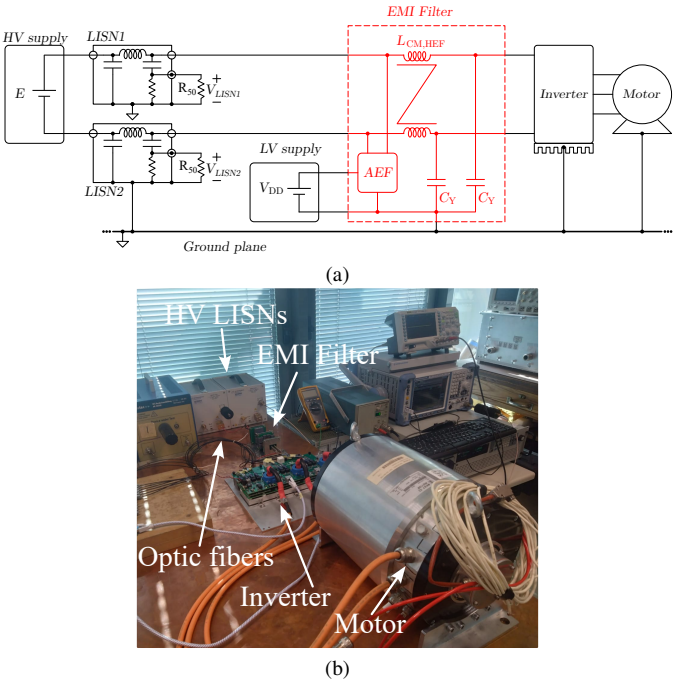

Fig. 17: Conducted emission measurement test bench (a) schematic and (b) picture.

that both filter versions, at low frequency, show an impedance close to that of C_{INJ}. As the frequency increases, the *standard* solution transitions smoothly towards an equivalent impedance close to that of $(1+G)C_{\mathrm{INJ}}$. The *proposed* filter, on the other hand, shows a narrowband impedance increase near f_{sw}, thanks to the presence of the notch filter, before transitioning towards the desired impedance. Subsequently, measurements were performed to assess the performance of the proposed HEF in the suppression of conducted CM EMI, employing the test setup of Fig. 17(a), a picture of which is shown in Fig. 17(b). A GaN inverter loaded by a motor, switching at $f_{\mathrm{sw}} = 32\,\mathrm{kHz}$ is employed. The inverter is supplied through two HV LISNs by a HV power supply. The LISNs, the HEF, the inverter and the motor are all grounded through the solid copper plane covering the table. Such a setup guarantees a low-impedance connection between the ground of the EMI filter, that of the inverter and that of the motor, ensuring a low-impedance path for the CM disturbance current. In the

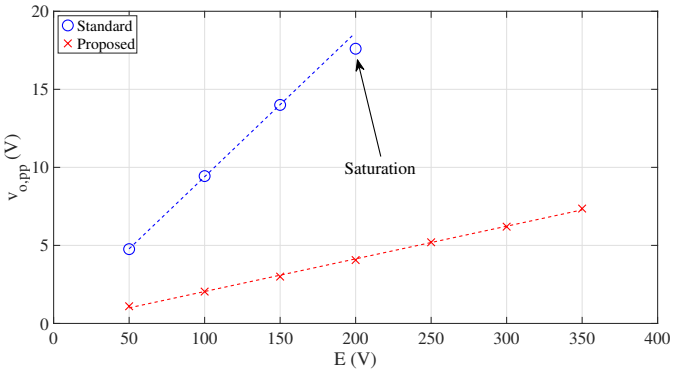

Fig. 18: Amplifier output voltage for both circuits. The markers represent measurement results while the dashed lines represent the best linear fit. In the case of the *standard* topology, the linear fit was performed on the first three points, as the fourth one coincides with amplifier output saturation.

application, the EMI filter and inverter are typically integrated within the motor enclosure, hence a low impedance connection among these components is achieved through the enclosure itself. First, the inverter supply voltage E was varied and the amplifier output voltage swing was measured. The measurement results are given in Fig. 18. In the figure, the markers represent measurements, while the dashed lines represent straight lines fitting the data. The *standard* topology operates correctly up to $E = 150\,\mathrm{V}$, while at $E = 200\,\mathrm{V}$ the output of the amplifier saturates due to the supply voltage limitation at $V_{\mathrm{DD}} = 20\,\mathrm{V}$. The *proposed* topology, on the other hand, presents a much smaller output voltage swing, thanks to the notch filter, operating correctly up to $E = 350\,\mathrm{V}$. It should be highlighted that the maximum value for E is limited for the inverter under consideration, while there is available headroom in the proposed AEF for higher E values. Furthermore, the behavior of the output voltage swing is nearly linear with E in both cases, confirming the initial theoretical analysis and resulting in a constant ratio between the output swing in the two cases. The time-domain behavior of output voltage with $E = 150\,\mathrm{V}$ and $E = 200\,\mathrm{V}$ is given in Fig. 19(a) and Fig. 19(b), respectively. In the case $E = 150\,\mathrm{V}$ both filters operate correctly. Besides the difference in the peak-to-peak value, already discussed, the output voltage of the *standard* filter is dominated by the fundamental switching component while that of the *proposed* filter is dominated by the second harmonic. In the case $E = 200\,\mathrm{V}$ the output of the *standard* filter saturates near the supply rails while the *proposed* filter operates correctly. Such saturation introduces nonlinear distortion and constitutes a limitation of the *standard* topology, as it may increase harmonic content in the conducted EMI spectrum. Conducted emissions at the LISNs were measured with the EMI receiver, and the results are presented in Fig. 20. The inverter was supplied with $E = 350\,\mathrm{V}$ and emissions were measured without the filter and with the *proposed* HEF. The HEF effectively attenuates the conducted interference with some attenuation levels given in Table III. Additionally, conducted EMI measurements were performed with both filters, for comparison. The results are given in

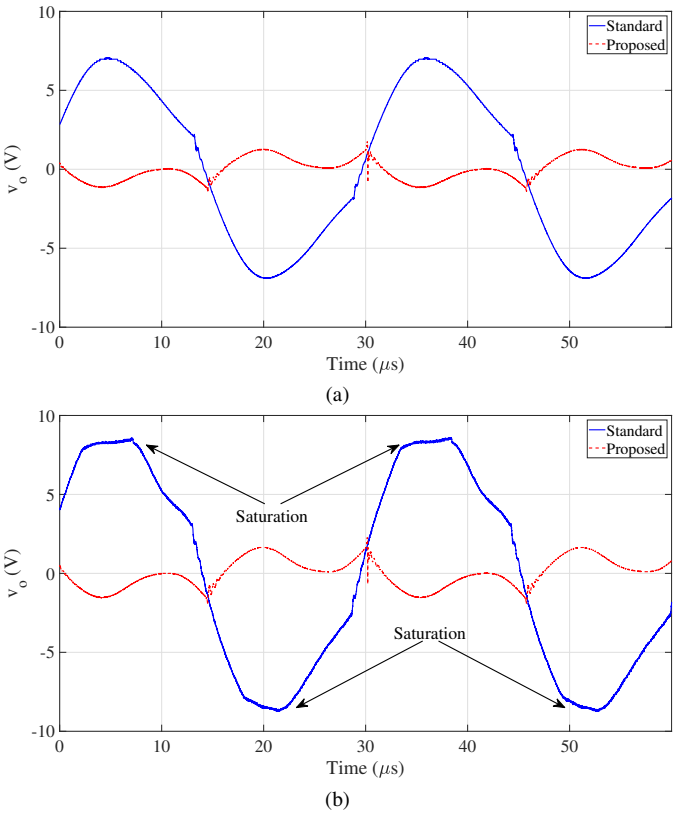

Fig. 19: Time-domain output voltage of the *standard* and *proposed* AEFs with (a) $E = 150\,\mathrm{V}$ and (b) $E = 200\,\mathrm{V}$.

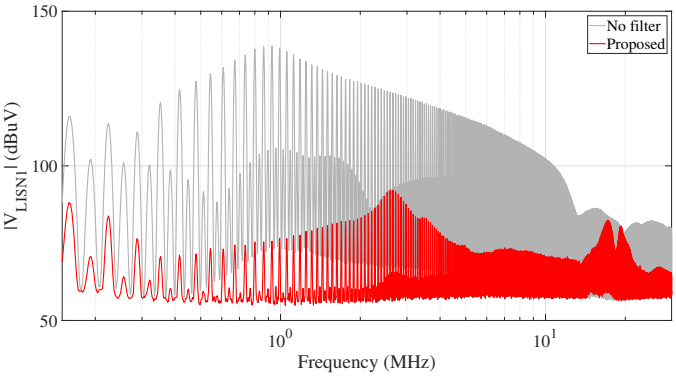

Fig. 20: Conducted emission measurement results with $E = 350\,\mathrm{V}$. The EMI receiver was configured with peak detector and $RBW = 9\,\mathrm{kHz}$ from $150\,\mathrm{kHz}$ to $30\,\mathrm{MHz}$.

TABLE III: Attenuation provided by the proposed EMI filter.

Frequency (MHz)	Attenuation dB
0.160	28
0.352	50
0.672	60
1.312	54
2.592	32
5.152	42
10.272	31
20.512	5.4

Fig. 21. In these measurements, the inverter was supplied with $E = 150\,\mathrm{V}$, which is the limit condition for the operation of

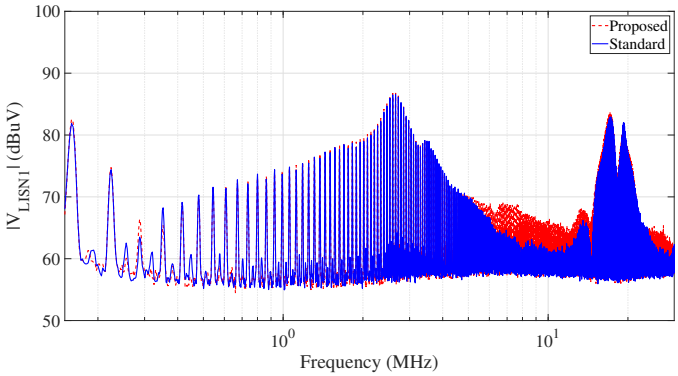

Fig. 21: Conducted emission measurement results with $E = 150\,\mathrm{V}$. The EMI receiver was configured with peak detector and $RBW = 9\,\mathrm{kHz}$ from $150\,\mathrm{kHz}$ to $30\,\mathrm{MHz}$.

the *standard* circuit. A slight increase in conducted emissions is observed for the *proposed* topology between $5\,\mathrm{MHz}$ and $15\,\mathrm{MHz}$. Nevertheless, the two topologies exhibit comparable attenuation within the regulated band overall. By significantly reducing the required amplifier output swing, the *proposed* topology lowers circuit complexity and cost, and enables operation with higher converter input voltages.

VI. Conclusions

This paper presented a novel technique to reduce the amplifier output voltage swing in VSCC AEFs for automotive traction inverters. It was shown that the amplifier output voltage is dominated by the fundamental component of the switching waveform. On this basis, considering that such frequency component is outside the EMI regulated band, this paper proposes the use of a notch fiter, tuned at the switching frequency, in the sensing branch of the VSCC circuit. A VSCC HEF prototype was built to validate the proposed idea. Small-signal equivalent impedance measurements showed good agreement with predicted curves. Conducted emission measurements confirmed that the proposed filter effectively suppresses interference between $150\,\mathrm{kHz}$ and $30\,\mathrm{MHz}$. Finally, measurements of the amplifier output voltage confirmed a reduction of the output voltage swing by nearly four and a half times with respect to the conventional AEF.

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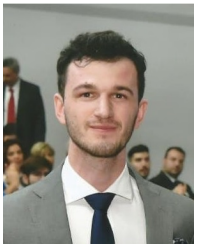

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