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Digital readout architectures for sensor arrays

By

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2026

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I dedicate this thesis to my grandparents. A fundamental brick of my life.

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Abstract

This thesis presents a comprehensive study of two custom-designed ASICs developed for high-energy physics experiments: ToASt, part of the PANDA project, and CLEOPATRA, within the HASPIDE project. The main goal was to evaluate their performance, reliability, and radiation tolerance, providing a detailed understanding of their behavior and guidance for future developments.
The work begins with an introduction to the scientific background and the experimental context, describing the PANDA and HASPIDE experiments, followed by a discussion of the silicon sensors employed in both systems, highlighting their design and operational principles. Building on this foundation, the characteristics and architecture of the ASICs under study are presented, emphasizing the key features that determine their performance.
A detailed characterization of ToASt was then carried out, including calibration, noise evaluation, Single Event Upset (SEU) tests, and Total Ionizing Dose (TID) studies. Calibration significantly reduced the gain spread and Time-over-Threshold (ToT) offset, while parameter optimization further enhanced uniformity and predictability across all boards. Noise measurements indicated slightly higher values compared to the first prototype, though ongoing optimization is expected to improve these results. SEU tests demonstrated a reduction in upsets relative to the previous version, confirming the effectiveness of the implemented triple redundancy. TID studies revealed increases in current consumption in both digital and analog sections, with the annealing phase allowing partial or complete recovery depending on the irradiation conditions.
CLEOPATRA was also characterized to evaluate the response of the new design. These measurements provided insights into the device behavior under operational conditions and identified areas requiring improvement, which are being addressed in the development of a second CLEOPATRA version.
Throughout the thesis, each set of results is presented in the context of the experimen-

tal methods and setups used, culminating in a discussion of the findings, comparison of the ASIC versions, and an outline of perspectives for future work. This approach ensures a coherent narrative linking the scientific context, experimental techniques, and performance evaluation.
Overall, the thesis delivers a thorough assessment of both ASICs, establishing a robust methodology for future characterizations. The results contribute valuable insights for optimizing high-performance front-end electronics, supporting the development of increasingly reliable and precise detector systems for high-energy physics experiments.

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Acronyms

APD Avalanche Photodiode

a-Si:H hydrogenated amorphous silicon

ASIC Application-Specific Integrated Circuit

CMOS Complementary Metal Oxide Semiconductor

DAQ Data Acquisition

EMC Electromagnetic Calorimeter

FAIR Facility for Antiproton and Ion Research

HASPIDE Hydrogenated Amorphous Silicon PIxels DEtectors

HESR High Energy Storage Ring

INFN Istituto Nazionale di Fisica Nucleare

ITO Indium Tin Oxide

MAPS Monolithic Active Pixel Sensors

MEMS Micro-Electro-Mechanical Systems

MVD Micro Vertex Detector

PANDA antiProton ANnihilation at DArmstadt

PECVD Plasma-Enhanced Chemical Vapor Deposition

SEU Single Event Upset

SPD Silicon Pixel Detector

SSD Silicon Strip Detector

STT Straw Tube Tracker

TID Total Ionizing Dose

ToA Time-of-Arrival

ToT Time-over-Threshold

Chapter 1

Introduction

1.1 Overview

This thesis is carried out in the context of two innovative projects: PANDA, an international experiment that investigates the strong interaction and employs silicon detectors for its microvertex, and HASPIDE, a multidisciplinary initiative exploring flexible detectors based on hydrogenated amorphous silicon used in several physics applications. Both projects aim to push the boundaries of particle detection in challenging environments, although with different physics goals and technological approaches.

In this Chapter, a general overview of the scientific motivations, technological frameworks, and detector systems involved in PANDA and HASPIDE is presented. A more detailed discussion on the readout electronics used in both experiments is provided in Chapter 3.

1.2 PANDA experiment

1.2.1 Scientific goals and context

The PANDA (antiProton ANnihilation at DArmstadt) experiment is one of the major projects being developed at the FAIR (Facility for Antiproton and Ion Research) research center in Darmstadt, Germany [14].

The goal of PANDA is to study with high precision the strong interactions between quarks and gluons by the annihilation of antiprotons on fixed targets. By using high-intensity, well-focused antiproton beams, PANDA will be able to explore a wide range of phenomena related to quantum chromodynamics in the nonperturbative regime. These include: the study of the internal structure of hadrons, the search for new states of matter such as tetraquarks, pentaquarks, and glueballs, and the investigation of baryonic interactions and high-density matter, with implications for astrophysics as well. Special attention will be dedicated to the physics of quark charm-containing states (charmonium state spectroscopy) and the search for violated symmetries, such as CP symmetry.
The experimental setup will utilize a fixed-target configuration, where antiprotons from the High Energy Storage Ring (HESR) collide with a hydrogen or nuclear target (see Fig. 1.1). These collisions produce a rich spectrum of final-state particles, whose trajectories and energies are reconstructed by a sophisticated multi-layered detector system.

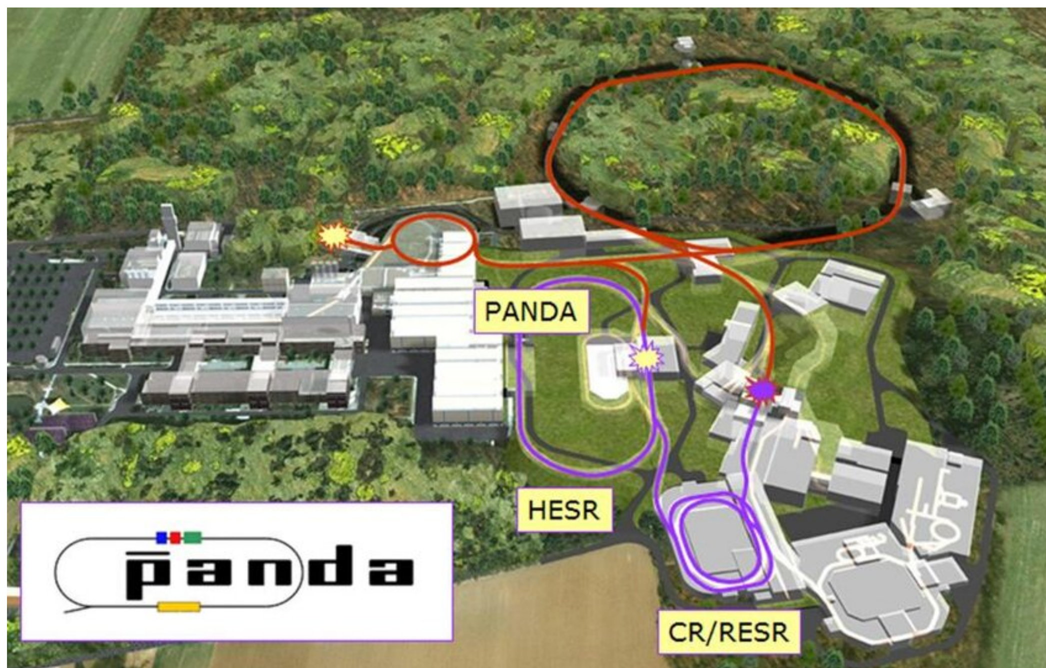


Fig. 1.1 Project of FAIR facility [1]

Fig. 1.2 illustrates the HESR designed for antiprotons, highlighting its main elements: a high-energy electron cooling section aimed at delivering beams with exceptional quality and precision, and an internal target area equipped with a state-of-the-art

detector system.

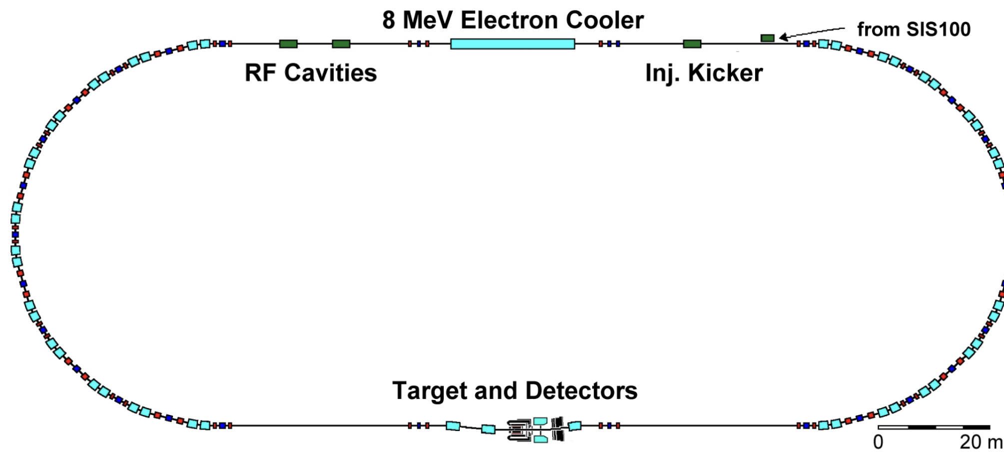


Fig. 1.2 Layout of HESR [2]

The PANDA experiment (Fig. 1.3) at FAIR operates in a triggerless mode, meaning that data are continuously acquired without relying on an external trigger signal. This approach was chosen to handle the very high interaction rates and the complexity of the events expected at PANDA, ensuring that all interactions can be recorded without any pre-selection or data loss. The main benefit of this scheme is the greater flexibility during offline analysis, since all the raw data are available for later processing, together with a reduction in the latency and complexity usually introduced by conventional trigger systems. At the same time, working in triggerless mode brings several challenges: it produces an enormous amount of data that must be read out, transmitted, and stored efficiently, requiring advanced real-time filtering and selection mechanisms to keep up with the continuous stream. Nevertheless, this approach is essential for achieving PANDA's physics objectives, which rely on the complete reconstruction of every event.

1.2.2 Detector architecture

Two essential components are at the core of the PANDA experiment: the beam pipe, which delivers the antiproton beam, and the target pipe, which places the target material precisely into the interaction region. The target can consist of either tiny solid hydrogen pellets, comparable in size to microscopic droplets, or a cluster-

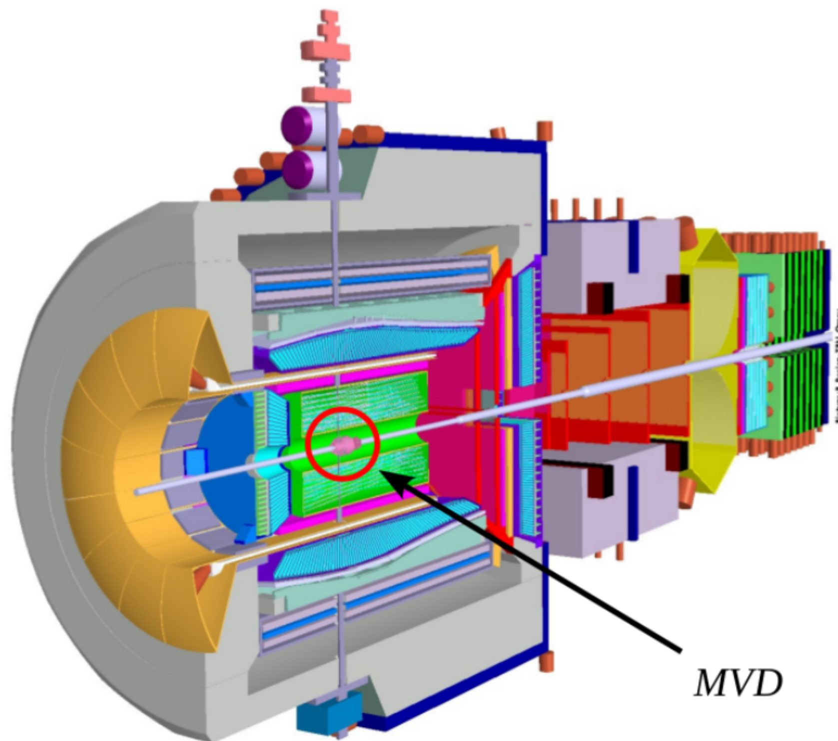


Fig. 1.3 PANDA apparatus [2]

jet stream of cold hydrogen gas. These systems are designed to inject the target with high spatial precision so that antiprotons collide with the target nuclei at a well-defined vertex. The target pipe is constructed to be as low-mass and as transparent as possible, meaning it uses lightweight materials with very thin walls, in order to minimize unwanted interactions with the secondary particles produced in the collision. This transparency is critical to ensure that the surrounding tracking detectors can accurately reconstruct the trajectories and kinematics of the particles emerging from the interaction point.

The PANDA detector system is designed to provide full and precise coverage of the particles produced in antiproton-target collisions. At its core lies the Micro Vertex Detector (MVD), which allows for extremely precise measurement of decay vertices of unstable particles; this detector will be described more in detail in the next section, as the work presented in this thesis focuses on the read-out front-end of the MVD strip detectors. Surrounding the MVD is the Straw Tube Tracker (STT), responsible for tracking charged particle trajectories with high spatial resolution. Several particle identification systems are employed, including Cherenkov detectors, which distinguish particles of different masses and velocities. The Electromagnetic

Calorimeter (EMC) measures the energy of electromagnetic particles such as photons and electrons, while the muon detectors identify muons exiting the apparatus. This combination of detectors enables a detailed and comprehensive reconstruction of the physical events.
The general layout of PANDA is shown in Fig. 1.4.

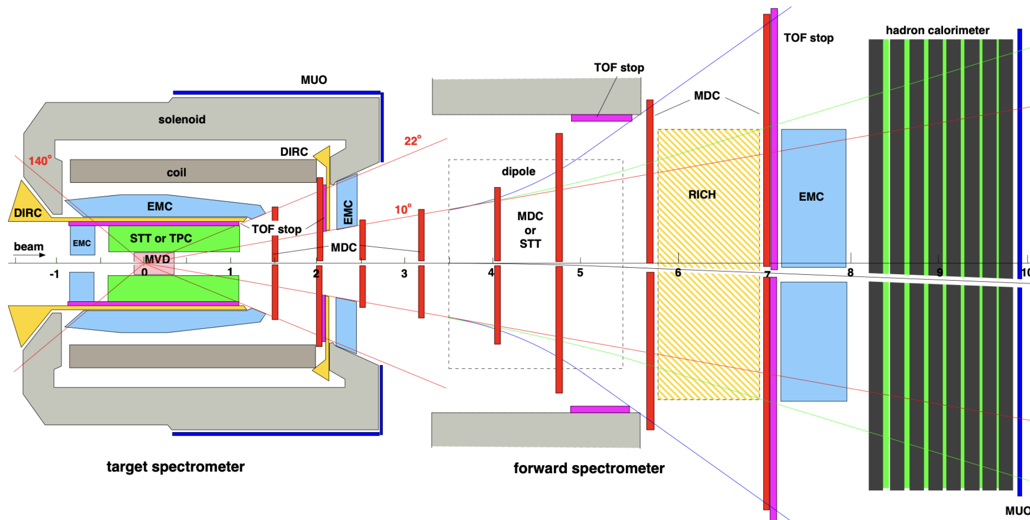


Fig. 1.4 Setup of the PANDA detector [2]

1.2.3 Micro Vertex Detector

The Micro Vertex Detector (MVD) is the innermost component of the PANDA tracking system, located very close to the interaction point at the crossing of the beam and target pipes. Its main purpose is to provide high-resolution spatial measurements of charged particle tracks, enabling precise reconstruction of decay vertices, which is essential for identifying short-lived particles containing heavy quarks.
The MVD consists of several concentric cylindrical layers surrounding the beam axis, complemented by forward disks to provide better coverage of the interaction region. The cylindrical layers provide measurements in the radial and azimuthal coordinates, while the disks offer additional information in the radial and longitudinal directions, improving the resolution along the beam axis.
In terms of sensor technology, the MVD combines pixel and strip detectors. Pixel sensors, with typical dimensions of around 100×100 μm or smaller, are placed in the innermost layers to ensure high spatial resolution near the beam. In the outer layers,

silicon strip detectors are used, optimized for covering larger areas with a reduced amount of material and number of readout channels.
The inner radius of the MVD is only a few centimeters, typically between 2 and 3 cm,while the outer radius extends up to approximately 10–15 cm. The total longitudinal length of the detector spans several tens of centimeters, sufficient to cover the region where most primary and secondary interactions occur.
Since the MVD is located very close to the interaction region, it is crucial to reduce the amount of material as much as possible to limit multiple scattering, photon conversions, and other effects that could degrade tracking precision. This is achieved by using low-density materials and minimizing the thickness of silicon sensors, support structures, and cooling systems.
Finally, the MVD has a modular architecture, composed of ladders and detector modules that facilitate assembly, maintenance, and replacement while ensuring mechanical precision and long-term stability.
A schematic of the structure of the MVD is shown in Fig. 1.5.

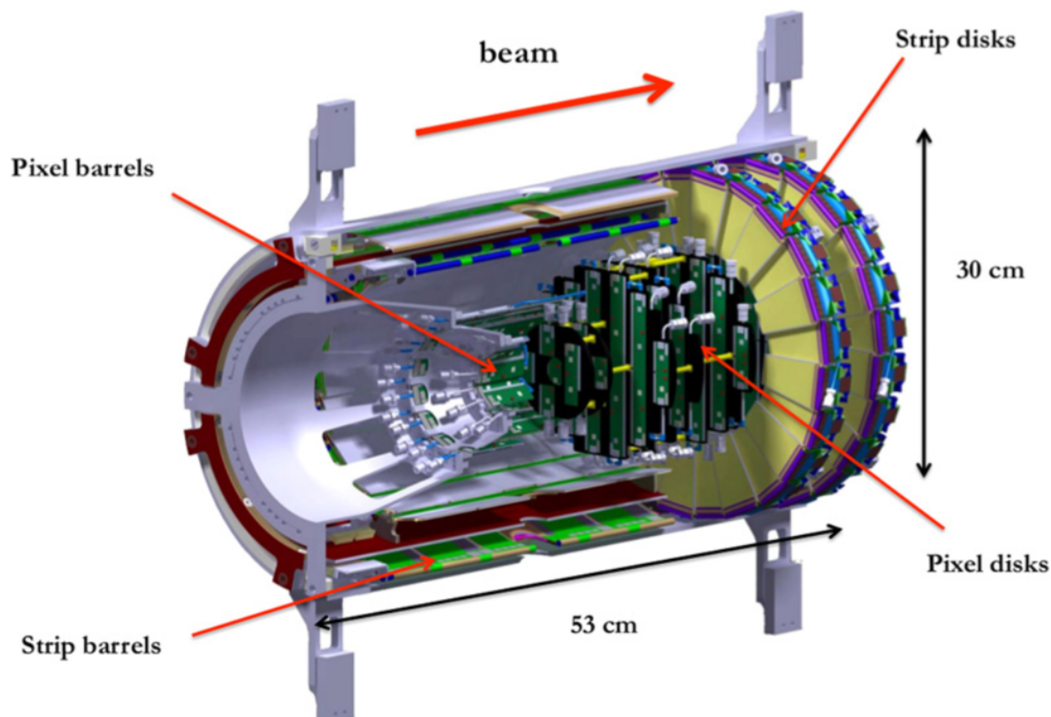


Fig. 1.5 PANDA Micro Vertex Detector [3]

Specifically, the MVD is structured into two main regions, ensuring nearly complete angular coverage around the interaction point. Its internal layout combines pixel

and strip detectors to achieve high spatial resolution with an efficient readout while keeping a low channel count and material budget.
These regions are:

- Barrel section:
  - Consists of four concentric cylindrical layers surrounding the beam axis.
  - The two innermost layers host pixel detectors positioned as close as possible to the interaction point, in order to achieve precise vertex reconstruction even under high particle density conditions.
  - The two outer layers use double-sided silicon strip detectors, which provide accurate tracking over a larger radius with fewer readout channels.
  - The detector modules are attached to lightweight supports, called ladders, arranged parallel to the beam axis.
- Disk sections:
  - The 6 disks are all on the forward side of the barrel region, that is on one side only of the barrel region.
  - Each disk is divided into radial sectors, with pixel sensors in the central part and strip sensors in the outer regions.
  - These disks enhance the tracking performance in the longitudinal direction, complementing the information provided by the barrel layers.

This hybrid configuration enables the MVD to achieve accurate spatial measurements across a wide angular range, while reducing multiple scattering and maintaining high track reconstruction quality [15].

1.2.4 Readout electronics

The PANDA MVD uses custom-designed front-end ASICs (Application-Specific Integrated Circuit) tailored to the detector's high granularity and timing requirements:

- ToPix (Torino ASIC for silicon Pixel detectors) [16] — the pixel front-end readout. This chip will be designed to measure the charge and timing of

signals generated by particles passing through silicon pixel sensors, using the Time-over-Threshold (ToT) technique. The chip enables precise, triggerless data acquisition and is optimized for high-rate, radiation-intense environments, making it crucial for accurate tracking and vertex reconstruction in hadron physics experiments.

- ToASt (Torino ASIC for silicon Strip detectors) — the strip front-end readout chip. It is a 64-channel ASIC designed for continuous, triggerless data acquisition, allowing each particle hit to be recorded independently as it occurs. The chip measures both the Time-of-Arrival (ToA) and the Time-over-Threshold (ToT) of each hit with high temporal precision, operating with a 160 MHz system clock. ToASt also supports continuous data transmission through high-speed serial links and includes integrated features for zero suppression and data buffering.

ToASt ASIC is designed by the INFN Torino group and optimized for low power consumption, low noise, and integration with the PANDA Data Acquisition System (DAQ). ToASt will be described in more detail in Chapter 3.

1.3 HASPIDE project

1.3.1 Motivation and applications

The HASPIDE project (Hydrogenated Amorphous Silicon PIxels DEtectors) [17] investigates the use of hydrogenated amorphous silicon (a-Si:H) to develop lightweight, flexible, and radiation-tolerant detectors. These sensors are well suited for applications such as space missions, radiation therapy, and beam diagnostics, where both mechanical flexibility and resistance to radiation are essential.
In contrast to conventional crystalline silicon detectors, a-Si:H sensors can be deposited at low temperatures on flexible polymer substrates such as Kapton, PET, or PEN. This technology enables the fabrication of thin-film devices capable of adapting to curved surfaces, opening the way to innovative solutions in dosimetry and imaging.

1.3.2 Sensor technologies

The core element of HASPIDE sensors is the hydrogenated amorphous silicon active layer, typically deposited via Plasma-Enhanced Chemical Vapor Deposition (PECVD). The structure commonly follows a n-i-p or p-i-n configuration, where an intrinsic a-Si:H layer is sandwiched between doped layers to facilitate charge separation and collection.
In addition to conventional diode structures, HASPIDE explores advanced architectures using charge-selective contacts, such as Indium Tin Oxide (ITO) and metal-oxide interfaces, which improve carrier selectivity and suppress leakage currents. These architectures aim to maximize the signal-to-noise ratio and enable stable operation at low bias voltages (10 V to 50 V).
When ionizing radiation passes through the sensor, it generates electron-hole pairs in the intrinsic layer. The applied electric field causes these charges to drift toward the electrodes, where they are collected and converted into an electrical signal.
Key performance features include:

- Radiation tolerance: tested up to several MGy with minimal signal degradation;
- Mechanical flexibility: reduces beam distortions during radiation flux measurements or medical dosimetry;
- High spatial resolution: achievable through pixelation or strip segmentation;
- Scalability: potential for cost-effective large-area production.

From the technological perspective, the project develops two main architectures:

- planar n-i-p diode structures, where an intrinsic layer several microns thick is enclosed between two thin doped regions (n^+ and p^+), to facilitate efficient collection of charge generated by ionizing particles;
- structures with charge-selective contacts, in which the injection or extraction of carriers is controlled through conductive oxides with a filter function for specific charges, avoiding the need for classical doping.

These devices have been designed with special focus on their linear response as a function of dose, long-term stability, and tolerance to ionizing radiation, which are

key parameters for reliability in radiological environments. Laboratory and beam tests have shown that HASPIDE detectors can efficiently detect both light charged particles (such as electrons) and ionizing photons while maintaining low dark current and good response uniformity.
One of the most interesting points of the project is the possibility of making low-profile active dosimeters that can be directly applied to curved or moving surfaces, such as human bodies or robotic devices. In addition, use in the space field emerges as another strategic area, due to their light weight, robustness, and ability to function in environments with high radiative exposure.
The project involved a number of Italian and international institutions, including INFN, Politecnico di Milano, University of Salento, CNR, EPFL and industrial partners. In summary, HASPIDE represents a relevant step toward a new generation of thin-film sensors for particle physics, radiation protection, and space. The combination of compatibility with industrial processes, robustness, geometric flexibility, and competitive performance makes it a highly attractive candidate for multiple future applications.
In Fig. 1.6 one of the first prototype of the sensor is shown.

1.3.3 Readout electronics

To read out the signals from a-Si:H sensors, HASPIDE has developed a dedicated front-end chip called CLEOPATRA. It includes:

- Low-noise charge-sensitive amplifiers.
- Pulse shaping and digitization circuits.
- Trigger logic for both continuous and event-based acquisition.
- Low-power operation for portable and embedded systems.

CLEOPATRA is optimized to operate in the presence of very small amplitude signals, in the order of 10 fA – 1 pA, typical of a-Si:H detectors, and includes an analog chain consisting of 12 analog channels, each including an active integrator, a comparator with a programmable threshold, a charge injection circuit and a test-pulse control logic. The chip is designed in 28 nm technology to have high resistance to radiation. CLEOPATRA also allows for easy integration with dosimetry modules made in

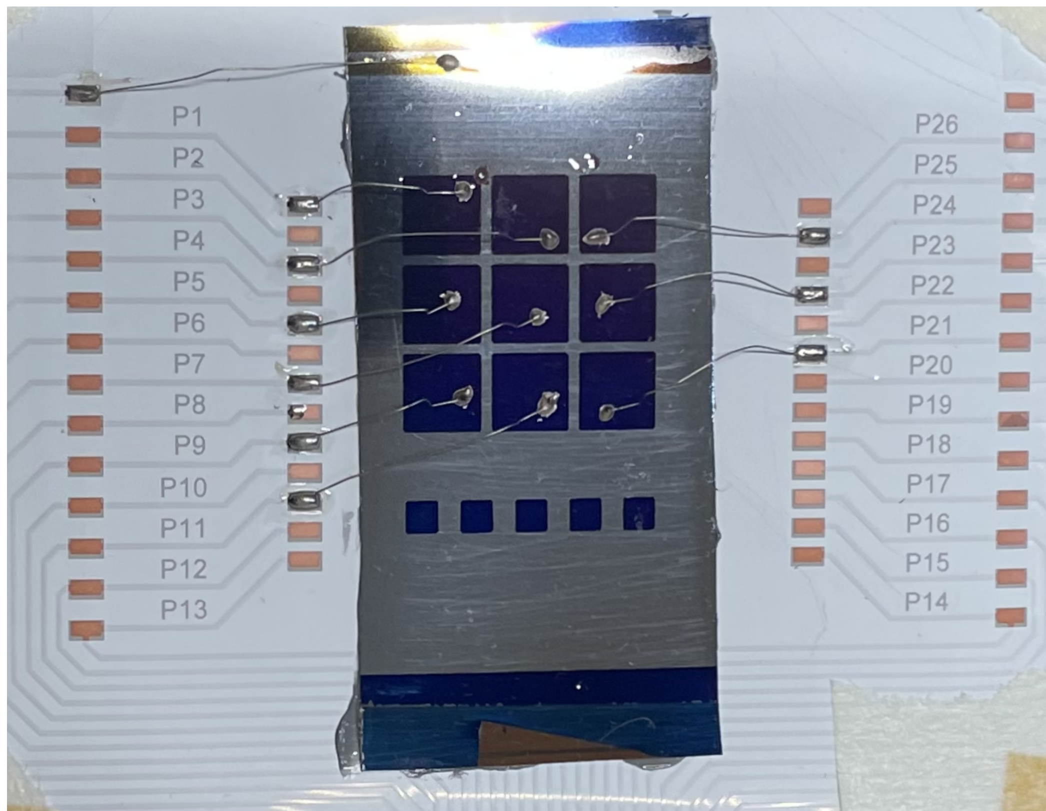


Fig. 1.6 One of the first prototype of the hydrogenated amorphous silicon sensor of the HASPIDE project

HASPIDE, thus promoting the miniaturization of systems and their portability. The configurability of threshold and gain parameters makes the ASIC versatile and suitable for different types of thin-film sensors, maintaining high detection efficiency even in unconventional geometries. Further technical details such as design choices and specifications will be discussed in Chapter 3.
In the HASPIDE project, CLEOPATRA chip is coupled with an amorphous silicon sensor to implement an integrated readout mode, where the total charge accumulated over a predetermined time interval is measured. This approach, while foregoing detailed reconstruction of the sequence and characteristics of individual events, offers simpler electronics and a generally better signal-to-noise ratio. At the same time, the coupling of the same sensors with ToASt is being evaluated to obtain a single-particle readout similar to that used in the PANDA project. In this scheme, each interaction is recorded individually, allowing for precise measurements of time and charge for each impact. This approach has the advantage of avoiding event overlap and ensuring

a clean reconstruction of the track, which is particularly effective in low-frequency or activated environments.

Chapter 2

Silicon sensors

In the field of modern sensor technologies, silicon-based sensors hold a prominent position due to their versatility, precision, and compatibility with the microfabrication techniques developed for the semiconductor industry. When combined with Complementary Metal Oxide Semiconductor (CMOS) processes and ASICs, these sensors can achieve exceptional levels of performance, enabling not only accurate detection but also real-time signal conditioning, processing, and data transmission within highly compact and energy-efficient systems. This chapter aims to provide an in-depth overview of the fundamental characteristics, physical principles of operation, and practical applications of silicon sensors, while also discussing the critical role played by CMOS and ASIC technologies in their design, optimization, and system-level integration.

The chapter begins with a discussion of the reasons why silicon has become the material of choice for sensor fabrication, analyzing its electronic, mechanical, and thermal properties that make it particularly well-suited for a wide range of applications, from pressure and optical sensors to particle detectors in physics. This section will also explore how CMOS technology offers the possibility to integrate sensing elements with on-chip readout electronics, significantly reducing noise, power consumption, and system size.

Furthermore, the contribution of ASIC design will be examined, emphasizing how custom-tailored circuitry can be optimized for specific measurement needs, environmental conditions, and performance constraints.

Subsequently, the chapter will explore the typical fabrication techniques used to produce silicon-based sensors, such as lithography, thin-film deposition, chemical

or physical etching, and doping processes. These methods, originally developed for the microelectronics industry, have been adapted and optimized for the field of sensor technology, and their compatibility with standard CMOS processes will be highlighted as a key factor enabling large-scale integration and cost-effective production.
A detailed discussion of the most common silicon sensor architectures and their technological developments will also be presented. Particular emphasis will be placed on sensor systems in which the sensing layer, CMOS readout circuits, and dedicated ASICs are co-designed to achieve optimal performance. The advantages and challenges associated with these integration strategies will be analyzed, highlighting their impact on signal quality, data acquisition speed, and overall device efficiency.

2.1 Properties of Silicon in Sensors

Silicon (Si) is the most widely used semiconductor material in the fabrication of electronic sensors, thanks to its abundance, thermal stability, and ease of processing. Its electrical properties can be modified through doping, the formation of P-N junctions, and the management of leakage current, fundamental elements for the operation and reliability of sensors. Other semiconductor materials are also used in radiation detectors depending on the application, including germanium (Ge) for high-resolution gamma spectroscopy, cadmium telluride (CdTe) and cadmium zinc telluride (CZT) for X-ray and gamma detection at room temperature, as well as materials such as gallium arsenide (GaAs), diamond, and silicon carbide (SiC) for high-radiation or high-temperature environments.

2.1.1 Doping of Silicon

Doping is an essential technique in the processing of silicon for electronic devices, as it allows its electrical properties to be modified in a controlled manner. Pure silicon, called intrinsic silicon, has very limited conductivity at room temperature, which makes it difficult to use directly in sensors and electronic circuits. To overcome this limitation, small amounts of impurities, called dopants, are introduced into the material, which increase the concentration of charge carriers and allow n-type or

p-type semiconductors to be obtained [18].
Typical dopants for n-type silicon are elements from group V of the periodic table, such as phosphorus, arsenic, and antimony. These elements provide extra electrons that become free charge carriers in the crystal lattice. For p-type silicon, on the other hand, elements from group III, such as boron, are mainly used, which create holes that behave as positive charge carriers.
The presence of these impurities allows the local electrical properties of silicon to be modeled, creating regions with different characteristics that are fundamental for the formation of devices such as P-N junctions. These junctions are the basis for the operation of numerous devices, including silicon sensors, as they allow the flow of current and the collection of charges generated by particles or photons to be controlled.
To introduce dopants into silicon, two main methods are used: thermal diffusion and ion implantation. In the first case, silicon is exposed to vapors or gases containing dopants at high temperatures, allowing the atoms to gradually diffuse into the material. Although this method is relatively simple and suitable for obtaining doping profiles over large areas, control over depth and concentration is less precise.
Ion implantation, on the other hand, is a more advanced and precise technique, which consists of bombarding the silicon with accelerated ions of the desired dopant. This allows the depth and quantity of impurities introduced to be controlled with high accuracy. After implantation, the material is subjected to heat treatment to repair the damage caused by the ions and activate the dopants, to bring them into an electrically active configuration.
Ultimately, doping is an indispensable technique for customizing the behavior of silicon according to the desired applications, from microelectronics to sensors, and the choice of doping introduction methodology depends on the precision, depth, and uniformity requirements of the final device.
In a semiconductor in thermal equilibrium, the concentration of free electrons and that of holes are related by a fundamental relationship known as the law of mass action [19]. This relationship expresses the fact that the product of the concentrations of charge carriers is constant and depends exclusively on temperature, regardless of the level of doping of the material. Formally, this condition is described by the following equation:

$$n_0 \cdot p_0 = n_i^2 \tag{2.1}$$

where:

- n_0 is the free electron concentration,
- p_0 is the hole concentration,
- n_i is the intrinsic carrier concentration in silicon.

For a non-intrinsic semiconductor in thermal equilibrium, the above relation holds and enables the control of resistivity, which is crucial for the design of high-precision sensors.

2.1.2 P-N Junction

The P-N junction is fundamental to the functioning of silicon sensors. It is created when two differently doped regions (p-type and n-type) come into contact, creating a depletion region that acts as a barrier to current flow.
The width of the depletion region w as a function of the applied reverse bias voltage V is given by:

$$w = \sqrt{\frac{2\varepsilon_{\text{Si}}(V_{\text{bi}} + V)}{qN_{\text{eff}}}} \tag{2.2}$$

where:

- ε_{Si} is the permittivity of silicon,
- V_{bi} is the built-in voltage,
- V is the applied voltage,
- q is the elementary charge,
- N_{eff} is the effective doping concentration.

The reverse saturation current I_{sat} as a function of temperature T is expressed as:

$$I_{\text{sat}} = I_{\text{sat0}} \cdot \left(\frac{T}{T_0}\right)^2 \cdot \exp\left(\frac{-E_g}{k}\left(\frac{1}{T} - \frac{1}{T_0}\right)\right) \tag{2.3}$$

where:

- I_{sat0} is the saturation current at reference temperature T_0,

- E_g is the silicon bandgap energy,
- k is the Boltzmann constant.

At thermal equilibrium, the charge distribution in the depletion region satisfies the Poisson equation:

$$\frac{d^2V}{dx^2} = -\frac{\rho(x)}{\varepsilon} \tag{2.4}$$

where V is the electrostatic potential, $\rho(x)$ the local charge density, and $\varepsilon = \varepsilon_r\varepsilon_0$ the permittivity of silicon. The depletion region width W depends on the doping concentrations N_A and N_D of the p- and n-sides:

$$W = \sqrt{\frac{2\varepsilon}{q}\frac{N_A + N_D}{N_A N_D}(V_{bi} - V)} \tag{2.5}$$

where q is the elementary charge, V_{bi} the built-in potential, and V the applied bias voltage. Under reverse bias, the depletion region widens, increasing the volume where incident photons can generate electron–hole pairs, which is essential for photodiodes and radiation detectors [20].
The current-voltage characteristic of the p–n junction diode follows the Shockley equation:

$$I = I_S\left(e^{\frac{qV}{kT}} - 1\right) \tag{2.6}$$

where I_S is the saturation current, k the Boltzmann constant, and T the absolute temperature. This non-linear behavior allows the p–n junction to act as a sensitive rectifier and detection element in various sensor applications.
An external voltage can be applied to the P-N junction, causing it to operate in the forward bias configuration, a positive potential difference is applied to the p-side with respect to the n-side. Under these conditions, electrons move from the n-region toward the junction, reducing the potential barrier and allowing a significant current to flow. The second case is the reverse bias configuration, when a positive potential difference is applied between the n-side and the p-side. In this case, the external voltage will increase the potential barrier across the junction and, as a result, the depleted region will extend. Free carriers will no longer cross the junction, and this system can be operated as a particle detector.

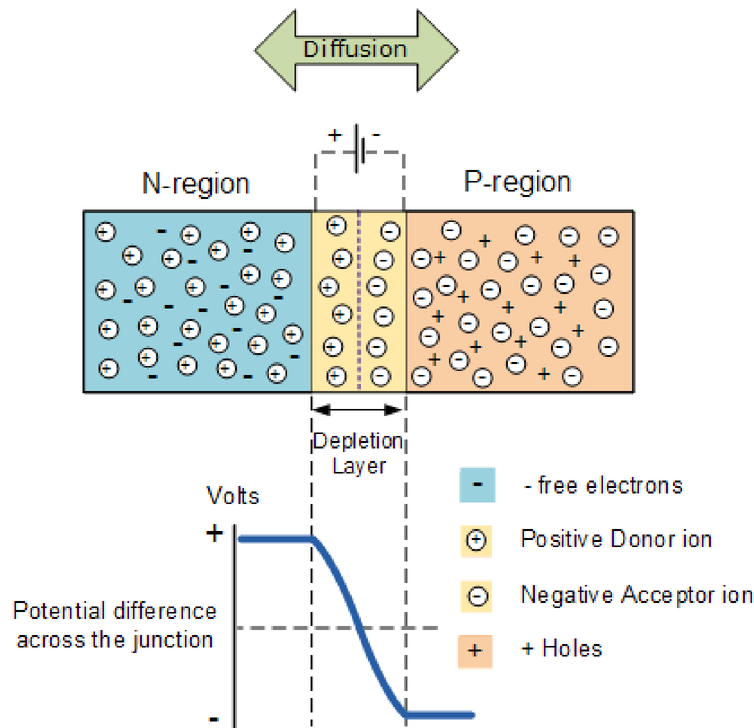


Fig. 2.1 Schematic representation of a p–n junction with depletion region, charge distribution, electric field, and built-in potential [4].

2.1.3 Leakage Current

Leakage current is an undesired current component that flows through a silicon sensor even in the absence of external ionization events [21]. It is mainly generated by charge carriers thermally created within the semiconductor material and by defects present in the crystal lattice or device interfaces. Although leakage current is generally very low, its presence can significantly affect sensor performance. One of the most significant effects of leakage current is the increase in electronic noise in the acquired signal. Since the sensor must detect very small charges generated by incident particles, even a minimal leakage current can mask or distort the useful signal, reducing the accuracy and reliability of the measurement. In particular, the increase in noise limits the ability to discriminate weak or low-energy events.
Furthermore, leakage current tends to increase with temperature according to an exponential relationship, since higher temperatures generate a greater number of thermal carriers. For this reason, cooling systems are often used in silicon detection systems to keep leakage current within acceptable limits, thus improving the stability

and sensitivity of the detector.
Another problem related to leakage current is the possible damage to the device itself. Excessive current can lead to localized heating (self-heating), which can accelerate the degradation of the material and electrical contacts, reducing the operational life of the sensor. Furthermore, in high-radiation environments, increased leakage current is also an indicator of structural damage to the silicon caused by particle-induced defects.
To minimize leakage current, various strategies are employed, such as cooling the sensor to reduce the thermal generation of charge carriers, using high-quality materials with low defect density, optimizing manufacturing processes to reduce surface imperfections, and designing junction structures with more effective energy barriers that limit unwanted current flow.
In summary, leakage current represents a major challenge in the design and use of silicon sensors, requiring technological solutions such as temperature control, the choice of materials with low defect density, and advanced manufacturing techniques to minimize its negative effects.
The total leakage current I_{leak} is the sum of:

$$I_{\text{leak}} = I_{\text{diff}} + I_{\text{gen}} \tag{2.7}$$

where:

- I_{diff} is the diffusion current,
- I_{gen} is the generation current.

The generation current I_{gen} as a function of defect concentration N_{def} is:

$$I_{\text{gen}} = qN_{\text{def}}v_{\text{th}} \cdot A \tag{2.8}$$

where:

- v_{th} is the thermal velocity of carriers,
- A is the junction area.

2.2 Material properties of Silicon for sensing applications

Silicon has established itself as the dominant material for sensor fabrication due to a unique combination of electronic, mechanical, and thermal properties that make it suitable for a wide range of detection principles and application scenarios. As a semiconductor with an indirect bandgap of approximately $1.12\,\text{eV}$ at room temperature [20], it combines low intrinsic carrier concentration, which reduces leakage currents, with the ability to be precisely doped with donor and acceptor impurities to tailor its electrical conductivity [22]. This tunability is fundamental for devices exploiting effects such as piezoresistivity or photodetection. Moreover, silicon naturally forms a high-quality native oxide (SiO_2) that plays a critical role in microfabrication, enabling reliable surface passivation, electrical insulation, and gate formation in MOS-based structures [23].
From a mechanical point of view, silicon is very stiff, with a Young's modulus between 130 and 185 GPa depending on the crystal orientation, ensuring structural integrity even at micrometer scales, as required in micro-electromechanical systems (MEMS). This means it can keep its shape even when made very small, which is important for tiny devices. Silicon is also relatively light, with a density of $2.33\,\text{g}\,\text{cm}^{-3}$, allowing for strong but lightweight parts. Additionally, its high thermal conductivity (around $150\,\text{W}/(\text{mK})$ at room temperature) helps devices cool down efficiently when they produce a lot of heat [24]. Furthermore, the low thermal expansion coefficient ($2.6 \times 10^{-6}\,\text{K}^{-1}$) ensures dimensional stability under varying temperature conditions, which is particularly advantageous for sensors deployed in rigid or fluctuating environments.
Compared to other semiconductor materials such as Gallium Arsenide (GaAs) or Silicon Carbide (SiC), silicon offers unmatched manufacturing maturity and scalability. Large, defect-free single-crystal wafers can be produced using techniques such as the Czochralski or float-zone methods [23], supporting high-yield and cost-effective mass production.
Beyond its intrinsic material properties, silicon's compatibility with CMOS and ASIC technologies enables the monolithic integration of sensing elements with on-chip readout and signal processing electronics, reducing parasitic effects, enhancing noise immunity, and ultimately improving overall system performance [25].
The combination of well-understood physics, established processing techniques, and

extensive design knowledge accumulated over decades of semiconductor research makes silicon not only the most widely adopted material in sensing technology but also one of the most reliable and versatile platforms for future developments.

2.3 Physical principles of Silicon-based sensors

The operation of silicon-based sensors is grounded in a variety of physical phenomena that enable the conversion of a measurable quantity such as pressure, temperature, acceleration, or light intensity into an electrical signal. At the core of these devices lies the fact that silicon, as a semiconductor, allows precise modulation of its electrical properties through doping, mechanical stress, or photon interaction, thus making it adaptable to multiple sensing principles.
The fundamental building block for many silicon sensors and optoelectronic devices is the p–n junction.
One of the most widely exploited mechanisms is the piezoresistive effect [22]. When a mechanical stress σ is applied to a doped silicon element, its electrical resistivity ρ changes according to:

$$\frac{\Delta\rho}{\rho} = \pi_l \sigma_l + \pi_t \sigma_t \tag{2.9}$$

where π_l and π_t are the longitudinal and transverse piezoresistive coefficients, and σ_l, σ_t are the respective stress components. This property is fundamental for pressure sensors and accelerometers, where mechanical deformation is converted into a measurable change in resistance, typically arranged in a Wheatstone bridge to improve sensitivity and temperature compensation [20].
Another key detection principle is the capacitive effect, where displacement of microstructure changes the capacitance C between two electrodes:

$$C = \frac{\varepsilon_r \varepsilon_0 A}{d} \tag{2.10}$$

with A being the electrode area, d the separation distance, and ε_r, ε_0 the relative and vacuum permittivity, respectively. In MEMS accelerometers and microphones, variations in d caused by vibration or pressure directly alter C, which can then be detected using integrated CMOS readout circuits [25].
Thermal sensing mechanisms exploit the temperature dependence of silicon's electrical conductivity and Seebeck coefficient. In thermistors, the resistivity follows an

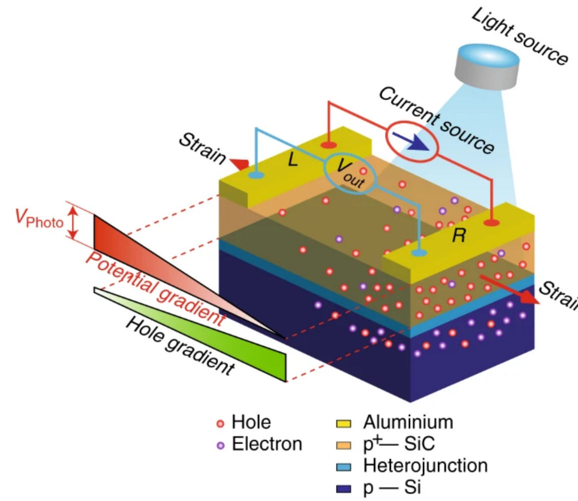


Fig. 2.2 Example of a piezoresistive sensing Silicon structure [5]

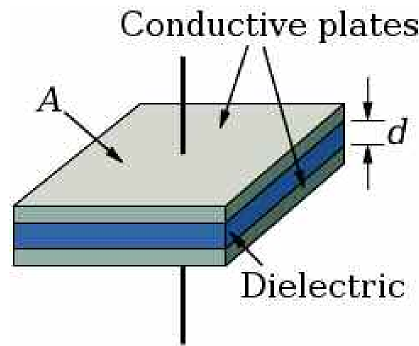


Fig. 2.3 Schematic of a capacitive sensing element with variable gap d [6].

approximately exponential relation:

$$R(T) = R_0 e^{\beta\left(\frac{1}{T} - \frac{1}{T_0}\right)} \tag{2.11}$$

where R_0 is the resistance at reference temperature T_0 and β is a material-dependent constant. In thermopiles, the thermoelectric voltage V_{th} is given by:

$$V_{\text{th}} = S \cdot \Delta T \tag{2.12}$$

where S is the Seebeck coefficient and ΔT is the temperature gradient across the junctions. Such devices benefit from the low thermal mass and high thermal conductivity of micromachined silicon structures, which allow rapid response times [24]. For optical detection, photodiodes and Avalanche PhotoDiodes (APDs) leverage

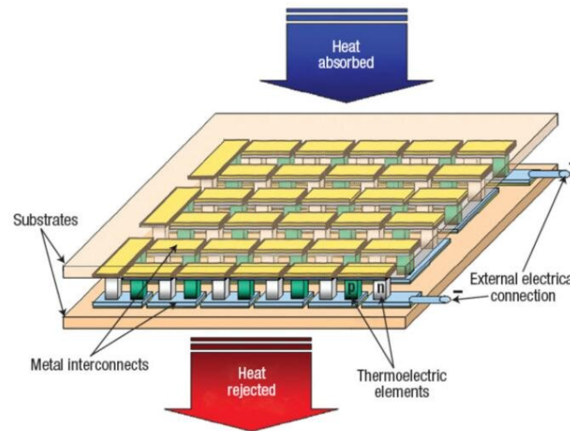


Fig. 2.4 Example structure of a thermopile with hot and cold junctions [7].

the generation of electron–hole pairs when photons with energy $h\nu > E_g$, where Eg denotes the semiconductor bandgap energy, are absorbed in the depletion region. The photocurrent I_{ph} is proportional to the incident optical power P_{opt}:

$$I_{\mathrm{ph}} = R_{\lambda} \cdot P_{\mathrm{opt}} \tag{2.13}$$

where R_{λ} is the responsivity, dependent on wavelength λ and quantum efficiency. In APDs, an internal gain mechanism via impact ionization amplifies this photocurrent, at the expense of higher bias voltage and increased noise [20].

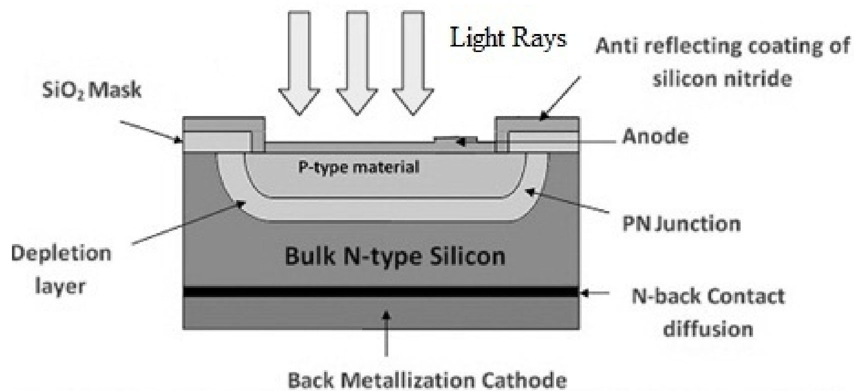


Fig. 2.5 Cross-sectional schematic of a p–n photodiode in silicon [8].

In practice, modern silicon sensors often combine these physical principles within a single device, integrating the sensing element with CMOS or ASIC-based readout electronics. This integration allows direct signal conditioning such as amplification,

filtering, and analog-to-digital conversion at the sensor level, which minimizes parasitic effects and improves signal-to-noise ratio [25, 23].

2.4 Silicon Pixel Detectors

Silicon Pixel Detectors (SPDs) represent an advanced class of semiconductor devices widely used in particle physics, medical imaging, and various high-resolution detection applications. These detectors consist of a two-dimensional matrix of small, discrete sensing elements called pixels, each capable of independently detecting ionizing radiation with high spatial resolution. This pixelation enables detailed tracking of particles or high-quality imaging, which is crucial in experiments and technologies where precision is essential [26].
The schematic diagram of a silicon pixel detector is shown in Fig. 2.6. The fundamental detection mechanism relies on the generation of electron-hole pairs within the silicon bulk when traversed by ionizing particles. A reverse-biased p–n junction creates a depletion region, an active volume with an electric field that efficiently separates and collects these charge carriers. The collected charge at each pixel electrode produces an electrical signal proportional to the energy deposited by the incident particle [27].
The number of electron-hole pairs generated, N_{eh}, can be expressed as:

$$N_{eh} = \frac{E_{\text{dep}}}{\varepsilon_{\text{Si}}}, \tag{2.14}$$

where E_{dep} is the deposited energy, and $\varepsilon_{\text{Si}} \approx 3.6\,\text{eV}$ is the average energy required to create one electron-hole pair in silicon [28].
Typical pixel dimensions range from a few micrometers to tens of micrometers, with the pixel pitch directly influencing the spatial resolution according to:

$$\sigma_{\text{pos}} \approx \frac{\text{pixel size}}{\sqrt{12}}, \tag{2.15}$$

assuming uniform charge deposition and binary readout [9]. Smaller pixels enhance resolution but demand more complex readout electronics and higher data rates. The space resolution can also be improved by measuring the charge injected by a single particle in multiple pixels and calculating the charge distribution centroid.

Modern pixel detectors integrate ASICs to amplify, discriminate, and digitize the signals from each pixel. Monolithic Active Pixel Sensors (MAPS) represent a cutting-edge technology where both sensing and readout electronics coexist on the same silicon substrate using CMOS processes, minimizing material and simplifying fabrication [29]. However, this architecture may present some limitations, such as a relatively smaller active sensing area and potential constraints in charge collection efficiency.
The charge collection time is governed by the carrier drift velocity v_d, defined as:

$$v_d = \mu E, \tag{2.16}$$

where μ is the carrier mobility and E the electric field magnitude within the depletion region [20]. Faster charge collection improves timing resolution and reduces charge trapping effects, vital for operation in high-radiation environments.
Radiation hardness remains a critical design parameter; silicon pixel detectors are engineered to withstand damage from high particle fluences through material selection and device architecture optimization [26].
Beyond high-energy physics, silicon pixel detectors are extensively used in X-ray imaging and other fields demanding fine spatial and temporal resolution [30]. Their scalability and compatibility with established microfabrication techniques allow for large-area arrays and versatile detector configurations.

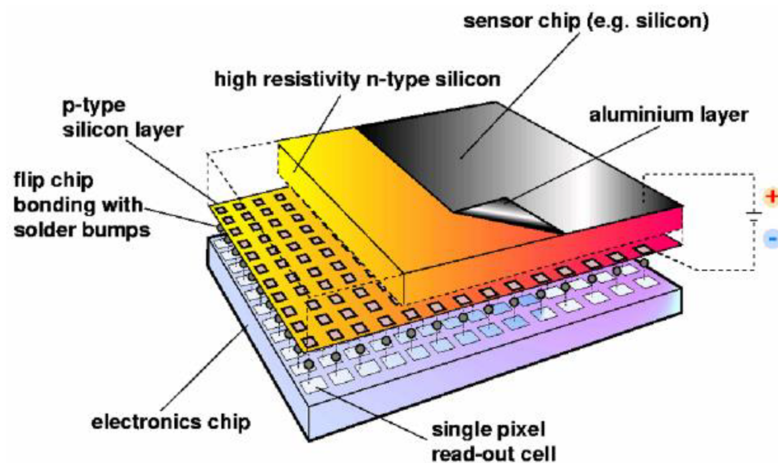


Fig. 2.6 Schematic illustration of a silicon pixel detector showing the pixelated sensor array and readout electronics [9].

2.5 Silicon Strip Detectors

Silicon Strip Detectors (SSDs) represent another fundamental technology in the field of semiconductor radiation detectors, widely employed in particle physics, nuclear instrumentation, and various imaging applications. These detectors exploit the intrinsic properties of silicon to convert the passage of charged particles or ionizing radiation into electrical signals, providing spatial information crucial for tracking and reconstruction purposes [31].
The working principle of a silicon strip detector is based on the segmentation of a silicon wafer into multiple narrow, parallel conductive strips. Each strip functions as an independent sensing element capable of collecting charge generated by ionizing particles traversing the detector. When a charged particle passes through the silicon bulk, it ionizes atoms along its path, creating electron-hole pairs proportional to the deposited energy. By applying a reverse bias voltage across the silicon substrate, a depletion region forms where these charge carriers are quickly collected by the electrodes corresponding to the strips. The detection system can then precisely localize the position of the particle along one dimension, namely, the direction perpendicular to the strips, by identifying which strip(s) have recorded a signal.
The schematic diagram of a silicon strip detector is shown in Fig. 2.7.

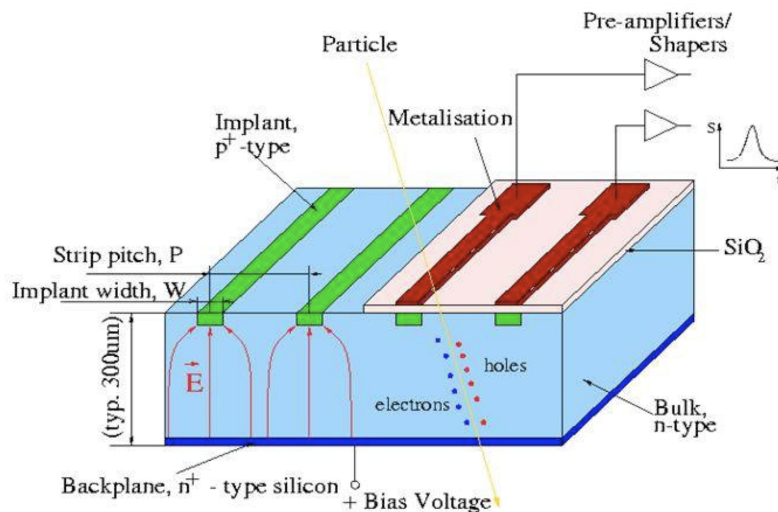


Fig. 2.7 Schematic illustration of a silicon strip detector [10].

The width of each strip typically ranges from a few tens to several hundreds of micrometers, with narrow gaps in between that electrically isolate adjacent strips.

This fine segmentation allows for high spatial resolution in one dimension, which is essential in many tracking detectors where precise positional information improves event reconstruction accuracy. The total active area of the detector can be extended by fabricating a large number of strips arranged in parallel, thereby covering substantial regions while maintaining detailed position sensitivity.
SSDs are widely employed in Time-of-Flight (ToF) systems due to fast response time, enabling precise measurement of particle arrival times and improving overall timing accuracy in high-energy physics experiments.
Fabrication of silicon strip detectors involves advanced semiconductor processing techniques including photolithography, ion implantation for doping, and metallization to create contacts. The thickness of the silicon wafer is typically on the order of 200 μm to 300 μm, balancing mechanical stability with efficient charge collection and timing properties.
In contrast, SPDs take this segmentation a step further by dividing the silicon surface into a two-dimensional matrix of tiny, discrete pixels, each operating as an individual sensor. Unlike strip detectors which provide only one-dimensional spatial information, pixel detectors offer high-resolution position measurement in two dimensions. This capability is particularly valuable in complex tracking environments, such as those encountered in vertex detectors at collider experiments, where precise spatial mapping of particle trajectories in all spatial directions is critical.
While pixel detectors offer superior spatial resolution and can manage higher particle multiplicities, this advantage comes with substantially increased readout complexity. Each pixel necessitates its own dedicated readout channel, leading to a significantly larger number of electronic channels than in strip detectors. Consequently, this imposes greater demands on data acquisition systems, power consumption, and overall integration complexity. Conversely, SSDs, characterized by their linear geometry, strike a balance between spatial resolution and simplicity of readout. They require fewer channels, yet still require sufficient position information for many experimental applications. This often translates into reduced fabrication and operational costs, as well as easier data management.
The choice between strip and pixel detectors ultimately depends on the specific requirements of the experiment. Strip detectors remain a preferred solution in large-area tracking systems where one-dimensional position resolution is adequate and minimizing the number of channels is advantageous. On the other hand, pixel detectors are selected when extremely fine spatial granularity and two-dimensional

position data are essential, despite the added system complexity.
In summary, SSDs represent a mature and vital technology that balances spatial resolution, coverage area, and readout efficiency. Their widespread use continues across particle physics experiments, medical imaging, and radiation detection. While the shift towards pixelated sensors reflects advances in electronics and the pursuit of higher resolution, strip detectors remain a fundamental and highly effective instrument in detector technology.

2.6 Amorphous Silicon Sensors

Amorphous silicon (a-Si) is a non-crystalline form of silicon characterized by a disordered atomic structure, which significantly influences its electrical and optical properties. Unlike crystalline silicon, which has a well-ordered lattice, amorphous silicon exhibits a lack of long-range order, resulting in a material that can be deposited as thin films over large areas and on flexible substrates at relatively low temperatures. This unique feature makes a-Si highly versatile for a range of applications where traditional crystalline silicon is unsuitable. Furthermore, hydrogenation of amorphous silicon (a-Si:H) is commonly employed to passivate dangling bonds within the material, substantially improving its electronic properties by reducing defect states that would otherwise act as charge traps [32].
The electrical conductivity of a-Si can be tailored through doping, enabling the formation of p-i-n junctions essential for electronic devices such as thin-film transistors (TFTs), photovoltaic cells, and sensors. However, a well-known limitation of amorphous silicon is the Staebler-Wronski effect, which causes degradation in its photoconductivity under prolonged illumination, leading to decreased device performance over time [32]. Despite this, a-Si remains widely used in applications where its deposition advantages and material flexibility outweigh such drawbacks.
Amorphous silicon sensors exploit these material properties to detect physical stimuli including light, pressure, and radiation. The deposition of a-Si films on large-area substrates enables the fabrication of thin, lightweight, and cost-effective sensors, which are particularly advantageous for imaging and monitoring technologies. For instance, photoconductive and photodiode-based sensors using a-Si are extensively employed in medical imaging devices such as flat-panel X-ray detectors, where they convert incident ionizing radiation into electrical signals for image reconstruction

[33]. The inherent flexibility of a-Si also allows for sensor integration on curved or flexible surfaces, expanding potential application domains.
Additionally, hydrogenated amorphous silicon sensors exhibit noteworthy radiation hardness, making them suitable for dosimetry and particle detection in high-radiation environments such as nuclear medicine and particle physics experiments [31]. The ability to deposit a-Si on flexible substrates like polyimide films (e.g. Kapton) facilitates the construction of compact, conformable sensor arrays that maintain performance under mechanical stress. The p-i-n structure in amorphous silicon sensors allows for efficient charge collection and fast response times, critical for real-time monitoring applications (Fig. 2.8).

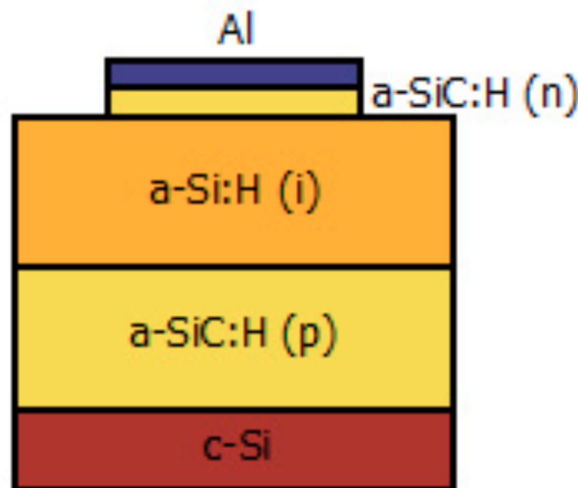


Fig. 2.8 Schematic structure of an amorphous silicon sensor highlighting the intrinsic layer and p-i-n junctions.

In comparison to conventional silicon sensors, such as silicon strip and pixel detectors, amorphous silicon sensors offer several distinct advantages and some limitations. Traditional strip and pixel detectors are fabricated from high-purity crystalline silicon, offering superior charge carrier mobility, lower noise, and excellent spatial resolution, which are essential for high-precision particle tracking and imaging in high-energy physics experiments [34]. However, their fabrication requires expensive processes, rigid substrates, and is typically limited to small areas.
On the other hand, amorphous silicon sensors, due to their large-area deposition capability and mechanical flexibility, provide cost-effective solutions for large-area detection and imaging systems, especially where ultimate spatial resolution is not the primary requirement. The trade-off lies in the lower charge carrier mobility and

the presence of localized defect states in a-Si, which result in slower response times and potentially higher noise levels compared to crystalline sensors. Furthermore, the Staebler-Wronski effect may affect long-term stability under illumination, a consideration less critical in particle detection applications where light exposure is limited.

Overall, amorphous silicon sensors complement the suite of silicon-based detection technologies, offering unique advantages in terms of scalability, flexibility, and cost, making them highly suitable for medical imaging, environmental monitoring, and applications demanding large-area sensors (Fig. 2.9). Conversely, silicon strip and pixel detectors remain the technology of choice for high-resolution and high-rate particle tracking applications.

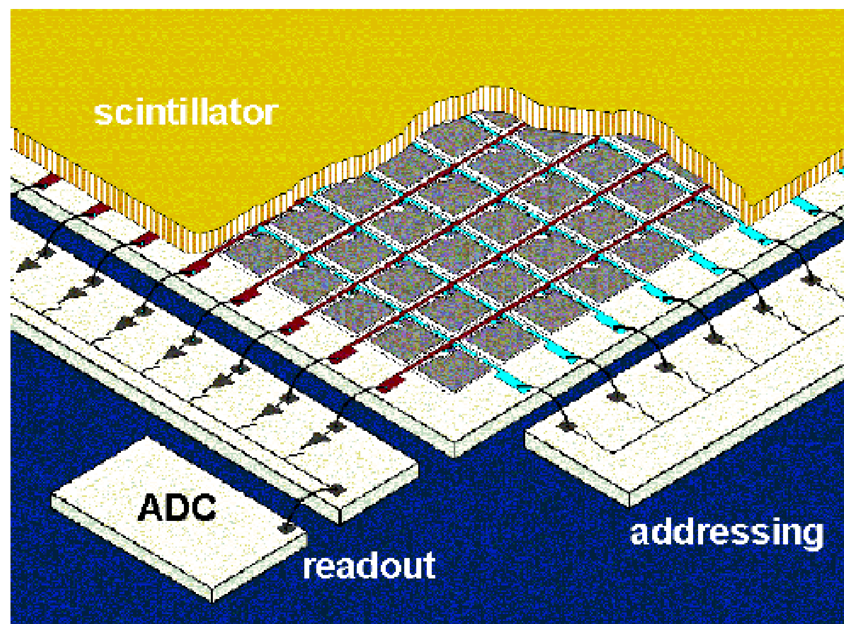


Fig. 2.9 Example of an amorphous silicon flat-panel detector used in medical X-ray imaging [11].

2.7 Readout Electronics for Silicon Detectors

The readout of silicon detectors is a crucial aspect that determines the performance, resolution, and speed of data acquisition in a wide range of applications, from high-energy physics to medical imaging. Different types of silicon detectors, such as strip

detectors, pixel detectors, and amorphous silicon sensors, employ dedicated readout systems designed to meet their specific structural and operational requirements. Central to modern readout systems are Application-Specific Integrated Circuits (ASICs), which provide tailored, compact, and high-performance signal processing directly interfaced with the sensors.

The readout ASICs for strip detectors are designed to process signals from each strip individually, amplifying and shaping the charge pulses generated by ionizing particles traversing the sensor. Due to the relatively low channel density compared to pixel detectors, these ASICs often emphasize low noise and fast shaping times to optimize timing resolution and minimize dead time.

The high channel density of pixel detectors demands ASICs with integrated front-end amplification, signal discrimination, and digital processing capabilities, often including time-stamping and zero-suppression functionalities. Pixel readout ASICs must handle significant data throughput and provide efficient multiplexing to transfer the large volumes of information generated during measurements.

Amorphous silicon sensors typically form large-area arrays with lower spatial resolution requirements compared to crystalline silicon detectors [35]. Their readout electronics often integrate TFTs directly on the substrate to enable multiplexed readout of the sensor elements. In some advanced systems, ASICs are employed to interface with the outputs of the TFT matrix, providing amplification, digitization, and further signal processing. The flexible nature and large size of amorphous silicon sensors require ASICs optimized for low power consumption and scalability rather than ultra-high-speed readout.

2.7.1 ASICs for Silicon Detector Readout

ASICs designed for silicon detector readout play a key role by integrating multiple essential functions in a compact chip tailored to the detector's characteristics and application demands [21]. Typically, an ASIC for silicon sensor readout includes the following components[36]:

- **Charge Sensitive preAmplifier:** Amplifies the small charge signals collected by the detector strips or pixels into a voltage signal suitable for further processing. It must exhibit low noise and high linearity to preserve signal integrity.

- **Shaping amplifier:** Shapes the preamplifier output signal to optimize the signal-to-noise ratio and define the pulse width, thereby improving timing resolution and minimizing pile-up effects.
- **Discriminator:** Compares the shaped signal with a programmable threshold to produce digital hits, enabling the identification of valid events in the presence of electronic noise.
- **Analog-to-Digital Converter (ADC):** Converts the analog signals into digital data for further processing and storage. Some ASICs perform this conversion on-chip, especially for pixel detectors where fine spatial information is crucial.
- **Digital processing and zero suppression:** Processes the digital signals to reduce data volume by discarding channels without significant hits and applying encoding schemes.
- **Time-stamping and synchronization:** Assigns temporal information to detected events to enable event reconstruction and correlation, particularly important in high-rate experiments.
- **Readout interface:** Manages the transfer of processed data to external data acquisition systems through multiplexed outputs or serial links.
- **Bias and calibration circuits:** Provide programmable biasing for the front-end components and allow injection of test signals for calibration and monitoring.

It should be noted that the components listed do not necessarily operate in a strictly cascaded configuration; their arrangement and interconnections may vary depending on the specific architecture and functional requirements of the ASIC.
A simplified schematic is shown in Fig. 2.10.

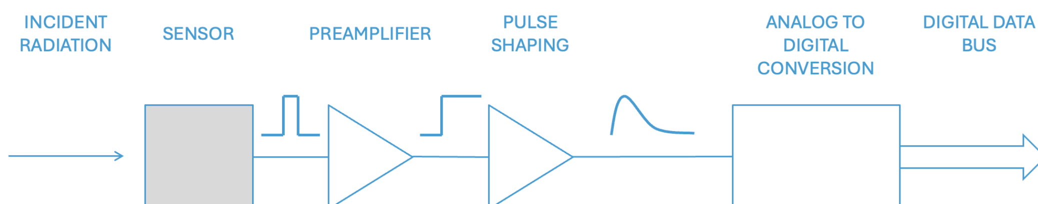


Fig. 2.10 Schematic diagram of a sensor readout

For silicon strip detectors, ASICs prioritize fast shaping and low noise performance, as the channel count is moderate and timing precision is often critical. In pixel detectors the ASICs integrate ADCs and digital logic within each pixel or pixel cluster to handle the high data density efficiently [37]. For amorphous silicon sensors, ASICs must be optimized for large-area coverage and low power, often interfacing with TFT arrays rather than individual pixels or strips.
Overall, the development of custom ASICs enables silicon detectors to meet stringent requirements in terms of spatial resolution, timing, noise performance, and power consumption, making them indispensable in modern detection systems.

2.7.2 CMOS Technology in ASICs and MOS Transistor Physics

Modern ASICs for silicon detector readout are typically implemented using CMOS technology, which offers crucial advantages:

- **Low Power Consumption:** In CMOS digital circuits, power is mainly consumed during switching, which results in high energy efficiency. However, radiation detector front-end circuits are mainly analog, and their power dissipation is directly related to performance parameters such as noise and bandwidth. The trade-off between power and noise depends on the circuit topology, but integrated preamplifiers can generally achieve wider bandwidth than discrete implementations with the same power budget because of lower parasitic effects.
- **High Integration Density:** CMOS allows integrating analog front-end amplifiers and digital processing blocks on the same chip, reducing parasitic capacitances and overall system complexity.
- **Scalability:** advances in CMOS fabrication enable transistor miniaturization, enhancing speed and reducing noise and power dissipation.
- **Radiation Hardness:** standard CMOS processes can be tailored to increase tolerance to radiation, critical in environments like particle accelerators.

A fundamental advantage of CMOS technology is the continuous scaling down of transistor dimensions, typically characterized by the channel width W and length L of the MOSFET devices [20]. The miniaturization of these dimensions allows

designers to increase the integration density significantly, packing more transistors, and consequently more functionality, into the same silicon area. This results in ASICs capable of hosting complex analog front-ends alongside sophisticated digital processing blocks, essential for managing the enormous data throughput of modern silicon detectors.
Mathematically, the transistor's current in the saturation region, which influences switching speed and gain, is approximately given by

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2, \tag{2.17}$$

where μ is the carrier mobility, C_{ox} the gate oxide capacitance per unit area, V_{GS} the gate-source voltage, and V_{TH} the threshold voltage. Reducing the channel length L while maintaining or increasing the width W generally increases the drain current I_D, thereby enhancing the transistor's speed and enabling faster signal processing [38].
However, shrinking transistor dimensions also brings several challenges. A smaller channel length L leads to short channel effect, such as drain-induced barrier lowering, increased leakage currents, and threshold voltage variability, which can degrade the analog performance crucial for low-noise front-end amplifiers. Another phenomenon to consider is the narrow channel effect, which occurs when the channel width W is reduced significantly. In this regime, the depletion regions from the channel edges penetrate further into the conductive channel, effectively increasing the threshold voltage V_{TH} and modifying the device's transconductance. This effect can limit the achievable current drive and introduce additional variability in small-width transistors, impacting the uniformity of analog front-end performance in readout ASICs.
Additionally, reduced W and L result in lower intrinsic gain and reduced voltage headroom, complicating the design of linear analog stages. The reduction of the supply voltage in advanced CMOS nodes, necessary to avoid device breakdown, further limits the dynamic range available for signal amplification.
Moreover, device mismatch and process variations become more pronounced as dimensions shrink, causing increased offset and noise in sensitive analog blocks. Designers must therefore carefully balance the trade-offs between speed, power consumption, noise performance, and reliability when choosing the transistor dimensions for front-end ASICs [39].
To visually appreciate these effects cross-section highlighting W and L is shown in Fig. 2.11.
In summary, while CMOS miniaturization has been instrumental in advancing ASIC

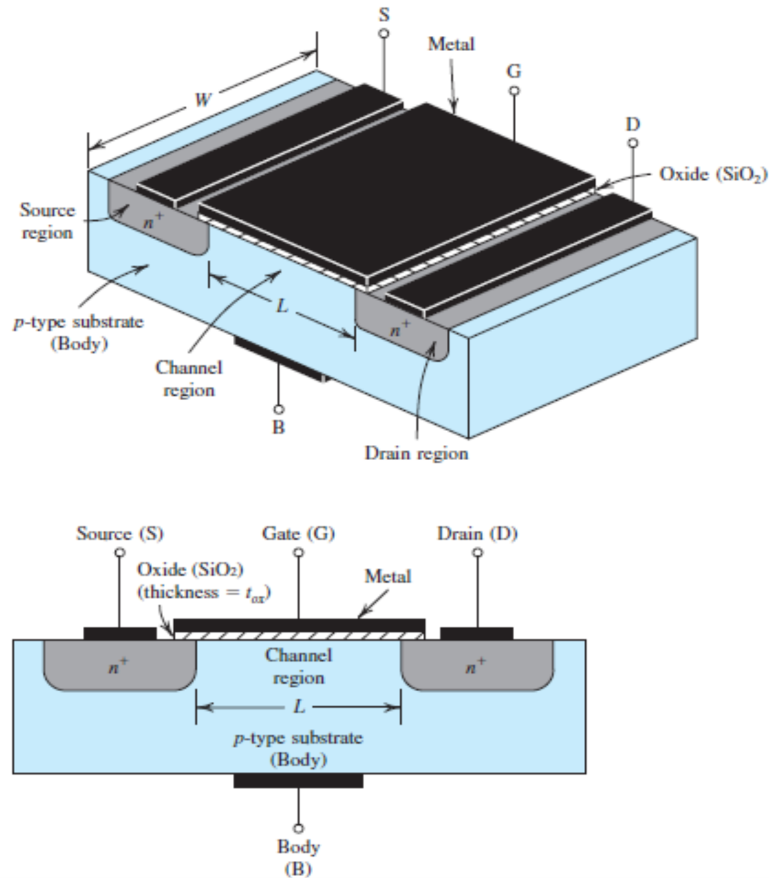


Fig. 2.11 Schematic diagram of MOSFET transistor [12].

technology for silicon detector readout, enabling higher integration, lower noise, and faster operation, it requires sophisticated circuit design techniques to mitigate the physical and electrical limitations imposed by ultra-scaled devices.
This technology based is therefore the core of most ASICs used for readout of strip, pixel, and amorphous silicon detectors, meeting their stringent requirements on power, speed, noise, and integration.

2.7.3 Charge Sensitive Amplifier

The fundamental analog block of CMOS ASICs for sensor readout is the charge sensitive amplifier (CSA), converting input charge Q into an output voltage V_{out} as:

$$V_{out} = -\frac{Q}{C_f} \tag{2.18}$$

where C_f is the feedback capacitance of the amplifier. A lower C_f improves sensitivity but can increase noise.

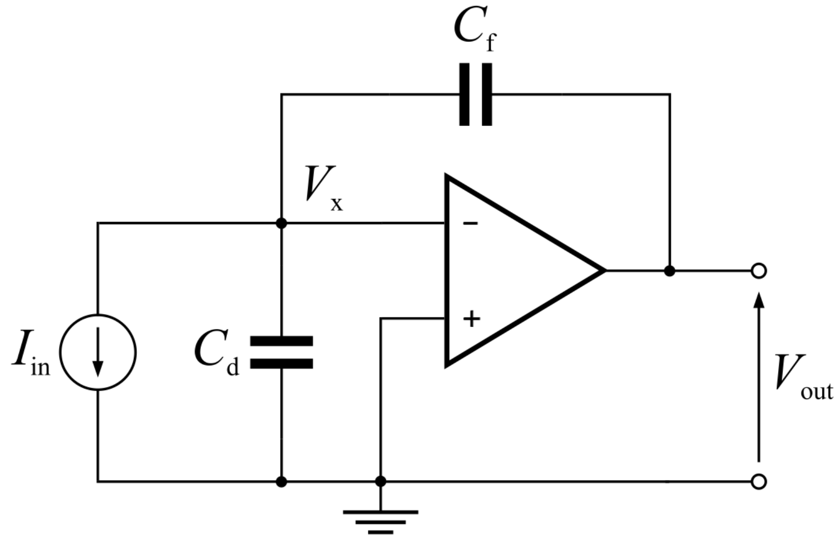


Fig. 2.12 Schematic of a charge-sensitive preamplifier.

The shaping amplifier that follows filters the signal to maximize the signal-to-noise ratio (SNR). The Equivalent Noise Charge (ENC), an important metric for front-end noise, can be modeled as:

$$ENC^2 = \frac{A_s}{\tau} C_T^2 e_n^2 + A_f C_T^2 K_f + A_p \tau i_n^2 \tag{2.19}$$

where the total input capacitance is defined as

$$C_T = C_D + C_{in} + C_{par} \tag{2.20}$$

with C_d the detector capacitance, C_{in} the input capacitance of the front-end amplifier, and C_{par} parasitic capacitance.
The other parameters are:

- e_n: spectral density of the series white voltage noise
- K_f: coefficient of the series $1/f$ noise
- i_n: spectral density of the parallel current noise
- τ: shaping time constant of the readout electronics

- A_s, A_f, A_p: dimensionless coefficients depending on the shaping filter

Optimizing τ balances noise reduction and signal processing speed.
CMOS technology also enables embedding discriminators with programmable thresholds, ADCs, digital zero-suppression logic, and time-stamping circuits, allowing efficient and precise data readout.

Chapter 3

ASICs in Particle Physics

3.1 What is an ASIC

An Application Specific Integrated Circuit (ASIC) is an integrated circuit designed to perform a very specific function, unlike more general purpose devices such as microcontrollers or FPGAs, which can be reprogrammed for different tasks. The choice of an ASIC is motivated by the need to achieve optimal performance in terms of speed, power consumption, size, and reliability, especially when the device must operate in complex applications or challenging environments, such as high-energy physics experiments.
ASICs can be designed for a wide range of applications, from telecommunications to imaging systems, to particle detectors. The design process involves an initial detailed specification, followed by circuit simulations, physical implementation, and prototype testing. Once produced, an ASIC cannot be reprogrammed, but it provides highly optimized performance compared to general purpose solutions.
In particle physics, ASICs are essential for reading out signals from high-granularity detectors, where it is necessary to measure with precision the Time of Arrival (ToA), signal amplitude, and simultaneously handle large data flows without introducing errors or losses.
In this chapter, two examples of ASICs developed for particle physics experiments will be presented:

1. **ToASt**: a 64-channel ASIC developed for the *Micro-Vertex Detector* of the *PANDA* experiment at FAIR, designed to measure both the ToA and the charge deposited by a particle in silicon strip detectors.
2. **CLEOPATRA**: an ASIC developed within the *HASPIDE* project, for the measurement of the integrated charge deposited and adapted to the specifications of that detector and its experimental environment, focusing on large dynamic range and optimized signal handling under challenging conditions.

The following sections will describe in detail the operating principles, internal architecture, calibration strategies, performance results, and the design choices made for these ASICs, highlighting similarities and differences between the two chip families.

3.2 ToASt

ToASt ASIC is a 64-channel chip specifically designed for the readout of silicon strip detectors in the PANDA MVD. Its architecture is optimized to measure both ToA and Time-over-Threshold (ToT) of the detector signals while handling high data rates and ensuring radiation tolerance.
The ASIC is fabricated using a commercial CMOS 110 nm process. This technology provides a good compromise between high-speed performance, power consumption, and radiation hardness. The chip has a total area of approximately 4.5×3.5 mm² and a nominal power consumption of around 180 mW.
ToASt ASIC provides spatial, energy and time information of the particle crosses the detector:

- **spatial information**: the position of the strip given by the associated channel number.
- **energy information**: the charge deposited in the detector measured from the difference between the trailing and the leading edge arrival time, i.e. with the ToT method.
- **timing information**: the ToA given by the rising edge arrival time.

In terms of hardware architecture, as shown in Fig. 3.1, the 64 channels are organized into 8 regions, each containing the logic required for reading and configuring 8 channels, as well as a 16-cell FIFO memory for data buffering. The entire data acquisition system is coordinated by a global read unit, which includes a 64-cell FIFO and two 160 Mb/s high-speed serial links for transmission of the acquired data.

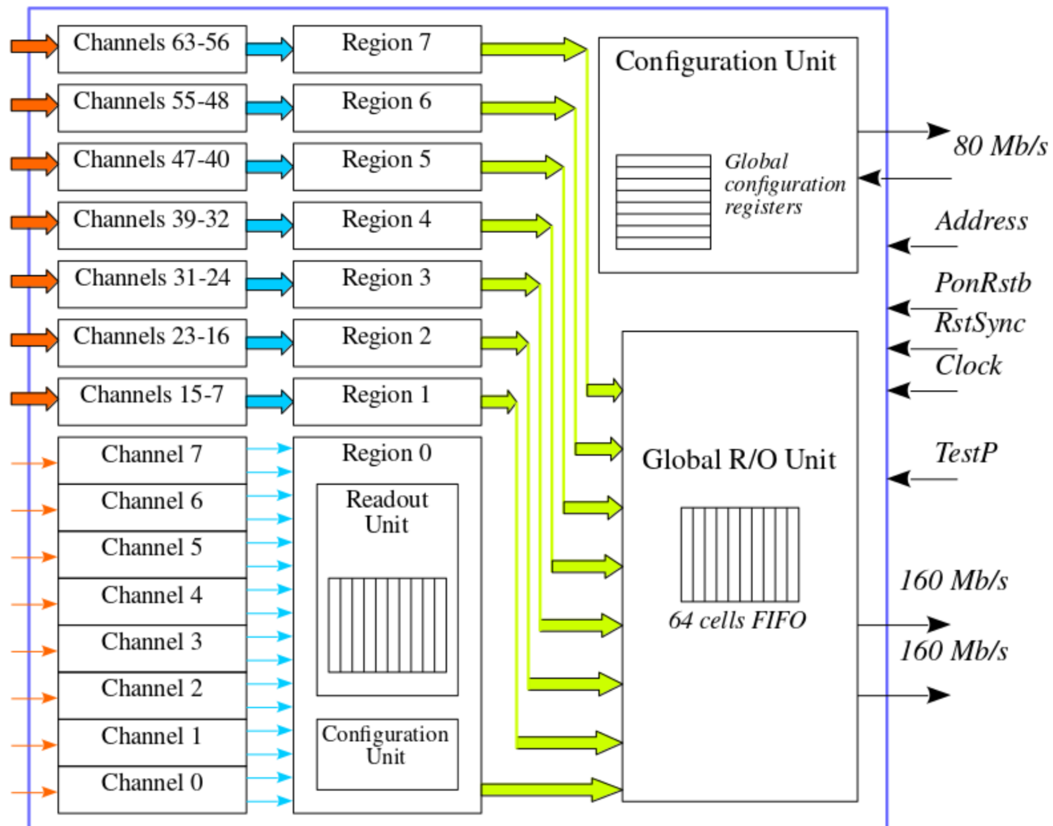


Fig. 3.1 ToASt architecture schematic [3].

Each of the 64 channels contains the following main blocks:

- **Charge-Sensitive Amplifier (CSA)**: converts the charge collected by the silicon strip into a voltage signal suitable for processing. It has a nominal gain of 5 mV/fC and can be configured to accept current inputs from either n-type or p-type detector signals.
- **Shaper**: shapes the analog signal to optimize the timing measurement and reduce noise. It has an adjustable peaking time to adapt to the increase of the leakage current in the detector due to the radiation damage.

- **Current buffer**: provides the current that will be integrated by the following stage.
- **Integrator stage**: where the feedback capacitor is discharged by a constant current to provide a linear ToT.
- **Dual-threshold comparator**: measures both the ToA and the signal amplitude (via ToT) by comparing the shaped signal against two programmable thresholds. Due to the linear discharge of the integrator capacitor, the duration of the comparator outputs is linearly proportional to the input charge.

The blocks are shown in Fig. 3.2.

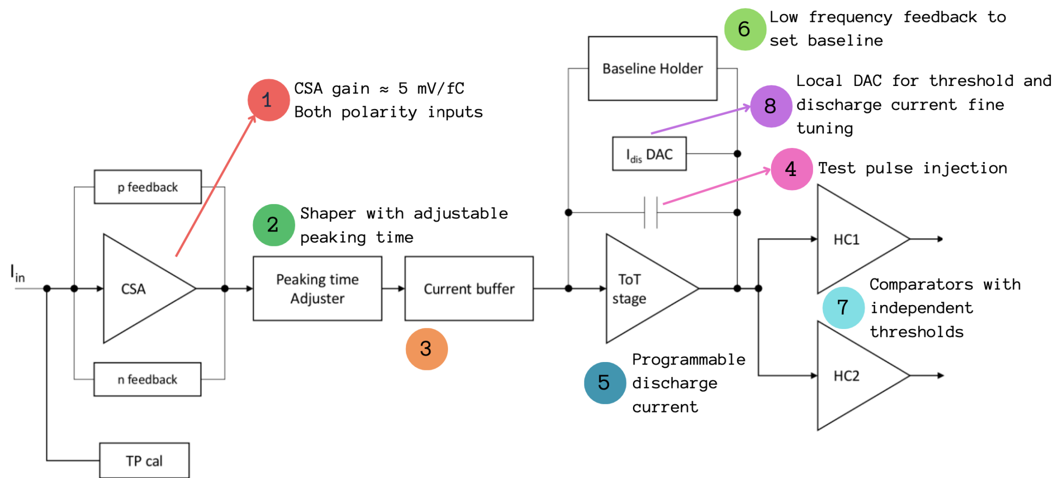


Fig. 3.2 ToASt channel schematic.

An important feature of ToASt is the ability to configure the system to accept signals of either polarity, which allows compatibility with different types of semiconductor detectors. In particular, the chip can operate with both n-type and p-type strips, by selecting the desired bit. This choice was made to adapt to the type of the coupled sensor.

The most relevant technical specifications of ToASt are summarized in Table 3.1.

The overall chip configuration is managed by a dedicated global unit, which uses a serial interface operating at half the main clock frequency to program the configuration registers for the ASIC control. This interface ensures that data from all 64 channels are efficiently transmitted without loss, even under high hit rates. In detail, the system allows control of 16 Global Configuration Registers (GCRn), 16 Regional

Configuration Registers (RCRs) distributed over 8 regions and 192 configuration registers dedicated to individual channels (3 for each channel).

Input capacitance	2 ÷ 17 pF
Max rate per strip	50 kHz
Input charge range	1 ÷ 40 fC
Max noise	1500 e.n.c.
Peaking time	50-100 ns
Channels per chip	64
Channel pitch	66 μm
Reference clock	160 MHz
Charge resolution	8 bits
Time resolution	6.25 ns (pk-pk)
	1.8 ns (r.m.s.)
Output drivers	2×160 MS/s
Max output rate	2×4.9 Mevents/s
Power consumption	180 mW @ 1.2 V
Die size	3.24 × 4.41 mm^2
Pads position	On two sides only

Table 3.1 ToASt specifics [3]

The analog frontend integrates two comparators, one with a lower threshold (time threshold, V_{th_T}), which is useful for accurately identifying the rising edge of the signal (leading edge), where the variation is steepest even for low amplitude signals. The second comparator, set at a higher threshold (energy threshold, V_{th_E}), allows the event to be validated by reducing the possibility of false positives due to noise fluctuations.

This dual comparator architecture allows the timestamp to be stored at the lower threshold, while at the same time confirming the event only if it also exceeds the energy threshold, as schematized in Fig. 3.3. However, it is possible to disable this mode and use a single comparator with a single threshold (the energy threshold) if a simpler configuration is preferred or the experimental context requires it. Setting independent thresholds for the two comparators minimizes jitter in weak signals while maintaining a reliable discrimination against dark noise.

To achieve proper signal discrimination and reliable charge measurement by the ToT

method, the ASIC ToASt provides adjustment mechanisms for both the threshold voltages (time and energy) and the current used in the ToT generator. These adjustments can be made either globally with a coarse resolution and at the channel level with a finer one:

- Coarse tuning: at the global level, two 5-bit DACs are employed to adjust the time and energy thresholds, respectively. These DACs are configurable via the GCR12 register and cover a range of 494 mV with a LSB of 15 mV. Since the DAC current sources are implemented with pMOS transistors, the DAC logic is reversed: the binary value `0` corresponds to the maximum threshold, while `31` represents the minimum threshold.
- Fine tuning: at the channel level, additional 6-bit DACs, configurable via the CCR1 register, are available for both thresholds. The overall range is 84 mV with a resolution of about 1.3 mV. Again, the logic is reversed: `0` indicates the highest threshold and `63` the lowest.

The current used for ToT measurement can also be adjusted:

- Coarse tuning: a 5-bit global DAC, configurable via the `GCR13` register, allows selection of a current value between 2.1 nA and 488 nA, in increments of 15.2 nA.
- Fine tuning: each channel has a 5-bit DAC for local tuning. The resolution (LSB) of this DAC depends on a second global 5-bit DAC, which is also managed via `GCR13`. This allows for:
  - a minimum range equal to 27 nA with LSB of 0.84 nA;
  - a maximum range equal to 906 nA with LSB of 28.3 nA.

ToASt ASIC is designed to operate reliably in the radiation environment of the PANDA Micro-Vertex Detector. The electronics must withstand both cumulative and instantaneous radiation effects without significant degradation in performance. The ASIC is specified to tolerate a Total Ionizing Dose (TID) consistent with the expected lifetime exposure in the MVD.
Another radiation effect is the Single-Event Upsets (SEU) which are transient errors induced by high-energy particles. To mitigate these effects, ToASt ASIC incorporates:

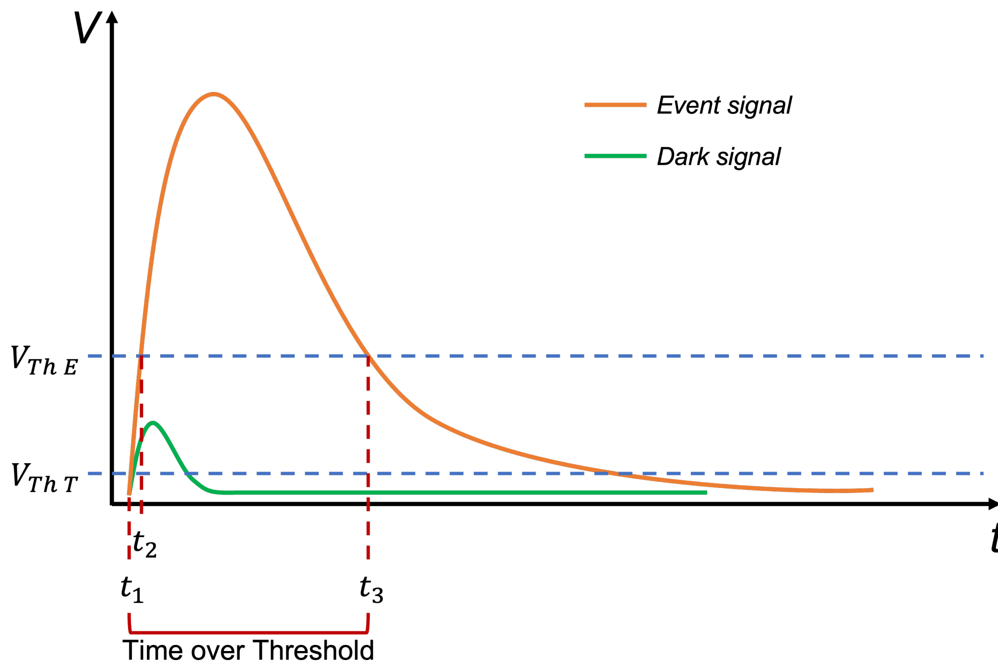


Fig. 3.3 ToT measurement with dual-threshold method

- Triple Modular Redundancy (TMR) for critical flip-flops
- Triplicated clock and reset nets
- Error detection and correction for configuration registers

ToASt ASICs are managed and controlled by the Module Data Concentrator (MDC), which acts as an interface between the front-end electronics and the Data Acquisition System (DAQ) of the PANDA experiment.
Each MDC receives and processes the data streams from up to eight ToASt chips, ensuring synchronization, configuration management, and coherent time alignment among all channels. Moreover, the MDC supervises the operation of ToASt ASICs, controlling their configuration and power modes to optimize system efficiency and stability.
The overall architecture of the readout chain, including the connection between the silicon sensor, ToASt, and MDC, is illustrated in Fig. 3.4.

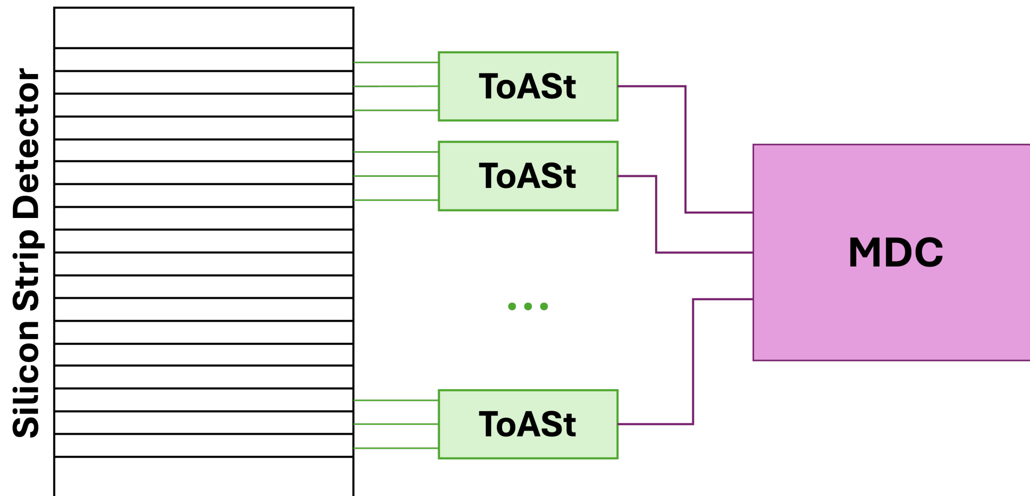


Fig. 3.4 MDC diagram

3.2.1 Test-pulse Control

ToASt ASIC has a built-in feature that allows the controlled injection of a test charge at the input of each channel in order to verify its proper operation and characterize its performance in the absence of real signals from the detector. This mode is particularly useful during calibration, laboratory testing and diagnostic phases.
Charge injection is triggered by an external signal called TestP, which generates a pulse whose rising edge and falling edge correspond to two complementary charge pulses. However, for the test to be meaningful, only one of the two fronts needs to be considered. Depending on the channel polarity setting : in polarity 1 (0) the rising (falling) edge of the TestP signal should be used.
If the other edge (the opposite edge with respect to the configured polarity) is also mistakenly considered, abnormal system behavior may occur: in particular, the charge-sensitive amplifier (CSA) may go into saturation and get stuck for a significant amount of time, during which the channel is inoperative. The duration of this blockage depends on the amplitude of the injected pulse. Under extreme conditions, recovery times up to about 1 us can be observed for pulses in the low end of the range and up to 1.6 us for pulses in the high end.
In order to inject charge in a specific channel, both the global calibration (bit 7 of GCR14) and the channel calibration (bit 5 of CCR0) must be set to 1.
Once enabled, the magnitude of the injected test charge is determined by the contents of the GCR14 register, specifically by bits 0 to 5 (GCR14[5:0]), which control the

amplitude of the test pulse voltage. This pulse is an inverted copy of the TestP signal and is transferred to the channel via a 350 fF series capacitor, which generates the two complementary charge components (one positive and one negative).
Two ranges of the injected charge are available : [0 ÷ 16 fC] and [0 ÷ 65.8 fC]. They can be selected via GCR14 bit 6.
A complete overview of the configurable values and the charge associated with the various DAC codes is given in Table A.1, which provides a useful reference for calibrating channel response.

3.2.2 Peaking-time Adjustment

The peak time (*peaking time*) is defined as the time required for the output pulse from the shaping circuit to reach its maximum value after the arrival of the input signal. Its adjustment is critical to adapt the behavior of the front-end system according to the expected pulse duration or electronic noise present.
In the ASIC *ToASt*, the peak time adjustment is done through bits 11 and 10 of the *GCR6* register. These two bits allow a discrete value of the peak time to be selected within a range of 50 ns to 100 ns. The mapping of the bits is as follows:

- `00` → minimum peak time (approximately 50 ns)
- `01` → intermediate value
- `10` → upper intermediate value
- `11` → maximum peak time (approximately 100 ns)

The ability to adjust this parameter makes the ASIC more flexible and suitable for different experimental applications, providing the best possible trade-off between temporal resolution, noise filtering and pulse width.

3.2.3 Channel Control Unit

The Channel Control Unit (CCU) is the digital block responsible for managing the operations of each channel. It receives as inputs the comparator outputs from the Energy Branch (EB) and Time Branch (TB) of the Analog Front-End (AFE),

together with a 12-bit timestamp provided by the global controller through the region controller.

The CCU includes four 12-bit register: two event registers (leading-edge and trailing-edge) for storing timestamp values, and two configuration registers for local control settings. The leading-edge register stores the timestamp at the rising edge of the comparator signal, while the trailing-edge register records the timestamp at the falling edge. The first value corresponds to the ToA of the event, whereas the difference between the two values provides the ToT, which is proportional to the deposited energy. Once an event has been processed, a data ready flag is generated. If a freeze signal is active, the event is kept internally but no data ready flag is asserted. This signal is generated by higher-level control logic to ensure proper synchronization and data framing across channels. Its generation conditions and management are described in more detail in Section 3.2.4. This mechanism ensures proper framing of the output data, meaning that each data unit is correctly structured with identifiable boundaries and necessary control information. Proper framing allows the receiver to interpret the data accurately and detect errors, preventing misalignment or miscommunication. Importantly, events whose leading edge arrives before the freeze activation are still read out. A busy flag is asserted whenever a channel has detected a leading edge and is waiting for the corresponding trailing edge.

Under standard operation, the rising edge of the TB comparator defines the leading-edge timestamp, while the trailing-edge timestamp is captured on the falling edge of the EB comparator, provided that an EB rising edge has occurred before the TB falling edge. If this condition is not met, the event is discarded. When the single-threshold mode is enabled, both timestamps are taken from the EB signal, and the TB comparator is ignored. In the leading-edge-only mode, only the first timestamp is stored. This configuration is particularly useful at high event rates, where the ToT measurement would lead to a non-acceptable dead time. In such cases, the ToT discharge current should be set to its maximum value to minimize the dead time of the AFE.

The channel diagram is shown in the Fig. 3.5.

The configuration registers of the CCU are organized as specified in Table A.2. Calibration DAC ranges are referenced to the values defined by the global calibration DACs, while a range bit allows halving the LSB step size ($0 \rightarrow 3.12$ mV, $1 \rightarrow$

1.56 mV). In addition, the CCU receives the set of global configuration signals summarized in Table A.3.

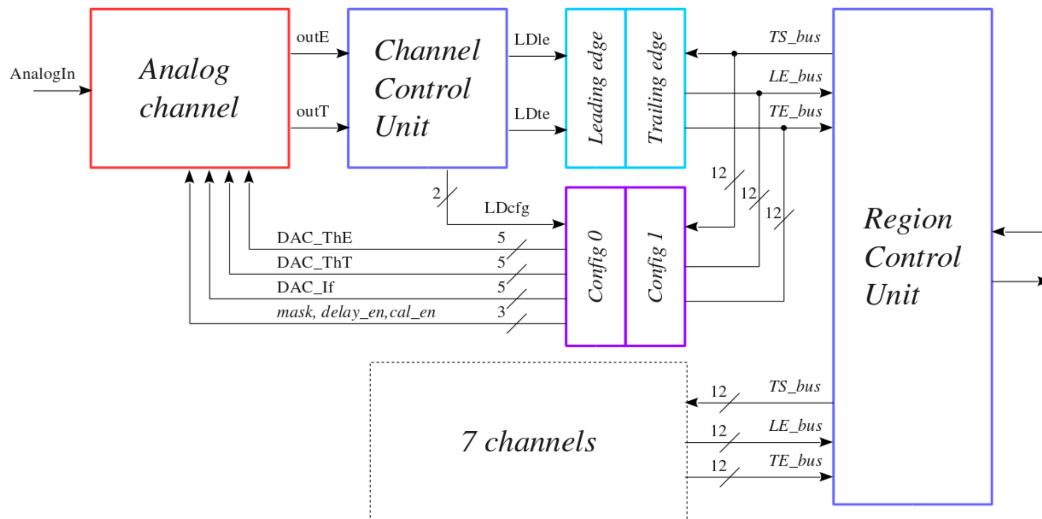


Fig. 3.5 ToASt channels diagram.

3.2.4 Region Control Unit

Each of the 8 region is managed by the Region Control Unit (RCU), which continuously scans the eight channels in a round-robin algorithm. For each channel, the RCU records the channel address along with the leading and trailing-edge timestamps, storing this information in a 27-bit, 16-cell FIFO protected with Hamming coding. Each region also includes two 12-bit read-only registers, summarized in Table A.4. The first register, RCR0, keeps track of the number of SEUs that have been corrected by the TMR mechanism within the region, covering the eight channels, the region controller, and the regional FIFO. The second register, RCR1, reflects the status of the busy signals from all eight channels. This feature allows the detection of faulty or noisy channels that may block the acquisition logic. At the system level, such problematic channels can be selectively masked to ensure proper operation of the data acquisition chain.

Freeze management

The freeze signal becomes active when the timestamp counter rolls over and is released once both the busy and data ready signals are inactive. As a result, all events whose leading edge occurred before the counter rollover are guaranteed to be read out prior to those occurring afterward, regardless of the length of their ToT.

3.2.5 Global Readout Unit

The Global Readout Unit (GRU) handles the collection and transmission of data from the different regions of ToASt chip. The structure of the output data is arranged in 32-bit words, which include the region and channel identifiers (2×3 bits) together with the leading and trailing-edge timestamps (2×12 bits). Data produced within the same timestamp counter cycle are grouped into frames, each bounded by a frame header and a frame trailer. The frame header carries the chip identifier (defined by the seven address pads) and the frame number assigned by the frame counter. The trailer, instead, specifies the total number of data words within the frame and appends a 16-bit CRC for error checking. In cases where no valid data are available, a synchronization packet is sent instead.
The output data format is described in Table 3.2.

Packet type	**Bits** 2 bits	**Description** 30 bits
Data	11	Region[2:0] Channel[2:0] Le[11:0] Te[11:0]
Header	10	10 ChipId[6:0] Reserved[12:0] FrameN[7:0]
Trailer	01	01 DataCnt[11:0] CRC[15:0]
Sync	00	00 1100 1100 1100 1100 1100 1100 1111

Table 3.2 Data formats

3.2.6 Global Control Unit

The Global Control Unit (GCU) controls the 8 regions corresponding to the 64 ToASt channels.

Reset management

The reset input of the chip is synchronous and controls two separate internal reset signals: the global reset and the time stamp counter reset. The generation of these internal signals depends on the duration of the external reset signal according to the following rules:

- A reset pulse of duration equal to 1 clock cycle is ignored.
- A reset pulse of 2 clock cycles generates a time stamp counter reset of 2 cycles.
- A reset pulse of 3 clock cycles duration is ignored.
- A reset pulse of 4 or 5 clock cycles generates both a global reset and a time stamp counter reset, with a pulse duration of 2 cycles.
- For reset pulses longer than 5 cycles ($n > 5$), both global and counter resets are generated, with a pulse duration of $(n-3)$ clock cycles.

Resetting the time stamp counter also causes the readout logic to be reset; therefore, whenever the configuration of the output driver enablers is changed, this reset signal must be sent to make the changes effective.

Configuration control

The configuration control logic acts as an interface between the external system and the configuration registers of ToASt. It receives 16-bit commands via a serial link operating at half the main clock frequency of the chip, and returns 16-bit data via an output serial link with the same reduced frequency.
The operating codes (opcodes) used are given in Table 3.3. In them, $a_6a_5a_4a_3a_2a_1a_0$ represents the 7-bit chip address, while `aB` is the broadcast address that allows the command to be executed simultaneously on all connected chips.
The interpretations of the addresses are as follows:

- **GCR write**: the bits $d_{11}d_{10}d_9d_8d_7d_6d_5d_4d_3d_2d_1d_0$ represent the 12 bits of data to be written to the register.
- **Region and channel selection**: $r_2r_1r_0$ is the region address, $c_2c_1c_0$ is the channel address.

Function	**Data** 4 bits	**Op code** 12 bits
Chip Select	1101	$01a_Ba_6a_5a_4a_3a_2a_1a_000$
Chip Deselect	0000	00xx xxxx xxxx
Register select (channel)	0100	$0000r_2r_1r_00c_2c_1c_0a_0$
Register select (region)	0100	$0000r_2r_1r_01a_3a_2a_1a_0$
Register select (global)	0100	$00010a_6a_5a_4a_3a_2a_1a_0$
Register write	0101	$d_{11}d_{10}d_9d_8d_7d_6d_5d_4d_3d_2d_1d_0$
Register read	0110	0000 0000 0000
No operation	1111	0000 0000 0000
GCR read word	1000	$d_{11}d_{10}d_9d_8d_7d_6d_5d_4d_3d_2d_1d_0$
Channel register read word	1010	$d_{11}d_{10}d_9d_8d_7d_6d_5d_4d_3d_2d_1d_0$

Table 3.3 Configuration operation codes

- **Channel selection by DAC register**: `a0` selects between the current DAC register (DAC_{If}, value 0) or the threshold DAC register (DAC_{th}, value 1).
- **Write to channel**: if current DAC is selected, the bits `d4d3d2d1d0` are written to the current DAC register of the channel. On the other hand, if threshold DAC is selected, the bits $d_9d_8d_7d_6d_5$ are written to the energy threshold DAC register (DAC_{th_E}), while $d_4d_3d_2d_1d_0$ are written to the time threshold DAC register (DAC_{th_T}).

The received command is immediately relayed back out via the serial link for cross check. After a read command, the configuration is not ready to accept a new command until the output word has been completely transmitted; therefore, further commands should be avoided in this interval in order not to interrupt or reset the serial link. Data word alignment is performed only after a reset, so it is recommended to enter commands of type No Operation (Nop) to properly maintain alignment during operation.
ToASt operations are managed through 12 global configuration registers GCR. The assignment of bits in the GCR0 and GCR1 registers is shown in Tables A.7 and A.8.

3.2.7 ToASt v2

The second version of the ASIC introduces several significant design enhancements aimed at improving both the performance and reliability of the device.

Firstly, an internal bandgap voltage reference has been integrated, thus avoiding an external component. This internal reference can be enabled or disabled according to specific application needs, offering increased flexibility in chip operation.
Moreover, the resolution of the per-channel threshold voltage DAC has been improved from 5 bits to 6 bits. This enhancement allows for much finer and more precise threshold calibration, which is essential for optimizing channel performance in detail.
From the region management perspective, the Region Control Registers have been expanded to include counters dedicated to monitoring Single Event Upsets (SEUs), which are transient faults caused by ionizing particles affecting digital circuits. Additionally, integrated busy status monitors have been added to detect and diagnose potential blocking or overload conditions within the chip regions.
Finally, the Global Control Registers have been extended with new features to support SEU counting at the chip-wide level, enhancing the system's robustness and self-diagnostic capabilities.
These improvements mark a significant advancement in the evolution of ToASt ASIC, contributing to increased precision, reliability, and error management in signal detection and readout.

3.3 CLEOPATRA

The ASIC named CLEOPATRA [40] represents an electronic front-end solution developed for direct interfacing with dosimeter sensors made of hydrogenated amorphous silicon (a-Si:H), with a focus on space, biomedical and environmental applications, where a combination of compactness, low power consumption, high integrability and robustness against radiation is required.
The need for dedicated ASIC design arises from the physical and operational peculiarities of a-Si:H sensors. This material, although less efficient than crystalline silicon in terms of mobility and charge collection, has significantly higher resistivity, which allows the fabrication of large-area passive devices with minimal leakage currents. In addition, fabrication versatility allows for variable geometries and flexible substrates, making readout circuitry capable of adapting to different values of input capacitance, geometric extensions, and particle fluxes a must.
CLEOPATRA adopts a current-to-frequency architecture (Fig. 3.6), in which the

current generated by the sensor is converted into a proportional digital frequency through a process of discrete integration and time quantization. This circuit choice enables continuous and accurate measurement of the input current, with a wide dynamic range and high noise robustness, which is particularly advantageous for medical applications where it is important to measure with high linearity both the dose delivered to the tumor and the (unwanted) dose on the healthy tissue.
The core of each analog channel consists of:

- an **active integrator** based on an Operational Transconductance Amplifier (OTA), designed to operate with input currents on the order of pA on input capacitances up to 50 pF;
- a programmable threshold **comparator**, synchronized with a 640 MHz reference clock, to stabilize digital signal generation;
- a logically controlled **charge injection circuit**;
- a **control logic** for generating and managing the digital response pulses.

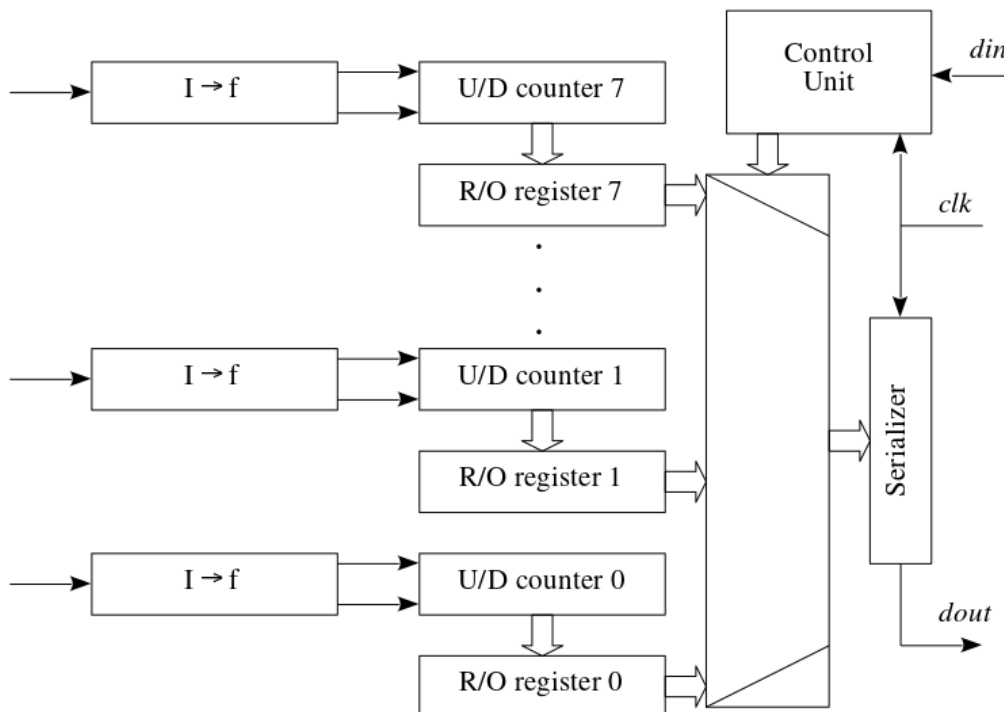


Fig. 3.6 CLEOPATRA architecture

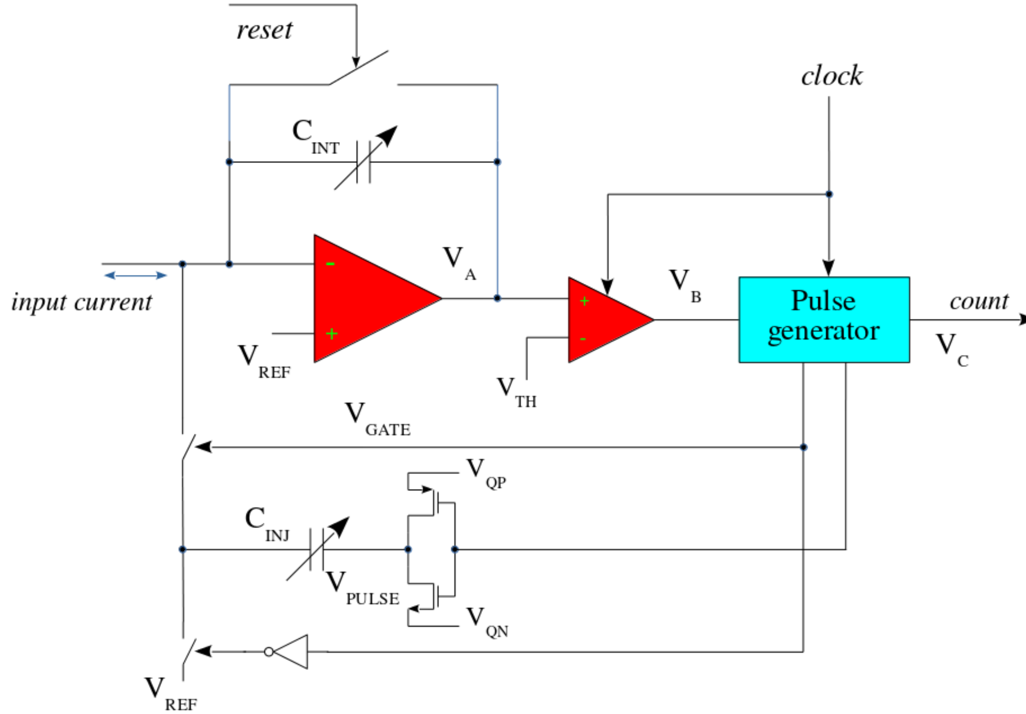


Fig. 3.7 Schematic diagram of CLEOPATRA front-end circuit

Fig. 3.7 shows the functional block diagram of the front-end circuit, highlighting the interactions between the main modules. All channels occupy the same physical area of 112 μm $\times$ 64 μm and share compatible layouts, facilitating replacement and integration in multichannel arrays.
The operating principle is based on the continuous integration of the input current I_{in} by the OTA on the feedback capacitor C_f, with the output voltage V_{CSA} increasing linearly over time second:

$$\frac{dV_{CSA}}{dt} = \frac{I_{in}}{C_f} \tag{3.1}$$

When V_{CSA} exceeds the preset threshold V_{thr}, the synchronized discriminator generates a logic pulse that activates the injection circuit. This injects a quantized charge packet Q_q of opposite sign to that of the signal, obtained by switching a capacitor C_q between two voltage levels V_{ih} and V_{il}:

$$Q_q = (V_{ih} - V_{il}) \cdot C_q \tag{3.2}$$

The effect is an abrupt transition of V_{CSA} to lower values, resulting in a reset of the cycle. The time required to reach the threshold is inversely proportional to the input current:

$$t_{thr} = \frac{Q_q}{I_{in}} \Rightarrow f_{out} = \frac{1}{t_{thr}} = \frac{I_{in}}{Q_q} \tag{3.3}$$

The output frequency is thus a direct measure of the input current, independent of the effective threshold and robust to circuit variations since it depends, at first order, only on the Q_q value.
The maximum counting frequency is:

$$f_{max} = \frac{f_{clk}}{4} \Rightarrow I_{max} = f_{max} \cdot Q_q = \frac{Q_q \cdot f_{clk}}{4} \tag{3.4}$$

CLEOPATRA allows configuration of the amount of charge injected via a bank of programmable capacitors (C_q varying from 20 fF to 140 fF in steps of 20 fF) and by adjusting voltage levels.
Since the OTA performances are the limiting factor to the max frequency, the design includes three separate versions of the CSA, optimized for different operating conditions:

1. Two-stage op-amp with active Feed-Forward current compensation (FF), for high gains and stability with high capacitance ($\sim$100 μW consumption), Fig. 3.8;

2. Two-stage op-amp with Telescopic second Stage (TS), characterized by high bandwidth and low consumption ($\sim$30 μW), ideal for fast signals and low capacitance, Fig. 3.9;

3. Two-stage op-amp with telescopic second stage and Gain Boosting (GB), combining high amplification and good dynamic stability ($\sim$90 μW), Fig. 3.10.

Finally, a reset mode that can be activated via digital signal (RST) has been provided to prevent static circuit locks due to abnormal conditions. The Signal-to-Noise Ratio (SNR) can be improved by integrating the signal over larger time windows, at the expense of instantaneous response. CLEOPATRA ASIC thus proves to be an extremely flexible and configurable platform for reliable readout of thin-film

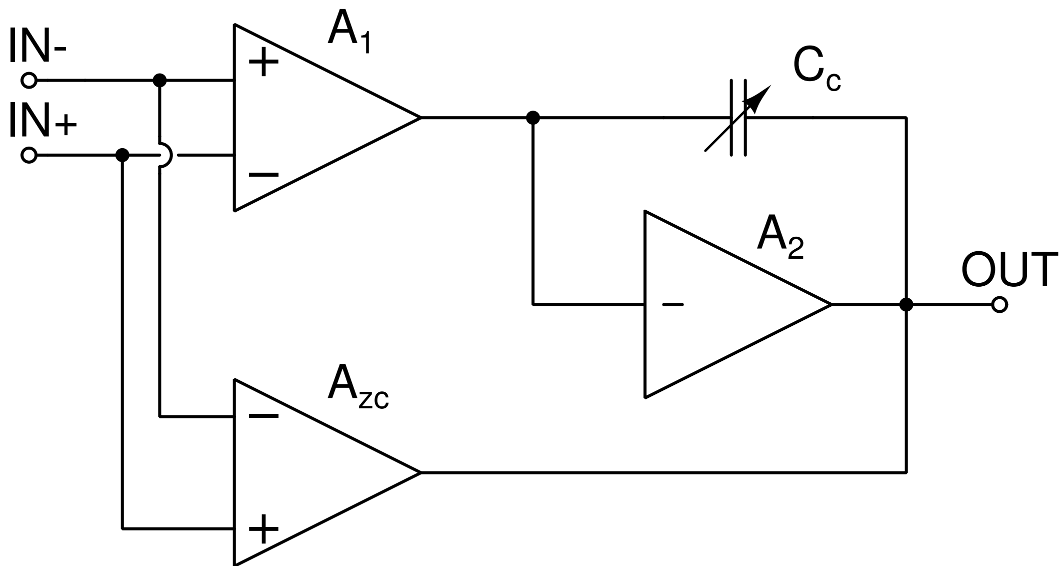


Fig. 3.8 Schematic diagram of the feed-forward amplifier.

dosimetry sensors in complex environments.
Fig. 3.11 shows the layout of the ASIC.
CLEOPATRA ASIC was designed to include an analog section consisting of a total of 12 readout channels, divided into three distinct architectural variants. Each group of channels implements a different analog front-end configuration, specifically in the topology of the OTA used for the active integrator circuit. This modular strategy allows a comparative analysis between different circuit solutions in terms of noise, bandwidth, power consumption, and interfacing capability with a-Si:H sensors having different capacitive characteristics.
The three architectures implemented in the different channel groups are distinguished as follows:

- CSA ZC (channels 0-3): employs a two-stage amplifier with feed-forward compensation, designed to provide a good trade-off between stability and fast response.
- CSA G (channels 4-7): employs a single-stage amplifier based on a folded cascode configuration, optimized to achieve high response speed with a small circuit footprint and low power consumption.

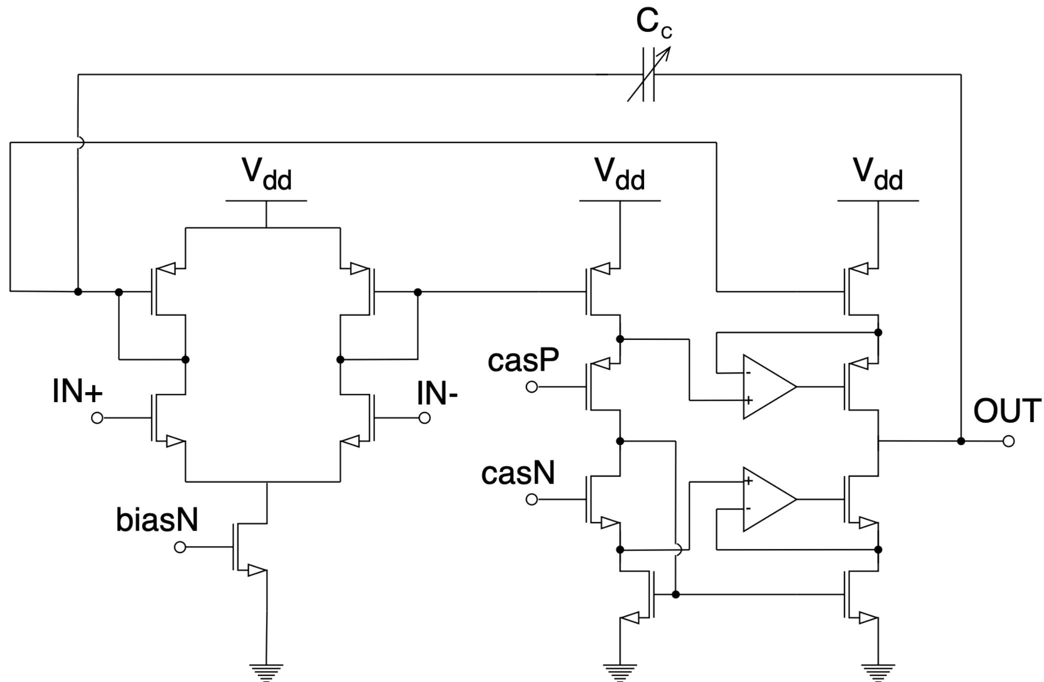


Fig. 3.9 Schematic diagram of the two-stage amplifier.

- CSA GB (channels 8-11): also adopts a single-stage folded cascode configuration, but integrated with a gain boosting technique, which allows a significant increase in open-loop gain without compromising the bandwidth.

The three OTA architectures have been designed to study the behavior of the different topologies in real application scenarios, particularly in reading signals generated by hydrogenated amorphous silicon thin-film sensors, whose capacitance can vary significantly depending on geometry and manufacturing process.
Reference values for the bias voltages and currents required for the proper operation of the analog section are given in Table B.1.

3.3.1 Input serial link

The input section of the serial link is responsible for receiving data via the differential `din±` inputs, which are essential for acquiring the control signals required for operation of CLEOPATRA ASIC. This interface supports the reception of commands encoded on 16 bits, transmitted via a serial link operating at half the system's main clock frequency. In parallel, data are returned via an output serial channel using the

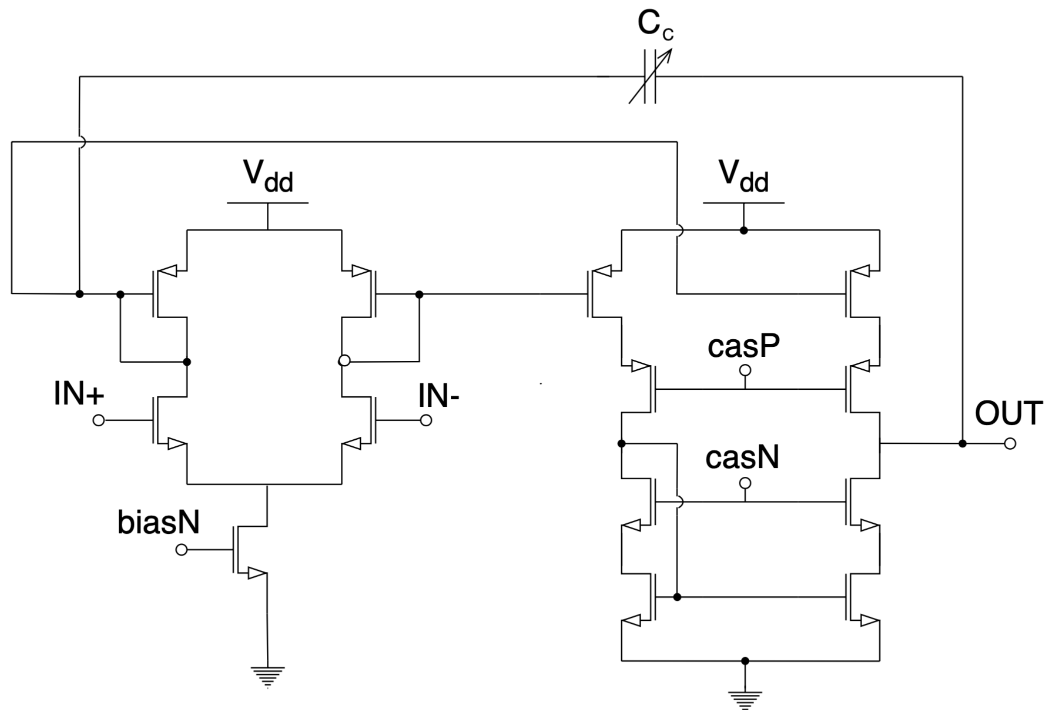


Fig. 3.10 Schematic diagram of the two-stage amplifier with gain boosting.

same reduced frequency, thus ensuring precise synchronism between transmission and reception.

The operation codes handled by this protocol are detailed in Table B.2. Each command is addressed to a specific chip identified by a 7-bit address, represented by the sequence $a_6a_5a_4a_3a_2a_1a_0$, or it can be sent in broadcast mode (a_B), so that all connected devices execute the command simultaneously. In the first prototype of CLEOPATRA, version v1, due to the limitations of pins available on the package, the chip address was set internally to the hexadecimal value `0x17`. In addition, this version has only 7 global registers, while the structure has been retained so that the number of registers can be extended, such as by single channel or by region, in future revisions of the device involving more channels.

Seven 12-bit configuration registers are integrated in the device. The configuration of the individual bits of the registers 0 to 5 is shown in Table B.3 This register structure and the flexibility of the serial protocol make it possible to precisely and modularly configure the behavior of CLEOPATRA ASIC, thus adapting it to the specific needs of the various sensors and applications envisaged in the HASPIDE project.

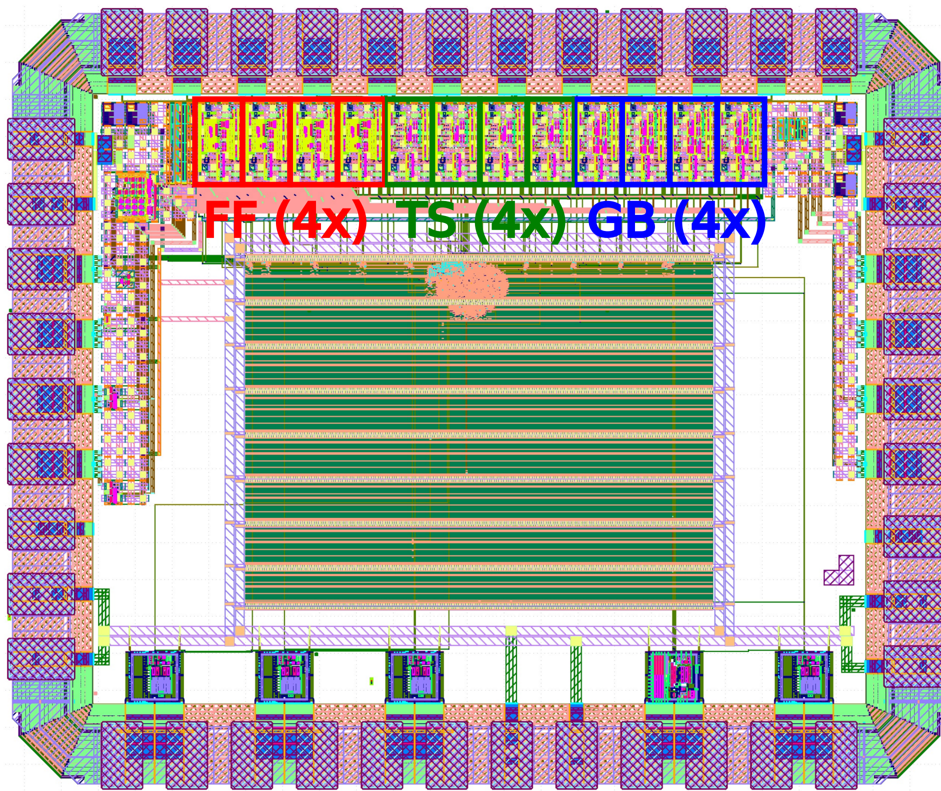
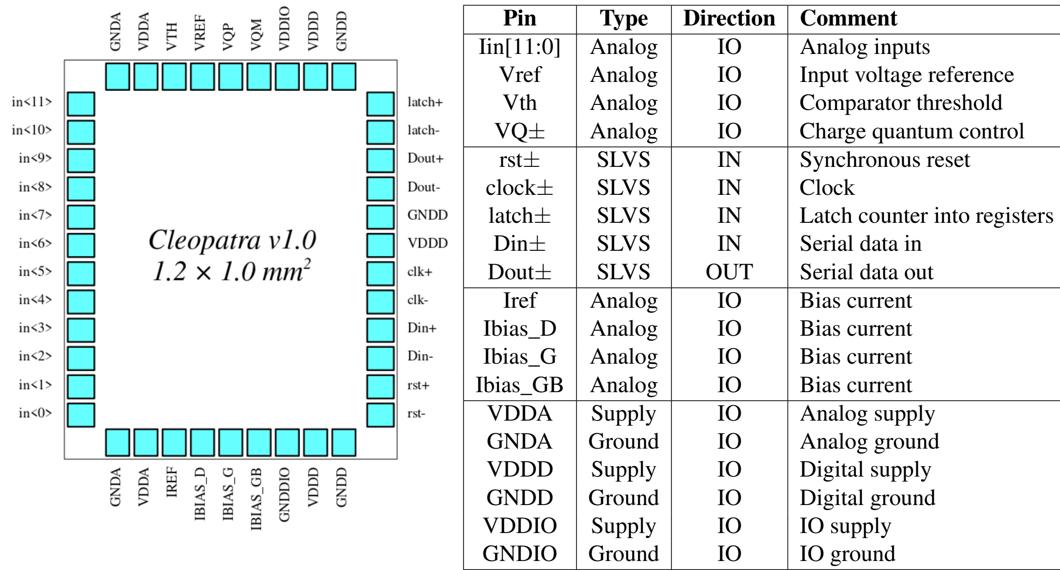


Fig. 3.11 CLEOPATRA layout [13].

3.3.2 Output serial link

The output serializer of the ASIC CLEOPATRA is designed to transmit 32-bit data words at a data rate set by the clock frequency by the system. When the device starts up, an idle pattern is sent, in order to facilitate synchronization of the transmitted words. This pattern is represented by the hexadecimal value `0xfeedda7a`. During register read operations, the system transmits a data word that can correspond to either a channel register or a configuration register, depending on the contents of the global configuration register `GCR06`. This mechanism makes it possible to dynamically select the type of data to be read and transmitted on a single output line. The format of the output data, including details on the meaning of individual bits and the structure of the 32-bit word, is described in Table B.5. As for the chip's pin layout, version 1 of the ASIC CLEOPATRA presents a detailed physical configuration in Table B.6. Each pin has a specific function, the description of which is given below to clarify the electrical and logical interface of the device.
A schematic of the position of the pins is shown in Fig. 3.12.



Pin	Type	Direction	Comment
Iin[11:0]	Analog	IO	Analog inputs
Vref	Analog	IO	Input voltage reference
Vth	Analog	IO	Comparator threshold
VQ±	Analog	IO	Charge quantum control
rst±	SLVS	IN	Synchronous reset
clock±	SLVS	IN	Clock
latch±	SLVS	IN	Latch counter into registers
Din±	SLVS	IN	Serial data in
Dout±	SLVS	OUT	Serial data out
Iref	Analog	IO	Bias current
Ibias_D	Analog	IO	Bias current
Ibias_G	Analog	IO	Bias current
Ibias_GB	Analog	IO	Bias current
VDDA	Supply	IO	Analog supply
GNDA	Ground	IO	Analog ground
VDDD	Supply	IO	Digital supply
GNDD	Ground	IO	Digital ground
VDDIO	Supply	IO	IO supply
GNDIO	Ground	IO	IO ground

Fig. 3.12 (a) Schematic diagram of CLEOPATRA pinout; (b) CLEOPATRA pinout details

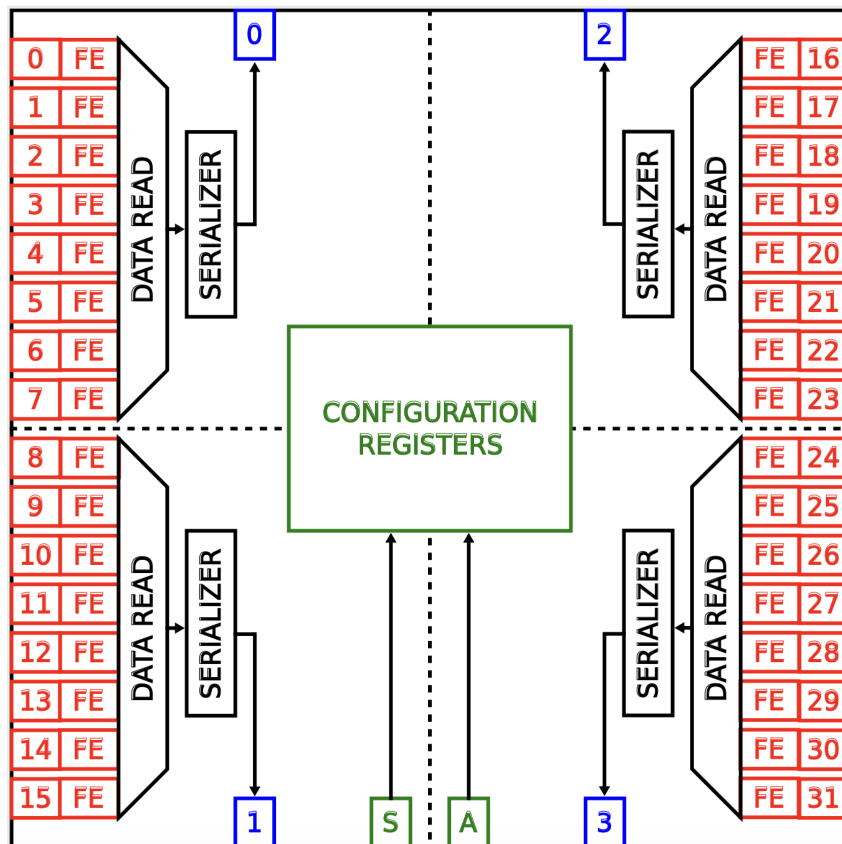


Fig. 3.13 Floorplan of CLEOPATRA v2

3.3.3 CLEOPATRA v2

Based on the results of the first version of CLEOPATRA ASIC, a second version is currently under development. This new iteration will expand the number of channels to 32 inputs, divided into 4 quadrants, each with a serial data output. It will implement the same serial configuratio interface as v1, upscaled for 32 channels.
To allow for better management of a board containing multiple CLEOPATRA chips, each chip address is included as an input to select the individual chip by its address. The recycling integrator architecture remains unchanged, but the goal is to improve system robustness, scalability, and parallel readout capability, which are fundamental aspects for use in large-area detectors and for future applications in both clinical and high-energy physics.
A floorplan of the ASIC final version is shown in Fig. 3.13.

Chapter 4

Test results

4.1 Introduction

This chapter presents the experimental studies carried out on ToASt and CLEOPATRA ASICs, described in the previous chapters. The goal of these activities is to characterize the performance of the devices under realistic operating conditions, assessing their signal response, noise behavior, and radiation tolerance.
For ToASt, the discussion begins with the first version of the chip. The initial part focuses on the procedures for gain calibration and ToT offset correction, followed by measurements of electronic noise. Radiation effects are then examined, with dedicated tests on Single Event Upsets (SEU) and Total Ionizing Dose (TID). The same series of tests are subsequently reported for the second version of ToASt, allowing a direct comparison with the prototype and highlighting the improvements introduced in the updated design.
The second part of the chapter is devoted to CLEOPATRA, where results are presented for the measurements of output frequency as a function of the input current, validating the operation of the recycling integrator architecture, and the differences between the three front-end circuit amplifiers.
For both ASICs, each section provides a detailed description of the test setup, ensuring that the reported results can be interpreted in the context of the measurement conditions and the experimental methodology adopted.

4.2 ToASt testing

4.2.1 Calibration

The calibration of the first ToASt prototype was carried out with the goal of minimizing channel-to-channel variations and ensuring uniform performance across the ASIC. The procedure focused on two aspects: the adjustment of the gain, determined by the ToT discharge current, and the correction of the ToT offset.
Fig. 4.1 shows the setup used during the characterization measurements of ToASt ASIC.

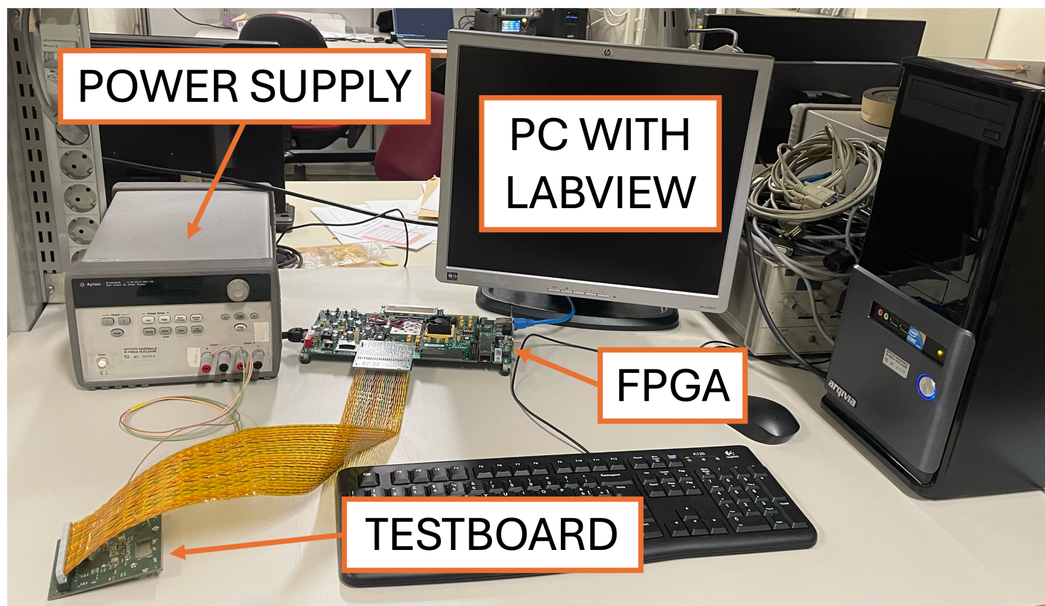


Fig. 4.1 Laboratory setup of ToASt ASIC measurements.

For each channel, transfer curves were recorded by scanning the ToT discharge DAC. Based on these measurements, a reference gain value was defined, and each channel was tuned by setting its local DAC accordingly. This method reduces the initial spread in gain. A similar approach was applied to the ToT offset, achieving a comparable improvement in consistency between channels.
The calibration relied on the internal test pulse generator, implemented through a 6+1 bit DAC. This system allowed controlled charge injection over two selectable ranges: up to about 16 fC with a fine step of 0.25 fC, or up to about 66 fC with a coarser step of about 1 fC. These injections were used to characterize the channel response and to determine the optimal DAC settings for calibration.

The calibration procedure and noise acquisition were carried out using a dedicated LabVIEW interface (Fig. 4.2), which enables the configuration of the ASIC parameters.

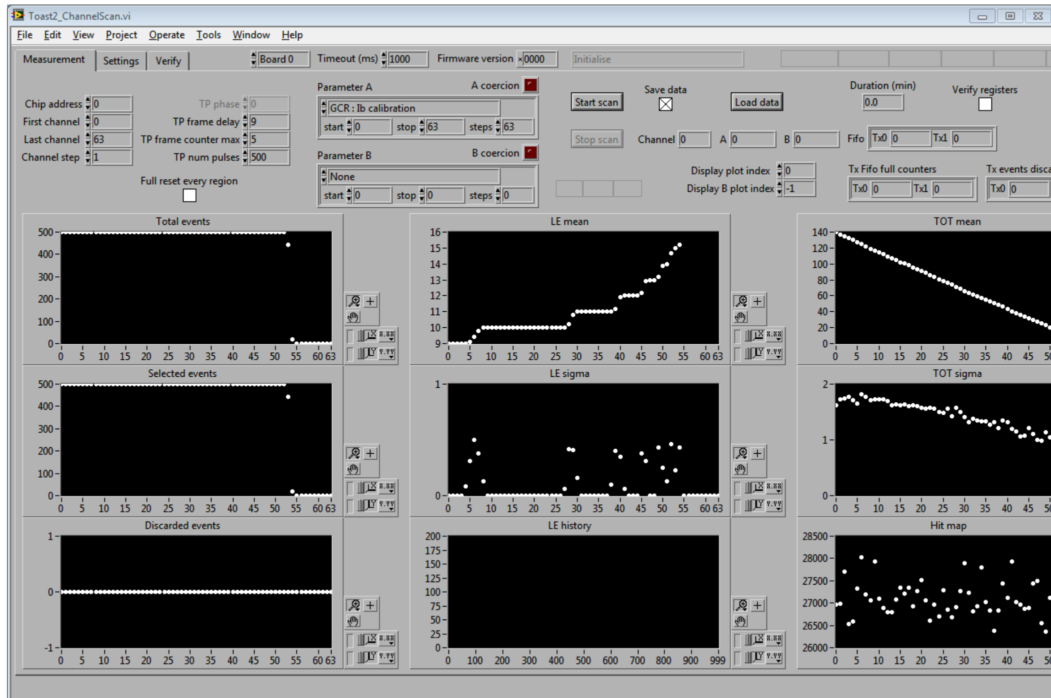


Fig. 4.2 LabVIEW interface used for ToASt calibration procedure.

The outcome of this process demonstrated the effectiveness of the internal calibration scheme in reducing parameter dispersion.
The calibration procedure consists of the following steps:

- For each channel, the transfer curve for each local ToT Ibias DAC value is measured;
- A target gain that can be applied to all channels is selected (Fig. 4.3);
- The DAC value providing a the gain closest to the target one is selected;
- For each channel, the ToT offset is measured;
- The DAC value providing a the offset closest to the target one is selected.

As can be seen from the Fig. 4.4a and 4.4b, comparing the curves before and after calibration, the spread is reduced from about 10 % to a few percent.

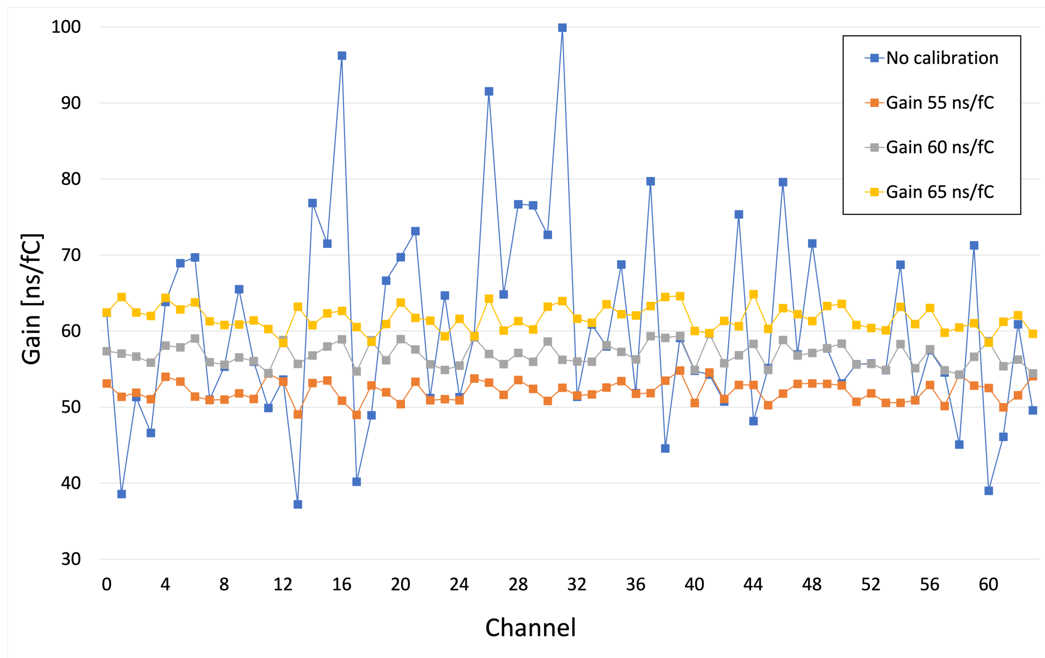
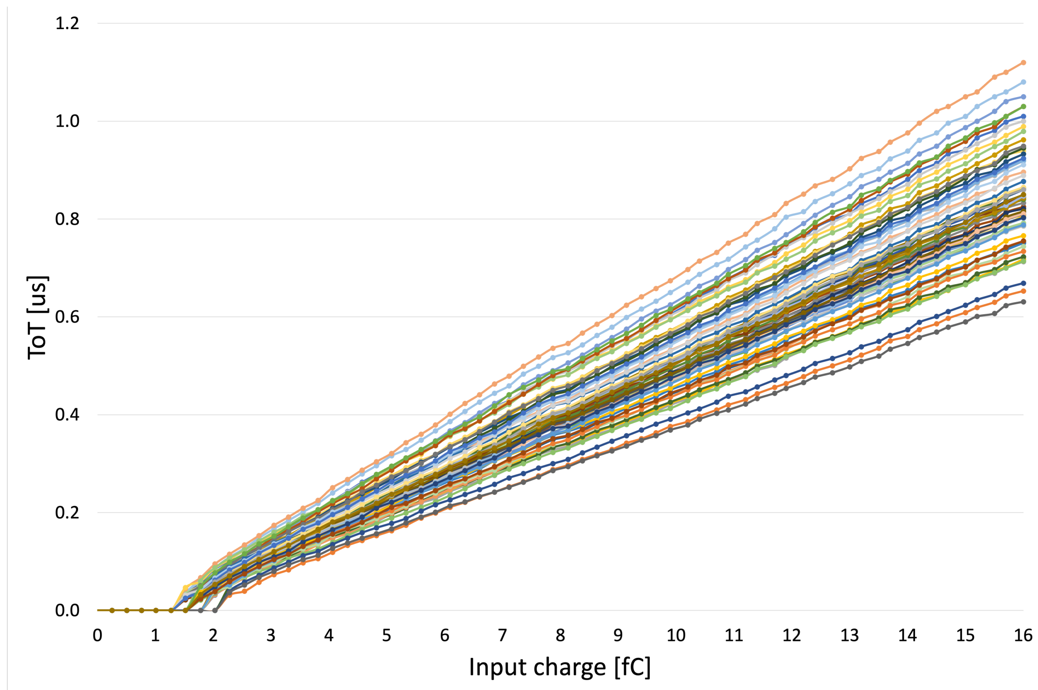


Fig. 4.3 ToASt gain calibration

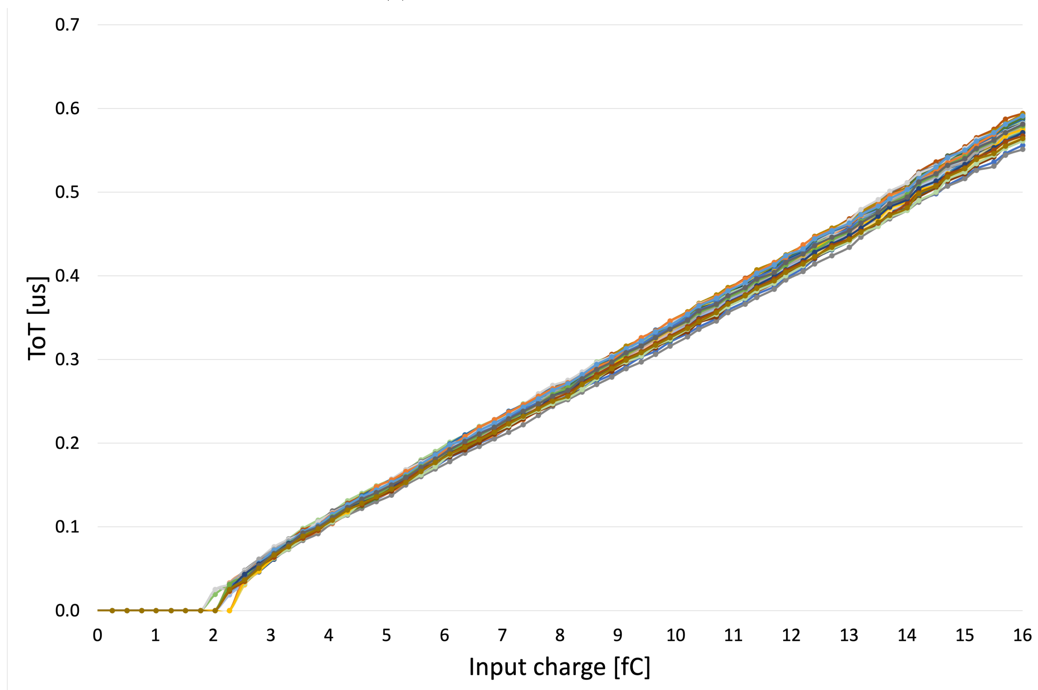
An optimization of the calibration parameters was carried out by adjusting the register settings of ToASt ASIC, specifically the discriminator threshold, DAC settings, bias currents, gain, and ToT offset, in order to achieve the best possible performance. The effects of these parameter variations on the main performance metrics are summarized in Table 4.1, which reports the progressive improvements obtained through successive optimization. This analysis demonstrates how fine-tuning the internal registers can significantly enhance the ASIC's response, leading to reduced gain spread, lower ToT offset, and improved charge sensitivity.

Finally, after evaluating the results of the different optimization steps, the best combination of calibration parameters was selected. This set corresponds to the configuration that provided the most uniform gain and ToT offset across all tested boards, ensuring optimal performance of ToASt chip. The chosen parameters were used as reference values for all subsequent measurements and characterization tests.

In conclusion, the calibration of ToASt chip successfully reduced both the gain spread and the ToT offset across all tested boards, improving the uniformity and predictability of the device response. These results confirm the effectiveness of the calibration procedure and provide a solid baseline for subsequent characterization measurements, such as noise, SEU and TID tests.



(a) ToASt before calibration



(b) ToASt after calibration

Fig. 4.4 ToASt ASIC ToT response to different input charges before (a) and after (b) calibration.

Step	Gain (%)		ToT Offset (%)		Minimum Charge (fC)	
N.	Before	After	Before	After	Before	After
1	11.87	2.67	15.39	5.09	1.23	1.23
2	12.04	2.10	81.14	12.63	0.52	0.52
3	11.42	2.34	33.33	11.28	0.69	0.69
4	11.49	2.15	105.37	46.04	0.45	0.45
5	11.58	2.09	25.92	9.05	1.10	1.10

Table 4.1 Summary of the improvements in key parameters (Gain, ToT offset, and Minimum charge) across five optimization steps, resulting from the tuning of ASIC internal current settings.

4.2.2 Noise

The characterization of the noise performance of ToASt ASIC represents a crucial step in the qualification of the chip. The intrinsic electronic noise sets the minimum detectable signal and directly affects both efficiency and time resolution. For this reason, a dedicated test campaign was carried out to quantify the Equivalent Noise Charge (ENC) of the device.
The measurements were first performed with the ASIC operated in standalone mode, i.e. with its inputs not connected to any sensor or external capacitance. This configuration isolates the intrinsic noise of the front-end electronics from additional contributions due to detector capacitance.
Each readout channel includes a discriminator with a programmable threshold. By systematically varying the fine threshold value and recording the channel response to injected test charges, a so-called threshold scan (or S-curve) is obtained. An example of an S-curve of a channel where noise is extracted is shown in the Fig. 4.5. The S-curve describes the hit probability as a function of the applied threshold.
The experimental S-curve data were fitted using an error function, which corresponds to the integral of a Gaussian distribution and can be expressed as:

$$f(x') = \frac{N}{2}\left(1 + \frac{2}{\sigma\sqrt{\pi}}\int_0^{x'} \exp(-s^2)\, dx\right), \tag{4.1}$$

$$s = \frac{x-\mu}{\sigma}. \tag{4.2}$$

where:

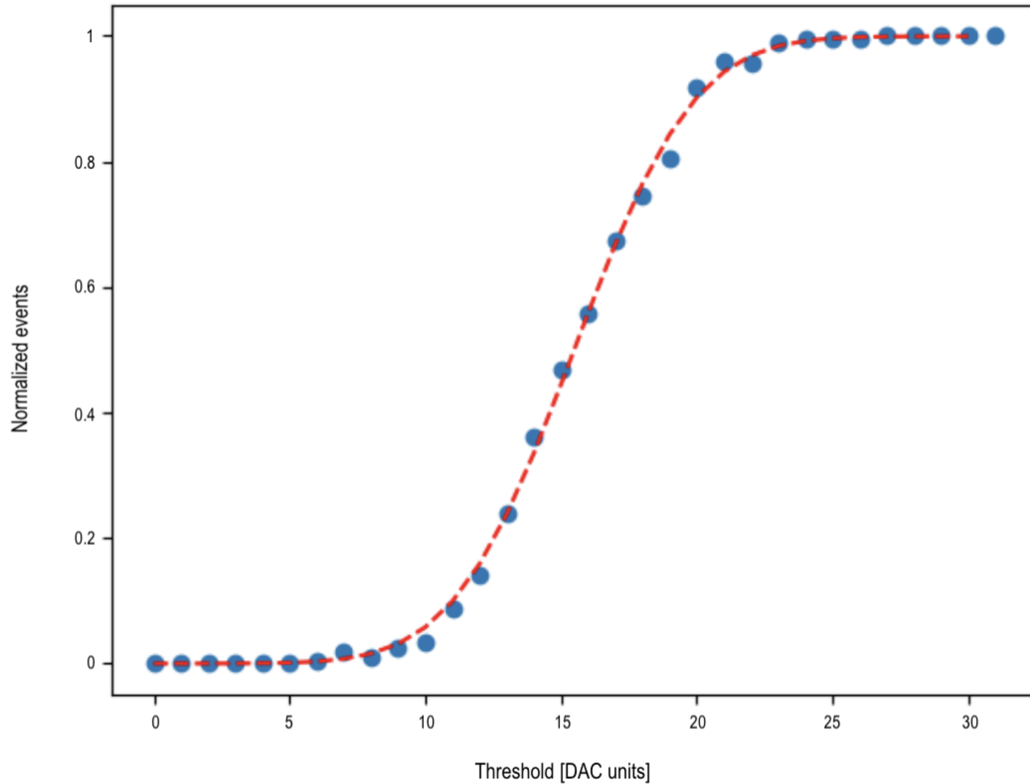


Fig. 4.5 Typical S-curve obtained from a threshold scan. The derivative of the curve is used to extract the noise distribution.

- N is the number of samples,
- μ is the mean value,
- σ is the standard deviation.

Assuming a Gaussian distribution of noise fluctuations, the derivative of the S-curve yields a normal distribution centered around the effective threshold value. The standard deviation of this distribution corresponds to the width of the noise. By converting this quantity into units of input charge through the simulated front-end gain all channels provides, the ENC is derived.
Applying the above procedure to all channels provided a distribution of ENC values across the chip. In the absence of external capacitance, typical results fall in the range of a few hundred electrons, in good agreement with simulations. The spread among channels is modest and the precision of the measurement is ultimately limited by the resolution of the threshold DAC, but this limitation does not compromise the

reliability of the results.
Additional measurements were carried out with the ASIC connected to a sensor biased at high voltage in order to fully deplete it. The sensor used has a capacity in the order of picoFarad units. As shown in Fig. 4.6, the noise level in this configuration is slightly higher than that observed with the standalone chip, although the difference is not significant. Furthermore, tests were repeated while varying the sensor bias voltage; the results, illustrated in Fig. 4.7, demonstrate that the noise remains essentially unchanged across the different bias configurations. Since the

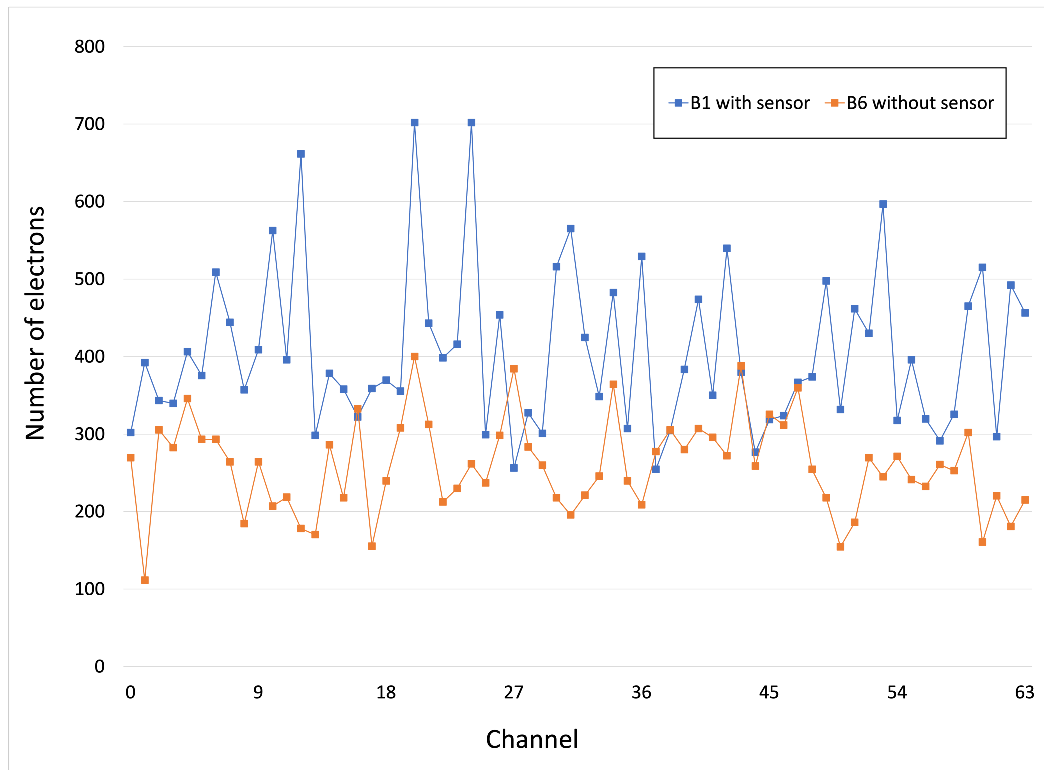


Fig. 4.6 Noise measured with ToASt ASIC connected to a fully depleted sensor.

design requirements of the PANDA MVD impose stringent noise constraints, these measurements are essential to assess the suitability of ToASt for long-term operation. Although the detector used in this work features a smaller capacitance than the one foreseen for the final experiment, the results provide a valid indication of the expected performance under realistic conditions. An ENC below roughly 1500 e^- per channel, even with the detector connected, these measurements are fundamental to validate the suitability of ToASt for long-term operation.
The methodology combining threshold scans, Gaussian noise modeling, and charge

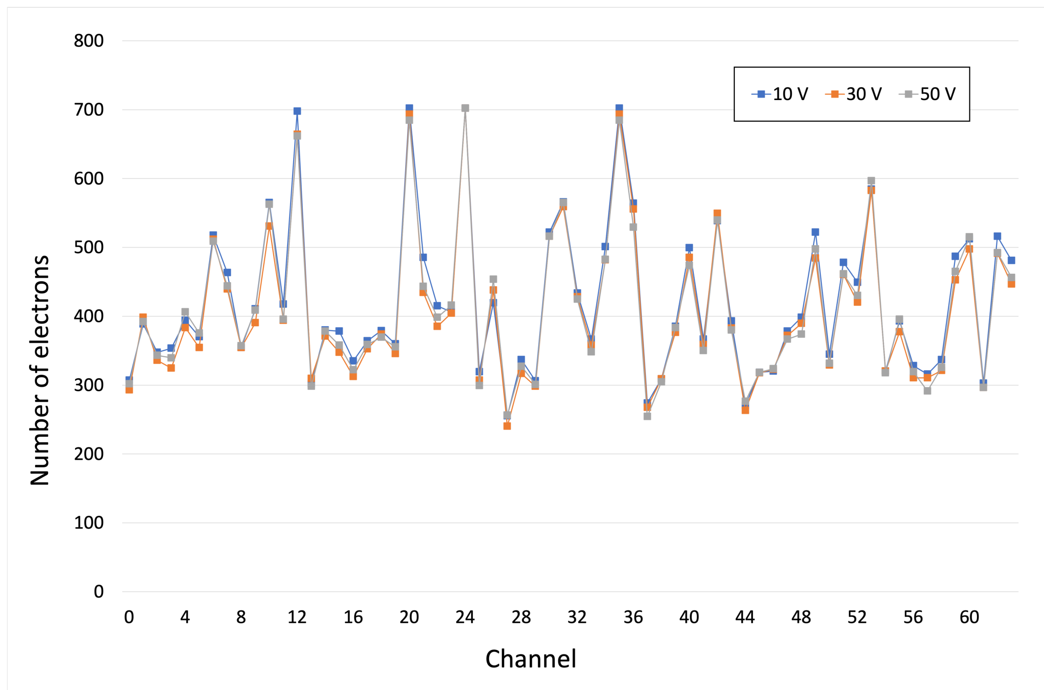


Fig. 4.7 Noise measured with the sensor biased at different voltages.

injection provides a robust framework for noise characterization of ToASt ASIC. The results confirm that the device exhibits low intrinsic noise and fulfills the requirements set by the PANDA experiment.

4.2.3 Single Event Upset

ToASt chip was subjected to radiation tests aimed at evaluating its sensitivity to Single Event Upsets (SEU). This effect consists of an unintended change in the logical state of a register or digital cell, induced by the passage of a high-energy ionizing particle through the silicon. Although such events are transient, they can generate a permanent change in the memory configuration and thus compromise if not properly mitigated.
The tests were performed at the INFN-LNL SIRAD facility using ion beams with a fluence of approximately $5 \cdot 10^7$ ions.
A flowchart of the SEU acquisition procedure is shown in Fig. 4.8.
The table 4.4 shows the ions used and their energies. The deposited energy was calculated from the beam energy by means of SRIM (Stopping and Range of Ions in Matter) simulations [41]. The SEU measurements on ToASt ASIC were performed

Ion	E_{beam} [MeV]	E_{dep} [MeV]
Ag	247.00	13.52
Ni	190.80	6.68
Si	141.60	2.11
Si at 30°	141.60	2.43
Br	218.90	9.79
Cl	162.66	3.02
Cl at 30°	162.66	3.49

Table 4.2 Deposited energy (E_{dep}) for different ions and incidence angles.

by configuring the chip registers with a predefined setup and continuously reading them back using a dedicated LabVIEW program during irradiation at a radiation facility. Any deviations from the expected register values were logged in real time. The tests were carried out under controlled beam conditions with known particle type, energy, and fluence, enabling the calculation of upset rates per register and per bit. This approach evaluates the digital circuitry's radiation tolerance, unaffected by the connected sensor's capacitance or type.

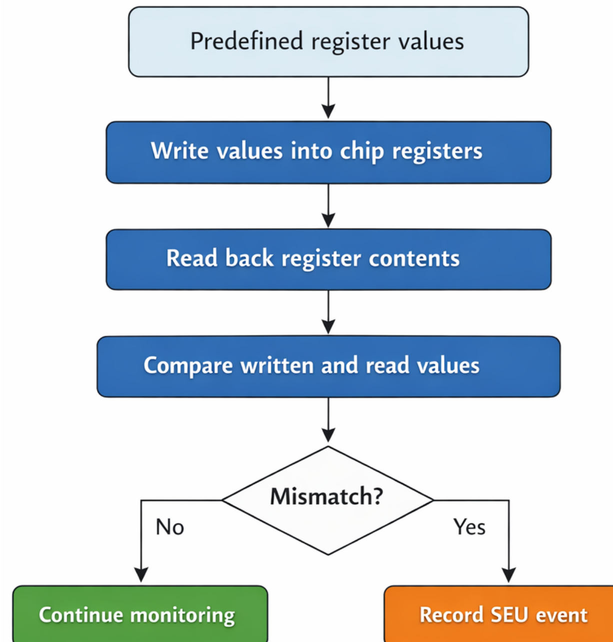


Fig. 4.8 Flowchart of the SEU acquisition procedure.

From these measurements, an estimated SEU cross section of about $3 \times 10^{-15}\,\mathrm{cm}^2$ was derived for 200 MeV protons [42]. Considering the expected hadron flux of

5×10^6 hadrons$/(\mathrm{cm}^2 \cdot \mathrm{s})$, this corresponds to a rate of roughly 9.3×10^{-2} errors per hour per chip in the PANDA operating environment. Importantly, only $1 \rightarrow 0$ transitions were observed during the tests, and further analysis revealed that a detected triplication error originated from a redundancy issue in the Verilog implementation rather than from radiation effects.
During the irradiation, the internal digital registers were continuously monitored to detect spontaneous state changes. This procedure made it possible to quantify the number of upsets and validate the calculated cross section. The results of the measurements are shown in Fig. 4.9. To translate the measurement from the ion environment to a more realistic one, the data were fitted using the function [43]:

$$\sigma(E) = \sigma_0 \left[1 - \exp\left(- \left(\frac{E - E_0}{w} \right)^s \right) \right], \tag{4.3}$$

where σ_0, E_0, w, and s are fitting parameters. This functional form captures the progressive saturation of the measured quantity with increasing energy E.

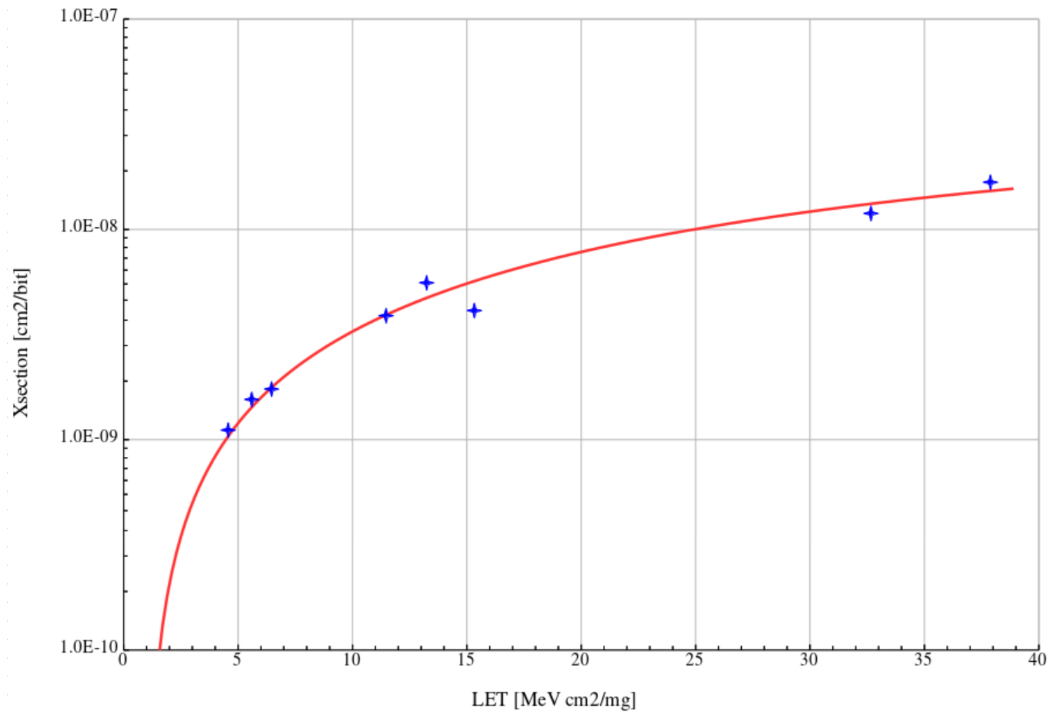


Fig. 4.9 SEU test results for ToASt ASIC at the INFN-LNL SIRAD facility, showing the number of observed upsets as a function of particle fluence.

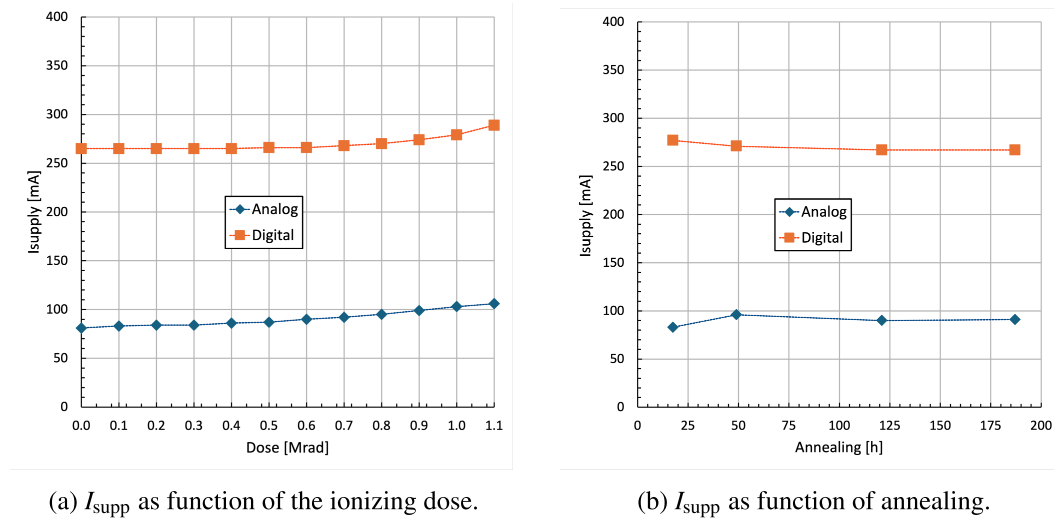
The results demonstrated that, although the chip shows generally good resistance

to SEUs, certain parts of the logic are more vulnerable and may require design improvements. Possible mitigation strategies include the use of hardened latch structures, error detection and correction logic, or redundancy in critical registers to minimize the impact of bit flips.
The SEU tests confirmed that ToASt maintains stable performance under irradiation, with a limited upset cross section of $3 \times 10^{-15}\,\mathrm{cm}^2$ and an expected error rate below one per hour per chip under PANDA operating conditions. The observation that only $1 \rightarrow 0$ transitions occurred provided a clue about the origin of the issue. The initially detected triplication error was traced back to the Verilog code rather than being caused by radiation effects. Overall, the results demonstrate that the ASIC can operate reliably in the expected radiation environment, with potential design refinements available to further enhance its resilience.

4.2.4 Total Ionizing Dose

To evaluate the cumulative impact of ionizing radiation on ToASt ASIC, dedicated Total Ionizing Dose (TID) tests were performed, complementing the characterization of transient effects. This type of irradiation study evaluates the cumulative damage produced by ionizing particles over time, which gradually degrade the transistor parameters and alter the behavior of analog and digital circuits.
The measurements were carried out at with a 10 keV X-ray machine at INFN Padova, where the two chips tested were irradiated. The first chip up to a total dose of 1.1 Mrad and the second up to a total dose of 2.5 Mrad with a dose rate of 350 rad/s. During irradiation, the supply current (I_{supp}) and the analog front-end gain were continuously monitored to detect possible degradation effects. Following irradiation, an annealing procedure was performed. Annealing refers to the natural recovery process that occurs in irradiated devices when they are left at elevated temperatures, allowing some of the radiation-induced defects in the semiconductor material to partially or completely heal. This procedure was carried out in two phases: from 0 to 49 hours at room temperature (15 °C) and from 49 to 121 hours at 100 °C, and finally from 121 to 195 hours at room temperature, in order to study the recovery of the device parameters.
Fig. 4.10 and 4.11 summarize the behavior of the supply current. In panel (a), I_{supp} is plotted as a function of the accumulated dose. An increase of about 15-20% is observed up to 2.5 Mrad, indicating the presence of radiation-induced leakage

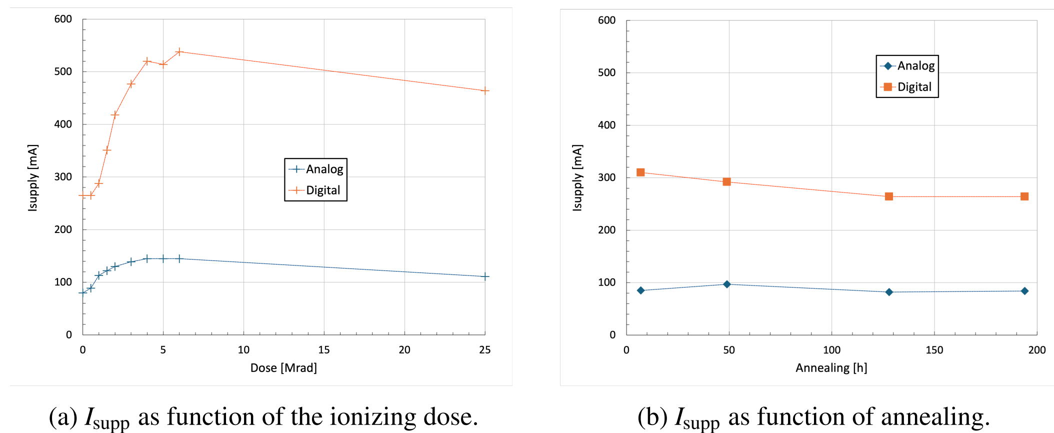
currents after a threshold of about 0.4 Mrad.



(a) I_{supp} as function of the ionizing dose.

(b) I_{supp} as function of annealing.

Fig. 4.10 Evolution of the supply current I_{supp} under irradiation (a) and during annealing (b) of the first chip tested.



(a) I_{supp} as function of the ionizing dose.

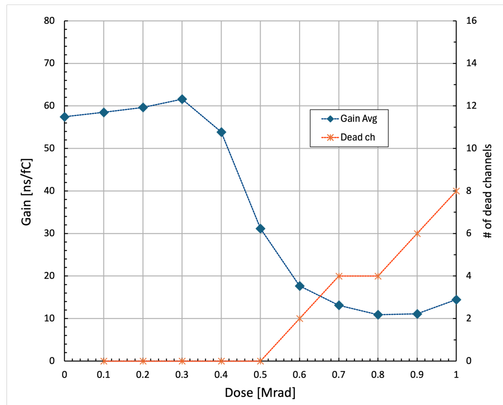
(b) I_{supp} as function of annealing.

Fig. 4.11 Evolution of the supply current I_{supp} under irradiation (a) and during annealing (b) of the second chip tested.

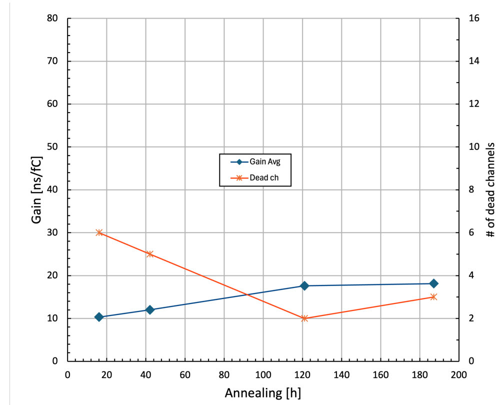
Panel 4.11b of Figure 4.11 shows the recovery during annealing. At room temperature (0 h to 49 h at 15 °C) only a modest reduction of about 5% is observed, while a much recovery occurs at elevated temperature (49–121 h at 100°C), where the current nearly returns to its pre-irradiation value. This behavior confirms that the increase in current is largely reversible and strongly dependent on the thermal conditions of the annealing process.

The effect of irradiation on the analog front-end gain is reported in Fig. 4.13. As

shown in panel 4.12a, the gain decreases gradually with dose, with a total reduction of about 10% at 250 kGy. This trend reflects the cumulative degradation of transistor parameters.

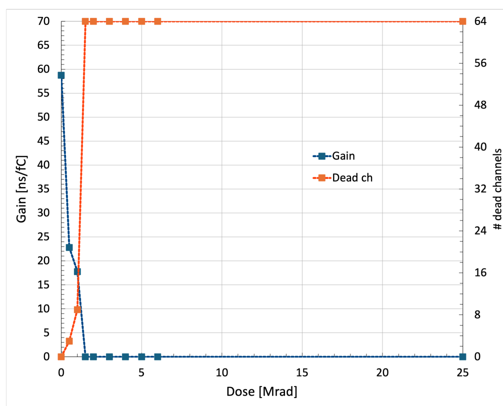


(a) Front-end gain as function of ionizing dose.

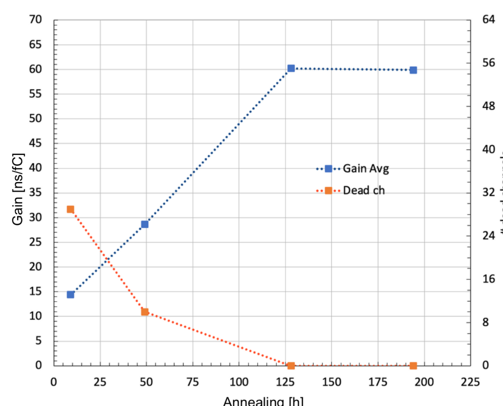


(b) Front-end gain as function of annealing.

Fig. 4.12 Evolution of the front-end gain under irradiation (a) and during annealing (b) of the first chip tested.



(a) Front-end gain as function of ionizing dose.



(b) Front-end gain as function of annealing.

Fig. 4.13 Evolution of the front-end gain under irradiation (a) and during annealing (b) of the second chip tested.

Panel 4.12b shows that, for the first chip tested, the gain does not exhibit a significant recovery during annealing, whereas for the second chip (Panel 4.13b) a partial recovery is observed. Although a slight increase occurs, particularly at 100 °C, the gain remains below its pre-irradiation value for both chips.
Overall, the measurements show that the supply current degradation remains moderate and largely reversible after annealing. However, the analog front-end gain

exhibits a strong degradation with increasing ionizing dose, eventually leading to a loss of functionality of the channels at higher doses, as shown in Fig. 4.13a. Therefore, stable operation of the ASIC over the full investigated dose range cannot be claimed.
This behavior may reflect a different balance between oxide-trapped charge and interface-trap buildup at different dose levels. Because oxide-trapped charge is generally more susceptible to thermal annealing, while interface-trap-related damage is more stable, annealing can result in a more noticeable recovery when the degradation is dominated by oxide charge trapping.

4.3 ToASt v2 tests

In order to ensure a coherent and systematic comparison between the two prototype versions, the same characterization procedures carried out on the first prototype were also performed on the second one.
Specifically, these activities included the calibration process, the noise measurements, as well as radiation-related tests such as the evaluation of Single Event Upsets and Total Ionizing Dose effects. Repeating the full set of measurements on the updated version of the prototype made it possible not only to validate the design choices introduced in this iteration, but also to assess whether the improvements achieved had any impact on the device performance and robustness under the experimental conditions applied previously.

4.3.1 Calibration

In Table 4.3, the results of the calibration procedure for the second version of the prototype are reported. In particular, the table summarizes the percentage spread of the gain and the Time-over-Threshold offset measured across the tested boards. These parameters provide a direct indication of the uniformity and stability of the calibration process within the system.
Although the values obtained for the second prototype are in good agreement and broadly comparable with those previously measured for the first version. Further work is currently being carried out to optimize the calibration parameters. This ongoing optimization aims to reduce residual variations, improve the overall accuracy

of the system response, and ensure a higher level of reproducibility across different boards.

Board	Type	Gain BC	Gain AC	ToT offset BC	ToT offset AC
B2	Ptype	15.66%	3.72%	43.63%	22.07%
B2	Ntype	18.49%	5.11%	21.08%	13.16%
B3	Ptype	14.13%	4.00%	15.09%	11.98%
B3	Ntype	18.70%	4.03%	18.06%	9.35%
B5	Ptype	18.04%	2.42%	25.81%	15.18%
B5	Ntype	17.82%	4.84%	18.28%	11.26%
B6	Ptype	13.36%	4.55%	20.85%	14.82%
B6	Ntype	18.62%	8.12%	20.93%	19.48%

Table 4.3 Gain and ToT offset spread for the tested boards of the second prototype, before (BC) and after (AC) calibration.

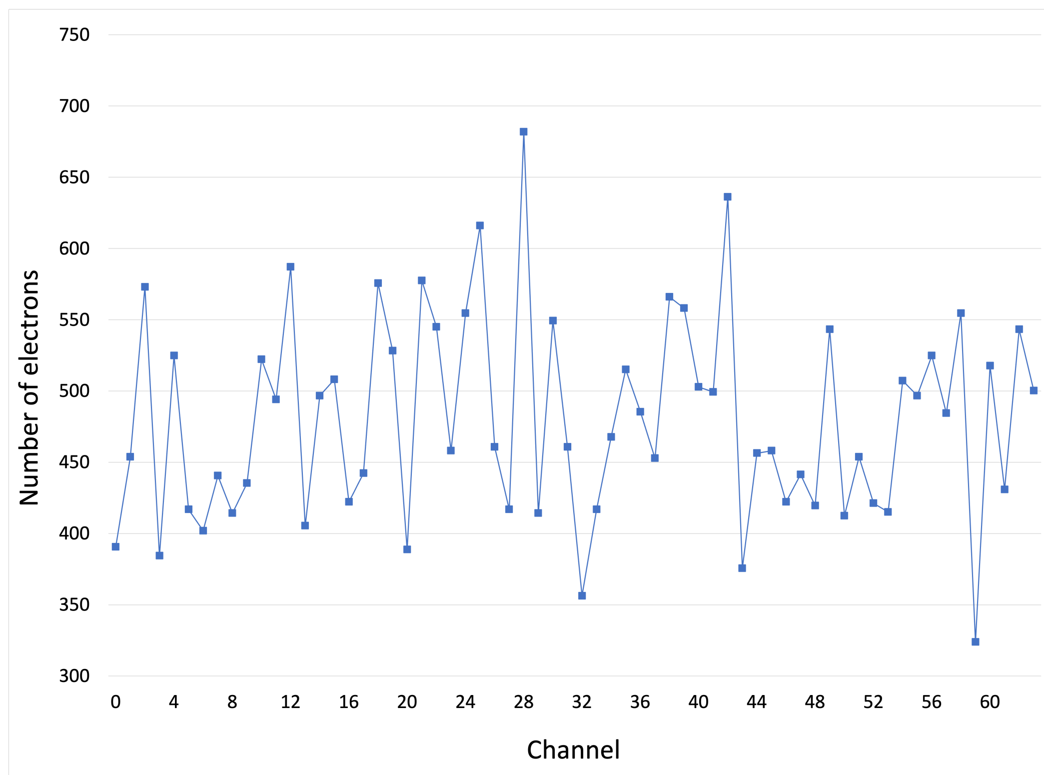


Fig. 4.14 Noise measured with ToASt v2.

4.3.2 Noise

Fig. 4.14 shows the noise measurement results obtained for the second version of the prototype. As can be seen, the noise levels are higher compared to those measured in the first prototype. Nevertheless, these results should be regarded as preliminary, since further optimization steps are currently in progress with the aim of reducing the noise contribution and improving the overall performance of the system. The ongoing refinements are expected to align the noise levels more closely with the design specifications and to enhance the stability of the measurements.

4.3.3 Single Event Upset

The SEU tests for the second version of the prototype were performed at the INFN-LNL SIRAD facility.
The table shows the ions used and their energies during testing of ToASt v2.

Ion	$E_{\mathbf{beam}}$ [MeV]	$E_{\mathbf{dep}}$ [MeV]
Ag	247.00	13.52
Ni	190.80	6.68
Si	141.60	2.11
Si at 30°	141.60	2.43
Br	218.90	9.79
Cl	162.66	3.02
Cl at 30°	162.66	3.49

Table 4.4 Deposited energy (E_{dep}) for different ions and incidence angles.

During the analysis of the acquired data, three types of errors were identified: single-bit SEUs affecting individual registers, multiple-bit SEUs occurring simultaneously across registers, and bit shifts in the data transmission circuits. Only the first two types were counted as SEUs, while transmission shifts were excluded, as they were likely caused by particles impacting the transmission circuitry rather than the internal logic of the chip. Similarly, events in which all the bits of a channel changed state at once were not considered, since, given the presence of triple redundancy in the design, such behavior is attributed to the Load circuit.
It is worth noting that no SEUs were observed in the global registers. These results show a significant improvement with respect to version 1, where GCR errors were present. Residual errors have been observed in the CCR. Analysisis ongoign to

understand the reason of this different behaviour.
As shown in Fig. 4.15, the SEU test results do not follow a clear functional trend. This irregular behavior is likely due to beam-related issues at the facility where the measurements were carried out.

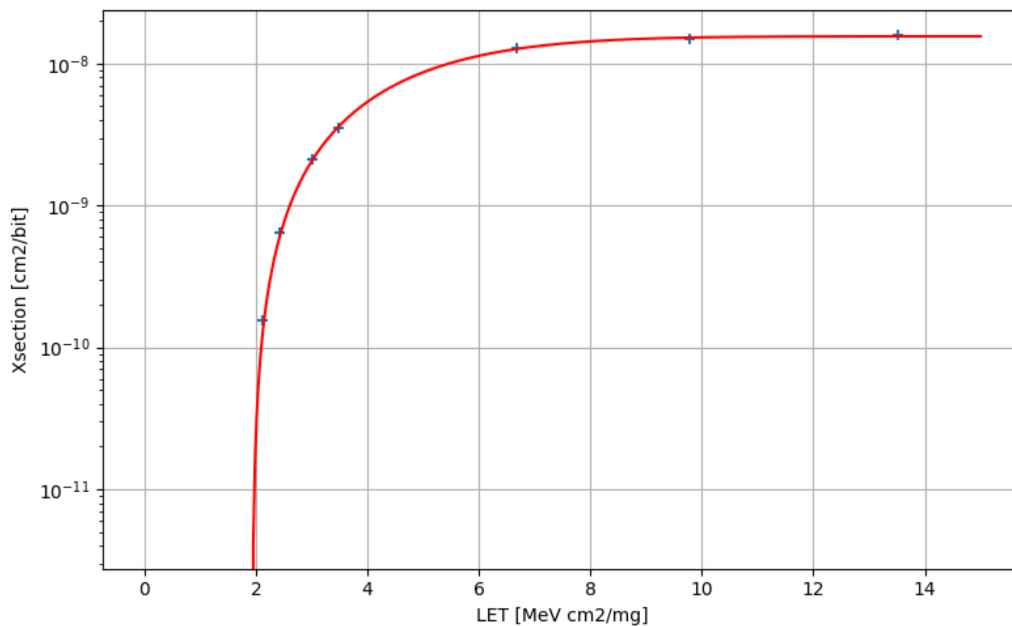


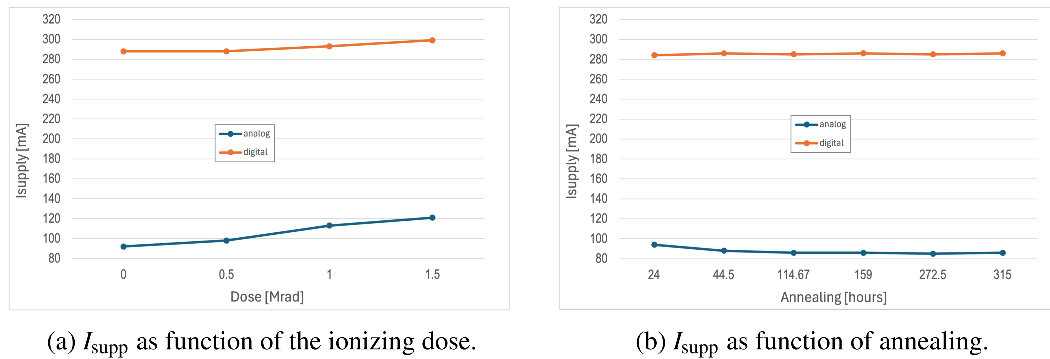
Fig. 4.15 SEU test results for ToASt ASIC at the INFN-LNL SIRAD facility, showing the number of observed upsets as a function of particle fluence of ToASt v2.

Nevertheless, the data indicate a noticeable reduction in the number of single event upsets compared to the first version of the ASIC. This decrease provides evidence of the effectiveness of the implemented triple redundancy, which successfully mitigates the impact of SEUs on the device operation.

4.3.4 Total Ionizing Dose

The Total Ionizing Dose tests were performed on two chips of the second prototype. In one case, the device was subjected to a dose increase applied in relatively large steps, while in the other case the irradiation was carried out in a more gradual manner. This approach allowed for a comparison between different exposure strategies and their effects on the device behavior.
The results in Fig. 4.16 and 4.17 show that in the analog section of the chips there is

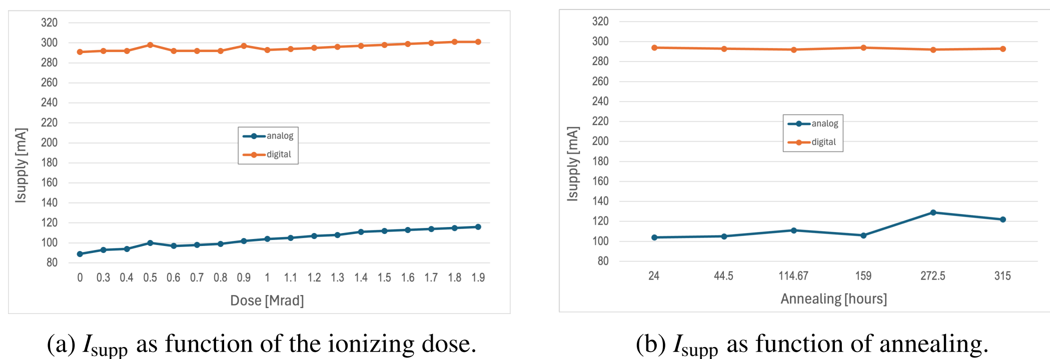
an increase in current consumption of approximately 30%, while in the digital section the increase is limited to about 3%. This is due to the fact that the digital section contains a large number of small transistors, which are more sensitive to leakage. On the other hand, no clear correlation was observed between the accumulated dose and the noise measurements, indicating that the noise performance remains unaffected by the irradiation levels applied during these tests.



(a) I_{supp} as function of the ionizing dose.

(b) I_{supp} as function of annealing.

Fig. 4.16 Evolution of the front-end gain under irradiation (a) and during annealing (b) of the first chip tested.



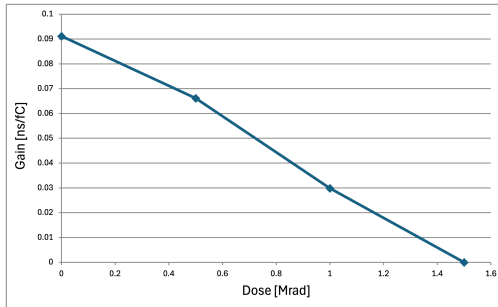
(a) I_{supp} as function of the ionizing dose.

(b) I_{supp} as function of annealing.

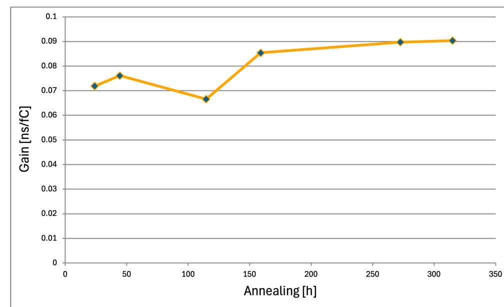
Fig. 4.17 Evolution of the front-end gain under irradiation (a) and during annealing (b) of the second chip tested.

Following the irradiation tests, an annealing phase was carried out. In this study, the annealing was performed in an oven at 100 °C for a total duration of 315 hours, with intermediate measurements taken during this period to monitor the recovery trend. A different behavior was observed between the two tested chips. The chip that was exposed to a higher dose rate exhibited a complete recovery of its current consumption during annealing. In contrast, the chip that had undergone a slower but higher overall dose increase showed only a partial recovery, with residual degradation still

present.

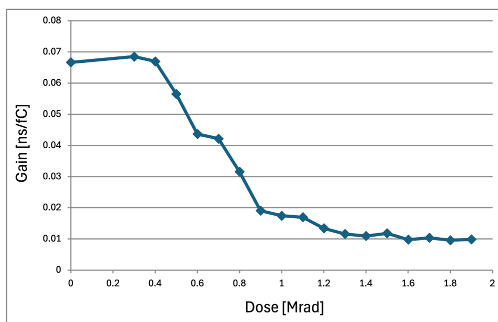


(a) Front-end gain as function of ionizing dose.

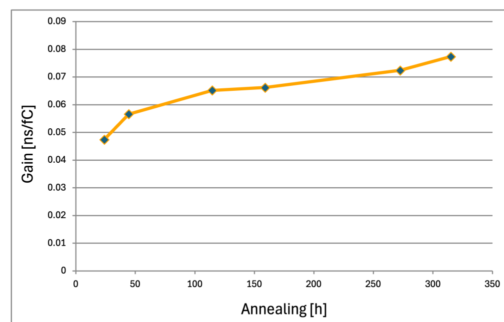


(b) Front-end gain as function of annealing.

Fig. 4.18 Evolution of the front-end gain under irradiation (a) and during annealing (b) of the first chip tested.



(a) Front-end gain as function of accumulated dose.



(b) Front-end gain as function of hours of annealing.

Fig. 4.19 Evolution of the front-end gain under irradiation (a) and during annealing (b) of the second chip tested.

The gain shows a gradual decrease as the accumulated dose increases, eventually becoming almost completely suppressed at around 1 Mrad. This behavior indicates a progressive degradation of the analog front-end performance under ionizing radiation, which is consistent with the expected effects of charge trapping and threshold voltage shifts in the transistors. The near-complete loss of gain at higher doses highlights the sensitivity of this parameter to radiation-induced damage and underlines the importance of optimizing the design for improved radiation tolerance.
The noise did not show any significant dependence on the accumulated dose, remaining stable throughout the irradiation campaign and indicating that the chip's noise performance is not strongly affected by the Total Ionizing Dose. This suggests that the main mechanisms responsible for noise generation are not substantially

influenced by the radiation-induced effects observed in other parameters, such as the gain or current consumption.

4.4 CLEOPATRA testing

The characterization of CLEOPATRA ASIC provided a set of quantitative results that confirm the validity of the recycling integrator approach.
The experimental setup, shown in Fig. 4.20, consists of an FPGA board controlled by a custom LabVIEW program (Fig. 4.21), a power supply providing the bias to the test board hosting CLEOPATRA ASIC via wire bonding, and a voltage generator, also driven by LabVIEW, used to vary the input voltage and thereby control the injected current.

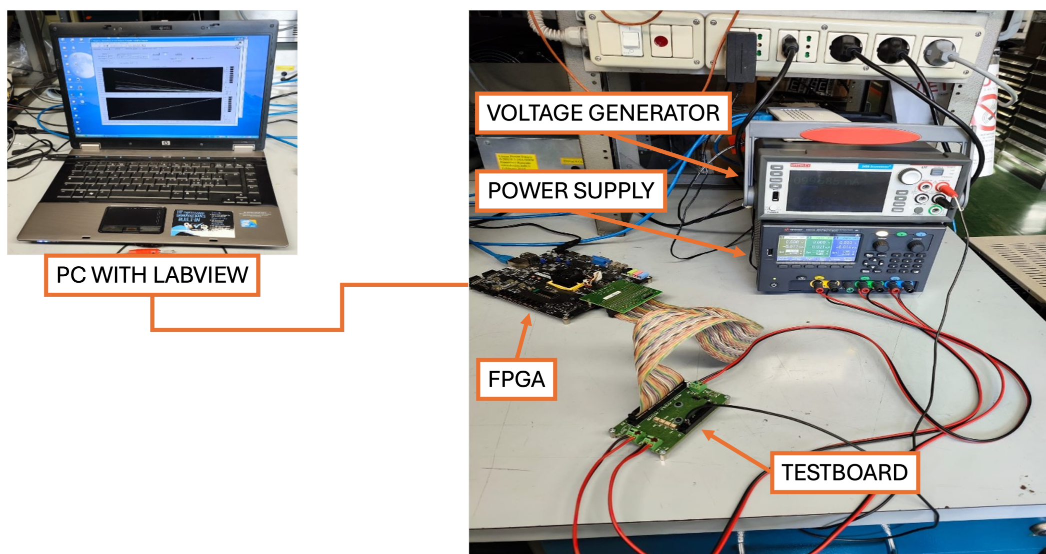


Fig. 4.20 Test setup of CLEOPATRA characterization

Fig. 4.22 shows the linearity in the response of a channel to an input current between 1 nA to 100 nA for the seven injection capacity values. Table 4.5 shows the comparison between measured and theoretical charge values for the seven configurations.
Linearity measurements demonstrated a non-linearity of about 1 % over the input current range between 1 nA to 100 nA, consistently across the different selectable values of the subtracting capacitor, as can be seen in Fig. 4.23.
For a threshold setting of 600 mV, the measured subtracted charge ranged from approximately 9.2 fC to 61 fC, which is about 25 % lower than the theoretical ex-

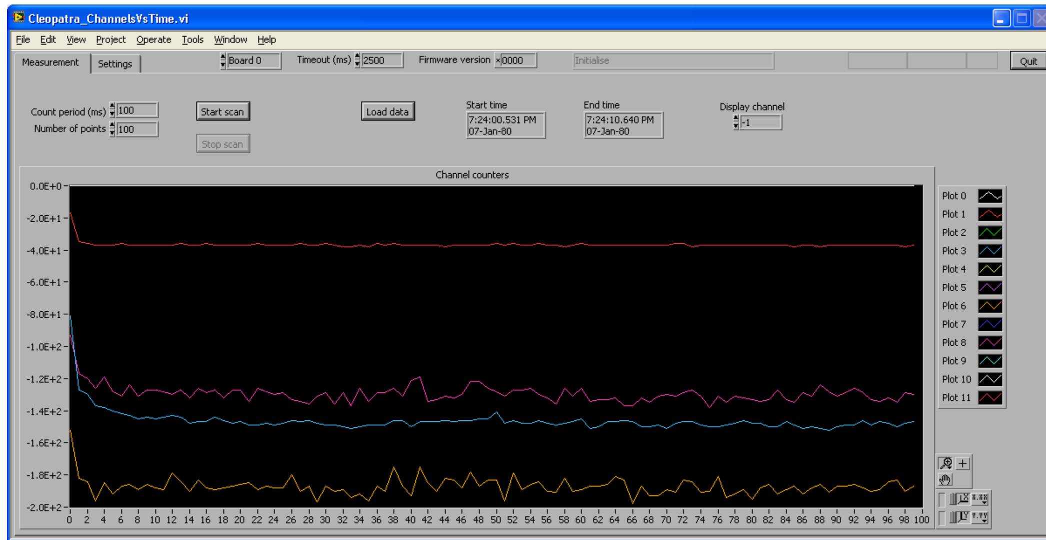


Fig. 4.21 LabVIEW interface used for CLEOPATRA characterization.

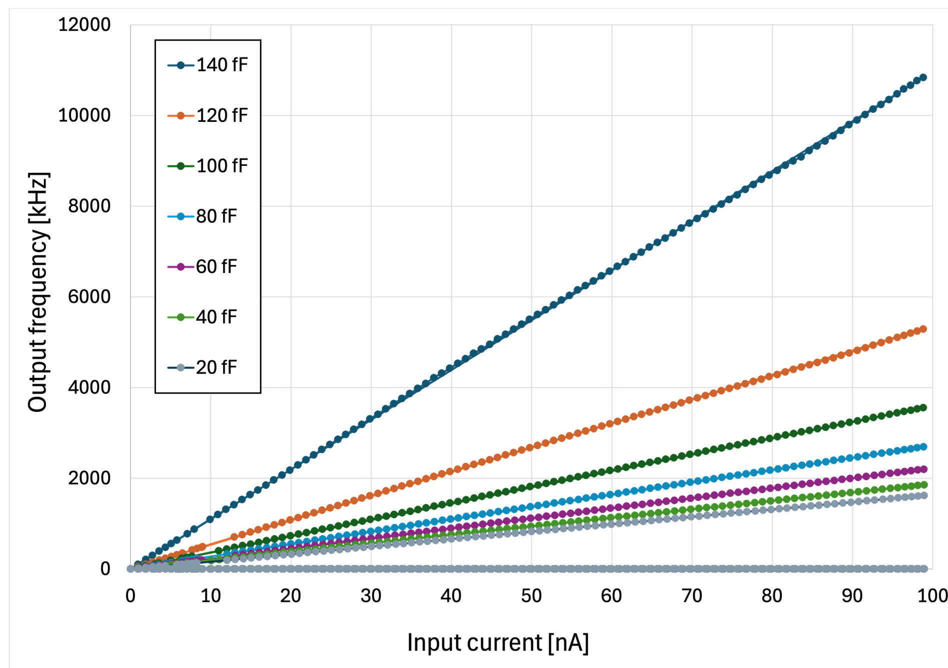


Fig. 4.22 Response of a typical channel to an input current ranging between 1 nA to 100 nA for different values of the injection capacities

pectation. This discrepancy highlights the need of a per channel calibration and, possibly, a minimization of the parasitic capacitance in the next design.
Tests were conducted at clock frequencies up to 500 MHz, confirming stable operation of the recycling integrator loop within these conditions. The variation of the

subtracting capacitor value (20–140 fF in 20 fF steps) allowed exploration of the achievable dynamic range, while maintaining a linear response in the tested input window. These measurements validate the core functional principle of CLEOPATRA and provide guidance for the design improvements planned for the next ASIC iteration.

Q_q (digital)	Q_q [fC] (measured)	Q_q [fC] (theoretical)
1	9.16	20
2	18.82	40
3	27.79	60
4	36.73	80
5	44.99	100
6	53.33	120
7	60.94	140

Table 4.5 Comparison between measured and theoretical charge values.

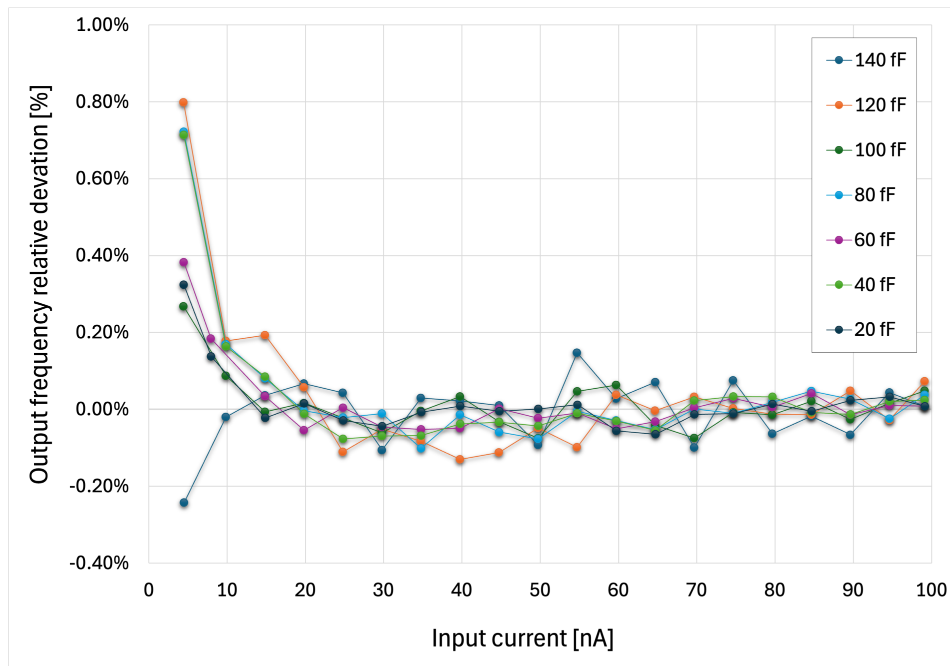


Fig. 4.23 Linearity of the recycling integrator up to 350 nA input current

When performing the measurements with a clock frequency of 500 MHz, it can be observed from the Fig. 4.24 that the system reaches the maximum counting frequency at 125 MHz, which corresponds to one fourth of the clock frequency. This

result is consistent with the theoretical expectation expressed in the corresponding equation in Chapter 3, confirming the correct behavior of the circuit.
In conclusion, the first characterization of CLEOPATRA shows that the ASIC achieves the required linearity and dynamic range for dosimetry applications for initial characterization without a sensor connected to the inputs. While the observed reduction in the effective subtracted charge suggests room for further optimization, the results validate the architectural choices and pave the way for improved prototypes (CLEOPATRA v2) and extended testing with amorphous silicon sensors and particle beams.

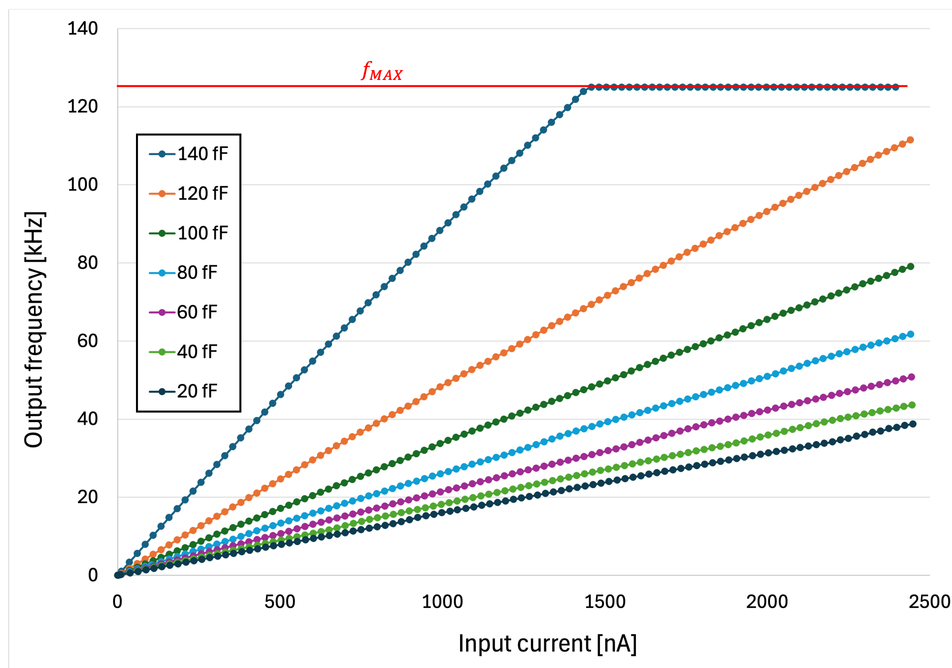


Fig. 4.24 Response of a channel which has reached the maximum counting frequency

Chapter 5

Conclusion

This thesis focused on the characterization and performance evaluation of two ASICs developed for high-energy physics experiments: the ToASt chip, designed for the Micro-Vertex Detector of the PANDA experiment, and CLEOPATRA chip, developed within the HASPIDE project. The primary objective was to provide a comprehensive assessment of their performance, reliability, and radiation tolerance under both laboratory and simulated operational conditions. Through a systematic set of measurements, this work aimed to deliver detailed insights into the behavior of these ASICs, identify potential areas for improvement, and establish characterization methodologies applicable to future developments.

For ToASt ASIC, extensive measurements were performed, including calibration, noise evaluation, Single Event Upset (SEU) tests, and Total Ionizing Dose (TID) tests. Calibration of the second chip version significantly reduced gain spread and Time-over-Threshold offsets, demonstrating improved uniformity and predictability of the device response. Systematic optimization of calibration parameters further refined performance, ultimately identifying a set of parameters that provided the most uniform response across all tested boards.
Noise measurements showed slightly higher values in the second version compared to the first prototype; however, trends suggest that ongoing optimization efforts are likely to align noise performance with design expectations. SEU tests revealed a clear reduction of upsets in the second version, confirming the effectiveness of triple redundancy and improved robustness against radiation-induced effects. TID tests showed an increase in current consumption, particularly in the digital section. During

the annealing phase, the chip subjected to rapid dose accumulation fully recovered, whereas the chip exposed to higher total doses exhibited gradual recovery. These results highlight the significant influence of both dose rate and total accumulated dose on the long-term stability and recovery potential of the ASIC.
Overall, the comparison between the first and second versions of ToASt highlights the improvements achieved through design refinements and parameter optimization. The second version demonstrates enhanced calibration uniformity, reduced susceptibility to SEUs, well-characterized TID behavior, and comparable noise performance, providing a solid foundation for future deployment in the PANDA experiment.

For CLEOPATRA ASIC, characterization focused on evaluating performance under nominal operating conditions. These measurements provided critical insights into the device response, identifying both strengths and areas requiring further optimization. While the characterization conducted in this work established a baseline understanding of the chip, a second version is currently under development. The updated design aims to address limitations observed in the first prototype and to further enhance performance, reliability, and radiation tolerance. The findings of this thesis will guide design decisions for the next iteration, ensuring that lessons learned from the initial characterization are fully incorporated. Several directions for future work emerge from this study. For ToASt, further optimization of calibration and noise parameters is expected to reduce residual variability and improve stability. Extended radiation testing, including long-term SEU monitoring and TID exposure beyond current limits, will provide deeper insights into the ASIC's robustness under extreme conditions. For CLEOPATRA, development of the second version should integrate lessons from the initial characterization, with particular focus on uniformity, noise performance, and radiation tolerance. More broadly, the characterization methodologies established in this thesis can be applied to future ASIC designs, ensuring that high-energy physics experiments have access to reliable, well-understood front-end electronics.

In conclusion, this thesis has successfully characterized two advanced ASICs, providing a detailed understanding of their performance under both nominal and radiation-influenced conditions. The work demonstrates the effectiveness of calibration and redundancy strategies, validates improvements achieved in the second version of ToASt, and sets the stage for the continued development of CLEOPATRA. Beyond

these specific results, this research contributes to the broader understanding of ASIC design and characterization in high-energy physics, providing useful insights and reference data that may support future developments in this field.

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Appendix A

This appendix collects the main configuration parameters and register settings used during the experimental characterization of the ToASt ASIC.
The reported tables provide a reference for the test pulse configuration, channel and region settings, and data formats adopted throughout the measurements.

GCR14[6]	GCR14[5:0]	VPULSE [mV]	QINJ [fC]
0	111111	0	0
0	110001	11.3	4
0	000000	47	16.5
1	111111	0	0
1	110001	44.8	15.7
1	000000	188	65.8

Table A.1 Test pulse tuning

Reg	Bits	Function	Default
0	11:10	Reserved for future use	00
0	9	Energy threshold DAC range	0
0	8	Time threshold DAC range	0
0	7	Channel mask	0
0	6	Delay enable	0
0	5	Calibration enable	0
0	4:0	ToT discharge current calibration DAC	00000
1	11:6	Energy threshold DAC	000000
1	5:0	Time threshold DAC	000000

Table A.2 Channel configuration registers bit assignment

Name	Function
single_th	use EB signal
le_only	only leading edge
polarity	only mode detector polarity

Table A.3 Common channel configuration signals

Reg	Bits	Function	Default
0	11:0	SEU counter	`hex 000`
1	11:8	Reserved for future use	`0000`
1	7:0	Busy signal monitor	`hex 00`

Table A.4 Region configuration registers bit assignment

Packet type	Bits	Description
Data	11	Region[2:0] Channel[2:0] Le[11:0] Te[11:0]
Header	10	10 ChipId[6:0] Reserved[12:0] FrameN[7:0]
Trailer	01	01 DataCnt[11:0] CRC[15:0]
Sync	00	00 1100 1100 1100 1100 1100 1100 1111

Table A.5 Data formats

Function	Data	Op code
Chip Select	1101	$01a_Ba_6a_5a_4a_3a_2a_1a_0 00$
Chip Deselect	0000	00xx xxxx xxxx
Register select (channel)	0100	$0000r_2r_1r_0 0c_2c_1c_0a_0$
Register select (region)	0100	$0000r_2r_1r_0 1a_3a_2a_1a_0$
Register select (global)	0100	$00010a_6a_5a_4a_3a_2a_1a_0$
Register write	0101	$d_{11}d_{10}d_9d_8d_7d_6d_5d_4d_3d_2d_1d_0$
Register read	0110	0000 0000 0000
No operation	1111	0000 0000 0000
GCR read word	1000	$d_{11}d_{10}d_9d_8d_7d_6d_5d_4d_3d_2d_1d_0$
Channel register read word	1010	$d_{11}d_{10}d_9d_8d_7d_6d_5d_4d_3d_2d_1d_0$

Table A.6 Configuration operation codes

Bit	Function	Default
11	not used	0
10	detector polarity	1
9	leading edge-only mode	0
8	single threshold mode	0
7	not used	0
6	Frame counter reset	0
5	Tx 1 enable	0
4	Tx 0 enable	1
3–2	not used	00
1	Time stamp counter Gray mode	1
0	Time stamp counter enable	1

Table A.7 GCR0 bit assignment

Bit	Function	Default
11	*not used*	0
10	CfgTx inversion	0
9	Tx_1 inversion	0
8	Tx_0 inversion	0
7:4	CfgTx output current control	1000
3:0	Tx 0 and 1 output current control	1000

Table A.8 GCR1 bit assignment

Appendix B

This appendix summarizes the configuration parameters and bias settings used for the CLEOPATRA ASIC.
The tables report the relevant register assignments, operation codes, and analog bias values employed during the experimental tests.

Pad	Min	Typ	Max	Unit	Description
VTH	0	750	900	mV	Discriminator threshold
VREF	0	525	900	mV	Amplifier reference
VQP	0	800	900	mV	Positive vpulse
VQN	0	300	900	mV	Negative vpulse
IREF	4	10	16	μA	CSA_ZC DAC ref
IBIAS_D	4	10	16	μA	bias discriminator
IBIAS_G	4	10	16	μA	bias channels G
IBIAS_GB	4	10	16	μA	bias channels GB

Table B.1 Analog Bias values

Function	Data	Op code
Chip Select	1101	$01a_Ba_6a_5a_4a_3a_2a_1a_000$
Chip Deselect	0000	00xx xxxx xxxx
Register select (channel)	0100	$0000r_2r_1r_00c_2c_1c_0a_0$
Register select (region)	0100	$0000r_2r_1r_01a_3a_2a_1a_0$
Register select (global)	0100	$00010a_6a_5a_4a_3a_2a_1a_0$
Register write	0101	$d_{11}d_{10}d_9d_8d_7d_6d_5d_4d_3d_2d_1d_0$
Register read	0110	0000 0000 0000
No operation	1111	0000 0000 0000
Register read word	1000	$d_{11}d_{10}d_9d_8d_7d_6d_5d_4d_3d_2d_1d_0$

Table B.2 Configuration operation codes

Register	Bits	Name	Default	Assignment
0	9:6	cap_fcomp	0	Analog control
0	5:3	cap_fback	0	Analog control
0	2:0	cap_inj	0	Analog control
1	6:5	Ib_a1	0	Analog control
1	4:3	Ib_a21	0	Analog control
1	2:0	Ib_a22	0	Analog control
2	11:4	Ib_zcT	0	Analog control
2	3:0	Ib_zc2	0	Analog control
3	11:0	chPolarity	00	Channel polarity
4	11:0	chRst	00	Analog channel reset
5	11:8	drvStrenght	1111	Drivers strenght control
5	7:4	cmMode	111	Drivers common mode control
5	3	enTermRst	1	Enable termination pad rst
5	2	enTermLd	1	Enable termination pad latch
5	1	enTermDin	1	Enable termination pad Din
5	0	enTermCk	1	Enable termination pad clk

Table B.3 Bit assignment for registers 0-5

Register	Bits	Name	Assignment
6	5:4	data_valid	0x $\rightarrow$ synch pattern 10 $\rightarrow$ channel register 11 $\rightarrow$ configuration register
6	3:0	adress	Channel/configuration address

Table B.4 Bit assignment for register 6

GCR06		Output word				
4	**3:0**	**31:28**	**27:20**	**19:16**	**15:4**	**3:0**
0	n	1001	$ReadOutReg(n)$			0110
1	m	1001	11001100	m	$GCR(m)$	0110
0	$n > 11$	1001	1100 1010	1100	1100 1010	0110
1	$m > 6$	1001	1100 1010	1100	1100 1010	0110

Table B.5 Data output format

Pin	Type	Direction	Comment
Iin[11:0]	Analog	IO	Analog inputs
Vref	Analog	IO	Input voltage reference
Vth	Analog	IO	Comparator threshold
VQ±	Analog	IO	Charge quantum control
rst±	SLVS	IN	Synchronous reset
clock±	SLVS	IN	Clock
latch±	SLVS	IN	Latch counter into registers
Din±	SLVS	IN	Serial data in
Dout±	SLVS	OUT	Serial data out
Iref	Analog	IO	Bias current
Ibias_D	Analog	IO	Bias current
Ibias_G	Analog	IO	Bias current
Ibias_GB	Analog	IO	Bias current
VDDA	Supply	IO	Analog supply
GNDA	Ground	IO	Analog ground
VDDD	Supply	IO	Digital supply
GNDD	Ground	IO	Digital ground
VDDIO	Supply	IO	IO supply
GNDIO	Ground	IO	IO ground

Table B.6 CLEOPATRA pinout