JCO: Optimization Framework for Nonlinear Superconducting Circuits Using a Lumped-Element Approach and Harmonic Balance

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E. Palumbo, A. Alocco, A. Celotto, L. Fasolo, B. Galvano, P. Livreri, and E. Enrico

***Abstract*—In this contribution, we present JosephsonCircuitsOptimizer.jl (JCO), a simulation and optimization framework based on the JosephsonCircuits.jl library for Julia. It models superconducting circuits that include Josephson junctions (JJs) and other nonlinear elements within a lumped-element approach, leveraging harmonic balance—a frequency-domain technique that provides a computationally efficient alternative to traditional time-domain simulations. JCO automates the evaluation of optimal circuit parameters by implementing Bayesian optimization with Gaussian processes through a device-specific metric and identifying the optimal working point to achieve a defined performance function. This makes it well-suited for circuits with strong nonlinearity and a high-dimensional set of coupled design parameters. To demonstrate its capabilities, we focus on optimizing a Josephson Traveling-Wave Parametric Amplifier (JTWPA) based on Superconducting Nonlinear Asymmetric Inductive eLements (SNAILs), operating in the three-wave mixing (3WM) regime. The device consists of an array of unit cells, each containing a loop with multiple JJs, that amplifies weak quantum signals near the quantum noise limit. By integrating efficient simulation and optimization strategies, the framework supports the systematic development of superconducting circuits for a broad range of applications.**

***Index Terms*—Superconducting quantum circuits, Josephson circuits, Josephson junctions, simulations, nonlinear circuit simulations, Bayesian optimization, JTWPA, SNAIL.**

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I. Introduction

SUPERCONDUCTING quantum circuits based on Josephson junctions (JJs) play a central role in the advancement of quantum technologies [1], [2], [3]. Their low dissipation, strong intrinsic nonlinearity, and suitability for coherent microwave control make them ideal candidates for implementing key components in quantum computing and quantum signal processing [4], [5], [6].

The simulation of such circuits presents significant computational challenges. Their strong nonlinearity and large number of degrees of freedom typically result in high-dimensional, nonlinear differential equations that are computationally expensive to solve. Traditional time-domain methods often require long integration times and fine temporal resolution, making them unsuitable for efficiently exploring circuit behavior across broad parameter spaces [7], [8], [9]. In contrast, frequency-domain techniques such as harmonic balance offer a more efficient strategy by directly computing the steady-state response of the system in terms of its frequency components, without simulating its time evolution. This approach is particularly well-suited for circuits operating under continuous, periodic driving, where capturing the long-term behavior efficiently and reliably is essential [7], [8].

To enable fast and scalable simulations of nonlinear superconducting circuits, the `JosephsonCircuits.jl` library [10] for the Julia programming language provides a powerful and flexible framework for modeling lumped-element superconducting circuits that include JJs and other nonlinear components. It implements harmonic balance for frequency-domain steady-state analysis [9], enabling efficient exploration of a large number of circuit configurations.

This paper presents `JosephsonCircuitOptimizer.jl` (JCO) [11], a simulation and optimization framework built on top of `JosephsonCircuits.jl`. Existing approaches to superconducting circuit optimization target objectives such as parameter matching through electromagnetic simulations [12], robustness to fabrication variations [13], and optimization of quantum properties from Hamiltonian models [14], [15], [16], using strategies such as physics-guided updates, gradient-based methods, and data-driven surrogate models [17], often within broader design frameworks [18]. However, they do not explicitly address strongly nonlinear systems with many interacting elements, such as large-scale circuit arrays.

JCO instead enables automated exploration of high-dimensional parameter spaces by evaluating specific cost functions. The framework iteratively explores the circuit configurations using efficient linear simulations to minimize a device-specific metric and identify optimal circuit parameters. Once the optimal configuration is found, the working point of the device is determined through nonlinear simulations by maximizing a target performance, such as gain, bandwidth, or noise figure [7], [19].

To demonstrate its applicability and utility, we focus on the design of a Josephson Traveling-Wave Parametric Amplifier (JTWPA) [20], [21], [22], a nonlinear superconducting device composed of an array of JJs, designed to amplify weak quantum signals with near-quantum-limited noise performance. In particular, we consider a Superconducting Nonlinear Asymmetric Inductive eLement (SNAIL)-based JTWPA [23] operating in the three-wave mixing (3WM) regime [24], [25]. This class of devices is particularly relevant as a test case due to the large and highly coupled parameters space, the strong intrinsic nonlinearity, and the large number of unit cells, which leads to high computational cost.

Section II discusses the code architecture of the framework, detailing its design, key components, and functionality. Section III presents the use case of a SNAIL-based JTWPA, demonstrating the application of the framework to a specific superconducting quantum circuit. Finally, Section IV concludes with a summary of the framework's capabilities and potential future developments.

II. Code Architecture

This section describes the internal structure of the JCO framework, which provides a structured pipeline that integrates circuit modeling, parametric sweeps, and Bayesian optimization into a unified and extensible workflow (Fig. 1). The JCO framework operates through a modular three-step pipeline that can be iterated to account for dynamic effects such as Kerr nonlinearity (Fig. 1).

At the foundation of the framework lies the device parameter space $\mathcal{P} \subset \mathbb{R}^d$, defined by fabrication constraints, where d is the number of design parameters. Every point $\mathbf{p} \in \mathcal{P}$ represents a unique circuit configuration. In our case, $d = 7$ (see Section III), and each parameter i can assume n_i discrete values.

Stage 1. Linear simulations: Linear simulations are performed for a grid of uniformly sampled parameter points in $\mathcal{P}$. Each configuration $\mathbf{p}$ is characterized by its S-parameters $S(\mathbf{p})$, fully describing the frequency-domain behavior in the linear regime. These are computed over a broadband range—from near-DC to tens of GHz—with a resolution of about 10 MHz, depending on the desired accuracy. Each simulation is relatively fast (~ 2 s) and scales with circuit complexity and frequency resolution. A device-specific metric $\mathcal{M}(S(\mathbf{p}))$ is defined to quantify the circuit's behavior and guide the subsequent optimization. Optionally, a metric cutoff can filter configurations, highlighting relevant regions for visualization and guiding the optimization. The resulting data can be visualized through correlation matrices and one-dimensional parameter plots, revealing the design landscape and inter-dependencies (Fig. 2).

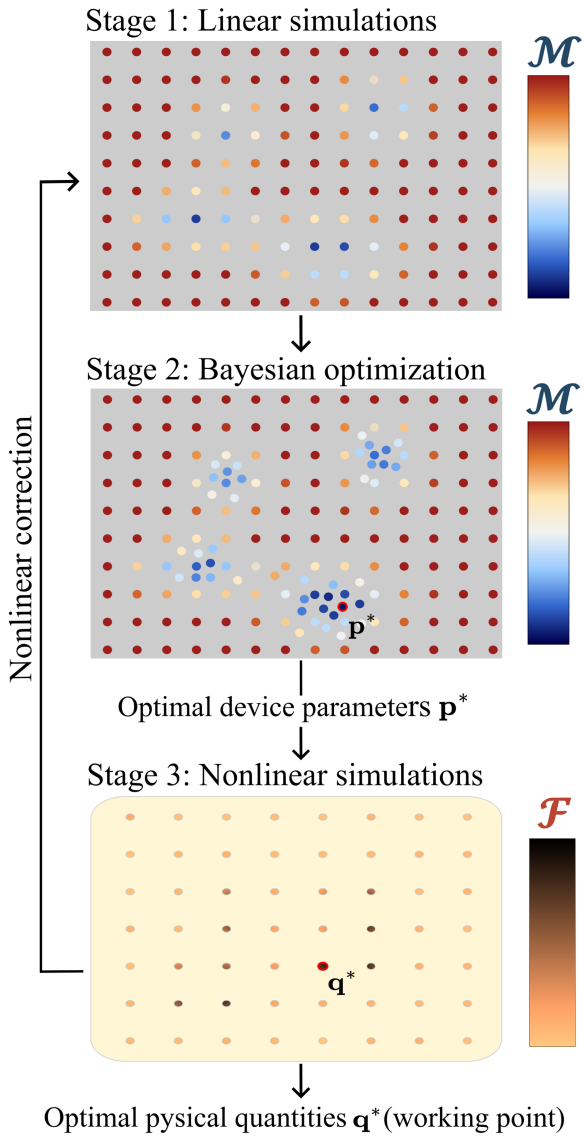

Fig. 1. Workflow of the JCO framework. The framework works as follows: (1) Linear simulations are performed across the device parameter space $\mathcal{P}$, uniformly sampled. Each configuration is assigned a metric value $\mathcal{M}$. (2) Bayesian optimization refines the sampling in regions surrounding local minima of $\mathcal{M}$ identified in the previous stage, in order to find the optimal parameters $\mathbf{p}^*$ minimizing $\mathcal{M}$. (3) Nonlinear simulations are performed by sweeping over the space of physical quantities $\mathcal{Q}$ (input frequencies and tone amplitudes) with $\mathbf{p}^*$ fixed. The process can be repeated to apply nonlinear corrections. The final outcome is the optimal device parameters $\mathbf{p}^*$ and working point $\mathbf{q}^*$ that maximizes the performance function $\mathcal{F}$. In this example, the first two stages explore two parameters taking 14 and 10 possible values, yielding 14×10 uniformly distributed configurations within $\mathcal{P}$. Each point $\mathbf{p}$ on the graph corresponds to a distinct circuit configuration, color-coded according to its metric value $\mathcal{M}$. In the third stage, two physical quantities are varied with 7×8 configurations in the $\mathcal{Q}$ space. Each point represents a different working point $\mathbf{q}$, color-coded according to the performance function $\mathcal{F}$.

Stage 2. Bayesian optimization: A Bayesian optimization strategy [26], with a Gaussian Process (GPs) [27] surrogate model, is employed to minimize $\mathcal{M}(S(\mathbf{p}))$ over $\mathcal{P}$, overcoming the limitations of uniform grid sampling by adaptively exploring the continuous design space. The algorithm focuses on regions surrounding local minima of $\mathcal{M}$, efficiently refining the search.

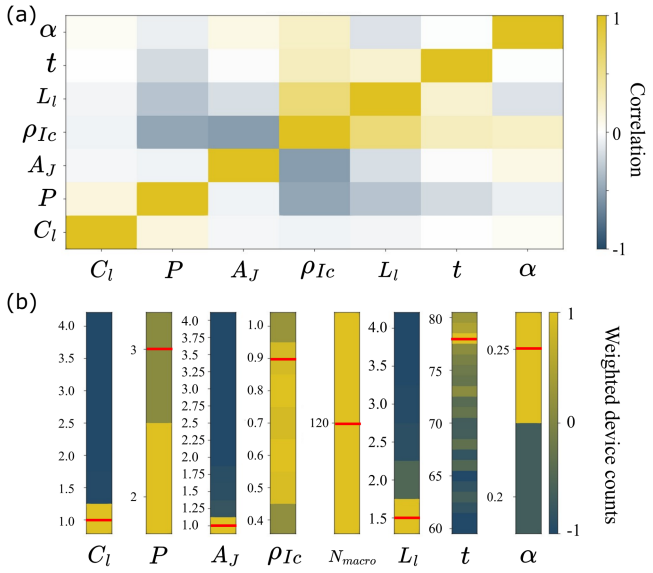

Fig. 2. (a) Correlation matrix of the device parameters and (b) 1D histogram of the parameter count weighted by the device-specific metric, for the use case presented in Section III in a larger device parameter space. The description of each parameter is provided in Fig. 3. The correlation matrix is computed over a subset of configurations filtered by a metric below a specified cutoff. These visualizations highlight parameter inter-dependencies and indicate which values contribute most to optimal circuit performance. After the optimization stage, the red lines define the best parameter configuration.

This stage converges to the optimal configuration

$$\mathbf{p}^* = \arg\min_{\mathbf{p}\in\mathcal{P}} \mathcal{M}(S(\mathbf{p})).$$

Stage 3. Nonlinear simulations: With $\mathbf{p}^*$ fixed, nonlinear simulations are performed by sweeping over a space $\mathcal{Q} \subset \mathbb{R}^k$ of k physical drive quantities, such as input frequencies and tone amplitudes. The system's response is characterized by its X-parameters $X(\mathbf{q};\mathbf{p}^*)$, which generalize S-parameters under strong tone conditions [7], [28]. A performance function $\mathcal{F}(X(\mathbf{q};\mathbf{p}^*))$ is defined to evaluate relevant figures of merit—such as gain, bandwidth, or quantum efficiency—depending on the application [7], [29]. These simulations are computationally heavier, typically requiring minutes, depending on circuit complexity and frequency resolution. After this stage, the framework can apply a nonlinear correction by updating the metric $\mathcal{M}$ to include nonlinear effects (Kerr effect) and repeating the three-step cycle as needed. The final result consists of the optimal parameter set $\mathbf{p}^* \in \mathcal{P}$ and optimal working point $\mathbf{q}^* \in \mathcal{Q}$,

$$\mathbf{q}^* = \arg\max_{\mathbf{q}\in\mathcal{Q}} \mathcal{F}(X(\mathbf{q};\mathbf{p}^*)),$$

which defines the best operating conditions for the selected circuit design.

In summary, the framework separates the process into two hierarchical stages: design-space optimization over $\mathcal{P}$ using $\mathcal{M}$, and working point selection over $\mathcal{Q}$ using $\mathcal{F}$, ensuring systematic and efficient device optimization.

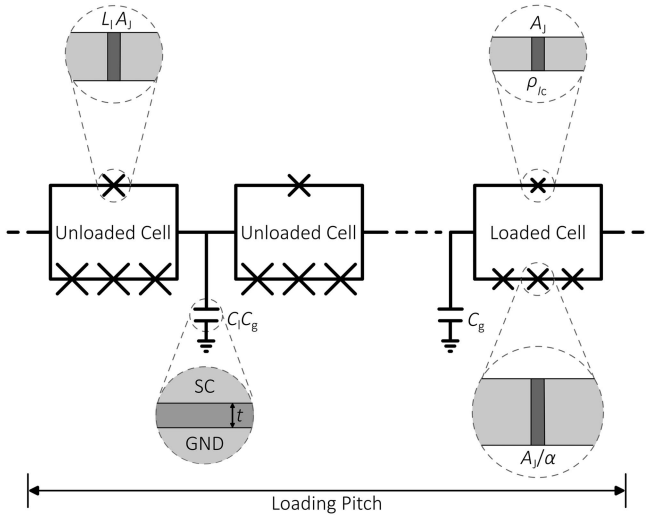

Fig. 3. Schematic of a SNAIL-based JTWPA. The device is composed of $N = N_{\text{macro}} \times P$ cells arranged in a 1D chain. Each macrocell N_{macro} consists of multiple unit cells: $P-1$ unloaded cells and one loaded cell, where P denotes the loading pitch. Each unit cell includes a SNAIL loop formed by two parallel branches. The first branch hosts a single small JJ with area A_J and critical current density ρ_{Ic}, yielding a critical current $I_c = \rho_{Ic} A_J$. The second branch contains three larger JJs, each with area A_J/α, where $\alpha \in (0,1)$ is the asymmetry parameter. The loop is threaded by an external DC magnetic flux Φ_{ext}, delivered via a dedicated flux line, which tunes the effective nonlinearity of the structure. Each cell is shunted to ground via a gate capacitance C_g, determined by the dielectric thickness t. Loaded and unloaded cells differ in their inductance and capacitance to modify the impedance and dispersion properties of the device. Particularly, L_ℓ is the ratio between the inductance of the small junction inductance of the loaded and unloaded cell, which is proportional to the ratio between the small junction areas. C_ℓ is the ratio between the ground capacitances of the loaded and unloaded cell.

III. Use Case: A SNAIL-Based JTWPA

To demonstrate the usefulness and practical relevance of the JCO framework, we consider a SNAIL-based JTWPA operating in the 3WM regime. This use case highlights how the framework adapts to a known and physically relevant problem, offering an efficient exploration of complex design spaces and identifying optimal device configurations.

The device consists of a transmission line composed of N periodically repeated SNAIL cells [23], with in our case $N = 360$ [25]. The computational cost of the simulation scales with N, as it sets the size of the underlying system. The periodic structure allows engineering of bandgaps and phase-matching conditions required for 3WM amplification.

A schematic of the circuit and a detailed description of its parameters are shown in Fig. 3.

The device parameter space explored is

$$\mathcal{P}_{\text{SNAIL}} = \{A_J, \rho_{Ic}, \alpha, t, L_\ell, C_\ell, P\}$$

where the parameters are limited by fabrication constraints imposed by lithography and material properties. Their respective ranges are reported in Table I.

The simulation is driven by the physical drive quantities:

$$\mathcal{Q}_{\text{SNAIL}} = \{f_{\text{range}}, f_{\text{DC}}, A^{\text{L}}_{\text{DC}}, A^{\text{NL}}_{\text{DC}}, f_{\text{p}}, A^{\text{L}}_{\text{p}}, A^{\text{NL}}_{\text{p}}\}$$

TABLE I
VALUES OF THE DEVICE PARAMETERS COMPOSING $\mathcal{P}_{\text{SNAIL}}$. THE COLUMN n_i INDICATES THE NUMBER OF DISCRETE VALUES CONSIDERED FOR EACH PARAMETER.

Parameter	Min	Max	Step	n_i	Unit
A_J	0.1	0.6	0.05	11	μm^2
ρ_{Ic}	0.5	1.5	0.1	11	$\mu\text{A}/\mu\text{m}^2$
α	0.23	0.25	0.02	2	adim.
t	1	20	1	20	nm
L_ℓ	1.5	2	0.5	2	adim.
C_ℓ	1	1.5	0.5	2	adim.
P	2	3	1	2	adim.

where each source i is characterized by a frequency f_{i} and amplitudes for linear A_{i}^{L} and nonlinear A_{i}^{NL} regimes. The simulated frequency span is $f_{\text{range}} = [0, 25]$ GHz with steps of 10 MHz. The first source ($f_{\text{DC}} = 0$) provides a DC flux bias, whose amplitudes depend parametrically on the SNAIL asymmetry α following a calibration curve g_{bias}, such that $A_{\text{DC}}^{\text{L}} = A_{\text{DC}}^{\text{NL}} = g_{\text{bias}}(\alpha)$. This relation enforces 3WM operation, strongly suppressing the four-wave mixing component [24]. The second source is a pump tone at $f_{\text{p}} = 11.5$ GHz, with low amplitude in linear simulations and higher amplitude in the nonlinear regime, in our case $A_{\text{p}}^{\text{NL}} = [0.1, 0.5]\,\mu$A with range 0.05 μA. The expected amplification band is centered in $f_{\text{p}/2} = 5.75$ GHz, considering a bandwidth $f_{\text{BW}} = [4.75, 6.75]$ GHz.

The metric function that evaluates the circuit's response in the first two stages is designed to quantify both impedance and phase matching, while also suppressing unwanted harmonic generation:

$$\mathcal{M}(S(\mathbf{p})) = \frac{\text{a}}{\left|\frac{1}{\Delta f_{\text{BW}}}\int_{f_{\text{BW}}} \mathbf{S}_{11}(f)\,df\right|} + \text{b}\cdot\Delta k + \text{c}\cdot|\mathbf{S}_{11}(f_{2\text{p}})|,$$

where $\text{a} = \text{c} = 10$ and $\text{b} = 1$ are weighted coefficients empirically optimized. The first term quantifies impedance matching through the mean value of the reflection coefficient $\mathbf{S}_{11}$ at f_{BW}. The second term

$$\Delta k = |k(f_{\text{p}}) - 2k(f_{\text{p}/2})|$$

evaluates the phase mismatch, where $k(f) = -\arg[\mathbf{S}_{21}(f)]/N$ is the wavenumber at frequency f. The third term penalizes transmission at the second harmonic frequency $f_{2\text{p}}$, discouraging second-harmonic generation and promoting stable three-wave mixing operation [24].

After identifying the optimal design parameters $\mathbf{p}^*$ via Bayesian optimization, a nonlinear simulation is carried out to determine the optimal working point $\mathbf{q}^*$. The nonlinear stages assess the circuit performance through

$$\mathcal{F}(X(\mathbf{q};\mathbf{p}^*)) = \frac{1}{\Delta f_{\text{BW}}}\int_{f_{\text{BW}}} \mathbf{S}_{21}(f)\,df$$

which quantifies the average transmission gain within the target bandwidth. The optimized configuration achieves a gain of approximately 20 dB at the optimal working point $\mathbf{q}^*$, as shown in Fig. 5.

The linear simulations require approximately 22 hours, while the Bayesian optimization phase took about 2 hours, exploring a total of $\prod_i n_i$ configurations. Each simulation takes ~ 2 s,

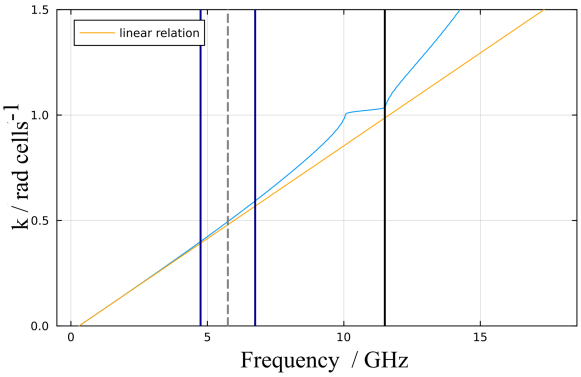

Fig. 4. Dispersion relation of the optimized SNAIL-based JTWPA, obtained by minimizing the device-specific metric to an optimal circuit configuration $\mathbf{p}^*$. The selected optimal design parameters are $\mathbf{p}^* = \{A_J = 0.49\,\mu\text{m}^2, \rho_{Ic} = 0.9\,\mu\text{A}/\mu\text{m}^2, \alpha = 0.23, t = 9\,\text{nm}, L_\ell = 1.5, C_\ell = 1, P = 3\}$. The orange line shows the linear relation $k_{\text{p}} = 2k_{\text{p}/2}$. Vertical black and dashed lines indicate f_{p} and $f_{\text{p}}/2$, while blue lines define the signal bandwidth f_{BW}.

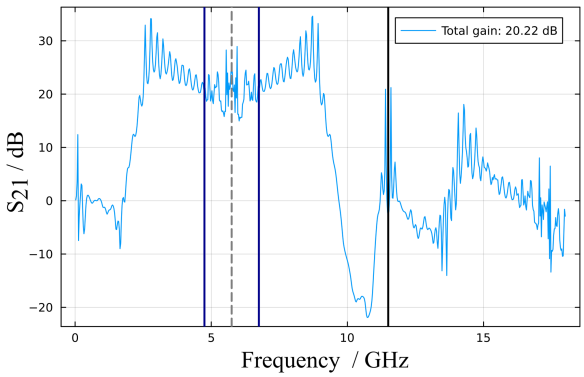

Fig. 5. Gain profile of the SNAIL-based JTWPA at the optimal working point $\mathbf{q}^*$, obtained by maximizing the performance function $\mathcal{F}(\mathbf{q}, \mathbf{p}^*)$. The selected working point is at $A_{\text{DC}}^{\text{NL}} = 212\,\mu$A and $A_{\text{p}}^{\text{NL}} = 0.1\,\mu$A. At this operating condition, the amplifier achieves a gain of approximately 20 dB. The vertical lines correspond to those in Fig. 4.

dominated by the number of cells and the fine frequency resolution. Simpler devices, such as flux-driven JPAs [30], reduce the runtime to about 0.03s per simulation. The nonlinear stage tests around 9 different configurations, varying A_{p}^{NL} and requiring tens of minutes each run. This use case demonstrates how the JCO framework efficiently identifies phase-matched operating regions and optimal drive parameters for complex superconducting circuits, providing a systematic and reproducible design workflow. Here, the reported average gain is obtained without introducing a nonlinear correction term on the linear metric, which accounts for the phase-matching relation; consequently, the gain function contains several ripples. Future work will incorporate the Kerr effect correction, leveraging existing capabilities of the framework to further improve phase matching and amplifier performance.

IV. CONCLUSION

In this work, we presented a modular framework for the simulation and optimization of superconducting quantum circuits, combining parametric circuit generation, multi-regime

simulations, and Bayesian optimization. Its effectiveness was demonstrated on a SNAIL-based JTWPA in the three-wave mixing regime, where the framework efficiently identified design and operating parameters satisfying impedance matching, phase matching, and broadband gain requirements.

The modular structure allows straightforward extension to other superconducting devices and optimization strategies, enabling systematic exploration of complex circuit topologies. Future developments include implementing nonlinear corrections such as Kerr effects, testing additional superconducting devices, applying dimensionality-reduction techniques like PCA, and exploring alternative optimization strategies. Overall, the framework provides a practical and extensible tool for designing quantum-limited amplifiers and other superconducting quantum technologies.

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