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Virtual Synchronous Compensator with Virtual Braking Resistor for Stable DC-link Voltage Control

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***Abstract*—The Virtual Synchronous Machine (VSM) algorithm represents a well-established control method for interfacing renewable energy sources with the grid. However, VSM suffers from transient stability issues, particularly when operating as a Virtual Synchronous Generator (VSG). Furthermore, maintaining control stability can be more challenging when the DC-link voltage control is implemented. Indeed, the DC-link voltage is controlled by regulating the power exchanged with the grid. However, the injected power can be limited by the applied current saturation strategy, potentially leading to DC-link overvoltage. Therefore, this article proposes implementing a Virtual Synchronous Compensator (VSC) algorithm to regulate the DC-link voltage. The VSC structure ensures the control remains stable even under current-saturation conditions. Furthermore, the Virtual Braking Resistor (VBR) concept is introduced to keep DC-link operation within the permitted voltage range without requiring communication between the DC/DC and DC/AC converters. The proposed control solution has been experimentally validated using a 30 kVA converter setup and a grid emulator, meeting both AC and DC test requirements.**

***Index Terms*— DC-link voltage, Transient Stability, Virtual Synchronous Compensator, Virtual Synchronous Machine (VSM)**

I. Introduction

Integration of Renewable Energy Sources (RES) is increasing significantly in modern power systems, introducing new challenges to system stability (e.g., lack of inertia, fault ride-through capability [1–4]). For power-electronics-interfaced RES, the VSM control represents a promising solution as it provides grid ancillary services by mimicking the dynamics of Synchronous Generators (SGs) [5–7]. Indeed, the mechanical emulation mimics the inertial behaviour [5], while the excitation control provides reactive power support to the grid [6, 7].

However, the VSM control features transient stability issues when operating as a VSG due to the mechanical emulation of SGs [8, 9]. Indeed, the virtual rotor accelerates if the reference power cannot be injected into the grid, potentially leading to the loss of synchronism. Moreover, the active power exchanged with the grid is limited during a fault, thereby causing uncontrolled dynamics and overvoltages on the DC-link [10, 11]. For the AC side, the literature demonstrates that the saturation condition affects the VSM's transient dynamics, depending on the applied strategy [12][13] (e.g., the active and reactive power priority strategies, and the angle priority strategy [12, 14]). On the DC side, the saturation strategy affects the DC-link capacitor behaviour by determining the power exchange with the grid.

Several studies in the literature analyse the DC-link dynamics when the VSM operates as a VSG (i.e., with its mechanical emulation block being commanded by the voltage control) [10, 11, 15]. The authors in [10] analyse how the voltage control parameters affect the VSG's transient response, as the necessary power exchange for the voltage regulation is achieved by using virtual rotor acceleration. Moreover, a Proportional-Integral PI feedback loop is proposed in [16] to reduce the DC-link overvoltage under fault conditions. However, the PI parameters vary the equivalent virtual inertia, as the PI block is inserted into the mechanical emulation, thereby affecting the control response to frequency perturbations. In [17], the voltage control output is saturated to reduce the acceleration of the rotor angle. However, appropriate thresholds must be defined to avoid overvoltage in the capacitor. Furthermore, the authors in [18] demonstrate how the DC-link voltage control significantly impacts the transient stability of a Phase-Locked-Loop (PLL), even for non-severe voltage dips.

Although the available solutions focus on the voltage control applied via rotor angle variations [10, 11, 16, 17, 19–21], the VSG control continues to feature transient stability and DC-link voltage control issues [8–11]. To overcome transient stability issues in conventional VSG with DC-link voltage control, this article proposes the Virtual Synchronous Compensator with voltage control. In the VSC control, the mechanical emulation operates at zero-power references, thereby ensuring the control's transient stability under fault conditions [22]. Moreover, the SG model operates in parallel with a power control block that sets the steady-state current reference (i.e., the Power-to-Current block) [6]. Indeed, the DC-link voltage is directly controlled via a Power-to-Current block, thereby decoupling transient stability issues from DC-link dynamics. Hence, the control solutions in [10, 11, 16, 17, 19] are not applicable for the VSC algorithm because of the way of they implement DC-link voltage control. To avoid overvoltage on the DC-link, the VSC is enhanced with a Virtual Braking Resistor (VBR) as a new concept. The VBR concept can be applied without affecting the transient response thanks to the VSC structure. Furthermore, two operating modes are considered to evaluate the proposed control solution: DC-link voltage controlled by the DC/DC inverter (Battery-Side Control mode (DC-BSC)) and by the DC/AC converter (Grid-Side Control mode (DC-GSC)).

The contributions of this paper are the following:

- To propose the VSC with DC-link voltage control as a

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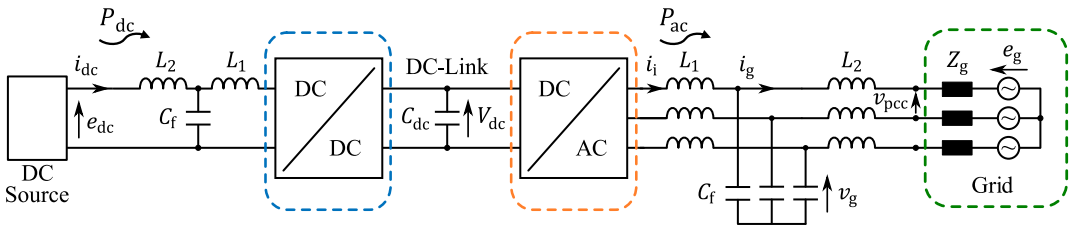


Fig. 1. Schematic representation of a DC/AC grid-tied inverter supplied from a DC source via a DC/DC inverter.

superior VSM solution that properly accounts for current saturation conditions on both DC and AC sides;
- To propose the VBR concept as a straightforward add-on solution to avoid DC-link overvoltage during fault conditions without modifying the system's hardware.

Notably, the proposed approach has the following advantages, both when the system operates in DC-BSC and DC-GSC modes:

- The control maintains transient stability under fault conditions;
- The DC-link voltage remains within the permitted range;
- No communication is required between the DC/DC converter on the DC side and the grid-tied DC/AC converter;
- No online parameter variation is needed;
- No fault detection is required;
- The VBR term depends only on the inverter's technical specifications.

The advantages above are experimentally validated in a laboratory environment using a 30 kW DC/DC inverter, a 30 kVA DC/AC inverter, and a 75 kVA grid emulator. The rest of the article is structured as follows. The control algorithm is presented in Section II along with the main AC and DC requirements. Section III analyses the control in terms of AC requirement, discussing the transient stability of the algorithm. Section IV evaluates the control for the DC requirement and presents the proposed VBR concept. The proposed solution is experimentally validated in Section V, while Section VI provides concluding remarks.

II. System Under Study

The system under study, schematically illustrated in Fig. 1, consists of a DC/DC and a DC/AC converter coupled via the DC-link with a voltage of $V_{\rm dc}$. The three-phase DC/AC inverter is connected to the grid through an *LCL* filter. Moreover, the voltage at the AC filter capacitor is indicated as $v_{\rm g}$, whereas the grid is represented as a voltage source $e_{\rm g}$ in series with its impedance $\bar{Z}_{\rm g} = R_{\rm g} + jX_{\rm g}$. On the DC side, an *LCL* filter connects the DC/DC converter to the DC source that is a battery with a voltage of $e_{\rm dc}$. The available measurements on the AC side are the inverter side current ($i_{\rm i}$), the grid side current ($i_{\rm g}$), and the voltage on the filter capacitor ($v_{\rm g}$). Moreover, the voltage at the Point of Common Coupling (PCC), $v_{\rm pcc}$, is measured. For the DC side, the DC-link voltage is measured, as well as the DC source current and voltage (i.e., indicated as $i_{\rm dc}$ and $e_{\rm dc}$ in Fig. 1).

Two main control modes are analysed in this work:

a) DC-link voltage controlled by the DC/DC converter (DC-BSC mode);
b) DC-link voltage controlled by the DC/AC converter (DC-GSC mode).

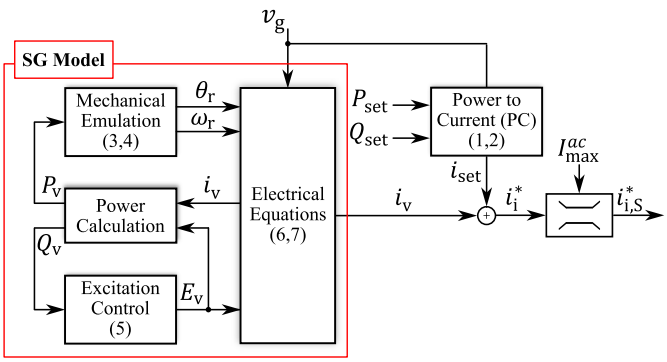


Fig. 2. Schematic overview of the VSC control.

While the control modes perform similarly under normal operating conditions, they exhibit significant differences under fault and saturation conditions (e.g., current saturation on the DC or AC side). Moreover, the AC power references strictly depend on the control mode. Therefore, the control modes are detailed in the following subsections.

A. Control Requirements

The proposed control is evaluated against AC and DC requirements, summarised in this section.

1) AC Requirements: The requirements on the AC side are related to grid code requirements and inverter/hardware constraints:

- Maintain the synchronism for 0.140 s under short-circuit [23];
- Inject reactive current during fault conditions [23, 24];
- The inverter current must not exceed the maximum allowed value $I^{ac}_{\rm max}$.

2) DC Requirements: The requirements on the DC side are related to two main components: the DC-link and the DC source. For the DC-link, the constraints depend on the DC-link capacitor. Moreover, the type of DC source defines the related constraints.

- The DC-link voltage must be kept within the permitted voltage range (i.e., $V^{dc}_{\rm min} < V_{\rm dc} < V^{dc}_{\rm max}$);
- The current must not exceed the maximum permitted value $I^{dc}_{\rm max}$;
- The power must remain within the limit of $P^{dc}_{\rm max}$;
- A rate limit can be applied to the power exchanged with the DC source to cope with its characteristics [25].

Note that the current constraint can be interpreted as a power constraint of $P^{dc}_{max} = I^{dc}_{\rm max} e_{\rm dc}$.

B. VSC Control

The VSC algorithm is applied to the DC/AC converter in Fig. 1. The control block diagram is shown in Fig. 2, and

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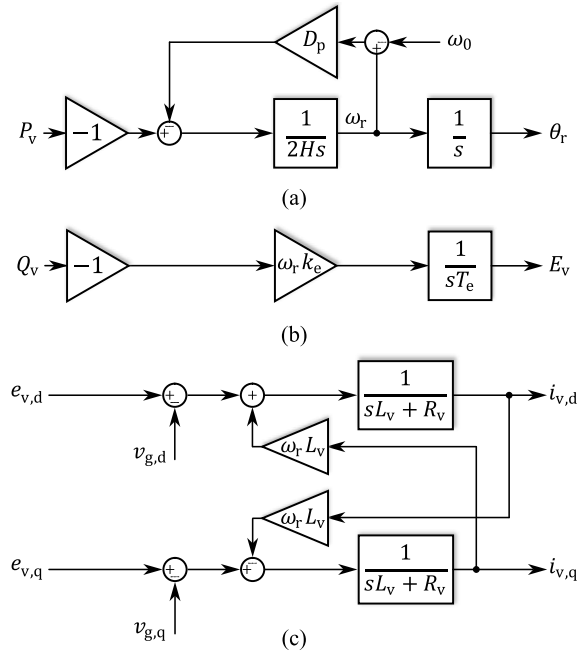


Fig. 3. Control blocks of the SG model in the continuous frequency domain: (a) mechanical emulation, (b) excitation control, and (c) electrical equations.

consists of two main components operating in parallel: the Power-to-Current (PC) block and the SG model block [6, 22]. Each control block sets the current references, denoted i_{set} and i_{v} for the PC and SG blocks, respectively. The current references are summed and sent to the current regulator implemented in the synchronous reference frame (i.e., dq-frame). The dq-frame representation allows the use of a conventional Proportional Integral (PI) controller, whose parameters are designed according to [26]. Moreover, the current reference i_{i}^* is saturated to the maximum permitted value I_{max}^{ac} according to the saturation strategy discussed in Section III-A. Note that the controlled current is the one at the inverter output, indicated as i_{i} in Fig. 1.

Starting from the PC block, it receives the active P_{set} and reactive Q_{set} power settings, from which the current references $i_{\text{set,dq}}$ are calculated as [27]:

$$i_{\text{set,d}} = \frac{P_{\text{set}} v_{\text{g,d}} + Q_{\text{set}} v_{\text{g,q}}}{v_{\text{g,d}}^2 + v_{\text{g,q}}^2}, \tag{1}$$

$$i_{\text{set,q}} = \frac{P_{\text{set}} v_{\text{g,q}} - Q_{\text{set}} v_{\text{g,d}}}{v_{\text{g,d}}^2 + v_{\text{g,q}}^2}. \tag{2}$$

Note that the power references P_{set} and Q_{set} depend on the control mode:

a) When considering DC-BSC mode, the power references are set by a higher control level (i.e., Maximum Power Point Tracking (MPPT));
b) In DC-GSC mode, the DC-link voltage control defines the active power reference, which is applied through the PC block.

Meanwhile, the SG model emulates the dynamics of a synchronous machine operating at zero power references [6, 22]. Therefore, the current reference i_{v} settles to zero in steady state, while the PC block is responsible for injecting the power references. Indeed, the SG model reacts in a dynamic way only to grid disturbances (i.e., voltage and frequency variations), thereby providing ancillary services to the grid (e.g., inertial response and reactive power support) [6, 22]. Refer to [6] for a detailed analysis of the VSC control under normal operating conditions.

As shown in Fig. 2, the three main control blocks that govern the SG model are mechanical emulation, excitation control, and electrical equations. Moreover, Fig. 3 illustrates each block in detail. The mechanical part, in Fig. 3a, mimics the inertial response through the inertial constant H. The applied damping is droop-based, via the parameter D_{p}, tuned as in [28]. The mechanical block output is the rotor angle θ_{r}, obtained as in (4), where the virtual rotor angular speed ω_{r} varies from the nominal grid angular speed ω_0 as in (4). As illustrated in Fig. 3b, the excitation control (5) determines the amplitude of the electromotive force $E_{\text{v}} = \Delta E_{\text{v}} + E_{\text{v,0}}$ according to the time constant T_{e} and the gain k_{e}, tuned as in [29]. As in conventional SGs, the virtual rotor is aligned with the q-axis (i.e., $E_{\text{v,d}} = 0$ pu, $E_{\text{v,q}} = E_{\text{v}}$, $V_{\text{g,d}} \approx 0$ pu, $V_{\text{g,q}} \approx E_{\text{g}}$).

$$\frac{d\Delta\omega_{\text{r}}}{dt} = \frac{1}{2H}\left(-P_{\text{v}} - D_{\text{p}}\Delta\omega_{\text{r}}\right) \tag{3}$$

$$\frac{d\theta_{\text{r}}}{dt} = \Delta\omega_{\text{r}} + \omega_0 \tag{4}$$

$$\frac{d\Delta E_{\text{v}}}{dt} = -\frac{\omega_{\text{r}} k_{\text{e}}}{T_{\text{e}}} Q_{\text{v}} \tag{5}$$

The SG model acts as a Thevenin equivalent (i.e., voltage source e_{v} in series with its virtual impedance $\bar{Z}_{\text{v}} = R_{\text{v}} + jX_{\text{v}}$) [30, 31][32], tuned based on [33]. Indeed, the electrical equations in the dq-frame are (6) and (7). Even though the virtual current settles to zero in steady-state, its dynamic response is described by differential equations (6) and (7) that are illustrated in Fig. 3c in the continuous Laplace domain.

$$e_{\text{v,d}} - v_{\text{g,d}} = R_{\text{v}} i_{\text{v,d}} - \omega_{\text{r}} L_{\text{v}} i_{\text{v,q}} + L_{\text{v}} \frac{di_{\text{v,d}}}{dt} \tag{6}$$

$$e_{\text{v,q}} - v_{\text{g,q}} = R_{\text{v}} i_{\text{v,q}} + \omega_{\text{r}} L_{\text{v}} i_{\text{v,d}} + L_{\text{v}} \frac{di_{\text{v,q}}}{dt} \tag{7}$$

Note that virtual powers P_{v} and Q_{v} are used as feedback to the mechanical and excitation emulations, as expressed in (3) and (5). The virtual power is the power at the virtual voltage generator e_{v}, calculated using virtual voltage e_{v} and virtual current i_{v}. For a detailed description of the virtual power concept, refer to [34].

C. DC-BSC mode

When the DC-BSC mode is implemented, the DC/DC converter controls the DC-link voltage, as illustrated in Fig. 4. A PI controller is used to regulate DC-link voltage V_{dc}. The control is implemented considering the square of the DC-link voltage, thereby obtaining power reference P_{dc}^* at the output of the voltage control block [10, 11][35]. The DC power reference, P_{dc}^*, is applied through a current controller, where current reference i_{dc}^* is calculated considering DC source voltage e_{dc}. Indeed, the controlled current is i_{dc} at the DC source side. Moreover, the current reference i_{dc}^* is saturated to the maximum permitted value of I_{max}^{dc}. In DC-BSC mode, the AC power references are set by a higher control level, whereas the DC/DC converter regulates the DC-link voltage, as shown in Fig. 4.

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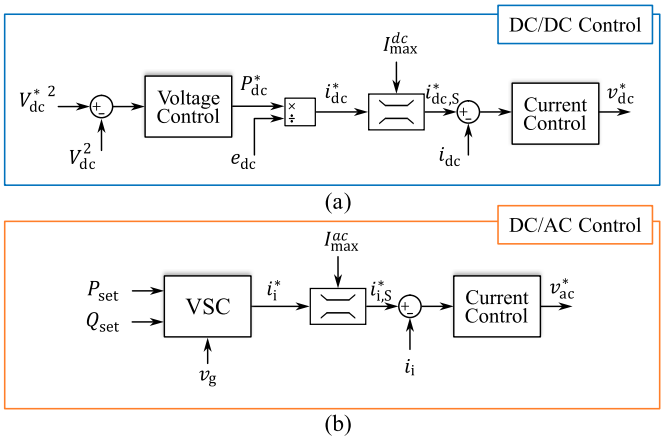


Fig. 4. Schematic representation of the DC-BSC mode (i.e., DC-link controlled by the DC/DC inverter): DC/DC control (a), and DC/AC control (b).

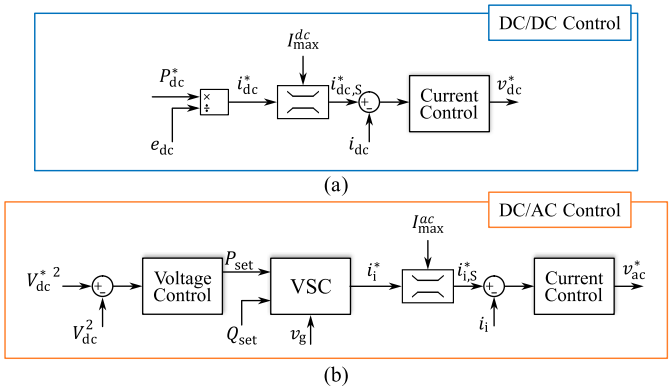


Fig. 5. Schematic representation of the DC-GSC mode (i.e., DC-link controlled by the DC/AC inverter): DC/DC control (a), and DC/AC control (b).

D. DC-GSC mode

In DC-GSC mode, the DC-link voltage control is implemented in the DC/AC inverter. The voltage control is the same as for DC-BSC mode, but the power reference is applied to the PC block as in Fig. 5. The DC power reference, $P^*_{\rm dc}$, is set by a higher control level (e.g., MPPT). Moreover, $P^*_{\rm dc}$ defines current reference $i^*_{\rm dc}$ of the current controller as illustrated in Fig. 5.

E. Concluding Remarks

As discussed in Section I, the main difference between the VSC and VSG algorithms lies in the application of the power reference:

- **VSC:** The power reference is applied via the PC block, as stated in Section II-B;
- **VSG:** The power reference is applied via the mechanical emulation [22].

Consequently, the DC-link voltage control system implementation differs significantly for the two VSMs representations:

- **VSC:** The DC-link voltage is controlled directly by the PC block;
- **VSG:** The DC-link voltage is controlled by varying the virtual rotor frequency (i.e., power reference applied to the mechanical emulation, or the voltage error is utilised to determine the virtual rotor frequency) [10, 11, 16, 17, 19–21].

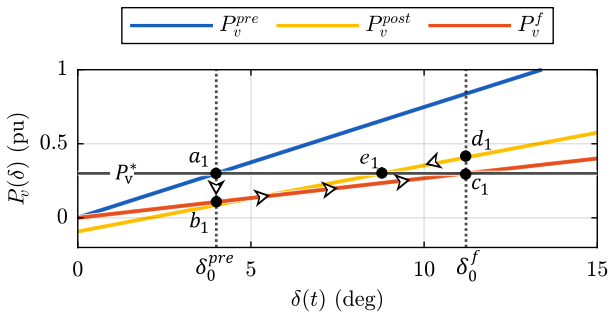


Fig. 6. Example of system trajectory during a voltage sag for a stable scenario: pre-fault power-angle curve in blue, fault power-angle curve in red, and post-fault power-angle curve in yellow.

Therefore, the distinctive feature of the VSC control structure is that it decouples transient stability from DC-link overvoltage issues, as discussed in Sections III-B and IV.

III. Actions for AC Requirements

This section considers the AC requirements presented in Section II-A1, providing actions to comply with typical grid-code requirements while the hardware ratings are not exceeded. For this purpose, Section III-B qualitatively analyses the transient stability of the VSC control, accounting for the reactive priority saturation strategy.

A. Current Saturation

According to AC requirements, the control must prioritise the reactive current to support the grid during a fault [23, 24]. Therefore, the reactive priority saturation strategy can be applied, as widely discussed in the literature [12, 14]. Note that the axis to be prioritised depends on the control alignment. For the algorithm in Section II-B, the d-axis current corresponds to reactive power since the control system aligns the grid voltage with the q-axis. Therefore, the reactive-priority saturation strategy is implemented as in (8), where the reference module is saturated to $I^{ac}_{\rm max}$. Moreover, the current control is equipped with an anti-windup, as the output voltage amplitude is saturated at $V_{\rm dc}/\sqrt{3}$ [27].

$$\begin{cases} |i^*_{\rm i,S,d}| &= \min\left(|i^*_{\rm i,d}|, I^{ac}_{\rm max}\right) \\ |i^*_{\rm i,S,q}| &= \min\left(|i^*_{\rm i,q}|, \sqrt{(I^{ac}_{\rm max})^2 - i^{*2}_{\rm i,S,d}}\right) \end{cases} \tag{8}$$

Note that the active power reaches zero when this saturation strategy is applied, thereby affecting the transient dynamics depending on the type of VSM control as discussed in Section III-B [12, 14].

B. Transient Stability Considerations

As is widely known in the literature, the VSM control algorithm can exhibit transient stability issues under fault conditions [8, 9]. In more detail, the mechanical emulation governs the control's transient response. Therefore, the VSM's transient stability varies for the VSC and VSG algorithms as follows:

- In the VSC, the mechanical emulation operates at zero power reference. Therefore, the rotor angle does not accelerate during the fault but settles at a stable equilibrium

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point. Consequently, the VSC maintains synchronism regardless of the fault duration [6, 22];
- In the VSG, the rotor angle typically accelerates during the fault because the power reference is not zero. Therefore, the transient stability of the VSG control is not guaranteed a priori and must be evaluated under pre-fault, fault, and post-fault conditions [8, 9].

To clarify the VSC behaviour, an example of power-angle curves is depicted in Fig. 6 for a symmetrical voltage sag, where δ represents the phase shift between the virtual voltage generator $e_{\rm v}$ and the grid $e_{\rm g}$. Note that the power reference $P_{\rm v}^*$ is greater than zero in Fig. 6 for the clarity of representation. As shown in Fig. 6, the system operates at point a_1 during the pre-fault condition (blue curve). When the fault occurs, the system moves to point b_1 and accelerates following the fault power-angle curve (in red). During the fault, a stable equilibrium point exists where power reference $P_{\rm v}^*$ intersects the power-angle curve at point c_1. Therefore, the system settles at the equilibrium point until the fault is cleared.

The VSC exhibits the transient behaviour as shown in Fig. 6, and it typically operates close to δ equal to zero [6]. Indeed, a stable equilibrium point exists under fault conditions as the power reference is set to zero. Therefore, the VSC can maintain the synchronism independently of the clearing time [22]. Refer to [22] for a comprehensive comparison between VSG and VSC transient stability based on Lyapunov's Direct Method.

1) Current Saturation Conditions: Note that the above considerations remain valid even when the reactive priority saturation strategy is implemented. Indeed, the saturation condition does not deteriorate the VSC's transient stability for two main reasons:

1) As shown in Fig. 3, the power reference is zero on the mechanical emulation. Therefore, the VSC control is stable even when the AC output power is limited to zero (i.e., reactive priority strategy);
2) As stated in Section II-B, the SG model utilises the virtual power feedback (i.e., $P_{\rm v}$ and $Q_{\rm v}$ in Fig. 2). The virtual power differs from the output power under saturation conditions, as $P_{\rm v}$ depends on the non-saturated virtual current $i_{\rm v}$. Therefore, virtual power $P_{\rm v}$ is not restricted by saturated output current $i_{\rm i,S}^*$ resulting in improved transient response of the VSM control [34].

Refer to [34] for a detailed description of the virtual power concept and its effect on VSMs' transient stability.

2) DC-link Voltage Control: As shown in Fig. 5, the DC-link voltage control is implemented via the PC block in the VSC algorithm. Therefore, the voltage control does not significantly affect the SG model's dynamic or transient stability, as the mechanical emulation remains unchanged. Indeed, the VSC structure maintains the synchronism when the system operates in DC-BSC and DC-GSC modes, as required by [23].

In contrast to the VSC, the VSG control is particularly challenging in DC-GSC mode because the DC-link voltage regulation is typically implemented via the mechanical emulation block [10, 11, 16, 17]. Consequently, the VSG algorithm can experience both transient stability and overvoltage issues.

C. Concluding Remarks

The control presented in Section II-B meets all the AC requirements defined in Section II-A1. Note that the main challenge concerns synchronism, which the VSC structure can guarantee through the zero-power reference in the SG model. Furthermore, the current saturation condition does not deteriorate the VSC transient dynamic, since the virtual power feedback is utilised in the control [34].

IV. Actions for DC Requirements

This section provides the control actions to meet the requirements stated in Section II-A2, particularly for the DC-link voltage constraints. To this purpose, the Virtual Braking Resistor concept is presented, analysing its impact on DC-link voltage control and current saturation conditions.

A. Virtual Braking Resistor (VBR)

Depending on the operating mode, current saturation on the DC and AC sides can cause overvoltage, damaging the DC-link capacitor. Therefore, the VBR concept is proposed and applied in both DC-BSC and DC-GSC modes.

1) DC-link voltage: The DC-link voltage control represents one of the main issues under fault or AC side current saturation conditions. In more detail, two main factors significantly impact the voltage control:

- The AC active power is lower due to the fault condition (e.g., output power is zero under a short-circuit scenario);
- Even with a voltage dip, the AC active power is saturated to zero due to the reactive priority saturation strategy discussed in Section III-A.

Consequently, the power drawn from the DC source charges the DC-link capacitor, thus leading to overvoltages and potential damage. Furthermore, the DC-link voltage response depends on the operating mode:

- In DC-BSC mode, power drawn from the DC source $P_{\rm dc}^*$ settles to the AC output power since it is directly controlled by the voltage regulator, as shown in Fig. 4. Therefore, the voltage control is ensured in DC-BSC mode;
- When the DC-GSC mode is applied, the DC-link voltage cannot be controlled if the current saturation limits the AC output power. Equivalently, the DC-link voltage control saturates, leading to uncontrolled dynamics in the capacitor.

Therefore, the DC-GSC mode is examined under AC-side current saturation conditions to assess the proposed control. Let us consider the worst-case scenario for the DC-link voltage control (i.e., AC output power saturated to zero due to a fault or short-circuit condition). In this scenario, the DC-link voltage dynamics can be represented by (9), where $\Delta V_{\rm dc}^2 = (V_{\rm dc})^2 - (V_{\rm dc}^*)^2$. Moreover, the reference DC power is constant and equal to the value under pre-fault conditions $P_{\rm dc}^{pre}$, while the DC-link resistance is neglected. Note that the

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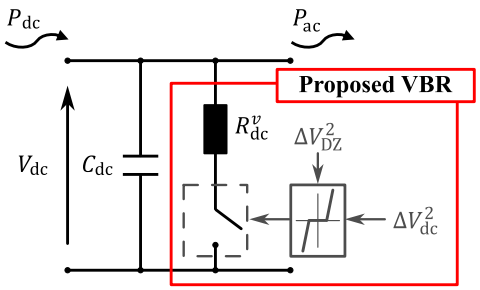


Fig. 7. Circuit representation of the DC-link when applying the proposed VBR term.

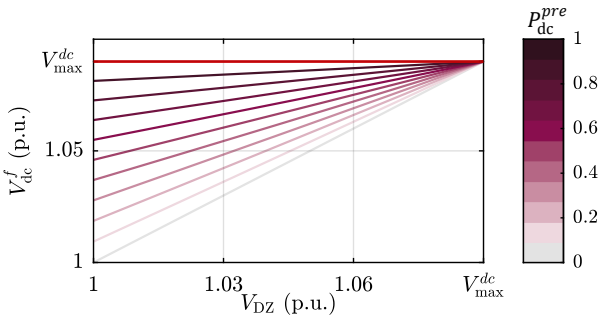


Fig. 8. Stable equilibrium point of the DC-link voltage ($V^f_{\rm dc}$) to the variation of $V_{\rm DZ}$ for multiple value of pre-fault DC power ($P^{pre}_{\rm dc}$).

DC/DC converter's current control is assumed to track the reference accurately (i.e., $P^*_{\rm dc} \approx P_{\rm dc}$).

$$\frac{1}{2}C_{\rm dc}\frac{d\Delta V^2_{\rm dc}}{dt} = P^*_{\rm dc} - P_{\rm ac} = P^{pre}_{\rm dc} \rightarrow \Delta V^2_{\rm dc}(t) = \frac{2}{C_{\rm dc}}P^{pre}_{\rm dc}t \tag{9}$$

As shown in (9), the capacitor is the only element governing the DC-link voltage dynamics during the worst-case scenario: the larger the capacitor, the slower the voltage rise.

To avoid oversizing the DC-link capacitor, power reference $P^*_{\rm dc}$ is modified according to $\frac{1}{R^v_{\rm dc}}\Delta V^2_{\rm dc}$ as in (10).

$$\frac{1}{2}C_{\rm dc}\frac{d\Delta V^2_{\rm dc}}{dt} = P^{pre}_{\rm dc} - \frac{1}{R^v_{\rm dc}}\Delta V^2_{\rm dc} \tag{10}$$

Observing the modified power equation (10), the additional term assumes a physical meaning. Indeed, the additional term represents the power dissipated across the virtual resistor, $R^v_{\rm dc}$, which is in parallel with DC-link capacitor $C_{\rm dc}$. However, the virtual resistor should act only if the voltage variation exceeds a defined range. Therefore, a dead zone $\Delta V^2_{\rm DZ} = V^2_{\rm DZ} - (V^*_{\rm dc})^2$ should be included to avoid the impact of the DC-link voltage control on the DC/AC inverter under normal operating conditions. Furthermore, Fig. 7 illustrates the resulting DC-link circuit when the VBR term is applied. As shown in Fig. 7, the virtual resistor participates in the DC-link power balance only when $\Delta V^2_{\rm dc}$ exceeds $\Delta V^2_{\rm DZ}$.

When applying the dead zone, the relation in (10) is modified as in (11) for $\Delta V^2_{\rm dc} > \Delta V^2_{\rm DZ}$.

$$\frac{1}{2}C_{\rm dc}\frac{d\Delta V^2_{\rm dc}}{dt} = P^{pre}_{\rm dc} - \frac{1}{R^v_{\rm dc}}\left(\Delta V^2_{\rm dc} - \Delta V^2_{\rm DZ}\right) \tag{11}$$

The voltage during the fault, $V^f_{\rm dc}$, can be calculated as in (12) by setting (11) to zero.

$$V^f_{\rm dc} = \sqrt{P^{pre}_{\rm dc}R^v_{\rm dc} + \Delta V^2_{\rm DZ} + (V^*_{\rm dc})^2} \tag{12}$$

Therefore, virtual resistor $R^v_{\rm dc}$ can be selected to ensure that $V^f_{\rm dc}$ is equal to or less than the maximum permitted value of $V^{dc}_{\rm max}$. To this purpose, $R^v_{\rm dc}$ can be calculated directly as in (13), where the worst-case scenario is considered (i.e., $P^{pre}_{\rm dc} = S_{\rm base}$, $P_{\rm ac} = 0$).

$$R^v_{\rm dc} = \frac{\left(V^{dc}_{\rm max}\right)^2 - (V^*_{\rm dc})^2 - \Delta V^2_{\rm DZ}}{S_{\rm base}} \tag{13}$$

Note that the transient stability on the DC side is only linked to the power balance on the DC-link capacitor, expressed in (11). With the VBR term, the control is stable during a transient as the DC-link capacitor's power is zero (i.e., a stable equilibrium point exists). Therefore, the VBR term prevents an increase of voltage and capacitor temperature.

Moreover, Fig. 8 depicts the fault voltage ($V^f_{\rm dc}$) as a function of the dead zone value ($V_{\rm DZ}$) for multiple pre-fault DC power levels. As shown in Fig. 8, the fault voltage is lower than $V^{dc}_{\rm max}$ across the entire dead-zone range, regardless of the pre-fault power. Therefore, the dead-zone value does not affect the functionality of the VBR term (i.e., ensuring a DC-link voltage within the permitted range). Nevertheless, the limits of $V_{\rm DZ}$ in Fig. 8 are only theoretical: the lowest limit is set by the voltage control, whereas $V^{dc}_{\rm max}$ sets the highest limit. In practice, the VBR term should not interact with the voltage control under normal operating conditions. A reasonable lowest limit for $V_{\rm DZ}$ is $1.02V^*_{\rm dc}$. Moreover, the dead-zone voltage should not be too close to the maximum permitted value (e.g., $1.06V^*_{\rm dc}$).

Note that the variation of DC power reference $P^*_{\rm dc}$ according to the VBR does not require communication between the DC/DC and DC/AC inverters. Indeed, the measurement of the voltage of the DC-link $V_{\rm dc}$ and its reference $V^*_{\rm dc}$ are available on the DC/DC converter when operating in DC-GSC mode. Furthermore, the capacitance value does not affect the voltage control stability since the VBR term is calculated to ensure a stable equilibrium point during the fault.

2) Current Saturation: The DC current must be limited for the source to operate within the permitted range, as stated in Section II-A2. Therefore, reference $i^*_{\rm dc}$ is saturated to its maximum permitted value $i^{dc}_{\rm max}$, as illustrated in Fig. 4. Note that the current saturation condition imposes a DC power saturation of $P^{dc}_{max} = I^{dc}_{\rm max}e_{\rm dc}$. Moreover, an anti-windup is implemented in the current and voltage controllers [27].

In more detail, the current saturation affects the overall control depending on the operating mode:

- In saturation conditions, the DC power is limited to P^{dc}_{max}. Therefore, the DC-link voltage control saturates in DC-BSC mode if the AC power reference P_{set} exceeds the maximum DC power;
- In DC-GSC mode, AC power reference $P_{\rm set}$ is adjusted to the saturated DC power according to the DC-link voltage control.

Therefore, the DC-BSC mode is considered to analyse the current saturation condition. For example, $i_{\rm dc}$ is saturated when AC reference power $P_{\rm set}$ exceeds the maximum available power on the DC side (i.e., $P^{dc}_{\rm max}$). In such a scenario, the dynamic of the DC-link voltage can be described by (14). Indeed, a negative power difference arises, thus reducing the

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DC-link voltage.

$$\frac{1}{2}C_{\rm dc}\frac{d\Delta V_{\rm dc}^2}{dt} = P_{\rm max}^{dc} - P_{\rm ac} \tag{14}$$

Therefore, the virtual resistor term is added to the AC power reference $P_{\rm set}$ as in (15). Note that $\Delta V_{\rm DZ}^2$ changes sign compared to (11) since the lower dead zone limit is reached.

$$\frac{1}{2}C_{\rm dc}\frac{d\Delta V_{\rm dc}^2}{dt} = P_{\rm max}^{dc} - P_{\rm set} - \frac{1}{R_{\rm dc}^v}\left(\Delta V_{\rm dc}^2 + \Delta V_{\rm DZ}^2\right) \tag{15}$$

In the same way as in Section IV-A, virtual resistance $R_{\rm dc}^v$ can be selected to ensure a minimum voltage value of $V_{\rm min}^{dc}$. Therefore, $R_{\rm dc}^v$ is calculated as in (16), where the worst-case scenario is considered (i.e., $P_{\rm max}^{dc} = 0$, $P_{\rm set} = S_{\rm base}$).

$$R_{\rm dc}^v = \frac{\left(V_{\rm dc}^*\right)^2 - \left(V_{\rm min}^{dc}\right)^2 - \Delta V_{\rm DZ}^2}{S_{\rm base}} \tag{16}$$

B. Rate Limiting

Depending on the DC source, a rate limit of $\rho_{\rm max}$ can be applied to the power (i.e., current reference $i_{\rm dc}^*$) exchanged with the source [25].

Let us consider a scenario in which the system operates in DC-GSC mode and the AC active power is saturated at zero. Although the VBR term is applied, the rate of power reference $P_{\rm dc}^f$ is limited to $\rho_{\rm max}$. Consequently, $P_{\rm dc}^f$ features a linear characteristic as in (17), where the time is related to the fault occurrence $t_{\rm f}$ (i.e., $\Delta t = t - t_{\rm f}$).

$$\frac{1}{2}C_{\rm dc}\frac{d\Delta V_{\rm dc}^2}{dt} = P_{\rm dc}^f(\Delta t) = P_{\rm dc}^{pre} - \rho_{\rm max}\Delta t \tag{17}$$

The maximum voltage, $V_{\rm max}^{dc}$, is reached when power reference $P_{\rm dc}^f$ is equal to zero. The corresponding time, $\Delta t_{\rm max}$, can be derived from (17), resulting in (18).

$$P_{\rm dc}^f(\Delta t) = 0 \Rightarrow \Delta t_{\rm max} = \frac{P_{\rm dc}^{pre}}{\rho_{\rm max}} \tag{18}$$

Next, the voltage $\Delta V_{\rm dc}^2(\Delta t)$ can be calculated as in (19) by integrating (17).

$$\Delta V_{\rm dc}^2(\Delta t) = \frac{2}{C_{\rm dc}}\left(P_{\rm dc}^{pre}\Delta t - \frac{1}{2}\rho_{\rm max}\Delta t^2\right) \tag{19}$$

The maximum voltage value of $V_{\rm max}^{dc}$ can be determined by substituting (18) into (19), resulting in (20).

$$V_{\rm max}^{dc} = \sqrt{\frac{\left(P_{\rm dc}^{pre}\right)^2}{\rho_{\rm max}} + \left(V_{\rm dc}^*\right)^2} \tag{20}$$

As can be observed in (20), $V_{\rm max}^{dc}$ depends on rate limit value $\rho_{\rm max}$: the faster the power is drawn from the source, the lower the maximum voltage reached during the fault. Indeed, the DC-link voltage increases until the energy is completely dissipated.

Therefore, a hardware solution must be implemented to ensure that the rate limit and maximum voltage constraints are met simultaneously [25]. Typical solutions in the literature include a resistive component in parallel with the DC-link capacitor or utilise hybrid structures (i.e., combining supercapacitors and batteries) [36, 37].

TABLE I
EXPERIMENTAL SETUP PARAMETERS.

Inverter		**Base Values**		**Grid**	
$S_{\rm N}$	30 kVA	$S_{\rm base}$	30 kVA	$\widehat{E}_{\rm g}$	$230\sqrt{2}$ V
$I_{\rm N}$	60 A	$V_{\rm base}$	$230\sqrt{2}$ V	$L_{\rm g}$	0.006 pu
$f_{\rm sw}$	8 kHz	$\omega_{\rm base}$	314 rad/s V	$R_{\rm g}$	0.0006 pu
VSM				**LCL Filter**	
$L_{\rm v}$	0.2 pu	$D_{\rm p}$	167 pu	L_1	0.0297 pu
$R_{\rm v}$	0.045 pu	$T_{\rm e}$	1 s	L_2	0.0148 pu
H	6 s	$k_{\rm e}$	0.221 pu	$C_{\rm f}$	0.166 pu
DC				**VBR**	
$V_{\rm dc}$	680 V	$V_{\rm max}^{dc}$	740 V	$R_{\rm dc}^v$ (DC-BSC)	2.47 Ω
$C_{\rm dc}$	6 mF	$V_{\rm min}^{dc}$	600 V	$R_{\rm dc}^v$ (DC-GSC)	2.9 Ω
		$V_{\rm DZ}$	700 V		

C. Concluding Remarks

The VBR approach ensures that the DC-link voltage remains within the permitted range. Note that this is achieved in both DC-BSC and DC-GSC modes, without communication between the DC/DC and DC/AC inverters. Furthermore, the VBR term does not depend on the system's parameters, and hence on their uncertainty. However, the rate constraint can be expressed in terms of an energy dissipation constraint, which entirely depends on the DC source (i.e., independent of the control), as discussed in Section IV-B. Therefore, additional hardware solutions must be implemented to ensure that both constraints are met simultaneously [36]. Typical solutions include a resistive component in parallel with the DC-link capacitor or utilise hybrid structures. In the later case, the active power reference is commonly shared between storage technologies using a high-pass filter (for the fast storage) and a low-pass filter (for the slow storage) [36]. However, more complex control methods can be also found in the literature [38]. Some common applications are microgrids [36] and wind-energy conversion systems [37]. Since the proposed solution is control-based, the hardware in Fig. 1 is not modified.

V. EXPERIMENTAL VALIDATION

The experimental setup is shown in Fig. 9, where a 30 kVA, three-phase, two-level DC/AC inverter is connected to a 30 kW, two-level, three-leg, interleaved DC/DC inverter. The cabinet containing the DC/DC and DC/AC inverters is highlighted in green in Fig. 9. Moreover, the DC-link capacitor is electrolytic, and its value and permitted range are indicated in Table I. The DC/DC inverter is supplied by a 30 kW DC source (highlighted in blue in Fig. 9). Furthermore, additional inductors are used to connect the DC/AC inverter to a 75 kVA grid emulator (shown in green in Fig. 9). The control presented in Section II is implemented in MATLAB/Simulink, where the code is generated for the experimental validation. The main system and control parameters are summarised in Table I. Note that the VSC's control parameters are defined in per-unit values, thereby being independent of the base power. The current controller is designed taking into account the *LCL* filter resonance so that the system is stable in closed-loop. Refer to [39] for more details on the electrical configuration of the laboratory.

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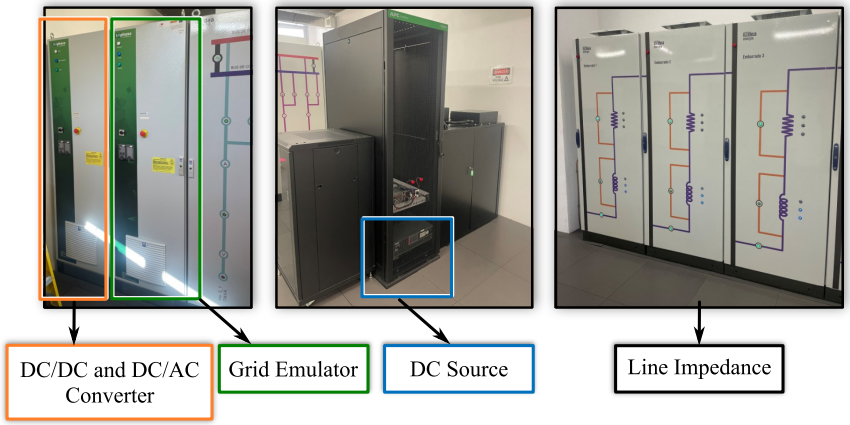


Fig. 9. Experimental setup.

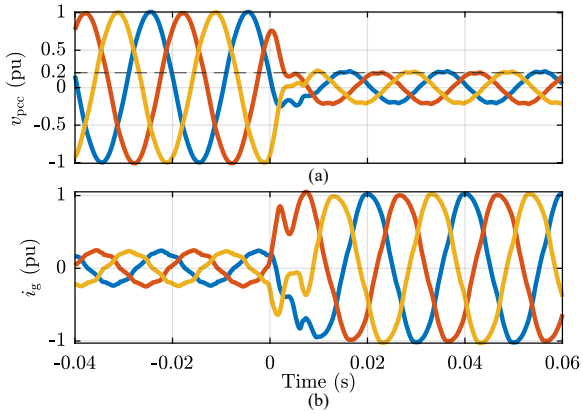


Fig. 10. DC-BSC mode. Experimental results for a symmetrical voltage sag of -0.8 p.u.: (a) three-phase voltage v_{pcc}, (b) three-phase grid current i_{g}.

To test the control for transient events, the following fault cases were applied via the grid emulator while the system operated in DC-BSC and DC-GSC modes:

- Symmetrical voltage sag of 0.2 pu of retained voltage;
- Symmetrical voltage sag of 0.4 pu of retained voltage, with a 20° phase jump;
- Unbalanced voltage sag with direct and inverse sequence amplitudes of 0.5 pu and 0.2 pu, respectively;
- Frequency drop of 0.1 Hz.

Under pre-fault conditions, the system injected 0.17 p.u. of active power into the grid. Then, voltage sags were applied for 1.5 seconds to verify the existence of a stable equilibrium point (i.e., the control's transient stability). For the DC-link voltage control, the DC-BSC mode had to maintain the voltage regulation even during AC saturation. In DC-GSC mode, the system was tested using the proposed VBR term to prevent damage to the DC-link capacitor. Moreover, the DC saturation condition was tested in the DC-BSC mode to validate the considerations stated in Section IV-A2.

A. DC-BSC mode

1) Symmetrical Voltage Sag: The system in Fig. 1 was tested under a voltage dip of -0.8 p.u. when operating in DC-BSC mode. As depicted in Fig. 10a, a fault of $E_{\mathrm{g}} = 0.2$ p.u. was applied at $t = 0$ s, when grid current i_{g} reached its maximum value of $I^{ac}_{\mathrm{max}} = 1$ p.u. Furthermore, the voltage at the filter capacitor, V_{g}, quickly decreased to 0.2 p.u., while virtual voltage E_{v} varied according to the excitation emulation block, as illustrated in Fig. 11. The VSM model responded

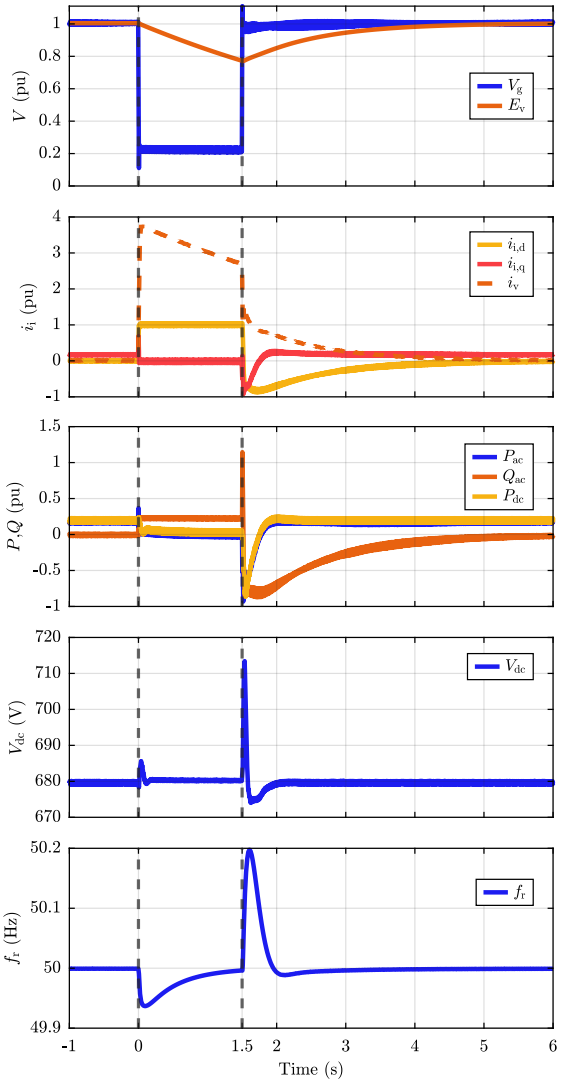


Fig. 11. DC-BSC mode. Experimental results for a symmetrical voltage sag of -0.8 p.u. From top to bottom: voltage amplitude at the filter capacitor V_{g} and virtual voltage amplitude E_{v}, dq output current $i_{\mathrm{i,dq}}$ and virtual current reference amplitude i_{v}, DC and AC powers P_{dc}, P_{ac}, Q_{ac}, DC-link voltage V_{dc}, virtual rotor frequency f_{r}.

to the voltage difference by increasing the reactive current reference i_{v}. Note that the reactive current injection persists throughout the fault due to the difference between V_{g} and E_{v}, whose dynamics depend on T_{e}. As a result, the d-axis current reference was saturated to $I^{ac}_{\mathrm{max}} = 1$ p.u., thereby limiting the AC output power to zero, as shown in Fig. 11. Consequently,

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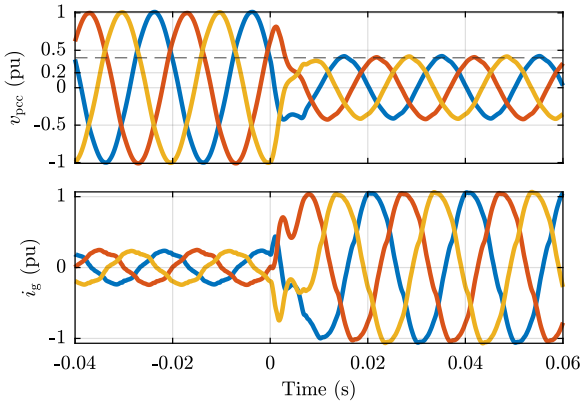


Fig. 12. DC-BSC mode. Experimental results for a symmetrical voltage sag of -0.6 p.u. and phase jump of $20°$. From top to bottom: three-phase voltage v_{pcc}, three-phase grid current i_g.

the DC-link voltage regulator reduced the power drawn from the DC source. Therefore, DC-link voltage V_{dc} returned to its pre-fault value, as shown in Fig. 11. Note that the DC-link voltage responses at $t = 0$ s and $t = 1.5$ s depend on the voltage and current control of the DC/DC converter. Moreover, the VSC synchronised with the grid during the fault, as the power references of the SG model were set to zero. As expected, virtual rotor frequency f_r settled to its nominal value during the fault, as shown in Fig. 11.

2) Symmetrical Voltage Sag with Phase Jump: Next, the symmetrical sag with phase jump was applied. The grid voltage and current are depicted in Fig. 12. As shown in Fig. 13, the control responded similarly to the case without the phase jump:

- The control injected reactive power, while the AC active power was limited to zero;
- The DC power automatically reduced, and the DC-link voltage was maintained within the permitted range by the DC/DC converter's voltage control;
- The virtual rotor frequency settled to the nominal value during the fault.

Note that the virtual rotor accelerated to adjust to the fault and the post-fault phase. Even with an abrupt phase jump, the control maintained synchronisation and the DC-link voltage settled to the reference value.

3) Unbalanced Voltage Sag: The control presented in Section II was not modified to test the unbalanced conditions (i.e., no dedicated control blocks were included for direct and inverse sequences detection). Consequently, the 100 Hz oscillation caused by the inverse sequence can be seen in the virtual rotor frequency [33], as depicted in Fig. 15. Since no direct sequence detection was applied to v_g, i_{set} contained a high harmonic content, thus causing the output current behaviour in Fig. 15. Nevertheless, the direct sequence governed the transient response:

- The virtual rotor frequency settled to the nominal value;
- The DC-link voltage settled to the reference value.

Note that the inverse sequence caused voltage oscillations on the DC-link, whose amplitude depended on the capacitor value and voltage control. To reduce AC-side power oscillations, the control can be modified to include dedicated blocks for direct and inverse sequence detection [40, 41].

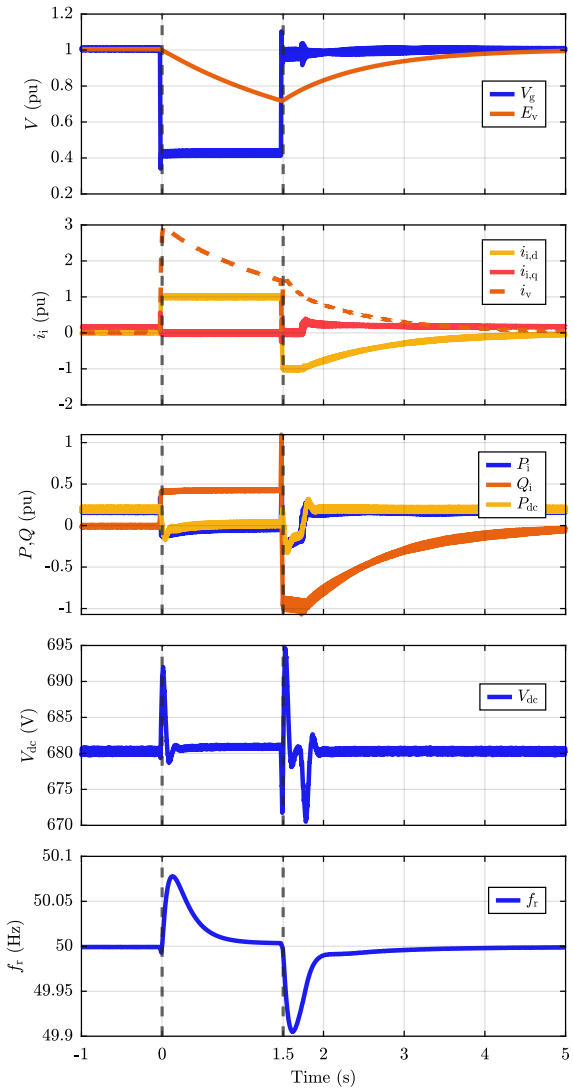


Fig. 13. DC-BSC mode. Experimental results for a symmetrical voltage sag of -0.6 p.u. and phase jump of $20°$. From top to bottom: voltage amplitude at the filter capacitor V_g and virtual voltage amplitude E_v, dq output current $i_{i,dq}$ and virtual current reference amplitude i_v, DC and AC powers P_{dc}, P_{ac}, Q_{ac}, DC-link voltage V_{dc}, virtual rotor frequency f_r.

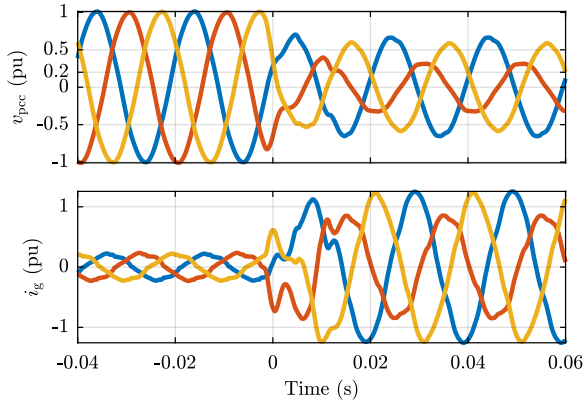


Fig. 14. DC-BSC mode. Experimental results for an unbalanced voltage sag with direct and inverse sequence amplitude of 0.5 p.u. and 0.2 p.u., respectively. From top to bottom: three-phase voltage v_{pcc}, three-phase grid current i_g.

4) Frequency Drop: Similarly to a voltage drop, the SG model injected active power through the $q-$axis virtual current for a frequency drop, as depicted in Fig. 16. Therefore, the $q-$axis output current increased, as did the AC active power.

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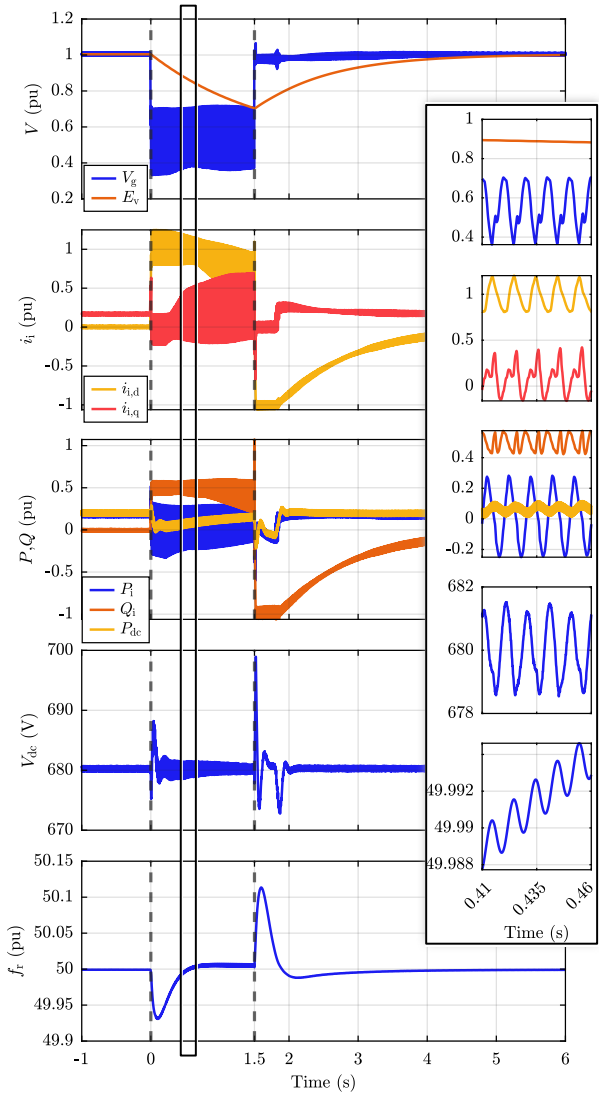


Fig. 15. DC-BSC mode. Experimental results for an unbalanced voltage sag with direct and inverse sequence amplitude of 0.5 p.u. and 0.2 p.u., respectively. From top to bottom: voltage amplitude at the filter capacitor V_g and virtual voltage amplitude E_v, dq output current $i_{i,dq}$, DC and AC powers P_{dc}, P_{ac}, Q_{ac}, DC-link voltage V_{dc}, virtual rotor frequency f_r.

Moreover, the DC/DC converter's voltage control adjusted the DC power to the AC active power. Therefore, the DC-link voltage settled to the reference value after the frequency drop, as shown in Fig. 16. It can be seen that the voltage variation at the frequency drop occurrence depended on the voltage control.

5) DC side Current Saturation: Then, the DC-BSC mode was tested under current saturation on the DC side, both with and without the proposed VBR term. For this purpose, the DC power was saturated at $P_{\max}^{dc} = 0.3$ p.u. Next, power reference P_{set} was changed from 0.17 p.u. to 0.5 p.u. at $t = 0$ s to enter the saturation condition. Fig. 17 depicts the experimental results when the VBR was and was not applied (in blue and orange, respectively). With the VBR term, AC power P_{ac} reduced to its maximum DC power value $P_{\max}^{dc}$. Therefore, the DC-link voltage settled at 661 V (i.e., within the allowed voltage range), as shown in Fig. 17. When the VBR was not applied, the voltage decreased to 597 V (i.e., below its minimum value). Due to the low DC-link voltage, the AC power oscillated while the DC/DC inverter operated under saturation conditions. Next, P_{set} was reduced to 0.17 p.u. at

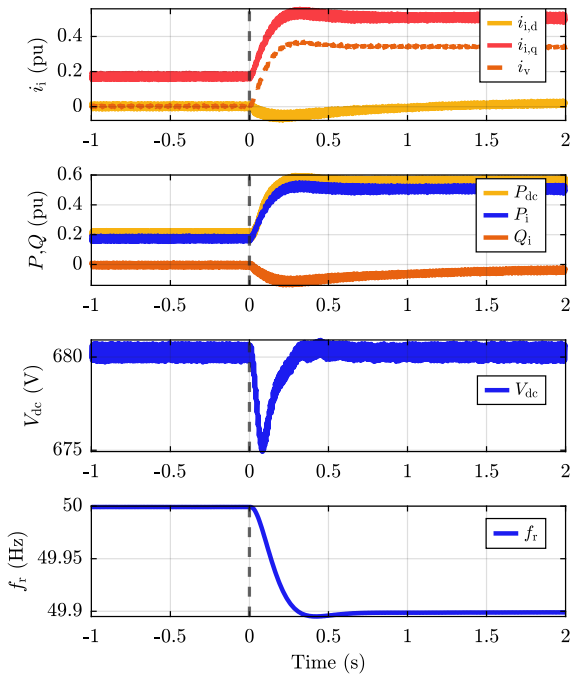


Fig. 16. DC-BSC mode. Experimental results for a frequency drop of 0.1 Hz. From top to bottom: dq output current $i_{i,dq}$ and virtual current reference amplitude i_v, DC and AC powers P_{dc}, P_{ac}, Q_{ac}, DC-link voltage V_{dc}, virtual rotor frequency f_r.

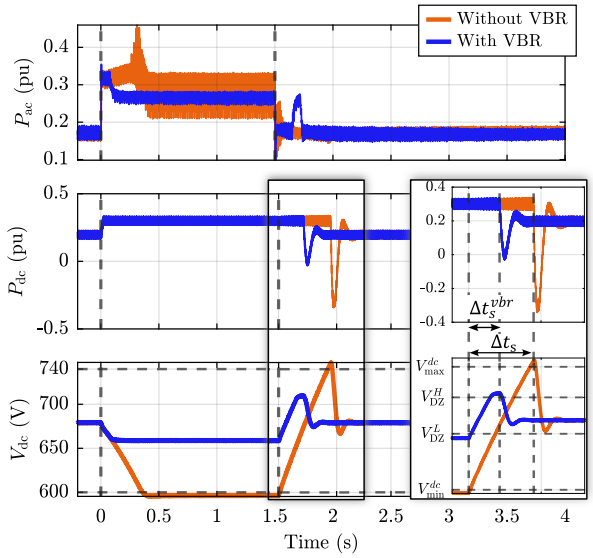


Fig. 17. DC-BSC mode. Experimental results for saturation condition with VBR (in blue) and without VBR (in orange). From top to bottom: AC active power P_{ac}, DC power P_{dc}, and DC-link voltage V_{dc}.

$t = 1.5$ s. As shown in the zoom-in in Fig. 17, the DC power remained saturated for $\Delta t_s^{vbr} = 0.21$ s when the VBR was applied. During Δt_s^{vbr}, the voltage increased to the upper limit of the dead zone. Consequently, the VBR was inserted to help reduce the voltage and bring the control out of saturation. Without VBR, the saturation condition persisted for a time of $\Delta t_s = 0.45$ s, thus determining a voltage of 747 V (i.e., above its maximum value).

Therefore, it can be concluded that the VBR approach successfully ensured the system operation within the permitted voltage range, while avoiding power oscillations and damage to the DC-link capacitor.

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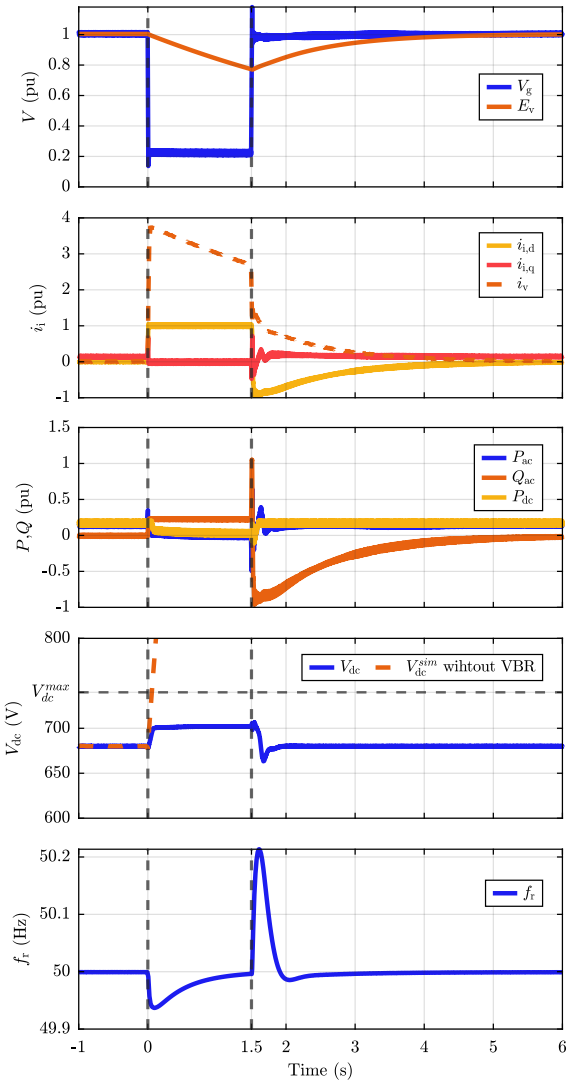


Fig. 18. DC-GSC mode. Experimental results for a symmetrical voltage sag of -0.8 p.u. From top to bottom: voltage amplitude at the filter capacitor V_{g} and virtual voltage amplitude E_{v}, dq output current $i_{\mathrm{i,dq}}$ and virtual current reference amplitude i_{v}, DC and AC powers P_{dc}, P_{ac}, Q_{ac}, DC-link voltage V_{dc} and simulated DC-link voltage without VRB V_{dc}^{sim}, virtual rotor frequency f_{r}.

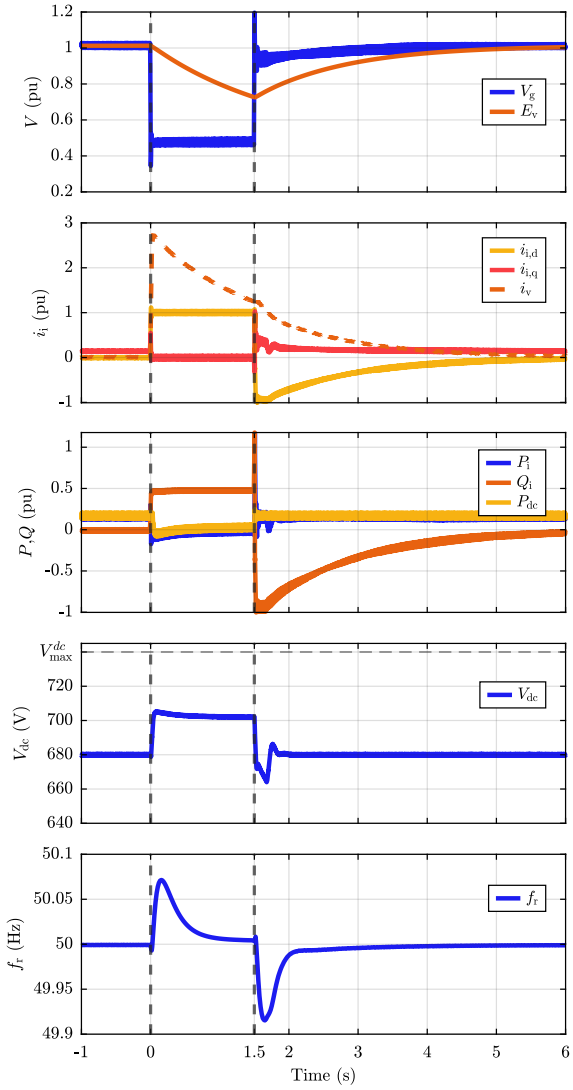


Fig. 19. DC-BSC mode. Experimental results for a symmetrical voltage sag of -0.6 p.u. and phase jump of 20°. From top to bottom: voltage amplitude at the filter capacitor V_{g} and virtual voltage amplitude E_{v}, dq output current $i_{\mathrm{i,dq}}$ and virtual current reference amplitude i_{v}, DC and AC powers P_{dc}, P_{ac}, Q_{ac}, DC-link voltage V_{dc}, virtual rotor frequency f_{r}.

B. DC-GSC mode

1) Symmetrical Voltage Sag: In DC-GSC mode, the fault condition was tested by considering the VBR term to ensure operation within the permitted voltage range. The main quantities are depicted in Fig. 18. Note that E_{v}, i_{v}, and f_{r} are internal control quantities. As in the DC-BSC mode, the SG block increased the reactive virtual current i_{v}. Consequently, the d-axis output current was saturated to I_{max}^{ac}, whereas the q-axis component was equal to zero, as shown in Fig. 18. Due to the reactive priority strategy, the AC active power was limited to zero during the fault. Consequently, the VBR term reduced the DC power P_{dc} to zero. Indeed, the difference between the AC and DC power references was virtually dissipated across the virtual resistor R_{dc}^{v}, thus preventing the DC-link voltage from increasing. Therefore, an equilibrium point existed during the fault, and the DC-link voltage settled to 702 V. For safety reasons, the fault was not applied without implementing the VBR term. Nevertheless, the PLECS simulation results for V_{dc} showed that the voltage would continue to increase during the fault. Furthermore, the VSC maintained synchronism throughout the fault, as shown in Fig. 18. Indeed, virtual rotor frequency f_{r} settled to 50 Hz during the fault. Note that the system is stable regardless of the fault duration (i.e., the DC-link voltage stays within the permitted range), as a stable equilibrium point exists during the fault.

2) Symmetrical Voltage Sag with Phase Jump: Similarly to the results in Section V-A2, the AC active power was limited to zero during the fault due to the reactive priority saturation strategy, as illustrated in Fig. 19. Consequently, the VBR term virtually dissipated the power on the DC-link capacitor by reducing the DC power reference. Therefore, the DC-link voltage settled to a stable equilibrium point during the fault, as shown in Fig. 19. At the fault occurrence, the virtual rotor frequency accelerated to follow the phase jump and then settled to the nominal value.

3) Unbalanced Voltage Sag: Same as in Section V-A3, no dedicated control blocks were implemented to detect the direct sequence. Therefore, the oscillation caused by the inverse sequence was observed in both the virtual frequency and output current, as depicted in Fig. 20. On the DC side, the

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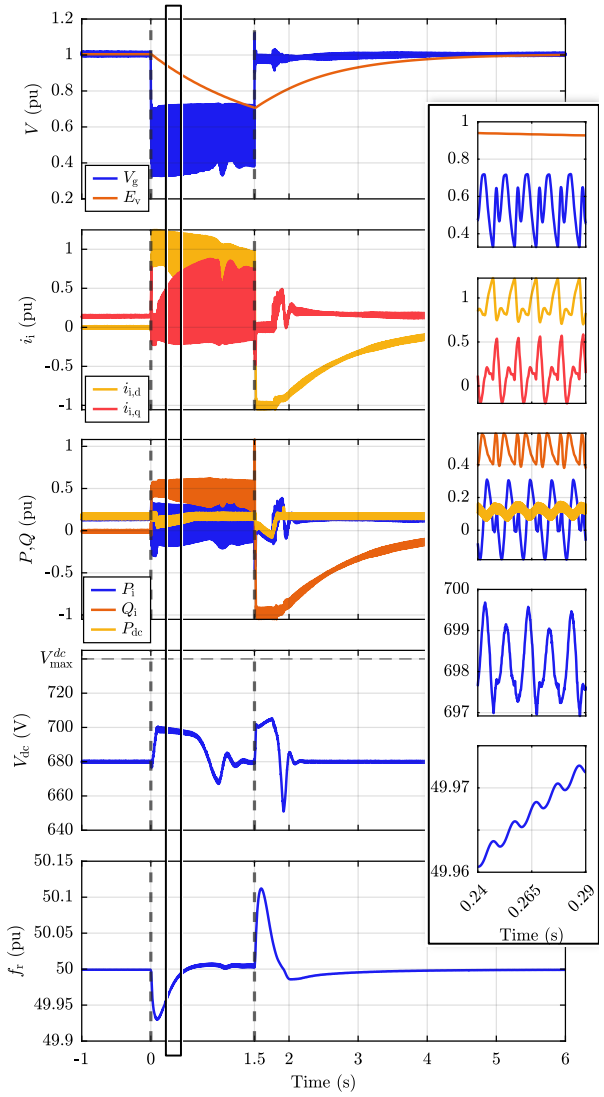


Fig. 20. DC-BSC mode. Experimental results for an unbalanced voltage sag with direct and inverse sequence amplitude of 0.5 p.u. and 0.2 p.u., respectively. From top to bottom: voltage amplitude at the filter capacitor V_g and virtual voltage amplitude E_v, dq output current $i_{i,dq}$, DC and AC powers P_{dc}, P_{ac}, Q_{ac}, DC-link voltage V_{dc}, virtual rotor frequency f_r.

VBR term was automatically applied for 0.5 s after the fault, and the voltage settled to a stable equilibrium point. Then, the DC-link voltage returned to the pre-fault value since the AC active power was no longer limited. At the fault clearance, the control injected only reactive power and the VBR term was again inserted. Next, the system returned to the pre-fault equilibrium point, as shown in Fig. 20. Indeed, the control's transient stability and voltage equilibrium point depend on the direct sequence, not on the inverse one.

4) Frequency Drop: In case of frequency drop, the DC-BSC and DC-GSC modes showed different responses. As depicted in Fig. 21, the SG model reacted by injecting active power (i.e., the virtual current increased). However, the DC-link voltage control law defines the AC output power in DC-GSC mode, as described in Section II-B. Therefore, the AC active power did not change after the frequency drop. Furthermore, the DC-link voltage remained at the reference value, whereas the dynamic response at the frequency drop depended on the voltage control.

In conclusion, it was demonstrated that the VBR approach prevents the DC-link capacitor from being damaged and that

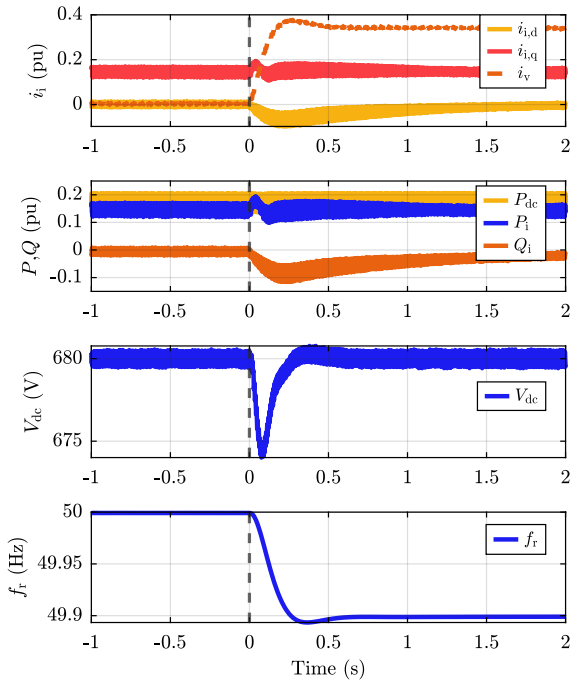


Fig. 21. DC-BSC mode. Experimental results for a frequency drop of 0.1 Hz. From top to bottom: dq output current $i_{i,dq}$ and virtual current reference amplitude i_v, DC and AC powers P_{dc}, P_{ac}, Q_{ac}, DC-link voltage V_{dc}, virtual rotor frequency f_r.

the VSC algorithm ensures the transient stability of the control.

C. Concluding Remarks

The DC-BSC and DC-GSC modes were tested under various fault scenarios. As expected from Section IV, the two modes reacted differently under AC and DC side current saturation conditions. For AC-side current saturation, the VBR term ensured that the DC-link voltage remained below the maximum value in DC-GSC mode. For DC-side current saturation, the VBR term prevented overvoltage during the recovery in DC-BSC mode. Even though the operating mode depends on the application, the proposed control solution guarantees DC-link operation within the permitted range under both DC and AC-side current-saturation conditions.

VI. Conclusion

This article proposes the VSC algorithm combined with DC-link voltage control to resolve transient stability and overvoltage issues occurring on the DC-link. Two main operating modes for DC-link voltage control have been assessed: DC-BSC and DC-GSC modes. Moreover, current saturation on the AC and DC sides was considered for the analysis of the control dynamics.

To overcome DC-link overvoltage, this article proposes the VBR concept, which offers a straightforward solution to handle current saturation in DC-BSC and DC-GSC modes during transients. Moreover, the VSC structure decouples the DC-link voltage from the transient behaviour, enabling direct voltage control without affecting transient stability.

The proposed control was experimentally validated using a -0.8 p.u. voltage dip lasting 1.5 s and evaluated based on both AC and DC requirements. Even with reactive current

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injection, the control maintained synchronism during a prolonged voltage sag, as expected from the transient stability considerations presented in Section III-B. In DC-BSC mode, the VBR ensured that the DC-link capacitor remained within its permitted range while the DC-side current was in saturation. When operating in DC-GSC mode, the DC-link voltage settled below its maximum permitted value during the fault because of the virtual power dissipation on the VBR.

Therefore, the proposed control meets the requirements stated in Section II-A, as demonstrated both theoretically and experimentally. Note that the implementation of the VBR term does not require any communication between DC/DC and DC/AC converters. In the future, additional hardware-based solutions will be investigated to apply the DC power rate limit without exceeding the maximum permitted voltage.

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