Abstract

Over the past decade, integrated circuits (ICs) have become increasingly complex and are now integrated into almost all modern systems. In the automotive industry, innovations such as Advanced Driver Assistance Systems (ADAS) have significantly increased the functional and safety requirements of electronic components. As a result, ensuring reliability has become more important than ever, as malfunctions can cause catastrophic events.

Testing plays a pivotal role in ensuring product quality and reliability. This is especially true in safety-critical domains, such as automotive, where safety standards, such as ISO26262, mandates strict requirements to be compliant with.

However, the exponential growth in complexity, the huge increase in the number of transistors, the complexity of deep operational logic, and the integration of third-party "black-box" intellectual property (IP) have made traditional testing strategies obsolete. Furthermore, conventional structural testing techniques, originally developed for smaller circuits, fail to scale to modern System-on-Chips (SoCs). These limitations result in reduced fault coverage and potential gaps in testing, highlighting the need for new methodologies.

This thesis addresses such limitations by proposing novel methodologies in the automotive manufacturing testing flow, targeting Burn-In, System-Level Test, and In-Field phases.

The first contribution focuses on the Burn-In (BI) phase, addressing testability issues that arise in the absence of netlists for third-party IPs, as this prevents the generation of effective test patterns. A novel methodology is proposed to synthesize functional stress patterns for AI accelerators based on indirect, netlist-less measurements. Unlike standard functional programs which fail to excite deep arithmetic pipelines due to high data sparsity and correlation, this approach maximizes toggle activity through specialized data patterns. Experimental results demonstrate that the

generated functional suite achieves higher switching activity and a more uniform stress distribution when compared to structural patterns, even without the netlist.

The second contribution addresses System-Level Test (SLT), specifically the inability of standard loop-back tests to excite error detection and correction logic in communication peripherals. In this regard, this thesis introduces an FPGA-based companion module that interacts with the Device Under Test (DUT) to inject protocol-level errors and timing violations. Validated on an industrial automotive SoC, this suite improves stuck-at fault coverage by approximately 50% over undetected structural faults and increases transition delay fault coverage by about 15%, effectively closing the coverage gap left by scan-based techniques.

To address the manual effort and lack of portability in SLT development, this thesis introduces a framework capable of generating functional test automatically. The proposed framework, exploiting the Device Tree Specification (DTS), abstracts the device architecture into a graph-based model, enabling the creation of portable test programs. Thus manages to reduce development time and eliminate the implicit bound of tests and a specific instruction set architecture (ISA), allowing the test suite to be used on different architecture of SoCs.

Finally, the thesis addresses the problem of devices that fail during in-field operation but pass all tests when returned to manufacturers, known as No-Trouble-Found (NTF). The proposed method leverages the on-chip Logic Built-In Self-Test (LBIST), executed at key/on-off events, to collect diagnostic information. Through a binary search algorithm, the index of the first LBIST error pattern and its corresponding signature are stored in non-volatile memory (NVM). A tree-based fault dictionary is then used to perform logic diagnosis using only the collected in-field diagnostic data.

The proposed approach was validated experimentally on both ITC'99 circuits and automotive SoCs. In this regard, real failing devices in the field were used to demonstrate the effectiveness of the methodology. Compared to state-of-the-art techniques, it provides similar or better accuracy, while remaining compatible with existing LBIST architectures, ensuring scalability and applicability.