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A Low-Cost and Ultra-Low-Data-Rate Event-Driven Platform for in-Vitro Real-Time Multichannel Neural Signal Acquisition

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***Abstract*—*In vitro* multi-electrode array (MEA) recordings are essential tools for neuroscience research, drug screening, and closed-loop neuromodulation. Yet, conventional MEA recording rely on continuous high-speed sampling, generating high data volumes that complicate processing, increase cost, and limit scalability. This work introduces a low-cost, low-data-rate, event-driven neural acquisition platform that detects neural spikes directly in hardware, encoding them as discrete digital events, retaining only their spatiotemporal information. This architecture removes the need for high-resolution digitization and post-processing, achieving over 99% data-rate reduction compared to continuous acquisition at 10 kS/s. Under controlled stress-test validation with synthetic signals across 15 simultaneous channels, the event-driven system reached F1-scores above 0.98 at 10 dB signal-to-noise ratio and remained stable up to 300 Hz firing rates, while maintaining sub-millisecond temporal accuracy. The platform can also be reprogrammed for conventional raw waveform acquisition, offering dual-use flexibility. Its modular design allows for straightforward scalability up to 60 channels, front-end upgrades or reconfiguration for other electrochemical measurements without a full hardware redesign. While the event-driven mode is not intended for experiments where spike morphology is critical, it provides an accessible and scalable solution for applications where spatio-temporal spike patterns are the key information, including network synchronization studies, burst detection, pharmacological assays, and long-term closed-loop protocols. By combining affordability, real-time performance, and high data reduction, this system establishes a practical and effective alternative to conventional electrophysiology systems for next-generation neuroscience research.**

***Index Terms*—Neural interfaces, spike detection, event-driven, MEA, hardware platform, data reduction, neural cultures**

I. Introduction

The study of *in vitro* neural networks has become an essential approach in modern neuroscience, enabling research in fundamental neurophysiology [1], [2], drug screening and neurotoxicity testing [3], and the development of closed-loop neuromodulation systems [4] and bio-hybrid interfaces [5], [6]. The ability to monitor the electrophysiological activity of cultured neurons over extended periods provides insight into network dynamics, developmental processes, and the mechanisms underlying pathological conditions.

A key element is the multi-electrode array (MEA), a substrate integrated with microelectrodes on which neurons are cultured, providing a non-invasive interface for recording neural activity. However, the full potential of this technology is often constrained by the readout instrumentation itself. Conventional MEA systems rely on high-resolution, high-speed analog-to-digital converters (ADCs) that continuously sample all channels, typically at rates above $10\,\mathrm{kS/s}$ per channel to capture action potential waveforms [7], [8]. While this strategy ensures high-fidelity recordings, it generates two major bottlenecks: data volume and cost. A standard 60-channel MEA system can produce several megabytes of data per second, placing heavy demands on transmission, storage, and real-time processing. The problem escalates further with high-density MEAs with hundreds or thousands of electrodes, where data-rate can rise to tens or even hundreds of megabytes per second [9], [10]. Such massive throughput severely limits scalability and poses challenges for applications requiring immediate feedback, such as closed-loop stimulation, as well as for long-term recordings where data storage becomes challenging [11]. Moreover, commercial 60-channel MEA platforms cost upwards of 30,000 USD, a substantial financial barrier for many laboratories [12], [13].

Several strategies exist to mitigate the high data-rate in neural recording. Lossless compression methods like delta encoding offer modest (2×) reduction with perfect reconstruction but require initial digitization [14]. Compressive sensing exploits signal sparsity for higher compression (e.g., 2.6×)

but increases computational complexity and chip area [15]. Machine learning approaches, such as autoencoders, achieve very high compression (up to 150×) but demand significant on-chip resources and introduce latency and waveform distortion [16]. Analog methods like the monostable multivibrator can achieve extreme compression (400:1) without digitization but sacrifice temporal accuracy and waveform fidelity [17].

In this work, we shift from the conventional sampling paradigm. We present a real-time, versatile multichannel neural readout platform that performs spike detection directly at the hardware level, encoding action potentials as discrete digital events using simple electronic circuits. This event-driven architecture eliminates the need for high-speed analog-to-digital conversion and subsequent digital signal processing for spike extraction, achieving lower system complexity and, crucially, an ultra-low output data-rate. The main trade-off of our approach is the loss of waveform information, making it unsuitable for studies requiring spike sorting based on shape or for fundamental electrophysiological research where morphology is critical. However, for a wide range of experiments focused on firing rates, burst detection, and network synchronization, spatiotemporal information is sufficient [4]–[6]. The system can also be reprogrammed at the firmware level to perform raw data acquisition when needed. Its modular design also allows future upgrades without a complete platform redesign.

In summary, our system follows a minimalist, hardware-centric event-detection approach, offering a powerful, accessible, and efficient alternative to conventional electrophysiology methods.

II. System Overview

The proposed platform is designed for real-time acquisition of spiking activity from up to 60 neural channels using standard passive MEAs. To reduce hardware complexity and improve data efficiency, the system adopts an event-driven architecture in which neural spikes are detected and transmitted as discrete digital events rather than continuously sampled waveforms. The system architecture is modular and consists of five primary blocks: (1) MEA interface (2) analog front-end (AFE), (3) motherboard, (4) control unit, and (5) a laptop with a graphical user interface (GUI).

An overview of the full system is illustrated in Fig. 1a, while the single-channel path is detailed in Fig. 1b. A picture of the whole platform is shown in Fig. 1c.

A. MEA Interface and Analog Front-End

The platform interfaces with MEAs of up to 60 channels, compatible with the standard pad layout of standard 60-channel MEAs by Multichannel Systems (MCS), through spring-loaded contacts, providing stable mechanical coupling and low-resistance electrical interfacing.

Each signal line routes to an edge connector that hosts a vertical plug-in AFE PCB (Fig. 1d), one per channel. This modular design allows AFEs to be easily replaced or upgraded without altering the rest of the system. Moreover, the vertical arrangement improves compactness.

Each AFE PCB performs low-noise amplification (gain = 2000) using multi-stage low-noise amplifiers (LNAs) that support an input dynamic range from fractions of a µV up to $1.5\,\mathrm{mV}$ before saturation, and band-pass filtering ($100\,\mathrm{Hz}$–$5\,\mathrm{kHz}$) to remove DC offsets, power-line interference, and high-frequency noise. The tested AFEs exhibited input-referred noise below $10\,\mu\mathrm{V}$ RMS over the passband.

The conditioned signals are then returned to the motherboard for event detection. Validation of the AFE performance was carried out separately and falls outside the scope of this work.

B. Motherboard and Control Unit

The motherboard is the central unit of the platform, providing both signal interfacing and system control. It connects the MEA to the AFE channels and distributes regulated power to all modules. It also hosts the final stage of the signal path and the circuitry that implements event-driven acquisition.

Each conditioned signal from the AFE is routed through a programmable gain amplifier (PGA), which matches the dynamic range of the detection circuitry.

The event-driven core consists of per-channel threshold comparators with hysteresis (Schmitt triggers). Each threshold crossing generates a digital pulse corresponding to a spike event, which is forwarded to the microcontroller unit (MCU) for timestamping. Thresholds are configured symmetrically to detect both positive and negative spike polarities. During calibration, the amplified signals are digitized by on-board 12-bit analog-to-digital converters (ADCs) and processed by the MCU to estimate channel-specific noise levels. Here, detection thresholds are computed and programmed into dedicated 8-bit digital-to-analog converters (DACs), which provide the reference voltages for each Schmitt trigger. This per-channel calibration ensures that event detection is automatically adapted to the noise characteristics of each electrode.

The control unit is based on an MCU (ARM Cortex-M7 @ $550\,\mathrm{MHz}$) that handles per-channel calibration, event timestamping, buffering, and host communication. A firmware's high-level flowchart is displayed in Fig. 2a

1) Calibration phase: At the beginning of each acquisition session, a calibration phase establishes the detection threshold for every channel. The MCU records $1\,\mathrm{s}$ of each conditioned signal at $10\,\mathrm{kS/s}$ using the motherboard's 12-bit ADCs to estimate channel-specific noise statistics. The noise level is quantified via the robust median-based estimator [18]:

$$\mathrm{Th} = K \cdot \sigma_n, \qquad \sigma_n = \frac{\mathrm{median}\,|x|}{0.6745}. \tag{1}$$

Prior studies indicate that choosing K between 3 and 5 provides a good compromise between sensitivity and robustness [19], [20]. In this work, $K = 5$ was adopted by default to minimize false positives, while still allowing users to adjust K through the GUI as needed. Each computed threshold is converted into an 8-bit word, and sent via SPI to a dedicated

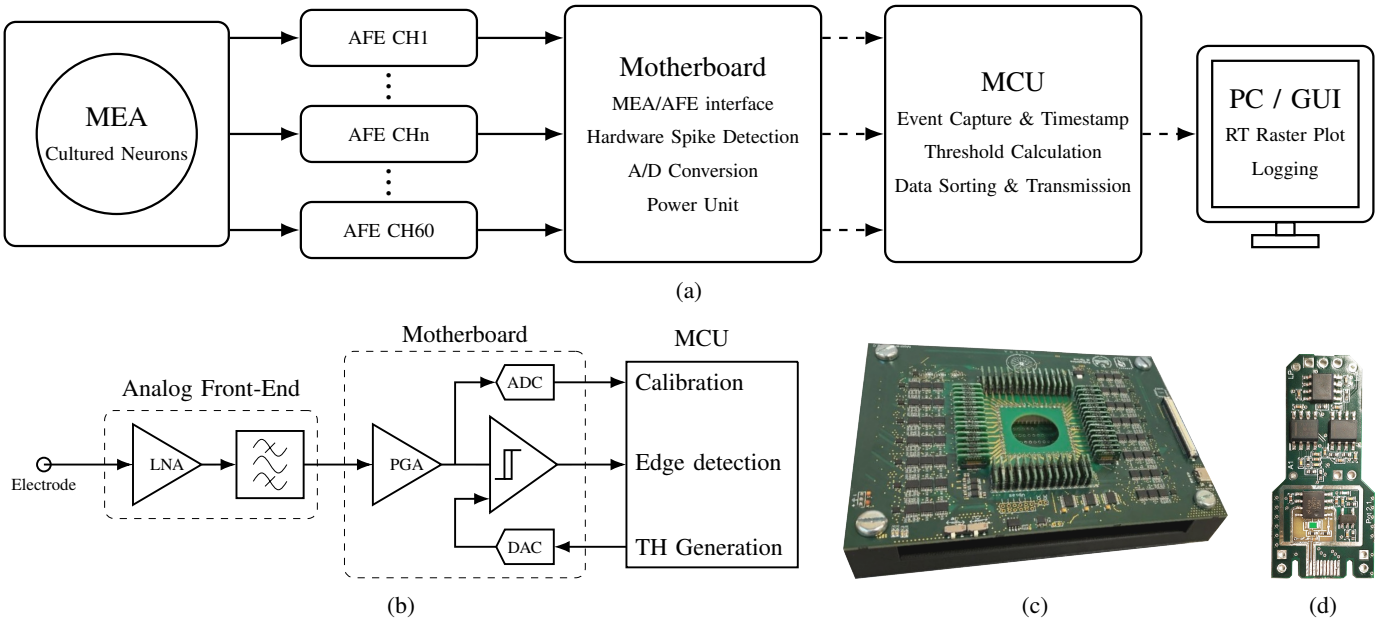


Fig. 1: System overview: (a) high-level multichannel architecture; (b) simplified single-channel path from electrode to MCU; (c) photo of a single analog front-end (AFE) PCB; (d) photo of the complete multichannel event-driven platform.

DAC channel, which sets the reference voltage for the corresponding Schmitt trigger. Calibration can be re-called at any time during acquisition by the user through the GUI.

2) Acquisition phase: After calibration, the host sends a start command to the MCU and the acquisition phase begins. Neural spikes, digitized by the Schmitt triggers, are delivered to the MCU as digital pulses. Each pulse is timestamped using the Input Capture functionality of the MCU hardware timers. All timers are synchronized to a common master reference, ensuring that timestamps across channels share the same time base. This provides precise temporal alignment of events with a resolution of $10\,\mu s$. To further suppress spurious detections, a refractory period of $2\,ms$ is enforced on each channel following a spike event [21]. This limits the maximum detectable rate to $500\,Hz$ per channel, preventing detections of true spikes within that window, but reduces susceptibility to ringing and false positives. The $2\,ms$ setting was found as a suitable trade-off based on typical instantaneous firing rates. Event storage and transfer are managed with a dual-buffer (ping–pong) architecture. The acquisition timeline is discretized into $1\,ms$ slots, where each slot is represented by a 16-bit (2-bytes) word encoding up to 15 channels (1 bit unused, Fig. 2b). A bit is set to 1 whenever a spike is detected on the corresponding channel; otherwise, it remains 0. Every $500\,ms$, the contents of the active buffer are copied to a secondary buffer for transmission, while logging continues in the primary buffer. Each 1000 bytes completed buffer is then assembled into a fixed-size packet, preceded by a 3-byte header (synchronization byte + 2-byte cycle counter), as shown in Fig. 2c. Packets are then streamed to the host PC over USB for real-time plotting and storing.

C. Graphical User Interface (GUI)

A custom MATLAB-based GUI provides implements the serial communication for real-time interaction. It features a scrolling raster plot updated every $50\,ms$ over a $1\,s$ window for real-time visualization of spiking activity (raster plot), with efficient binary bitmask decoding to display up to 60 channels at low computational cost. During acquisition, data are continuously logged for allowing further spatio-temporal analysis. The script also allows bidirectional communication for automatic (first calibration and acquisition phase) and interactive (set K value, trigger recalibration) control.

D. Additional Features and Cost Considerations

The firmware can be reconfigured to support conventional raw signal acquisition from all 60 channels, providing full waveform data when required. In addition, the motherboard is hardware-reconfigurable, enabling alternative electrochemical techniques such as amperometry and cyclic voltammetry (beyond the scope of this paper).

The complete 60-channel prototype was built for less than 3000 USD, corresponding to roughly 25 USD per AFE channel plus about 1500 USD for the motherboard and MCU. Costs would decrease further in scaled production. By comparison, commercial 60-channel MEA systems typically exceed 30,000 USD, highlighting the cost-effectiveness of the proposed platform.

III. Experimental Set-up and Validation Metrics

Although designed for up to 60 parallel neural channels, the platform was experimentally validated in a 15-channel setup using synthetic signals. This choice was motivated by upcoming *in vitro* experiments that will employ a custom

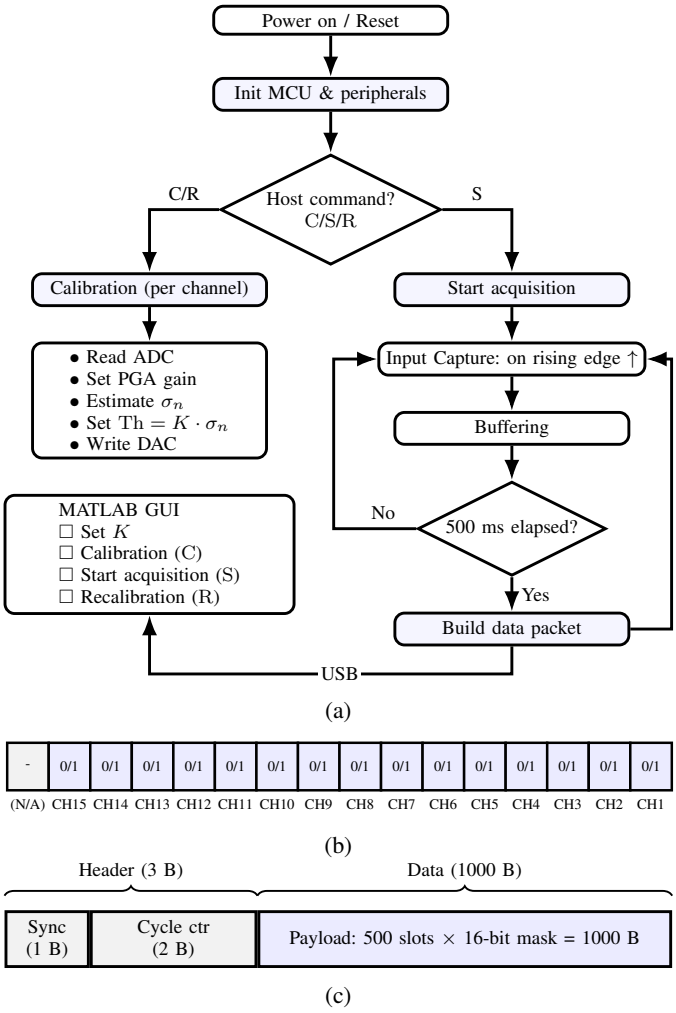


Fig. 2: (a) High-level firmware/host workflow. (b) Single 1 ms time slot: 16-bit mask covering 15 channels (one bit per channel; one bit unused). (c) USB Packet structure: a 3-byte header (1-byte sync, 2-byte cycle counter) precedes a 1000-byte payload of 500 time slots.

16-channel (15 channels + reference) MEA developed at the University of Turin by Picollo *et al.* [22]. Extending validation to the full 60-channel configuration is underway, but the 15-channel case provided a practical, controlled testbed for benchmarking core performance.

A. Test Setup

The input consisted of synthetic extracellular biphasic spikes generated in MATLAB, with morphologies resembling those typically observed in neuronal cultures. To emulate realistic conditions, additive Gaussian noise was superimposed, covering SNRs between 3 dB and 20 dB. An example waveform is shown in Fig. 3a. Signals were sent to the system through a digital-to-analog converter (DAC) at amplitudes already matched to the output range of the AFE, bypassing this stage to directly characterize the event-driven detection circuitry.

A custom PCB was used to split the synthetic signal into 15 parallel channels, enabling simultaneous spike activity across all inputs. This configuration was designed to stress the acquisition pipeline with the highest channel concurrency.

Spike trains were generated at varying firing rates (10 Hz to 500 Hz) with fixed inter-spike intervals. This provided reproducible conditions for benchmarking and allowed us to probe both physiological regimes (baseline activity at 10 Hz, bursting activity up to 300 Hz) and stress scenarios beyond typical biological rates (500 Hz).

B. Evaluation Metrics

System performance was assessed using standard metrics commonly adopted in neural signal processing:

- **Recall**: proportion of true spikes correctly detected among all ground-truth spikes [23]–[25].
- **Precision**: proportion of detected spikes that correspond to true events [26].
- **F1-score**: harmonic mean of precision and recall [25].
- **Jitter**: standard deviation of the time difference between detected and ground-truth spike times [21], [27]–[29].
- **Latency**: average delay between the spike onset and its detection [27]–[29].
- **Data-rate reduction**: decrease in transmitted data volume compared to conventional continuous acquisition.

Published studies provide quantitative guidelines for detection performance at sufficiently high SNR (above 10 dB): precision and recall above 90% with F1-scores typically exceeding 0.85 [24], [26]; false positives below 1 event/s/channel for *in vitro* electrophysiology [26]. Temporal accuracy within 1 ms is widely adopted for real-time MEA studies [27]–[29].

IV. Results

The system was characterized under more than 50 test conditions by sweeping SNR (3 dB to 20 dB) and firing rate (10 Hz to 500 Hz) with 15 simultaneous active channels. Validation metrics were extracted by comparing detected events against the known ground-truth spike timings of the input signals. An example of detections superimposed on the synthetic input is shown in Fig. 3b, while Fig. 3c illustrates a representative 15-channel raster plot recorded during acquisition. The key results are summarized below.

A. Spike Detection Performance

Spike detection accuracy was assessed in terms of precision, recall, and F1-score across the physiological firing-rate range (0–300 Hz) and multiple SNR levels, considering more than 500,000 input spikes per channel.

The system proved highly robust to false positives: with $K = 5$ and a 2 ms refractory period, spurious events were almost absent (<0.05 false positives/s/channel at the lowest SNR level). As a result, precision ≈ 1, and the F1-score can be expressed solely as a function of the accuracy:

$$F1 = \frac{2 \cdot \mathrm{Precision} \cdot \mathrm{Recall}}{\mathrm{Precision} + \mathrm{Recall}} \approx \frac{2 \cdot \mathrm{Recall}}{1 + \mathrm{Recall}}. \quad (2)$$

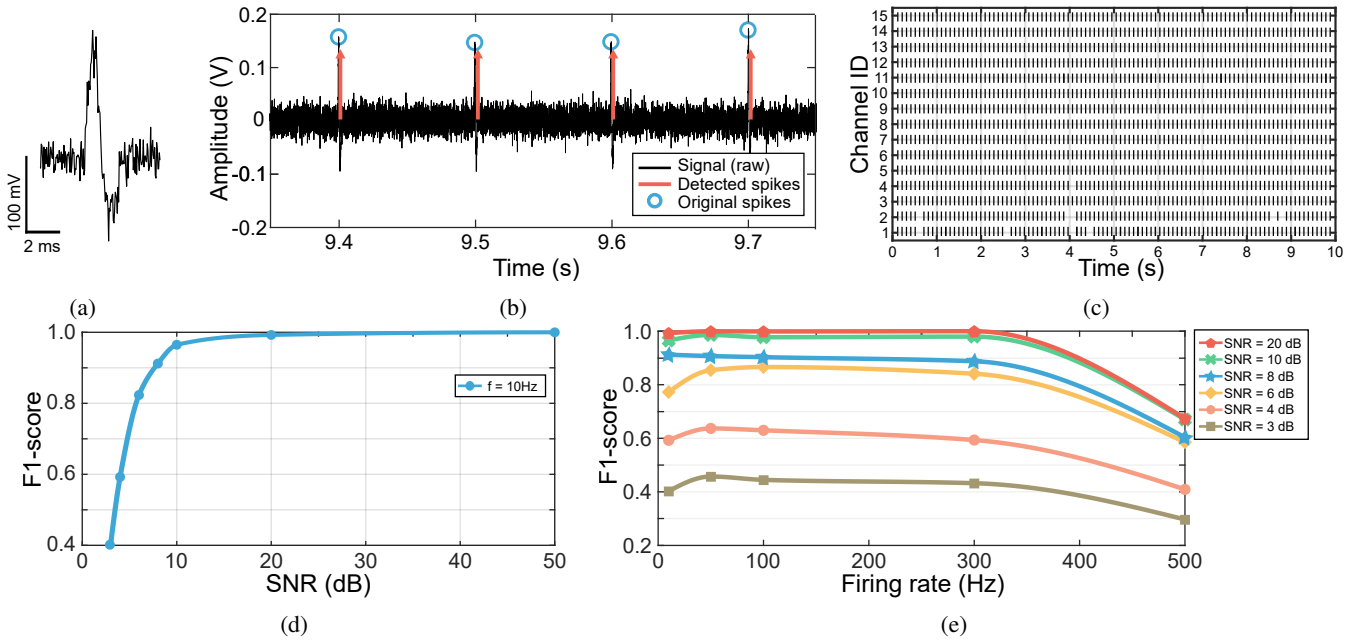


Fig. 3: (a) Synthetic single-spike waveform with added noise (SNR = 10 dB); (b) 400 ms segment of synthetic input (SNR = 10 dB, firing rate = 10 Hz, black) with ground-truth spikes (blue circles) and detected events (red arrows); (c) example raster plot of 15 channels during a 10 s acquisition; (d) F1-score as a function of SNR for a 10 Hz firing rate (averaged across 15 channels); (e) F1-score as a function of firing frequency for different SNRs (averaged across 15 channels).

The F1-score rises quickly with SNR: it reaches ∼80% at 5 dB, surpasses 90% from ∼8 dB, attains ∼98% at a moderate 10 dB, and exceeds 99% for high SNRs (>20 dB). Fig. 3d displays the F1-score as a function of the SNR, obtained at 10 Hz firing rate.

We also profiled performance vs. firing rate to probe frequency limits (Fig. 3e). Under physiological conditions (up to ∼300 Hz, e.g., during bursting), the F1-score remained stable. As expected, a consistent drop appears as rates approach 500 Hz, mainly caused by the chosen 2 ms refractory period.

These results were obtained using a conservative thresholding policy ($K = 5$) to suppress false positives. Adapting K dynamically to the input SNR could further improve recall at the cost of a modest increase in spurious detections.

Table I summarizes the system performance at 10 dB SNR against widely accepted literature benchmarks.

B. Temporal Accuracy

Because spikes are detected directly in hardware, without additional digital processing, the on-board temporal accuracy is determined only by the analog front-end response, the 10 µs resolution of the MCU input-capture timers, and interrupt handling time. As a result, the firmware achieves timing precision well below 1 ms, a capability that can support future on-MCU, time-accurate closed-loop protocols. Off-board, the temporal resolution is limited by the 1 ms binning used for transmission. At this level, jitter was quantified across all SNRs and firing rates within 0–300 Hz. At low frequencies (≤50 Hz), average jitter remained below 0.6 ms (0.59 ms at 50 Hz). A modest increase was observed at higher rates, reaching 0.68 ms at 300 Hz, still satisfying the 1 ms timing requirement commonly adopted in closed-loop MEA experiments.

TABLE I: Performance of the proposed system at 10 dB SNR compared to literature benchmarks (averaged up to 300 Hz).

Metric	This Work	Benchmark Target	Refs.
Recall	96%	>90%	[23]–[25]
Precision	≈100%	>90%	[26]
F1-score	0.98	>0.85	[25]
Jitter (std)	0.66 ms	<1 ms	[21], [27]–[29]

C. Data Efficiency

A key advantage of the event-driven architecture is its extremely low and fixed data-rate. Each 500 ms acquisition window is represented as a binary spike mask of 500 time slots, with one 16-bit word per slot. Including a 3-byte header, this yields a constant packet size of 1003 bytes, corresponding to an average throughput of ∼2.0 kB/s. For comparison, conventional raw acquisition at 10 kS/s across 15 channels produces about 225 kB/s (12-bit), i.e., a data reduction greater than 99%, without the need of additional digital processing. To scale to the full 60-channel configuration, each time slot will use four 16-bit words, maintaining the same percentage of data reduction since both raw and event-driven data volumes scale proportionally with channel count.

V. Conclusion and Future Work

We introduced a versatile, event-driven neural acquisition platform that detects spikes directly at the hardware level,

prioritizing spatio-temporal information over waveform capture. This system is not intended for applications where spike morphology is essential (e.g., electrophysiological research), but it is highly effective when spatio-temporal information is the primary variable of interest (e.g., network synchronization studies, burst detection, pharmacological assays, closed-loop neuromodulation, and long-term monitoring).

Despite evaluation under stress conditions (15 simultaneous channels at firing rates up to $300\,\mathrm{Hz}$, across a wide SNR range), the platform delivered high detection performance (F1-scores $\sim$0.98 at $10\,\mathrm{dB}$ SNR), sub-millisecond on-board temporal precision — with $1\,\mathrm{ms}$ off-board resolution — and $>$99% data-rate reduction vs. continuous sampling. These results were obtained under controlled conditions using synthetic signal inputs. In *in vitro* recordings, spike amplitude, morphology, and noise levels may vary significantly over time and across electrodes. The ability to perform per-channel recalibration is expected to mitigate these effects and help maintain robust detection performance during biological experiments.

Future work will focus on: (i) expanding the diversity of synthetic test conditions, including different spike waveforms, dynamic amplitude and noise variations; (ii) assessing the impact of different refractory-period windows and detection thresholds on performance; (iii) scaling the system to its full 60-channel capacity; (iv) conducting in vitro experiments to validate the complete acquisition chain, including the AFE; (v) exploring FPGA-based time-stamping to further reduce jitter and enable deterministic scheduling; (vi) integrating stimulation circuitry and on-board real-time closed-loop algorithms.

Overall, the platform combines accuracy, efficiency, and affordability in a single design, establishing a practical and scalable alternative for next-generation electrophysiology and closed-loop neuroscience experiments.

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