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31 October 2026

A Volume-Optimized Hybrid EMI Filter for Automotive Traction Inverters

Markeljan Fishta, and Franco Fiori, *Member, IEEE*

***Abstract*—Electromagnetic interference (EMI) filters play a crucial role in automotive inverters but can occupy a significant portion of the overall system volume, particularly in wide-bandgap (WBG) semiconductor-based designs, due to their higher power density compared to Silicon-based ones. To address this issue, this paper proposes the use of active capacitors as a replacement for passive ones, effectively reducing the required common-mode (CM) inductance. A detailed analysis of the active capacitor operation is presented, along with design equations to aid implementation. Based on this approach, a hybrid EMI filter is proposed. Experimental prototypes have been developed and tested to validate the concept. The results demonstrate that the hybrid EMI filter achieves comparable filtering performance to conventional passive designs while reducing the volume of magnetic components by 50%.**

***Index Terms*—Active electromagnetic interference (EMI) filter, Automotive, Common-mode (CM) interference, Conducted emissions, Hybrid EMI filter, Traction Inverter**

I. Introduction

EMI filters are necessary for the compliance of automotive traction inverters with conducted emissions regulations [1]. In recent years, efforts have been made to decrease the EMI filter volume by mitigating EMI at the source [2], [3], [4], [5]. However, the use of such techniques requires access to the converter under consideration during the design phase, which is not always possible. For this reason, the use of Active EMI Filters (AEFs) has quickly increased as an alternative to or in combination with Passive EMI Filters (PEFs). Indeed, AEFs allow to improve the attenuation performance compared to PEFs, as it has been demonstrated for DC/DC converters [6], [7], AC/DC converters [8], and inverters [9], [10]. An updated overview of AEFs has been published in [11]. In general, all AEFs base their operation on the sensing of a disturbance current/voltage and the injection of a suitable cancellation current/voltage, resulting in a lower residual disturbance level than the starting one. AEFs suffer from bandwidth limitation [11], hence a PEF is still needed to cover the entire regulated frequency range [1]. However, thanks to the attenuation provided by the AEF at low frequency, the required PEF can have a higher cutoff frequency. This, in turn, results in smaller components and reduced volume occupation. Based on the sensed and injected quantities, whether voltage or current, four filter topologies can be identified [11]. Concerning three-phase inverters, the Voltage Sensing Current Cancellation (VSCC) topology has become one of the most utilized, since it does not require a sensing or injection transformer. However, solutions employing Current Sensing Current Cancellation (CSCC) [12], [13] and Current Sensing Voltage Cancellation (CSVC) [14] have been demonstrated as well. Zhang et al. [15] proposed a transformerless AEF, inserted at the output of the motor drive system, which provides up to $15\,\mathrm{dB}$ attenuation up to $3\,\mathrm{MHz}$. However, the presented solution may not be suitable for high-voltage systems, as the sensing path is DC-coupled and could give rise to safety concerns. Moreover, the solution relies on the accurate modeling of the disturbance source impedance to generate the compensation current. However, the effectiveness of the proposed approach in cases where there is a mismatch between the target impedance and the artificially fitted one was not discussed. Han et al. [12] proposed a CSCC AEF placed at the input of a high-current inverter. However, the AEF was demonstrated with low inverter supply voltage and an additional magnetic component is required to perform current sensing at the input, increasing design complexity. Zhang et al. [16] proposed an AEF to be inserted in the grounding circuit of the motor drive system. The circuit operates by increasing the impedance of the parasitic path between the motor chassis and the system ground, hence decreasing the conducted CM current. While it is claimed that the motor frame voltage is kept low, such a solution can represent safety concerns in case of fault, leading to ungrounded motor. Takahashi [17] proposed a Hybrid EMI Filter (HEF) to be placed at the input of a SiC-based inverter operating at $200\,\mathrm{V}$ supply voltage. The

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The authors are with the Department of Electronics and Telecommunication, Politecnico di Torino, 10129 Torino, Italy (e-mail: markeljan.fishta@polito.it, franco.fiori@polito.it).

proposed filter provides up to $8.2\,\mathrm{dB}$ additional attenuation up to $1.4\,\mathrm{MHz}$, and it reduces the volume of one of the CM cores by $75\,\%$ with respect to the PEF. However, the employed load was $750\,\mathrm{W}$, indicating a rated input current of only a few ampere. Liu et al. [13] presented a CSCC AEF for CM reduction in three-phase inverters. The AEF can operate up to $20\,\mathrm{MHz}$ but it has the drawback of requiring an additional magnetic component, which must be fine tuned to achieve the required performance. Zhang and Bazzi [18] proposed a CSCC AEF, demonstrating up to $20\,\mathrm{dB}$ attenuation in an inverter application. The circuit was based on shunt current sensing, hence no DC isolation is present between the supply line and the amplifier, indicating that the filter is not suitable for HV applications. Zhang et al. [19] proposed an output AEF for three phase inverters. The circuit achieved up to $30\,\mathrm{dB}$ attenuation, which further increased to $70\,\mathrm{dB}$ when paired with an input AEF. The proposed output AEF requires an injection transformer to perform series voltage cancellation. This increases the design complexity as the filter performance depends on the symmetry of the transformer windings, as demonstrated by the authors. Besides the solutions based on analog signal elaboration, digital-based AEFs have been proposed as well [14], [20]. In these systems, the disturbance is digitally elaborated and complex cancellation signal waveforms can be synthesized, achieving good EMI suppression capability. However, such solutions require costly FPGA boards, which increase the overall cost of the EMI filter.

The present work proposes the use of capacitance multiplier circuits to reduce the volume of EMI filters, by replacing the passive filter capacitors. The target application is that of high input current inverters, where rigid conductive bars are used, as in recently published PEFs [21], [22], [23], [24]. The paper provides a detailed analysis of the active circuit performance, as well as design formulas. Moreover, the main goal of the paper is to provide a quantitative evaluation of the HEF benefit with respect to the traditional PEF, in terms of volume occupation reduction.

The paper is organized as follows: Sect. II lays the bases for the volume reduction estimation due to CM capacitance increase. Sect. III presents the analysis and design formulas for the proposed HEF. Experimental validation is given in Sect. IV, while the paper is concluded in Sect. V.

II. EMI Filter Volume Analysis

A single-phase equivalent circuit is employed to analyze the CM or DM conducted interference, as illustrated in Fig. 1(a). The disturbance is represented by the voltage

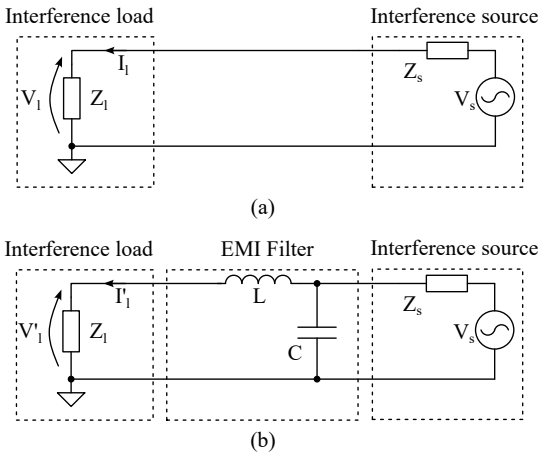


Fig. 1. Single-phase equivalent circuit (a) without and (b) with the EMI filter inserted.

source $V_\mathrm{s}(s)$ and its internal impedance $Z_\mathrm{s}(s)$, with s being the complex frequency. The disturbance load is represented by the impedance $Z_\mathrm{l}(s)$, which consists of the Line Impedance Stabilization Network (LISN) impedance [1]. The conducted emissions at the LISN, given by

$$V_\mathrm{l}(s) = \frac{Z_\mathrm{l}(s)}{Z_\mathrm{l}(s) + Z_\mathrm{s}(s)} V_\mathrm{s}(s) \tag{1}$$

should be kept below limits set by [1]. To achieve this, EMI filters can be inserted to modify the disturbance propagation paths. The minimum attenuation required from the filter, also known as Insertion Loss (IL), is given by

$$IL_{\mathrm{dB,min}}(\omega) = V_{\mathrm{l,dBuV}}(\omega) - L(\omega) + M, \tag{2}$$

where $V_{\mathrm{l,dBuV}}(\omega)$ is the magnitude of the voltage spectrum across the disturbance load, in $\mathrm{dB\,\mu V}$, $L(\omega)$, in $\mathrm{dB\,\mu V}$, is the limit posed by regulations, M, in dB, is a design margin, and ω is the angular frequency. For the sake of simplicity a single-stage CL filter is considered here, as shown in Fig. 1(b). The IL of the filter is defined as

$$IL(s) = \frac{V_\mathrm{l}(s)}{V_\mathrm{l}'(s)} \tag{3}$$

and, for a generic filter described by its chain matrix, it is given by [23]

$$IL(s) = \frac{AZ_\mathrm{l}(s) + B + CZ_\mathrm{s}(s)Z_\mathrm{l}(s) + DZ_\mathrm{s}(s)}{Z_\mathrm{s}(s) + Z_\mathrm{l}(s)}. \tag{4}$$

The magnitude of the IL provided by the filter must be larger than that of the required one over the entire frequency band of interest, i.e. $|IL(\omega)| \geq |IL_{\min}(\omega)|$. Assuming that an EMI filter compliant with such criterion has been designed, one would like to assess the volume reduction following a certain increase in the

TABLE I
INVERTER PARAMETERS

Parameter	Value	Unit
E	350	V
f_{sw}	32	kHz
$C_{\mathrm{s,cm}}$	10	nF
$C_{\mathrm{s,dm}}$	100	µF

capacitance value. Considering the single-stage filter of Fig. 1(b), the IL results

$$IL(s) = \frac{Z_{\mathrm{s}}}{Z_{\mathrm{s}} + Z_{\mathrm{l}}} \left(1 + \frac{Z_{\mathrm{l}}}{Z_{\mathrm{s}}} + s\left(\frac{L}{Z_{\mathrm{s}}} + CZ_{\mathrm{l}}\right) + s^2 LC\right). \tag{5}$$

The load impedance, determined by the LISNs, is considered as resistive ($Z_{\mathrm{l}} = R_{\mathrm{l}}$), while the source impedance as capacitive ($Z_{\mathrm{s}} = 1/(sC_{\mathrm{s}})$). For CM, $R_{\mathrm{l,cm}} = 25\,\Omega$ while $C_{\mathrm{s,cm}}$ models the overall capacitance of the inverter towards the chassis. For DM, $R_{\mathrm{l,dm}} = 100\,\Omega$ and $C_{\mathrm{s,dm}}$ represents the DC link capacitance. Under these assumptions, the IL is given by

$$IL(s) = \frac{1 + sR_{\mathrm{l}}(C + C_{\mathrm{s}}) + s^2 L(C + C_{\mathrm{s}})}{1 + sR_{\mathrm{l}}C_{\mathrm{s}}}. \tag{6}$$

Considering inductance L as the independent variable, the IL magnitude can be expressed as

$$|IL(\omega)|^2 = \frac{aL^2 + bL + c}{1 + \omega^2 R_{\mathrm{l}}^2 C_{\mathrm{s}}^2} \tag{7}$$

with

$$a = \omega^4 (C + C_{\mathrm{s}})^2 \tag{8}$$

$$b = -2\omega^2 (C + C_{\mathrm{s}}) \tag{9}$$

$$c = 1 + \omega^2 R_{\mathrm{l}}^2 (C + C_{\mathrm{s}})^2 \tag{10}$$

Recalling that it must be

$$|IL(\omega)|^2 \geq |IL_{\min}(\omega)|^2 \tag{11}$$

the inequality for L yields

$$L \geq \frac{1 \pm \sqrt{|IL_{\min}(\omega)|^2 \left(1 + \omega^2 R_{\mathrm{l}}^2 C_{\mathrm{s}}^2\right) - \omega^2 R_{\mathrm{l}}^2 C'^2}}{\omega^2 C'} \tag{12}$$

where $C' = C + C_{\mathrm{s}}$ has been used. Such an expression was evaluated for a disturbance source modeled as a trapezoidal voltage with amplitude E and frequency f_{sw}, as in Table I. The emission limit was incremented by a safety margin $M = 6\,\mathrm{dB}$. The evaluation result is plotted in Fig. 2. The plot reveals how the value of the required CM inductance varies in relation with the value of the CM capacitance. As C is increased, the discriminant becomes negative for all ω values, which corresponds to the case in which no inductor is required, since the capacitor alone provides sufficient IL. Volumetric models of inductors have been proposed in [25], suggesting linear dependence of the choke volume on the inductance values, as

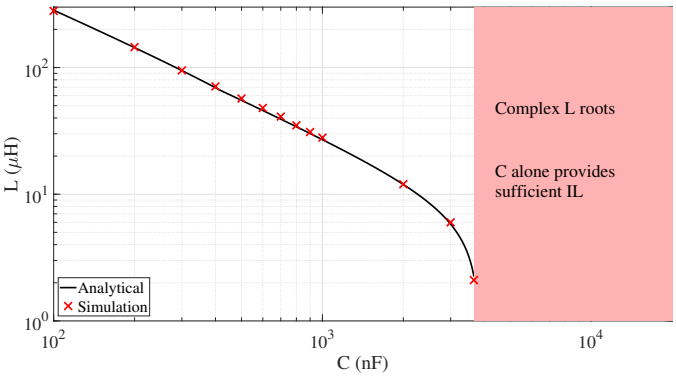


Fig. 2. Minimal required filter inductance as the capacitance is swept.

$$U_{\mathrm{L}} = \alpha L + \beta \tag{13}$$

where α and β are model parameters. It results that the volume of the chokes, which are the most bulky components, can be decreased by increasing the filter capacitance. However, due to safety constraints [26] on the maximum value of total CM capacitance, an active circuit, that mimics a large capacitor can be employed to decrease the value of the CM inductors and, consequently, the overall volume. On the other hand, no similar constraints exist for the DM capacitance, which can be increased sufficiently to minimize the DM inductor volume.

III. PROPOSED EMI FILTER

This section presents the proposed EMI filter design. The initial step is the PEF, which is used as a reference design. Then, to decrease the volume occupation of CM chokes, the active capacitor circuit design is presented, finally resulting in the proposed HEF.

A. Reference PEF

The design of the EMI filter starts with the evaluation of the required IL in the bandwidth of interest. In the present case, the System Under Test (SUT) is an inverter with the parameters given in Table I. The considered load impedance was that of the LISNs [1]. The CM and DM conducted emissions were obtained by simulation and the required IL was obtained as per (2), referring to [1]. The resulting passive EMI filter employs a two-stage CL topology for CM, and a single-stage LC topology for DM, as shown in Fig. 3, with the component values given in Table II. Nanocrystalline material was considered for the CM chokes to achieve high inductance per unit

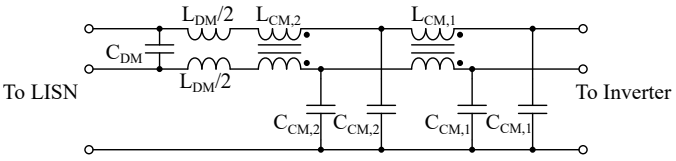


Fig. 3. Reference PEF.

TABLE II
REFERENCE FILTER COMPONENT VALUES

Param.	Value	Unit
C_{CM1}	100	nF
C_{CM2}	100	nF
L_{CM1}	75	µH
L_{CM2}	75	µH
C_{DM}	6.6	µF
L_{DM}	280	nH

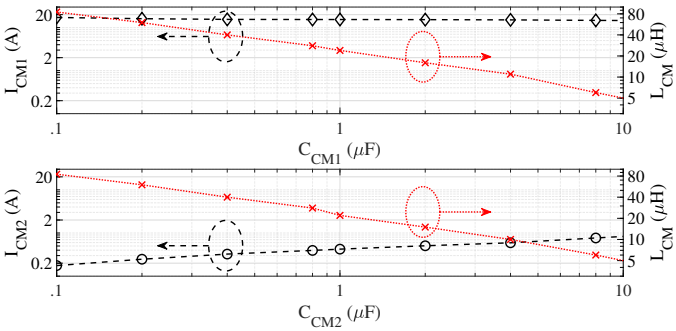


Fig. 4. Time-domain simulation results when (top) sweeping the value of C_{CM1} and (bottom) that of C_{CM2}. On the left y axis, the RMS current flowing through the capacitor whose value is being swept is shown. On the right y axis, the optimal value of the CM inductance, employed for both CM chokes, is represented.

volume, while ferrite material was considered for the DM inductor, due to the small required inductance. The complex permeability behavior of the magnetic materials was modeled [27] and included in the PEF design procedure.

To decrease the required CM inductance active capacitors can be employed in place of passive ones. With the aid of computer simulations, the feasibility of increasing the value of CM capacitors was evaluated. To this purpose, time-domain simulations employing the parameters in Table I were carried out. Considering one filter stage at a time, the value of the CM capacitors was swept, and the current stress of the capacitors was monitored. The results of such analysis are given in Fig. 4. For every CM capacitor variation, the required CM inductance to satisfy the minimum IL was recomputed, assuming equal inductance among the two CM chokes, $L_{\mathrm{CM1}} = L_{\mathrm{CM2}} = L_{\mathrm{CM}}$. In the top plot, the second stage CM capacitors were kept at their default value,

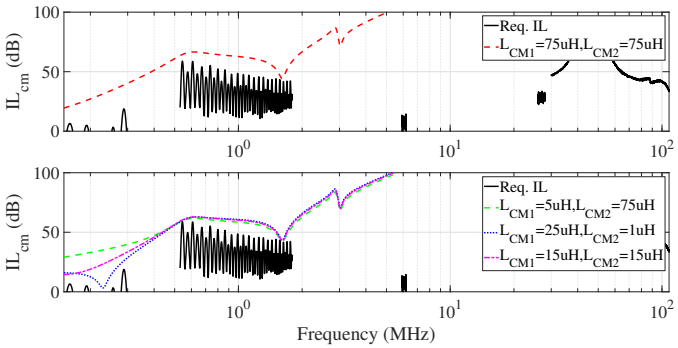


Fig. 5. (Top) IL design for two-stage CL filter, assuming $C_{\mathrm{CM1}} = C_{\mathrm{CM2}} = 100\,\mathrm{nF}$ and (bottom) assuming $C_{\mathrm{CM1}} = 100\,\mathrm{nF}$ and $C_{\mathrm{CM2}} = 1\,\mu\mathrm{F}$.

i.e. $C_{\mathrm{CM2}} = 100\,\mathrm{nF}$, and the C_{CM1} value was changed. Sweeping the capacitance value from $C_{\mathrm{CM1}} = 100\,\mathrm{nF}$ to $C_{\mathrm{CM1}} = 10\,\mu\mathrm{F}$ resulted in inductance decrease from $L_{\mathrm{CM}} = 75\,\mu\mathrm{H}$ to $L_{\mathrm{CM}} = 5\,\mu\mathrm{H}$. However, the RMS current stress over C_{CM1} is roughly independent of its value. More importantly, the resulting current stress is relatively high, impairing the replacement of the passive capacitor with an active one. On the contrary, as seen in the bottom plot, where the first stage CM capacitors were kept at their default value, the current stress over C_{CM2} is much lower, while the inductance decrease is almost identical to the previous case. For this reason, it is convenient to implement the capacitance amplification solution at the second filtering stage. The current stress over C_{CM2} results roughly proportional to its value, hence a trade-off between inductance reduction and current stress must be found. In the present work, it was selected $C_{\mathrm{CM2}} = 1\,\mu\mathrm{F}$, which results in a modest increase of the current stress, and a reduction of the required inductance by a factor of 3. Having set the desired capacitance values, the non-equal allocation of the inductance among the two stages was explored, to evaluate further decrease of the choke volume. The optimal IL for the reference case is shown in Fig. 5(top) while that obtained for larger C_{CM2} and different combinations of the CM inductors is shown in Fig. 5(bottom). The dash-dotted curve represents the case in which with $L_{\mathrm{CM1}} = L_{\mathrm{CM2}} = 15\,\mu\mathrm{H}$. In the dashed curve scenario, the L_{CM2} value was increased up to $75\,\mu\mathrm{H}$, while the L_{CM1} value was decreased as much as possible, until the IL was the optimal one. In the dotted curve case, the L_{CM2} value was reduced to a minimum, and that of L_{CM1} was tuned until the IL was the optimal one. The various scenarios result in different placement of zeros and poles in the filter transfer function, but the total required inductance is largely reduced in all cases, compared to the PEF. The design was carried out for the case $L_{\mathrm{CM1}} = 25\,\mu\mathrm{H}$, $L_{\mathrm{CM2}} = 1\,\mu\mathrm{H}$, which allows for

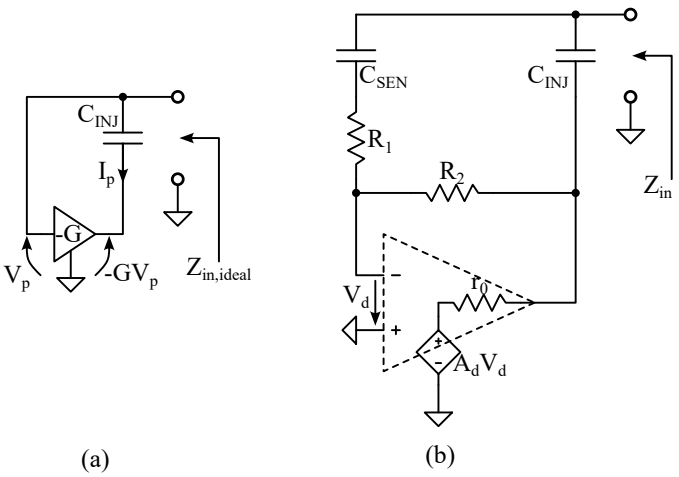


Fig. 6. (a) Working principle of capacitance multiplier and (b) detailed circuit schematic for evaluation of the equivalent impedance.

the removal of the second core altogether, resulting in the largest volume reduction. Indeed, since the required inductance at the second stage is so small, it can be achieved as the CM contribution of the DM choke [28].

B. Active capacitor operating principle and design formulas

Capacitance multiplier circuits can be used to obtain an equivalent capacitance that is larger than that of the passive component used in the circuit. The working principle of such a circuit is illustrated in Fig. 6(a). An amplifier with voltage gain $-G$ is used to sense the voltage at one end of the capacitor C_{INJ} and drive the other end of the capacitor. The input impedance of such a configuration results

$$Z_{\mathrm{in,ideal}} = \frac{V_{\mathrm{p}}}{I_{\mathrm{p}}} = \frac{1}{sC_{\mathrm{INJ}}(1+G)}, \tag{14}$$

which shows that, seen from the input port, the capacitor is boosted by a factor $(1+G)$. Considering a more realistic scenario, the schematic of Fig. 6(b) is presented. The circuit implementation makes use of an amplifier in inverting configuration, with open-loop gain $A_{\mathrm{d}}(s)$ and equivalent output resistance r_0. The input impedance of the amplifier is considered infinite and a capacitor C_{SEN} is added to decouple the input signal at DC. According to the Rosenstark's formula [29], the input impedance can be written as

$$Z_{\mathrm{in}} = Z_{\infty}\frac{T_{\mathrm{OC}}}{1+T_{\mathrm{OC}}} + Z_0\frac{1}{1+T_{\mathrm{OC}}} \tag{15}$$

where Z_{∞} is the input impedance when the gain of the amplifier goes to infinity, $T_{\mathrm{OC}}(s)$ is the return ratio with the impedance calculation port open and Z_0 is the input impedance when the gain of the amplifier goes to zero [30]. Such an impedance corresponds to the desired one for frequencies higher than

$$f_{\mathrm{z}} = \frac{1}{2\pi R_1 C_{\mathrm{SEN}}}, \tag{16}$$

which represents the cutoff frequency of the sensing branch. Hence, R_1 and C_{SEN} should be designed so that the cutoff frequency is compatible with the regulated frequency range. Above the cutoff frequency,

$$Z_{\mathrm{in}} \approx R_1 \parallel \frac{1}{sC_{\mathrm{INJ}}\left(1+\frac{R_2}{R_1}\right)}, \tag{17}$$

from which the gain factor can be derived as

$$G = \frac{R_2}{R_1}. \tag{18}$$

So, R_1 and R_2 must be chosen to achieve the desired amplification. Furthermore, the sensing capacitance does not contribute to the equivalent impedance, but it contributes to the total capacitance, from a safety standpoint. Hence, the sensing capacitance should be designed as small as possible. Concerning the amplifier, an output stage with unity voltage gain can be included to boost the output current capability [12], [13], [15], [16], [17]. The open-loop gain then can be modeled as a two-pole response, written as

$$A_{\mathrm{d}} = \frac{A_{\mathrm{d0}}}{\left(1+\frac{s}{2\pi f_{\mathrm{P1}}}\right)\left(1+\frac{s}{2\pi f_{\mathrm{P2}}}\right)} \tag{19}$$

where A_{d0} is the DC gain, f_{P1} is the dominant pole frequency due to the main amplifier and f_{P2} is the pole frequency due to the output stage. In order for the output stage to not limit the bandwidth of the amplifier, it is assumed $f_{\mathrm{P2}} \gg f_{\mathrm{U}}$, with $f_{\mathrm{U}} = A_{\mathrm{d0}} f_{\mathrm{P1}}$ being the unity-gain frequency of the main amplifier. The self-resonant frequency of the equivalent impedance is given by [30]

$$f_{\mathrm{SR}} = \sqrt{\frac{f_{\mathrm{U}}}{2\pi r_0 C_{\mathrm{INJ}}(1+G)}}, \tag{20}$$

resulting in an equivalent series inductance of

$$ESL = \frac{r_0}{2\pi f_{\mathrm{U}}}. \tag{21}$$

The equivalent impedance is shown in Fig. 7 for $f_{\mathrm{U}} = 50\,\mathrm{MHz}$, $r_0 = 5\,\Omega$, $R_1 = 3\,\mathrm{k}\Omega$, $R_2 = 27\,\mathrm{k}\Omega$, $C_{\mathrm{SEN}} = 1\,\mathrm{nF}$, $C_{\mathrm{INJ}} = 100\,\mathrm{nF}$. At low frequency, the equivalent impedance equals that of C_{INJ}, since the frequency is below the cutoff of the sensing network. At higher frequencies the sensing capacitor shows sufficiently low impedance, hence the circuit exhibits the desired impedance, meaning that of $C_{\mathrm{INJ}}(1+G)$. As the frequency increases, the loop gain magnitude decreases and the impedance approaches r_0.

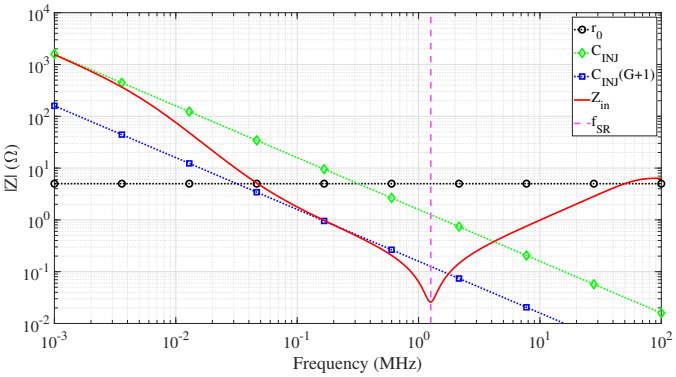


Fig. 7. Equivalent impedance calculation. At low frequencies the impedance is that of C_{INJ}, at middle frequencies that of $(1+G)C_{\text{INJ}}$ and at high frequencies approaches r_0.

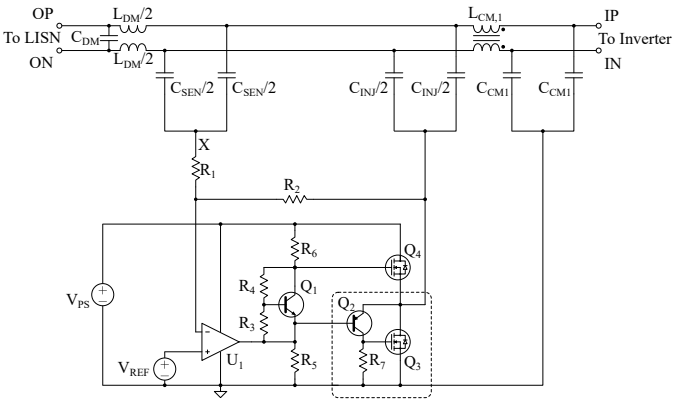


Fig. 8. Proposed HEF schematic.

C. Hybrid EMI filter

The complete schematic of the HEF is shown in Fig. 8. It is based on the PEF topology, where the second-stage CM capacitors have been replaced by the active circuit, and the second CM choke has been removed, while the DM filter remains unchanged. Moreover, the capacitive insulation barrier between the HV lines and the chassis is maintained, hence the filter is suitable for HV applications as long as Y-rated capacitors are used for C_{CM1}, C_{INJ} and C_{SEN}. To increase C_{CM2} from 100 nF to 1 µF, an overall amplification factor of 10 is needed, resulting in $G = 9$. Moreover, the cutoff frequency of the sensing network should be significantly lower than the lower limit of the regulated frequency band [1], so it was chosen $f_{\text{z}} = 33\,\text{kHz}$. These requirements can be achieved by setting $C_{\text{SEN}} = 2\,\text{nF}$, $R_1 = 2.4\,\text{k}\Omega$, and $R_2 = 22\,\text{k}\Omega$. The amplifier parameters f_{U} and r_0 should be designed so that the desired self-resonant frequency is achieved for the active capacitor, as per (20). This requires setting the transconductance of the output devices as

$$g_{\text{m}} \simeq \frac{1}{r_0}, \tag{22}$$

TABLE III
CIRCUIT PARAMETERS

Param.	Value	Unit	Param.	Value	Unit
V_{PS}	20	V	C_{SEN}	2	nF
C_{INJ}	200	nF	R_1	2.4	kΩ
R_2	22	kΩ	R_3	1.5	kΩ
R_4	3.3	kΩ	R_5	2.2	kΩ
R_6	2.2	kΩ	R_7	47	Ω
V_{REF}	10	V	$V_{\text{PS,max,U1}}$	40	V
$f_{\text{U,U1}}$	16	MHz	SR_{U1}	9	V/µs
$\lvert V_{\text{CEO,Q1,Q2}}\rvert$	65	V	$\lvert I_{\text{C,Q1,Q2}}\rvert$	100	mA
$V_{\text{DS,Q3,Q4}}$	40	V	$I_{\text{D,Q3,Q4}}$	4	A

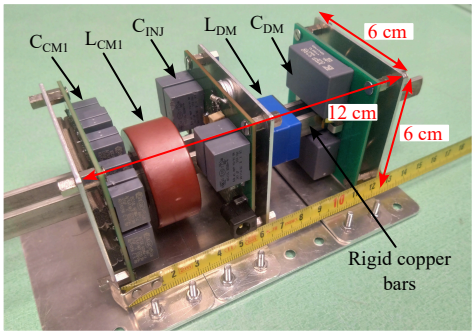


Fig. 9. Hybrid EMI filter prototype.

which determines the quiescent drain current as

$$I_{\text{D,Q}} = \frac{g_{\text{m}} V_{\text{OD,Q}}}{2} \tag{23}$$

with $V_{\text{OD,Q}}$ being the overdrive voltage at rest. It results that the quiescent power consumption is determined by the self-resonant frequency of the active capacitor. The design was carried out resulting in the component values in Table III.

IV. Experimental Results

Prototypes for the PEF and HEF were built for validation purposes. A picture of the prototype HEF, along with its dimensions, is shown in Fig. 9. Rigid copper bars with cross-section of $3\,\text{mm} \times 10\,\text{mm}$ were used, resulting in a rated current of $I = 150\,\text{A}$, for a maximum current density of $J = 5\,\text{A/mm}^2$. For both filters, CM inductors were implemented as single-turn chokes with nominal inductance $L_{\text{CM1}} = L_{\text{CM2}} = 85\,\mu\text{H}$, while the DM inductor was implemented by means of an E-shaped ferrite core with nominal inductance $L_{\text{DM}} = 300\,\text{nH}$. Filter capacitors were placed on dedicated PCBs. HEF differs from PEF since the active capacitor replaces the second stage passive capacitor, and the second CM choke is removed.

Measurements were first carried out on the active capacitor board. The equivalent CM input impedance

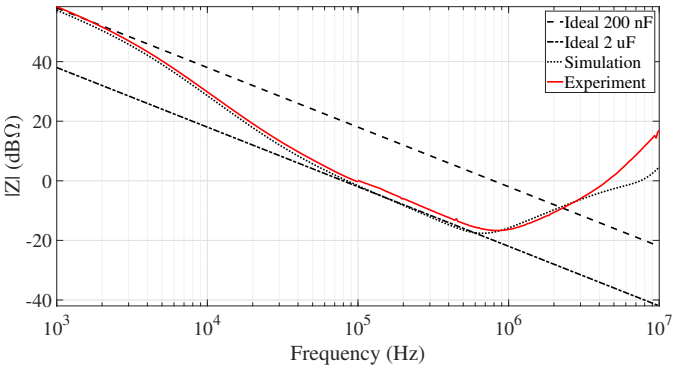


Fig. 10. Active capacitor circuit equivalent input impedance.

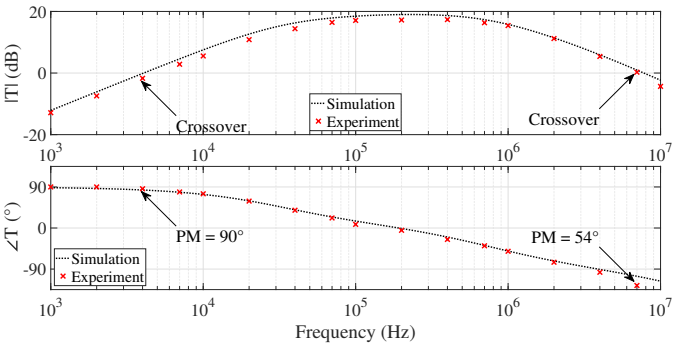


Fig. 11. Loop gain experimental measurement compared to simulation results.

was measured by means of a network analyzer, and the result is given in Fig. 10. The resulting impedance is close to the simulated one and the equivalent capacitor achieves $f_{\mathrm{SR}} \simeq 1\,\mathrm{MHz}$. The loop gain of the active capacitor was measured, by opening the loop at location "X" of the circuit in Fig. 8. The results are given in Fig. 11. The loop gain measurements were performed at a few frequency points, and the results show a good agreement with simulation. The first crossover frequency results at $4\,\mathrm{kHz}$ and it achieves $90°$ phase margin, while the second crossover results around $7\,\mathrm{MHz}$ and achieves $54°$ phase margin. Next, small-signal IL of the HEF was obtained from 4-port S parameter measurements. A schematic of the measurement setup is given in Fig. 12. The 4x4 scattering matrix of the filter is measured by means of a VNA. From these data, mixed-mode s-matrices

$$\mathbf{S}_{(\mathrm{cm/dm})} = \begin{bmatrix} s_{(\mathrm{cm/dm})11} & s_{(\mathrm{cm/dm})12} \\ s_{(\mathrm{cm/dm})21} & s_{(\mathrm{cm/dm})22} \end{bmatrix} \tag{24}$$

are evaluated [31]. The IL of the filter, for CM and DM,

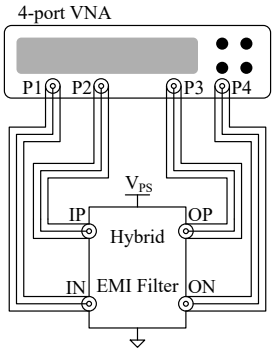


Fig. 12. 4-port S parameters measurement setup.

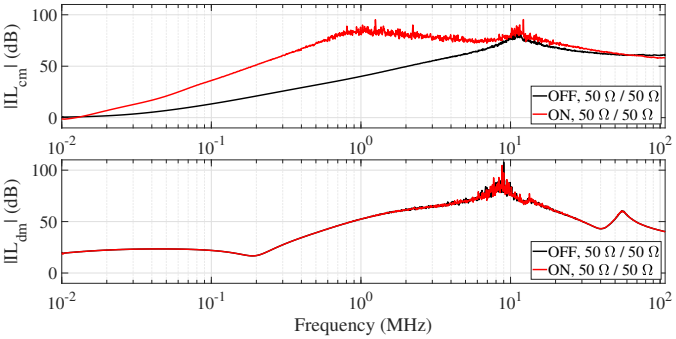


Fig. 13. Experimental IL for proposed HEF, CM and DM, with AEF OFF and ON.

can be written as

$$IL_{(\mathrm{cm/dm})} = 20\log\left|\frac{(1-\rho_{\mathrm{s(cm/dm)}}s_{\mathrm{cc11}})(1-\rho_{\mathrm{lcm}}s_{\mathrm{cc22}})}{(1-\rho_{\mathrm{scm}}\rho_{\mathrm{lcm}})s_{\mathrm{cc21}}} - \frac{\rho_{\mathrm{scm}}\rho_{\mathrm{lcm}}s_{\mathrm{cc12}}s_{\mathrm{cc21}}}{(1-\rho_{\mathrm{scm}}\rho_{\mathrm{lcm}})s_{\mathrm{cc21}}}\right| \tag{25}$$

where

$$\rho_{\mathrm{s(cm/dm)}} = \frac{Z_{\mathrm{s(cm/dm)}} - Z_0/2}{Z_{\mathrm{s(cm/dm)}} + Z_0/2} \tag{26}$$

$$\rho_{\mathrm{l(cm/dm)}} = \frac{Z_{\mathrm{l(cm/dm)}} - Z_0/2}{Z_{\mathrm{l(cm/dm)}} + Z_0/2} \tag{27}$$

with Z_0 being the port reference impedance, $Z_{\mathrm{s(cm/dm)}}$ being the source impedance and $Z_{\mathrm{l(cm/dm)}}$ being the load impedance. Results for a $50\,\Omega$ system are provided in Fig. 13, where it is shown that the AEF provides additional IL for CM while it does not affect the DM.

Measurements were performed with both filters, to assess their performance in the suppression of conducted EMI. A schematic of the measurement test bench is given in Fig. 14, while a picture can be seen in Fig. 15. The inverter was supplied with $E = 350\,\mathrm{V}$ and the measurement results are given in Fig. 16. The resulting emissions with both filters are compliant with class 4 limit from [1] up to $30\,\mathrm{MHz}$. The two filters achieve

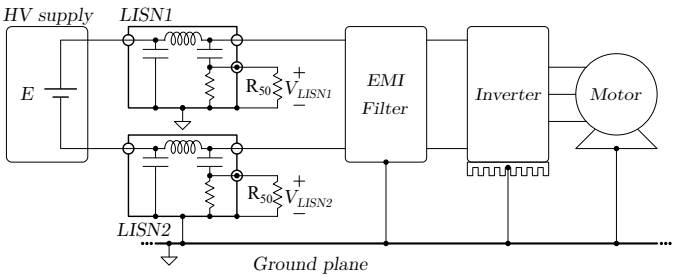


Fig. 14. Conducted emission measurement testbench schematic.

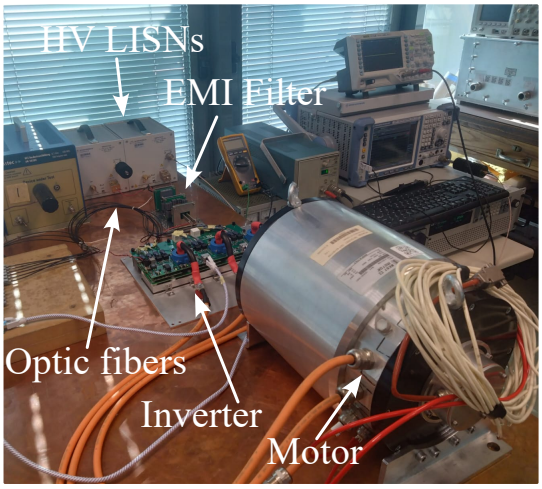


Fig. 15. Conducted emission measurement testbench picture.

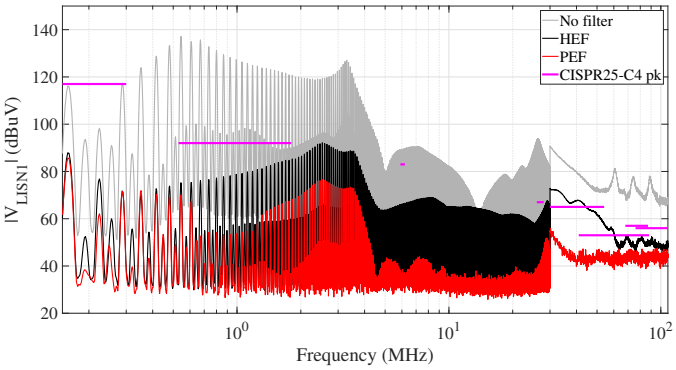


Fig. 16. Conducted emission measurement results with $E = 350\,\mathrm{V}$.

similar attenuation performance near the lower edge of the regulated band (150 kHz). However, as the frequency increases, the bandwidth limitation of the amplifier starts to kick in, and the attenuation of the HEF deviates from that of the reference PEF. The emissions in the frequency band above 30 MHz are not compliant, but such frequency range can be targeted by dedicated small components, without significantly impairing the volume reduction advantage enabled by the AEF, which results in a 47 % decrease of the magnetic components volume, from $57.2\,\mathrm{cm}^3$ to $30.2\,\mathrm{cm}^3$. Furthermore, the proposed HEF results in a lower overall cost by approximately 23 % with respect to the PEF. A comparative table of the proposed filters with recently published EMI filters for three phase inverters is given in Table IV. With respect to existing works on PEFs, the proposed PEF achieves the highest EMI attenuation at 200 kHz and 1 MHz. Concerning AEFs, the proposed filter shows the highest current rating and the highest EMI attenuation at 200 kHz. Finally, the proposed topology maintains the safety properties of the passive EMI filter thanks to the Y-rated capacitive barrier between the HV bus and ground.

V. Conclusions

This paper presented a CM HEF tailored for traction inverter applications, with a focus on reducing the filter volume. The proposed design is centered on a capacitance multiplier circuit, which replaces a portion of the CM capacitors used in a conventional PEF. Differently from existing solutions, the proposed HEF is suitable for high-current applications that utilize rigid conductive bars. Detailed design equations for the capacitance multiplier were derived, and a case study with an amplification factor of 10 and a bandwidth around 1 MHz was designed. A complete HEF prototype was built, including the proposed capacitance multiplication circuit. The proposed HEF maintains the safety-rated capacitive barrier of the PEF, making it suitable for use in HV systems. Conducted emission measurements confirmed the effectiveness of the HEF, achieving performance comparable to the reference PEF at low frequency, while reducing the CM magnetic components by 50 % and the overall cost by 23 %.

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TABLE IV
METHODS COMPARISON

	Inverter			Filter					
Reference	$E_{\mathrm{DC}}(\mathrm{V})$	$I_{\mathrm{DC}}(\mathrm{A})$	$f_{\mathrm{sw}}(\mathrm{kHz})$	Type	Location	IL@200 kHz (dB)	IL@1 MHz (dB)	Total chokes (cm^3/µH)	PCB footprint (cm × cm)
[21]	336	300**	10	Passive	Input	33	44	100/0.6	NA
[23]	336	300	NA	Passive	Input	47	50	NA/30	NA
[17]	200	3.75*	100	Passive	Input	32	63	8.62/782	7×5*
This work	**350**	**150**	**32**	**Passive**	**Input**	**55**	**73**	**57.2/171**	$\mathbf{6 \times 6}$
[15]	100	16*	10	Active	Output	33	31	11.9/220	7×6
[12]	48	130**	10	Active	Input	0	18	NA/2	5.4×3.9
[16]	150	16*	10	Active	Output	26	34	11.9/220	7.5×6
[17]	200	3.75*	100	Active	Input	32	63	3/413	7×5*
[13]	200	2.75*	10	Active	Input	34	36	NA	NA
[14]	400	37.5*	70	Active	Input	35	17	NA	NA
[18]	100	0.5*	10	Active	Input	11	7	0	5×3.5
[20]	48	5.2*	100	Active	Input	27	36	30/6.4	NA
[19]	306	NA	16	Active	Output	10	18	17.9/2810	6×3.8
[32]	100	5*	30	Active	Input	10	13	NA	NA
This work	**350**	**150**	**32**	**Active**	**Input**	**41**	**48**	**30.2/86**	$\mathbf{6 \times 6}$

*Derived from information presented in the paper. **Output RMS current. NA - Not available.

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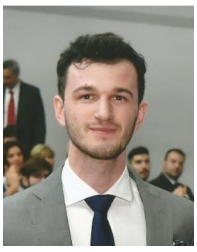
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Markeljan Fishta received the M.Sc. and the Ph.D. in electronic engineering from Politecnico di Torino, Torino, Italy in 2019 and 2023, respectively. He is currently a Research Assistant with the Department of Electronics and Telecommunication, Politecnico di Torino, Torino, Italy. His current research interests include electromagnetic compatibility of integrated circuits, analysis and mitigation of conducted EMI for power converters, and underwater acoustic communications.



Franco Fiori (Member, IEEE) received the Laurea and Ph.D. degrees in electronic engineering from the Politecnico di Torino, Turin, Italy, in 1993 and 1997, respectively. From 1997 to 1998, he was with STMicroelectronics, Italy, as an R&D team leader. In 1999, he joined as a Researcher the Polytechnic University of Turin. Currently, he is a Full Professor in electronics and Scientific Director of the Microelectronics EMC Laboratory in the same University. In his academic career, he has served as a Principal Investigator for several national and international research projects, mostly on the electromagnetic compatibility of integrated circuits. He has authored or coauthored more than 200 papers published in international journals and conference proceedings. His research interests include analog circuit design, power electronics, smart power devices, and electromagnetic compatibility.