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An Energy-Efficient Voltage-Doubler-Based DC–DC Stage for Current Source Inverter Operation

Roberto Giacomobono[1], Fabrizio Marignetti[2], *Senior Member, IEEE*, Francesco Iannuzzo[3], *Senior Member, IEEE*, Ariya Sangwongwanich[4], *Senior Member, IEEE*

***Abstract*—This paper proposes the usage of a combined full-bridge voltage doubler DC/DC stage as a way to supply a Current Source Inverter from a low-voltage photovoltaic source. The proposed solution avoids the usage of traditional step-up stages and positively impacts both efficiency and system complexity. The topology uses a full bridge for the generation of the AC voltage that goes to the input of the doubler. This enables high-frequency AC that reduces the size of the capacitors in the doubler. The paper also presents a possible technological solution to allow bidirectional power flow by bypassing the voltage doubler. An analytical discussion is presented alongside simulations and experimental validation, showing a 97.5% peak experimental efficiency.**

***Index Terms*—Current source inverter, CSI, Photovoltaics, Fuel-Cells**

I. Introduction

The applications of DC to AC conversion are a broad subject that can range from very small domestic installations to fully fledged power plants. These different environments require a host of different solutions that are catered towards the different needs that arise from these different applications. One peculiar need that usually arises from lower power installation is the necessity of stepping up voltage to a level that is usable to feed into the grid. When faced with the question of what can be the most effective topology of inverter to employ in a given setting, the first solutions derived from the literature are usually related to some form of Voltage Source Inverter (VSI) [1] [2]. This is due to the simplicity of the topology and the low cost of the DC link. Capacitors tend to have lower costs compared to inductors that can store the same amount of energy. Capacitors also don't require a design effort since they don't have to be tailored to the application and can be bought off the shelf. This solution, unfortunately, has step-down behavior, so it has to be combined with a high gain DC-DC stage to compensate for this behavior. Another major drawback of this kind of topology is the inability to draw a steady current from the DC side, and also the lifetime of the capacitors used in the DC-link is a key contributor to reduced system reliability. VSIs also require substantial LC or LCL filters at the output to comply with power quality standards [3], and especially if considering a full bridge solution, the output filter inductor can become large [4]. Current Source inverters (CSI), on the other hand, have an inherent boost capability and can be coupled to a DC-DC stage with lower gain. It can also draw steadier currents from PV sources, improving PV panels' lifetime [5] and the predictability in current injection that characterizes the CSI also impacts their capability of working with higher power factor [6] and with reduced filtering. The most common PWM strategies are SVM and SPWM. Having boost capabilities means that the CSI can also be employed as a Microinverter, used on smaller strings of PV to achieve increased flexibility. This translates into an installation that can better contrast the effects of both partial shading and non-uniform panel performance due to other effects such as soiling, thanks to the use of Distributed maximum power point tracking. [7] [8] [9] [10]

CSIs are a valid option for both grid connection and other applications, such as fuel cells. In fact, they can guarantee better power quality [11] and are also interesting due to their inherent protection against short circuit failure. This paper focuses on a specific but not uncommon situation in which power has to be supplied to the grid from a source whose operating voltage is significantly lower than the peak voltage of the grid. In this situation, if a VSI inverter was employed, it would be necessary to step up the voltage to a value at least equal to said peak voltage. A CSI is advantageous since it requires a voltage before the DC-link inductor high enough to enable the current steady state but lower than peak grid voltage, thanks to the inherent boost capabilities of this topology. In both cases, though, when dealing with a very low voltage source, multi-stage step-up inverter topologies are usually employed [12]. The boost topologies employed can be both isolated or non-isolated [13] [14]. From the isolated standpoint, flyback topologies are a popular solution [15] [16]. Since converter level isolation is not necessarily required and employing transformerless topologies leads to cost reduction, two very popular choices for the boost stage are the canonical boost converter, maybe with some variations such as a double cell [17]and the buck-boost [18] [19] [20]. Both solutions pose an issue in CSI implementations, which is the necessity of employing two custom-sized inductors in the topology, one in the boost stage and an additional one for the DC link. This poses a probably avoidable layer of complexity both in terms of sizing and materials to be employed. It is unlikely that the two inductors needed will use the same gauge and type of Litz wire (essential for this kind of application), and the cores used to wind them will likely be different, resulting in an uncompetitive and inefficient solution. This paper proposes a DC-DC stage that is specifically designed to minimize the DC-link inductor size of any major topology of CSI. The

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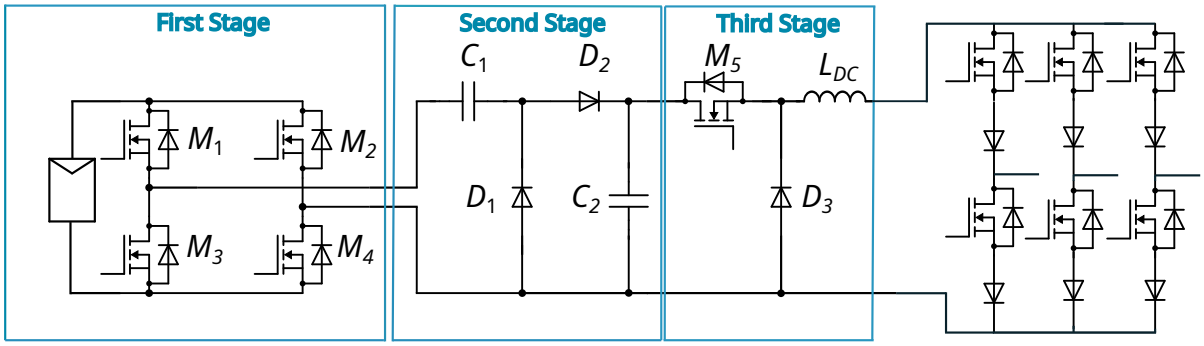


Fig. 1: Proposed Topology for the DC-DC pre-regulating stage

solution proposed is agnostic with regard to the kind of CSI that would be employed. The CSI could be both grid connected or load connected. The proposed solution is a capacitor-based DC-DC boost stage, which can be assembled with off-the-shelf parts, providing an efficient, easier-to-size solution. The solution presented can also be flexibly adapted to shifts in the supply chain since it uses only electronic switches, diodes and capacitors, which can be more easily replaced when changing suppliers. The topology proposed is most suitable for CSI applications as the number of components needed increases with the need of higher gain, and therefore it is most suited as a pre-regulator for a boost topology like the CSI. In this instance, the overlap time will be managed to create the rest of the boost capability. Since the amount of boost that the CSI provides is related to the overlap time, this will have to be determined in relation to the input voltage. This paper is divided into four sections and a summary of the conclusions. In section II, the topology is presented, and its main inner workings are explained and modeled; some brief considerations about what modulation is to be adopted are also introduced here. Section III presents some considerations about the sizing of the voltage doubler capacitors, which are one of the main components and certainly the most multifaceted in terms of the approaches that can be adopted to size them. Section IV is dedicated to the frequency behavior of the proposed converter, with much of the focus on input voltage ripple mitigation. Section V describes the experimental setup employed, showcasing the experimental results obtained.

II. Proposed DC-DC stage

Switched capacitor solutions are by far the most efficient boosting circuit in the literature [21], and they have already have been employed in literature to create boost inverter topologies [22] [23]. They rarely get employed in PV applications due to the fact that their peak efficiency is expressed only at integer values of voltage gain. This makes them less flexible and difficult to employ as a single-stage boost solution. This characteristic is not a problematic feature in a CSI multi-stage application, since the switched capacitor stage can be used as a pre-boost. The fine tuning of voltage and current regulation is subsequently carried over by the second stage. A CSI is the optimal topology of inverter to apply this solution. Since the CSI is a boost topology, the pre-boost will have to be sized to withstand voltages that are lower than grid voltage. Also, the size of the DC link inductor is proportional to the maximum difference in voltage between the two terminals, so the smaller the voltage boost that has to be performed by the CSI, the smaller the inductor. This relationship arises from the fact that the operating principle of the inductor in a CSI is analogous to that of a boost converter. Consequently, the sizing of the inductor follows the same dependency on voltage gain, as described in Eq. (2.16) of [24], and more explicitly in Eq. (5) of [25]. Having a smaller inductor will dramatically lower the equivalent series resistance in the DC-link, which is a major contributor to the losses. In a VSI on the other hand, the pre-boost would have to boost to a voltage that is higher than peak grid voltage, since the VSI steps down the input voltage. This means that the pre-boost would have to be sized to withstand higher voltages and the VSI would have to be sized as a normal VSI, with no cost reduction effect. The DC-link capacitor bank in a VSI is also usually bigger in value and has to serve the purpose of guaranteeing the desired voltage ripple at the DC link. To perform this task, it has to be able to hold the necessary charge at a voltage that is higher than grid voltage. In the CSI implementation, the energy storage is split between the output capacitor of the voltage doubler and the DC link inductor. This results in a smaller capacitor, especially because it will have a smaller voltage rating. The proposed DC-DC stage uses a Cockcroft-Walton voltage multiplier, employed to step up the voltage by integer values. This topology was originally introduced to achieve very high voltage, traditionally with low current and it has been employed even recently with great success with regards to efficiency [26] [27] [28]. In the configuration shown in this paper, the voltage is stepped up by a factor of two, but any multiplication factor n can be achieved theoretically. The proposed topology is shown in Fig. 1. The solution proposed uses a full bridge to create a high-frequency AC waveform, ideally square wave like, but that can also have injected ripple-noise as will be shown in section IV. The high frequency AC gets fed to the voltage doubler to produce a DC output. A buck converter structure is then cascaded after the voltage doubler structure to act as a controllable current regulator for the DC-link inductor that serves as the input of the CSI stage. The full bridge structure is modulated via a two-level square wave modulation that could be variable, but this paper considers a fixed AC frequency input. The first reason for this choice of modulation is switching losses. The objective of the full-bridge is to create an AC waveform

at high frequency without having to produce a sinusoidal voltage, since the voltage doubler would work with virtually any symmetric waveform. Choosing a square wave modulation gives the minimum number of switching states in a period, although not necessarily minimizing losses. The second reason is the fact that with square wave modulation, there is no need to have a PWM frequency higher than the AC frequency, so very high-frequency AC can be generated without needing a MHz-scale controller.

The voltage doubler is a passive element whose critical aspect is the sizing of the capacitors, which will be delved into later. The converter presented in this paper uses a voltage doubler with a theoretical gain of two. Lastly, a Buck converter structure is inserted to serve as a current regulator in the full CSI topology. The modulation strategies for the Buck converter can be numerous, and this paper will not focus on the modeling of this last part of the topology as much. The modulation strategy can be both an SVM, but more peculiar implementations are possible in case of special CSI applications. One such implementation would be a CSI-7, which is a specific 3-phase CSI that has an extra switch. A full control of a CSI-7 is discussed in [29]. In the case of Photovoltaic application, the MPPT will determine the DC link current setpoint from the MPP. This is possible because, if G is the gain of the DC-DC stage, then:

$$I_{Dclink} = I_{mpp}/G \tag{1}$$

A single current feedback loop and one MPPT is therefore all that is necessary to control the whole DC-DC stage.

The advantage of the DC-DC stage that was proposed with respect to the classical implementation of the voltage multiplier is the use of high frequency AC in a relatively high power application for grid connection. This enables the use of lower sized capacitors and gives the possibility of using the doubler in a higher rated power converter setting instead of the more typical low power switched capacitor applications. The novelty is also in the use of a full bridge at the input to generate high frequency AC. The full bridge can then also be used for bidirectional power flow by bypassing the voltage doubler. In that case, the converter would act similarly to the input bridge of a DAB. The necessity of having an active switch to bypass the doubler would slightly decrease the performance of the converter by a constant value equal to the P_{on} losses of the bypass switch. This will therefore be mainly conduction losses, since the bypass switch will stay on for very long intervals of time, with negligible switching losses. The capacitors can be either polarized or unpolarized. Choosing a polarized capacitor pair solution would reduce cost but also reduce reliability, due to electrolyte degradation phenomena [30]. Unpolarized capacitors are usually pricier but more reliable, especially due to the self-healing nature of metallized thin film capacitors [31] since the beginning stage is based on an h-bridge, a ready made module can be used, bringing down system complexity and part count.

The argument of using a single module for the input full bridge

From the standpoint of voltage behavior, the equation for output voltage can be obtained by chaining the effect of the various stages. In the most basic rendition of the output voltage equation that was proposed by the authors, the only non-ideality that is considered is the voltage drop across $D2$, while the voltage drop due to the equivalent series resistance of the various components is neglected. In (2), the voltage output for the proposed stage is given. The parameter D represents the duty cycle of the MOSFET $M5$. The power required at the output by the CSI-Grid is represented by a load R_L since up until the DC link inductor the system is effectively a DC/DC stage.

$$V_{out} = D(2V_{in} - V_{\gamma D_2}) \tag{2}$$

In case of non-negligible voltage drops on either the input MOSFETS or the DC link inductor, these two contributions have to be taken into account. (2) becomes:

$$V_{out} = D(2V_{in} - V_{\gamma D_2} - 2R_{DS}I_{in}) - R_{L\_DC}I_{out} \tag{3}$$

the input current I_{in} can be written as:

$$I_{in} = \frac{P_{in}}{V_{in}} = \frac{1}{\eta}\frac{P_n}{V_{in}} \tag{4}$$

(4) can be simplified assuming high efficiencies, which will later be demonstrated as a feasible assumption for the majority of use cases:

$$I_{in} = \frac{1}{\eta}\frac{P_n}{V_{in}} \approx \frac{P_n}{V_{in}} \tag{5}$$

Regarding the expression of the output current, from the definition of nominal power, the following can be obtained:

$$I_{out} = \sqrt{\frac{P_n}{R_L}} \tag{6}$$

Substituting (5) and (6) into (3) The full expression for V_{out} is obtained:

$$V_{out} = D\left(2V_{in} - V_{\gamma D_2} - 2R_{DS}\frac{P_n}{V_{in}}\right) - R_{L\_DC}\sqrt{\frac{P_n}{R_L}} \tag{7}$$

These two equations both give similar results, which are comparable to the laboratory test results obtained. Fig. 2 and 3 portray the expected behavior of the voltage output, using data from the components used in the experimental prototype that will be presented later. It can be noted that the difference between the two models (Model from Eq.2 in orange-full

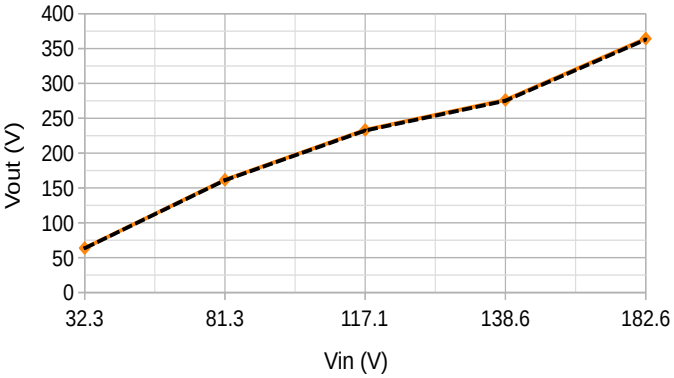


Fig. 2: Predicted voltage at constant load (155 Ohm)

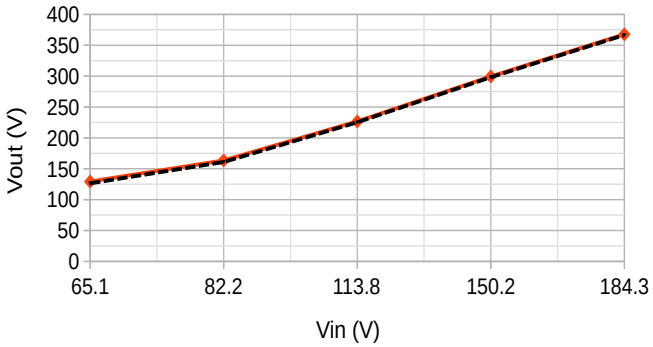


Fig. 3: Predicted voltage at constant power (500 W)

line, Eq.7 in black-dashed line) is low in the specific case presented, but it would get more noticeable for bigger DC-link inductors featuring higher ESR. The values predicted by these two models have been verified experimentally, and the results concerning the coherence between models and measurements will be discussed in Section IV.

Focus will now shift to the possible implementation of bidirectional capability. As stated at the beginning of the paper, this work presents an easily implementable technological solution. The first prerequisite to achieve bidirectional capability is to substitute the classic Mosfet-Diode combination for a CSI inverter with bidirectional switches. This is now a well established technique that has been documented in various recent works [32] [33] [34]. The commercial availability of monolithic GaN-based switches is currently pushing towards a reintroduction of current source inverters in applications where there were previously efficiency and thermal management concerns. This technological development will mean that bidirectional solutions will become increasingly feasible. A possible solution for reversed direction functionality will be showcased on a single phase variant. The core idea is to obtain an equivalent circuit as the one shown in Fig. 4 by bypassing the voltage doubler and first quadrant chopper structure, save for C_1 and L_{DC} that are employed as link components.

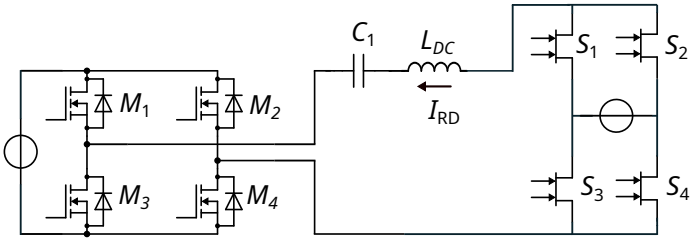


Fig. 4: Sample single phase topology in reverse direction mode (with bypassed doubler)

From the topology shown in Fig.4, by keeping S_3 and S_4 in the OFF state, M_4 in the ON state, and M_2 in the OFF state, the resulting structure is equivalent to that of a transformerless Dual Active Half-Bridge converter. This topology has been examined in [35] and represents one of the natural solutions that can be adopted. The relevance of the remark regarding bidirectional capability lies in the fact that the input bridge can also operate as a rectifier; therefore, any topological configuration capable of supplying it with an AC waveform is suitable for reverse-direction operation. Consequently, the efficiency of the topology will depend on both the technological implementation considered and the number of phases featured by the cascaded CSI structure at the output. In general the, the efficiency penalties would be limited to the conduction losses of the bypass switches, that can be very low do to the fact that there is virtually no lower bound to the switching speed, and the switches can therefore be chosen to minimize conduction losses as much as possible

It can be fruitful to introduce considerations about the cost of this solution to other more established topologies already present in the literature. A suitable alternative solution is represented by the interleaved boost converter, widely employed for its inherent redundancy and the many commercially available controller ICs. Side to side the component count of the topology proposed in this paper in relation with the one here contained in this paper are shown in Table I

TABLE I: Part count comparison between interleaved boost and presented topology

Topology	Switches	Diodes	Inductors	Capacitors
Interleaved Boost	N	N	N	0
Proposed Solution	4	2	1	2

N = number of branches

From this simple comparison we could infer that the only solution that the most cost competitive configuration of interleaved boost is the 2 branch variant, since alreadi with 3 stages we have the same amount of switches and reactive elements as the proposed solution (6 switches and 3 inductors) but capacitors are generally considerably cheaper than inductors. An example minimal bill of materials has to take into account the main design parameters for the main elements. Table II

TABLE II: Device sizing for an interleaved boost converter compared to proposed solution

Device	Voltage Rating	Current Rating
IB Switch (MOSFET)	V_{out}	$\frac{I_{out}}{N}$
IB Diode	V_{out}	$\frac{I_{out}}{N}$
IB Inductor	$V_{out} - V_{in}$	$\frac{I_{out}}{N}$
D Switch (MOSFET)	$\frac{V_{out}}{2}$	$2I_{out}$
D Diode	V_{out}	I_{out}
D Inductor	$V_{out} - 2V_{in}$	I_{out}

IB = interleaved Boost, D = proposed converter

There is no clear-cut, definitive answer with regard to the comparison between the 2-branch interleaved boost and the proposed solution, since the power level and voltage input will determine the commercial availability of readily available inductors, which are the main driver of cost in both topologies.

Chosen sizing parameters

V_{in} (V)	P_{out} (W)	V_r (V)	f_{sw_min} (Hz)
120	2000	15	10000

Worst case scenario parameters

V_{in} (V)	P_{out} (W)	V_r (V)	f_{sw_min} (Hz)
80	2500	15	10000

The proposed solution is competitive, both in terms of part count and voltage and current rating of components.

III. Sizing considerations

After having obtained an estimate of electrical quantities, it is possible to proceed to the sizing of the switching components to achieve a desired switching frequency. The switching frequency is not only crucial for the behavior of the active components but also dictates the size of the capacitors. To achieve voltage doubling, these have to be of the same size. The most convenient capacitor to size is the shunt capacitor C_2 due to the fixed voltage across it. At steady state, the voltage doubler has a 50% duty cycle; therefore, the capacitor has to be able to supply the required output power for half a period. The sizing is made on the basis of the power that the capacitor has to supply to the output when D_2 is off. The capacitor C_2 charges for half of the period T and discharges in the other half. The power supplied by the capacitor can be written as:

$$P = \frac{\Delta E}{\Delta t} = \frac{1}{2} C_2 (V_{max}^2 - V_{min}^2) \frac{2}{T} \tag{8}$$

where V_{max} and V_{min} are the highest and lowest voltages reached during a period, thus it can be written that:

$$V_{max} \approx 2V_{in} - V_{\gamma D_2} + \frac{V_r}{2}$$
$$V_{min} \approx 2V_{in} - V_{\gamma D_2} - \frac{V_r}{2}$$

Where V_r is the total voltage ripple. Since $V_{\gamma D_2}$ is relatively small, it can be neglected in the calculation of the value of the capacitor, since it would be necessary to settle for commercial capacitance values anyway. (8) then becomes as follows

$$P = \frac{\Delta E}{\Delta t} = \frac{1}{2} C_2 (V_{max} + V_{min})(V_{max} - V_{min}) \frac{2}{T} = C_2 (4V_{in}) V_r f_{sw} \tag{9}$$

Where f_sw is the switching frequency. An explicit formula for the sizing of the capacitor can be derived from (9). The formula can be expressed as follows

$$C_2 = \frac{P}{(4V_{in}) V_r f_{sw}} \tag{10}$$

In the prototype that will be presented in this paper, the parameters chosen for sizing are the following: with those parameters a value of $C_2 = 27.8\mu F$ is obtained from (10). On the prototype proposed in this paper, $C_2 = 20\mu F$ is actually employed, so the ripple is expected to be higher than 15V. The voltage ripple must be chosen as a trade-off between the voltage ripple and the small capacitor size. The latter is desirable as smaller capacitors have a lower ESR and thus can provide higher efficiency. However, degradation of their ESR related to wear must be considered for durability.

When choosing the parameters to implement the sizing, it is also possible to be conservative in terms of power quality and envision the worst-case scenario with respect to output voltage ripple. In terms of the absolute value of V_r, this scenario happens with the minimum input voltage, minimum switching frequency, and maximum expected power output. In this scenario, a capacitor value of $52\mu F$ would be obtained, which is double the size of the required value in the nominal case. The choice to use either of the two strategies presented here is up to the designer and is also dependent on input filtering specifications. It must be kept in mind that the DC_{link} inductance will act as a low-pass filter as well, so exceeding caution may lead to unnecessary oversizing.

A short digression has to be dedicated to the sizing of the major active components. The most straightforward components to size are the voltage doubler diodes. Both the diodes withstand a voltage equal to $2V_{in}$ by virtue of the working principle of the voltage doubler. The on current, on the other hand, can go up to $I_D C_{link} + I_{ripple}$. For a desired ripple percentage, the following current can be considered

$$I_{D_{max}} = \frac{I_{r\_max} + I_{DC\_max}}{I_{DC\_link}} I_{DC\_max} = \frac{I_{r\_max} + \frac{P_n}{2V_{in}}}{\frac{P_n}{2V_{in}}} \frac{P_n}{2V_{in}} = \frac{2V_{in} I_{r\_max} + P_n}{P_n} \frac{P_n}{2V_{in}} \tag{11}$$

where I_{r_max} is the current ripple expressed as:

$$I_{r_max} = I_{r\%} I_{DC\_max} \tag{12}$$

Concerning MOSFET sizing, they have to withstand a voltage equal to V_{in} and a current which is the same as the voltage doubler's.

A final consideration in the sizing process concerns the thermal management of components, with particular emphasis on the switching devices. The power dissipation of the main categories of switches within the converter was determined through simulation, and the corresponding results are presented in Table III. These values were obtained under nominal operating conditions, corresponding to an output power of approximately 1.5kW. The selection and sizing of heatsinks can be significantly facilitated by a recent Wolfspeed application note [36], which provides an extensive evaluation of the thermal performance of TO-247 Silicon Carbide based devices under various conditions, including the influence of silpad characteristics and interface pressure.

According to the referenced application note, a typical junction-to-case thermal resistance is approximately 0.46 °C/W. The thermal resistance of the silpad, however, exhibits significant variation depending on factors such as material type, insulation class, and the applied mounting pressure, with reported values ranging from 1.4°C/W to 3.0°C/W. Once the

TABLE III: Power loss distribution across components

Component	Power loss (W)
Buck Mosfet	6.37
H-bridge Mosfet	13.57
Shunt Diode	8.96
Series Diode	8.90

heatsink has been selected, the total thermal resistance can be expressed as:

$$R_{\theta,\text{total}} = R_{\theta,\text{jc}} + R_{\theta,\text{cs}} + R_{\theta,\text{sa}} \tag{13}$$

It is then possible to compute the resulting temperature rise, ΔT, based on the selected configuration. Alternatively, the desired ΔT may be specified a priori as a design constraint.

$$\Delta T = P_{\text{loss}} \cdot (R_{\theta,\text{jc}} + R_{\theta,\text{cs}} + R_{\theta,\text{sa}}) \tag{14}$$

IV. Frequency behavior and ripple rejection

When analyzing the frequency behavior of the converter, the sheer number of switches poses a weighty challenge on the shoulders of the designer. The basic premise of the discourse hereby presented is to split the analysis between the buck converter structure and the full bridge/doubler. Since these two structures are in series, it can be assumed that the total amplitude gain for a signal at a given frequency is the product of the voltage gain that the two stages have at that frequency. This can be denoted as follows:

$$\frac{v_{OUT@w}}{v_{IN@w}} = G_M(w)G_{Buck}(w) \tag{15}$$

Where $G_M(w)$ and $G_{Buck}(w)$ are the real parts of the transfer functions of the first stage and the buck converter evaluated at frequency ω. The frequency behavior of the buck converter is thoroughly discussed in the literature [37] [38] [39]. Therefore, the focus will be placed on the frequency behavior of the first stage. In the experimental case presented, the full bridge topology has no input filter and is operated in square-wave mode; therefore, its effect on the transfer function is in practice negligible. This stage has however another effect, which is only related to the square wave modulation, namely the fact that the harmonics generated by the square wave modulation become part of the input ripple and get summed to the input noise. To be precise, the input noise also gets flipped by $180°$ during the negative half wave since the input polarity of the voltage doubler gets reversed every half period, and therefore, the whole input signal gets multiplied by -1, not just the DC part. The input to the voltage doubler can therefore be written as:

$$v_{in_M} = \mp v_{noise} + \frac{4}{\pi} V_{in} \sum_{n=0}^{\inf} \frac{sin((2n+1)\pi f_{sw} t)}{2n+1} \tag{16}$$

Fig. 5 illustrates an example of the waveforms described by (16). This is the voltage input waveform that the doubler receives with $V_{in} = 100$, a switching frequency of 20kHz, and an injected 5V 100kHz sinusoidal noise. The fact that the phase of the input noise flips by $180°$ during the negative half-wave is very evident here.

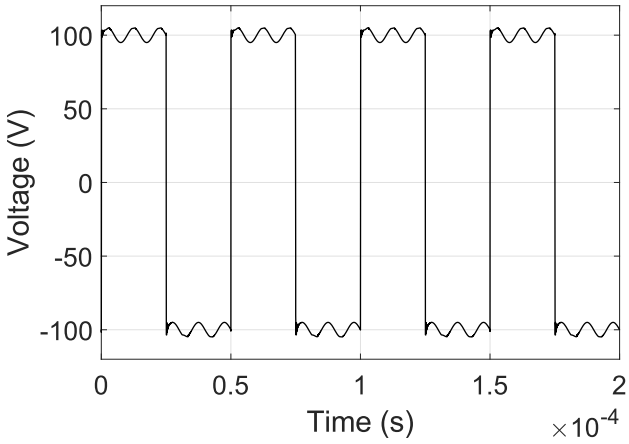


Fig. 5: Sample voltage doubler input waveform obtained in simulation (SPICE) by injecting a 100kHz sine wave noise on the DC input

Now the only part left to describe is the actual main contributor to ripple attenuation, which is represented by the frequency behavior of the voltage doubler circuit. There are two possible states of this circuit, corresponding to which diode is conducting at a given moment. By applying time-dependent LKV to the equivalent circuits obtained the following can be derived:

$$\begin{cases} \frac{dv_{in}}{dt} = \frac{1}{C} i_{out} + l_{DC\_link} \frac{d^2 i_{out}}{dt^2} + R_{out} \frac{d_{iout}}{dt} & if\ D_2\ on \\ \frac{1}{C} i_{out} = l_{DC\_link} \frac{d^2 i_{out}}{dt^2} + R_{out} \frac{d_{iout}}{dt} & if\ D_1\ on \end{cases} \tag{17}$$

Since all the capacitors in a Cockroft-Walton multiplier have the same value, the letter C will be used in all the equations to indicate either C_1 or C_2, the text will then explain how the equation has been derived. The two expressions in (17) refer to the loop containing the output load. In case $D1$ is on, the output loop becomes just an RC circuit discharging on the load. For this reason, in this paper, the focus will only be on the transfer function in the case in which $D2$ is on, since in this case the input and output voltage are actually influencing each other. A crucial simplification that was done in the case that considers $D2$ is that the current flowing in and out of $C2$ is low and therefore negligible. This assumption will be much more accurate for higher frequencies, but not as precisely representative of low-frequency behavior. Starting from the corresponding differential equation, the following transfer function can be obtained:

$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{sR_L C}{1 + sR_L C + s^2 L_{DC\_link} C} \tag{18}$$

This type of transfer function is a typical band-pass filter behavior. To validate the approximation, the Bode diagram of the equivalent circuit of the voltage doubler when $D2$ is on was also simulated in SPICE, including the DC link inductance

and the load. In Fig. 6 and Fig. 7, the Bode diagram of

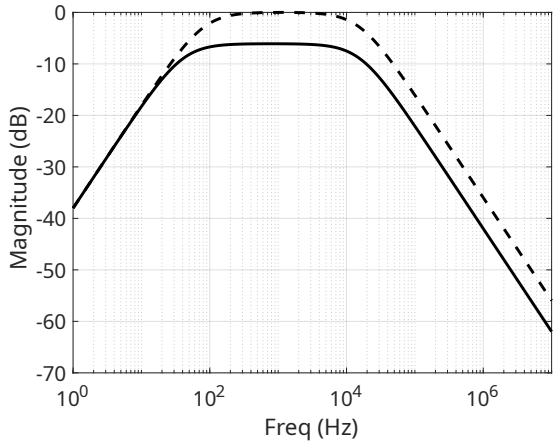


Fig. 6: Amplitude plot of voltage doubler and DC-link stage obtained in Matlab(Dashed) and in Spice(solid)

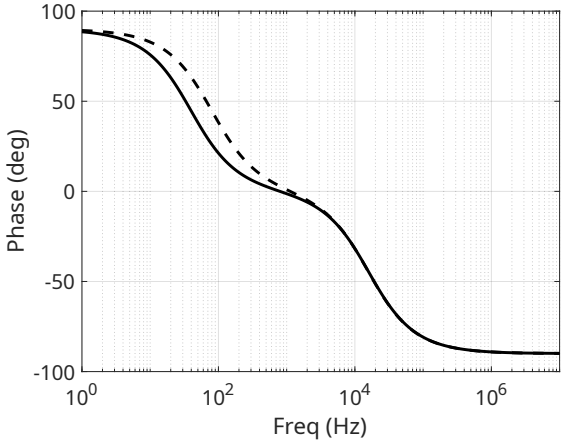


Fig. 7: Phase plot of voltage doubler and DC-link stage obtained in Matlab(Dashed) and in Spice(solid)

the transfer function calculated from the presented simplified model in MATLAB for $C = 20\mu f$, $L_{DC\_link} = 1mH$, $R_L = 100$ is shown alongside the results obtained in SPICE. The phase data is shown in Fig. 7. The SPICE simulation also takes into account the effect of the capacitance $C2$, which is neglected in the simplified analytical model, and yet the results obtained are very similar. The only notable difference is the -6dB plateau in the SPICE simulation, which is due to the neglected capacitance. Still, the goal of the simplification was to predict the stability and the cutoff frequencies, which are well predicted. Furthermore, since the error of 6Db at the middle band is systematic, it can eventually be corrected by taking it into account after the calculation. This Bode diagram does not take into account any parasitic effect, but there is a parasitic element that has been observed to be especially influential in simulating the frequency behavior. This parasitic element is the $C1$ capacitor's equivalent series resistance. In this case, the equivalent circuit when $D2$ is on becomes as shown in Fig. 8. In this instance, the effect of $C2$ cannot be

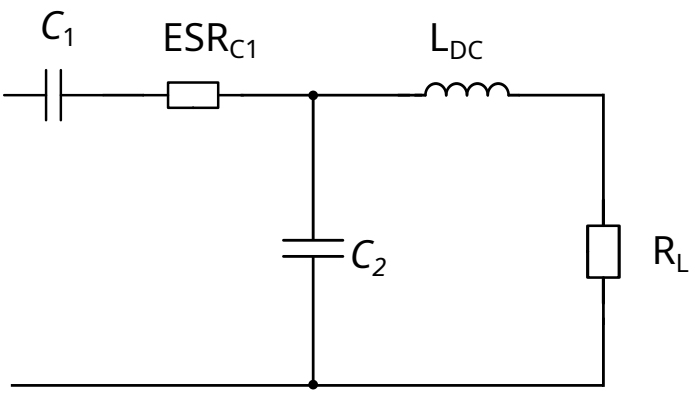


Fig. 8: Equivalent circuit of voltage doubler circuit with DC link and load considering equivalent series resistance of $C1$

neglected, but there is still a sensible approximation that can be done to obtain an analytical transfer function. The effect of the low-pass filter formed by $C2$ and ESR can be considered as independent from the effect of the rest of the circuit, and then consider the superposition. This would be exactly true if the low-pass filter formed by ESR and $C2$ were put before $C1$, while it introduces an error in the instance at hand. The transfer function obtained via superposition can be expressed as follows:

$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{1}{1 + sC * ESR_{C1}} \frac{sR_L C}{1 + sR_L C + s^2 L_{DC\_link} C} \tag{19}$$

The results obtained analytically from (19) will now be compared with the Bode diagram obtained by simulating the circuit in Fig. 8 on SPICE. The results of this second version of the model are shown in Fig. 9 and 10.

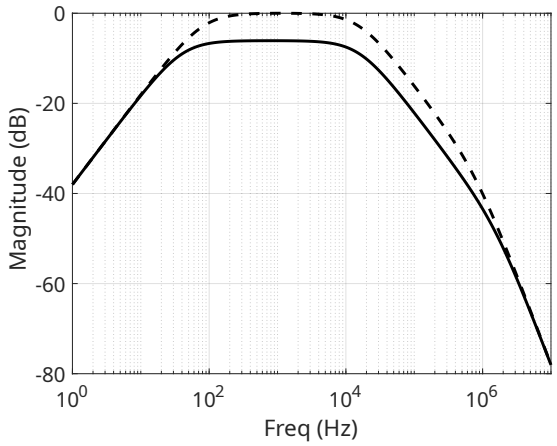


Fig. 9: Amplitude plot obtained by considering non-zero equivalent series resistance in Matlab(Dashed) and in Spice(solid); $C = 20\mu F$, $L_{DC\_link} = 1mH$, $R = 100$, $ESR = 10m$

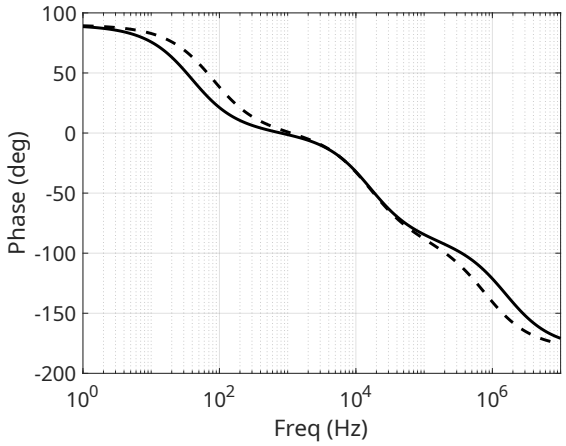


Fig. 10: Phase plot obtained by considering non-zero equivalent series resistance in Matlab(Dashed) and in Spice(solid)

Regardless of the introduced error the adherence of the analytical and simulation model is quite remarkable also in this second instance. The simulated voltage ripple waveforms under various load conditions are presented in the following paragraphs. As expected for this topology, the ripple exhibits a characteristic triangular shape, which is a direct consequence of the continuous conduction mode operation. Fig. 11 illustrates the percentage ripple across different load levels, providing a quantitative assessment of its variation. For completeness, Fig.12 displays the corresponding voltage waveforms from which the ripple values in Fig.11 were derived. Both figures were included to allow to correlate the numerical ripple values with the actual waveform characteristics.

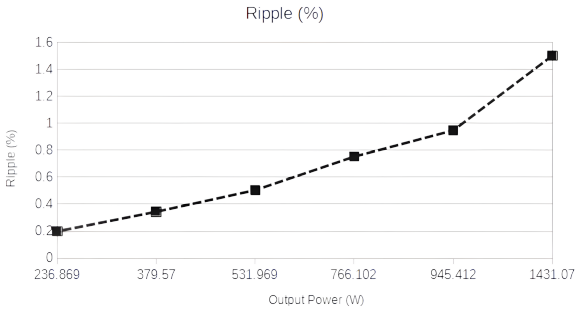


Fig. 11: Voltage ripple in percentage relative to DC link Voltage at various output power levels

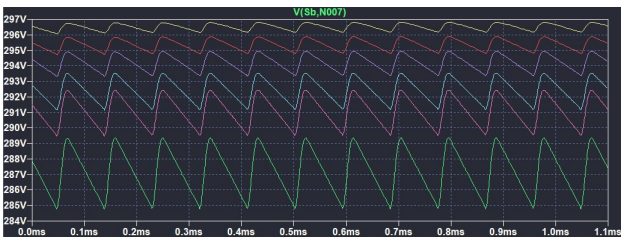


Fig. 12: Ripple waveforms under varying load conditions

V. Experimental setup

In the experimental setting, the board was tested being supplied from a DC source and tested on a passive load. The choice to employ a passive load is not so far-fetched, as the CSI structure that has to be put after this topology will behave in a first quadrant operation. The experimental setup is shown in Fig. 13.

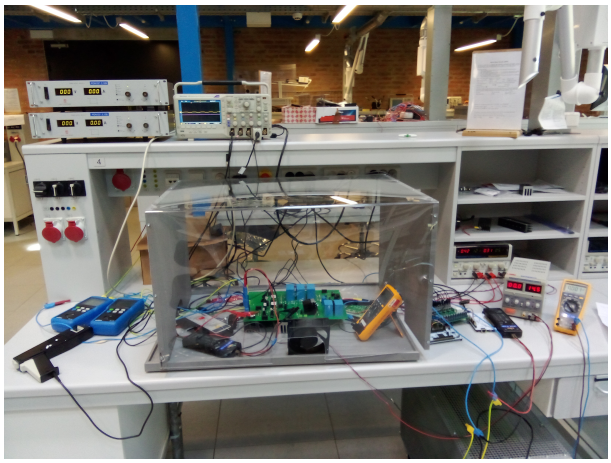


Fig. 13: Image of the experimental setup employed

The converter was sized for a rated absolute maximum power of 2000W, maximum continuous input voltage of 200V, and maximum input current of 10A. The topology was controlled using a square wave open-loop modulation for the full bridge, and a constant duty cycle for $M5$. In Fig. 14, a snapshot of some sample experimental waveforms is shown. The output voltage waveform is shown in purple, while the output current waveform is shown in green. The blue trace is the AC voltage generated by the full bridge that serves as an input for the voltage doubler. As it is immediately evident, the amount of ripple at the output is low even for a rather low frequency of $11kHz$, such as the one presented in the figure. This frequency was chosen to avoid EMI problems and as a compromise to avoid excessive losses in the diodes. The case presented in Fig. 14 is for an output of 960W.

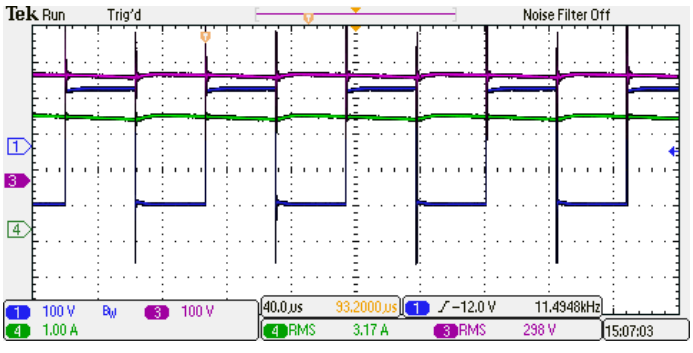
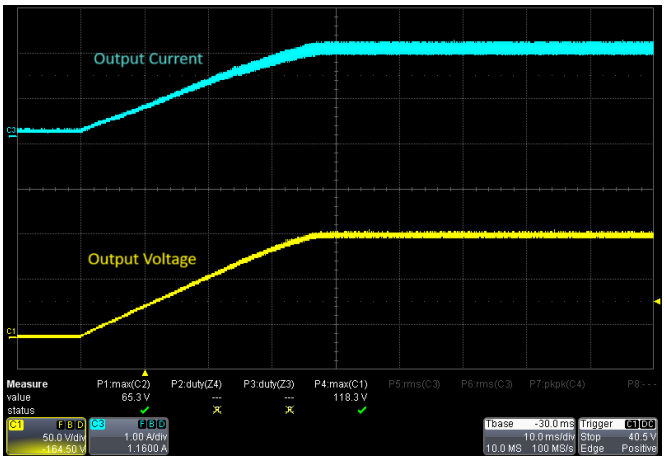


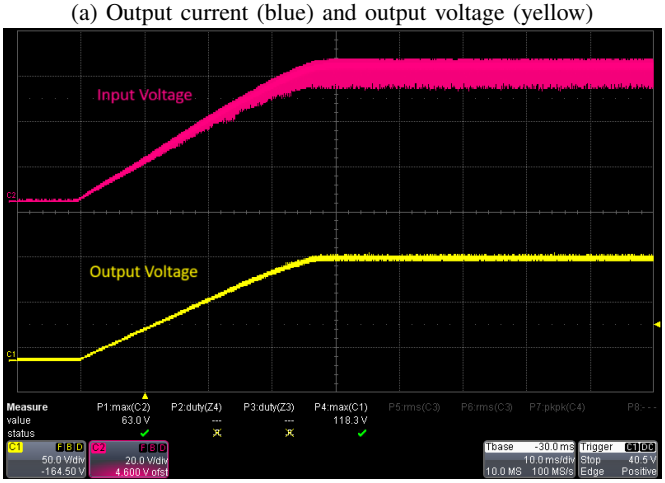
Fig. 14: Sample waveforms for an output of 960W,$V_{out} = 300V$(Channel 3), $I_{out} = 3.2A$(Channel 4), output of the h-bridge (Channel 1)

One of the most important tests conducted was measuring output voltage and comparing it with the proposed models.

The working points shown in Fig. 2 and 3 were all tested experimentally, and for the 155 ohm load case an average error of 4,79% was obtained. In the constant $500W$ test, most values of error were under 6% aside from two noticeable outliers corresponding to the 65.1V and 82.2V input, which gave an error well over 10%. This suggests model limitations, but there is nevertheless fundamental adherence between the model and the data. The transient behavior to a step of input voltage is shown in Fig. 15. It can be seen that the converter needs either a softstart strategy or a pre-charging phase for the capacitors of the doubler, to avoid surges in power drain in the first moments of operation of the converter.



(a) Output current (blue) and output voltage (yellow)



(b) Input voltage (red) and output voltage (yellow)

Fig. 15: Turn-on transient behavior of the converter.The waveforms shown in the subfigures are relative to the same transient, and have been separated for clarity

Efficiency measurements were also carried out with promising results. The results obtained are reported in Table IV. This data gives an impression of the capabilities of the proposed converter, leaving encouraging signals for the field application of this technological solution.

For comparison, Table V contains reported efficiencies [40] [41] [42] [43], for some of the most interesting competitors for this solution. Most solutions, such as soft switching boost converter and interleaved boost, reach relatively similar values of efficiency when compared to the proposed solution, around

TABLE IV: Measured output efficiency of the DC-DC stage

Pout (W)	Pin (W)	efficiency (%)	Vin
1658	1741	95.23	206
1013	1065	95.12	160
1028	1054	97.53	166
829	873	94.98	119
528	552	95.69	119

TABLE V: Reported output efficiency of competing topologies

Type	Source	efficiency (%)	Power Rating (W)
Buck	[40]	96-97	1500
Cuk	[40]	91	1500
Soft switching Boost	[43]	97.28	1200
Step down partial power	[41]	97.5	820
Step up partial power	[41]	98.5	820
interleaved Boost	[42]	96	1000

96-97%. The efficiency reached is very high, in accordance with what is reported in [44]. There are also other modern topologies that should be considered for a comparison in this case, which are the reported output efficiency of competing technologies boost and resonant topologies. The Interleaved boost is a competitive solution and the choice of using it instead of the proposed stage stems from the extensive considerations done in section II about the cost effectiveness. Resonant converters are more efficient but more difficult to control due to the nonlinear gain curve that requires a more careful approach to control. The proposed converter has a natural upper limit for voltage, which is equal to n times the input voltage, where n is the number of stages. This means that if the pre-boost is sized in such a way that $nV_{in} < V_{peak}$, we can run the full bridge in open loop and handle the current control with the first quadrant chopper feedback. This is much easier than having to implement MPPT, optimizing the gain of a resonant converter, and a CSI simultaneously.

VI. CONCLUSION

A novel topology for a pre-regulation DC-DC stage was proposed based on a combination of a full bridge stage and a voltage doubler, able to feed a current source inverter, including a complete analytical description of it. The model has been validated experimentally with good adherence between the model and experimental results, with prediction error generally below 6%. An analytical frequency domain model has also been provided, which closely matches simulation results. Future developments of the models presented in this paper should analyze EMI aspects as well as MPPT integration. These last two aspects will be important to assess grid integration applications. The converter has shown very good efficiency even with a basic open loop control scheme, reaching 97.5% efficiency at 1054W output.

The proposed topology represents a competitive alternative to other well established solutions as a DC/DC intermediate stage for low voltage source applications such as fuel-cells or low voltage photovoltaics.

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