

POLITECNICO DI TORINO  
Repository ISTITUZIONALE

Norme e regole, tra adattamento e resistenza, nella città e negli insediamenti: la documentazione d'archivio e la costruzione reale / Norms and rules, between adaptiveness

*Original*

Norme e regole, tra adattamento e resistenza, nella città e negli insediamenti: la documentazione d'archivio e la costruzione reale / Norms and rules, between adaptiveness and resistance, in towns and settlements: archival documents and true realisations / Devoti, Chiara; Bodrato, Enrica; Ordasi, Zsuzsanna - In: Adattabilità in circostanze ordinarie / Ordinary Conditions Adaptability / Devoti Chiara, Bolca Pelin (a cura di). - ELETTRONICO. - Torino : AISU International, 2024. - ISBN 978-88-31277-09-9. - pp. 13-16

*Availability:*

This version is available at: 11583/2991630 since: 2024-09-05T15:40:11Z

*Publisher:*

AISU International

*Published*

DOI:

*Terms of use:*

This article is made available under terms and conditions as specified in the corresponding bibliographic description in the repository

*Publisher copyright*

(Article begins on next page)

# An Integrated GaAs HBT Doherty Power Amplifier for Wi-Fi 6

Francesco Manni<sup>#1</sup>, Rocco Giofrè<sup>#</sup>, Corrado Florian<sup>§</sup>, Alberto Maria Angelotti<sup>§</sup>, Gian Piero Gibiino<sup>§</sup>, Marco Pirola<sup>\*</sup>, Chiara Ramella<sup>\*</sup>, Paolo Colantonio<sup>#</sup>.

<sup>#</sup>Department of Electronic Engineering, University of Roma Tor Vergata, Italy

<sup>§</sup>Department of Electrical, Electronic and Information Engineering “G. Marconi”, University of Bologna, Italy

<sup>\*</sup>Department of Electronics and Telecommunications, Politecnico di Torino, Italy

<sup>1</sup>francesco.manni@uniroma2.it

**Abstract**— This paper presents an integrated three-stage Doherty power amplifier for Wi-Fi 6 applications operating in the 5-6.2 GHz frequency range. The H20U-C4 GaAs HBT technology available at WIN semiconductors is chosen for its excellent linearity and good efficiency features. The power cells adopted as active devices are designed to be thermally and RF stable through the proper selection of ballast resistors and capacitors. A comprehensive measurement campaign was conducted, demonstrating an output power, efficiency and gain larger than 32 dBm, 35 % and 22.5 dB, respectively, at saturation. At 6 dB of output back-off the efficiency is better than 20 % all over the specified bandwidth. Moreover, when tested with a 20 MHz MCS11 signal having 10 dB PAPR, the DPA provides an average output power of 22 dBm with an efficiency and EVM of 11 % and -25 dB, respectively.

**Keywords**— Doherty power amplifier, MMIC power amplifier, GaAs, HBT technology, WiFi-6.

## I. INTRODUCTION

The growing need for higher data transmission rates to support emerging services, combined with the rapid proliferation of user terminals, continuously drives the evolution of Wi-Fi communication standards. The introduction of Wi-Fi 6 (802.11ax standard) increases bandwidth and incorporates advanced technologies to improve communication speeds while efficiently managing multiple users [1]. It exploits higher-order modulation schemes, including 1024-QAM, and Orthogonal Frequency Division Multiple Access (OFDMA), which result in time-domain signals with high peak-to-average power ratio (PAPR). This leads to more severe linearity constraints to minimize distortion and maintain signal integrity for reliable communication. Achieving the specified output power level along with acceptable power-added efficiency (PAE) while respecting the stringent Error Vector Magnitude (EVM) threshold is a significant challenge for power amplifier (PA) designers working on these systems. To handle high PAPR signals, back-off efficiency enhancement PA architectures are typically adopted, while linearity requirements are usually accommodated through the selection of a suitable semiconductor technology and the use of digital predistortion techniques (DPD). This work aims to evaluate the effectiveness of the Doherty power amplifier (DPA) architecture, in combination with HBT GaAs technology, for such kind of peculiar application. For this purpose, a MMIC

DPA using the 5 V H20U-C4 InGaP/GaAs HBT technology of WIN semiconductors has been designed, fabricated and tested. In particular, a three stage architecture is exploited to fulfill the gain requirement while a 2:1 active periphery ratio has been selected among final/driver and driver/pre-driver stages to maximize the efficiency.

The fabricated prototype demonstrates a linear gain exceeding 24 dB and an output power greater than 32 dBm in the frequency range from 5 GHz to 6.2 GHz. In this frequency range, the PAE is higher than 33% with a peak of 44%, while it remains above 20% at 6 dB output back-off (OBO). An output power of 22 dBm and a PAE of 11 % were measured at -25 dB of EVM using an MCS11 standard (1024-QAM) signal, without any DPD.

## II. POWER CELL DESIGN AND LOAD PULL RESULTS

Accounting for the power density of the selected process and the desired peak output power of 32 dBm, a power cell (PC) composed of several elementary HBTs has been firstly conceived to be adopted in the final stage of both branches of the DPA. Specifically, the PC combines four HBTs, each one with 4 fingers of  $3 \mu\text{m}$  and  $40 \mu\text{m}$  emitter width and length, respectively, as shown in Fig. 1. Since HBTs exhibit a gain reduction as the temperature increases, a base ballast resistor of  $R_B = 150 \Omega$  is introduced to prevent any possible imbalance in the collector currents, which could otherwise lead to gain collapse and potential device failure [2]. Additionally, a series RC circuit (i.e.,  $r_b = 2.1 \Omega$  and  $C_b = 1.7 \text{ pF}$ ) is added at the base of each HBT to ensure PA stability over the whole band, while  $R_P = 65 \Omega$  and  $R_C = 14.9 \Omega$  have been properly selected to guarantee stability against internal loops.

The PC was manufactured and tested with a Load-Pull system at 5.6 GHz with a collector bias voltage and current of  $V_C = 5 \text{ V}$  and  $I_{CQ} = 192 \text{ mA}$ , respectively. Fig. 2 shows a picture of the PC and the comparison between the measured and simulated PAE as a function of output power when the device is terminated on the optimum load for maximum efficiency and power, respectively. Notably, the device model predicts quite accurately the measured results for both loading conditions, even if it shows a more pronounced compression behavior near saturation, due to a higher sensitivity to the second-harmonic load.

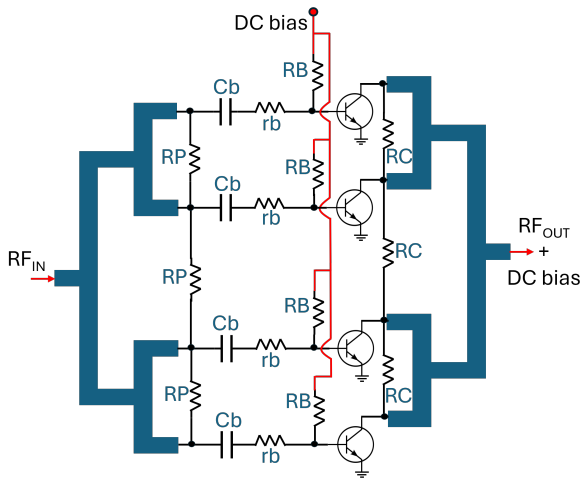


Fig. 1. Schematic of the power cell of the DPA final stage.

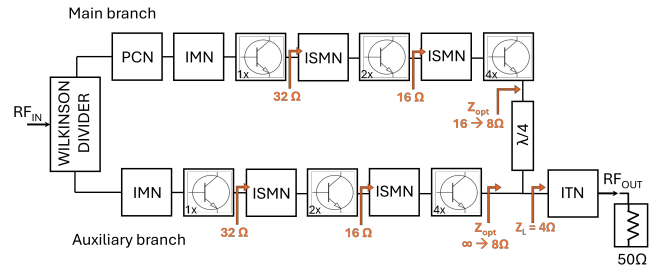


Fig. 3. Block diagram of the designed DPA.

PCs in the final stage. To achieve a compact layout, the IIN was implemented with its equivalent lumped T-shaped network, that is, two series capacitors and a short-circuit-terminated stub in between. Each PC is then independently biased through a further parallel stub, which is also exploited to neutralize the residual output parasitic capacitance of the PCs. The inter-stage matching networks (ISMNs) have been implemented following a semi-lumped design strategy to transform the input impedance of the following stage to the optimum load impedance required by the scaled devices (ref. Fig. 3). The main design challenge was represented by the input impedance variation of the cells with dynamic operating conditions, which required careful optimization of these ISMNs. The same architecture and design approach was adopted in both branches, but some circuit elements have been then independently optimized to properly compensate for the different biasing conditions of the devices, i.e., class AB and deep B, within the Main and Auxiliary branches, respectively. The same biasing condition was set to all stages belonging to the same branch to keep the DPA biasing as simple as possible. The input of each branch is finally matched to  $50\ \Omega$  through an input matching network (IMN), while the phase misalignment between them is corrected by adding a lumped  $\Pi$ -shape network with  $-90^\circ$  phase shift at the input of the Main branch (PCN in Fig. 3). The circuit is completed with a lumped symmetric Wilkinson divider. Fig.4 shows a picture of the fabricated MMIC.

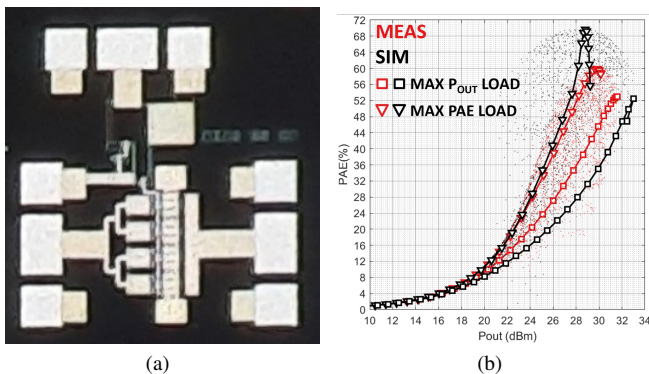


Fig. 2. Picture of the PC (a) and comparison between Load-Pull measurements (red lines) and simulations (black lines) for two different output loads (b): the one corresponding to maximum PAE (triangles) and the other corresponding to maximum output power (squares).

To maximize the trade-off between efficiency and linearity, a 2:1 active periphery ratio among final, driver and pre-driver stages has been selected for both branches of the three-stage DPA architecture. Therefore, the driver device is based on the same circuit topology of Fig.2(b) but with only two elementary HBTs, while the pre-driver device uses only one elementary HBT where RC and RP are no longer present.

### III. DPA ARCHITECTURE AND DESIGN STRATEGIES

The block diagram of the proposed three-stage DPA is shown in Fig. 3.

For the PC in the final stage, the optimum output load was selected as a trade-off between the loading conditions for maximum power and efficiency, resulting in a resistance value of  $R_{opt_F} = 8\ \Omega$ . Therefore, targeting an OBO of 6 dB, the output termination of  $50\ \Omega$  has to be transformed in  $R_{opt_F}/2 = 4\ \Omega$  at the common node connecting the main and the auxiliary branches. This is accomplished through a two-section semi-distributed impedance transforming network (ITN in Fig.3). Then a proper load modulation was achieved with a  $\lambda/4$  impedance inverting network (IIN), with characteristic impedance  $Z_c = 8\ \Omega$ , inserted between the two

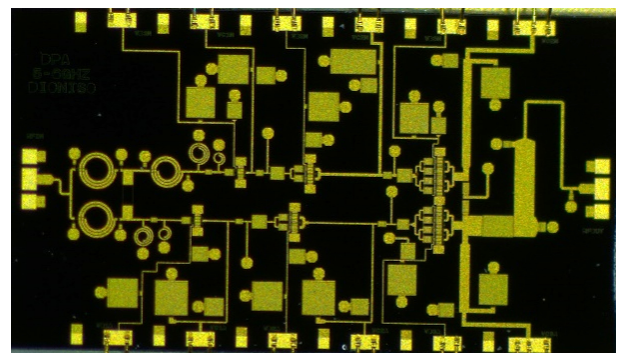


Fig. 4. Picture of the implemented integrated DPA (size: 4.5 mm x 2.5 mm).

#### IV. EXPERIMENTAL CHARACTERIZATION

The fabricated MMIC has been glued to a copper support before starting an extensive testing campaign. The collector supply voltage is fixed at 5 V, while the corresponding collector quiescent currents of the power cells (pre-driver/driver/final) are:

- Main devices: 27 mA/54 mA/108 mA ( $V_{BB} = 1.34$  V);
- Auxiliary devices: 2.5 mA/5 mA/10 mA ( $V_{BB} = 1.27$  V).

The class B bias condition for the Auxiliary branch has been selected to improve linearity in the Doherty region.

Fig. 5 shows the comparison between measured and simulated small-signal performance. The overall behavior across the tested frequency range is well predicted by the models, also in terms of absolute values. In the specified frequency band, i.e., 5-6.2 GHz, measurements show a small signal gain in excess of 24 dB, with input and output return losses better than 8 dB and 13 dB, respectively.

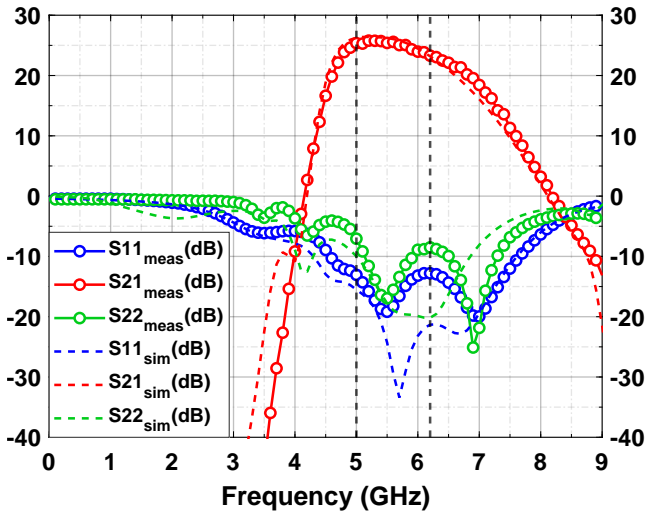


Fig. 5. Measured (circle lines) and simulated (dashed lines) S parameters.

The DPA was tested with continuous wave (CW) signal from 4.7 GHz to 6.5 GHz with steps of 0.1 GHz and capturing the output power, efficiency, gain and amplitude to phase distortion (AM/PM) as a function of input power.

Fig. 6 shows the comparison between measurements and simulations at 6 dB OBO and at saturation. Notably, the measured PAE and output power are slightly better than the simulated ones, confirming the trend already observed in Fig. 2(b). The PAE at 6 dB OBO is always higher than 20 %, while it is in the range of 33-44 % at saturation, where the output power and the power gain exceed 32 dBm and 22.5 dB, respectively.

The AM/PM and AM/AM performance at center frequency and at both edges of the band are shown in Fig. 7. The measured AM/PM response is much better than the simulated one approaching saturation, where also AM/AM simulated curves show a sharp variation. The reason behind this discrepancy is likely related to the different behavior of the DC collector currents predicted by the model close to gain

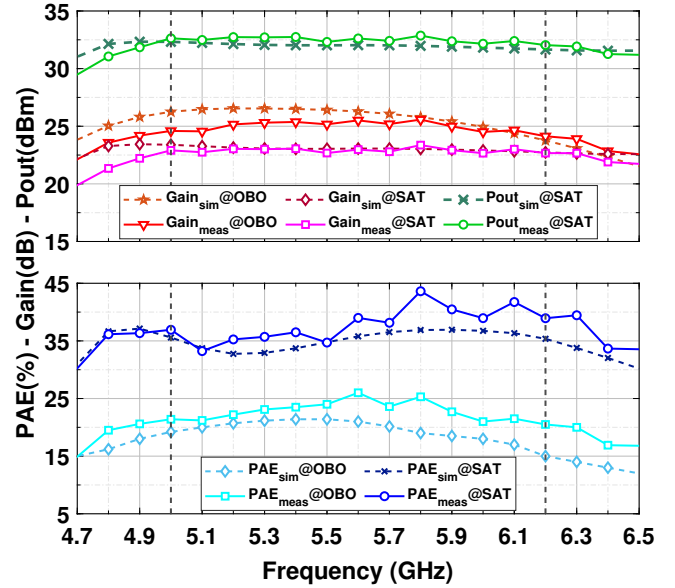


Fig. 6. Comparison between measurements and simulations at 6 dB OBO and at saturation.

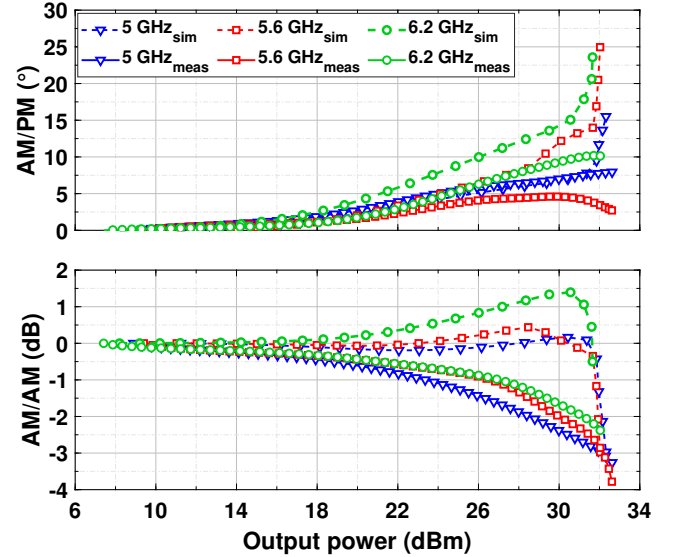


Fig. 7. Measured and simulated AM/AM and AM/PM performance.

compression with respect to the actual measured one, as reported in Fig. 8. Although the behavior is well predicted up to medium power, the simulated DC current stops increasing close to the saturation. As already discussed, the reason is probably due to the stronger influence of the second harmonic predicted by the model with respect to reality.

The amplifier has been finally tested using a 20-MHz-bandwidth 802.11ax MCS11 signal (1024-QAM), showing a PAPR around 10 dB, obtaining the results reported in Fig. 9. The amplifier, without any predistortion correction, achieves 22 dBm of output power, with an EVM of -25 dB and PAE of 11 % at 5.6 GHz. The level of -45 dB of EVM has been measured with an output power of 10 dBm. Table 1

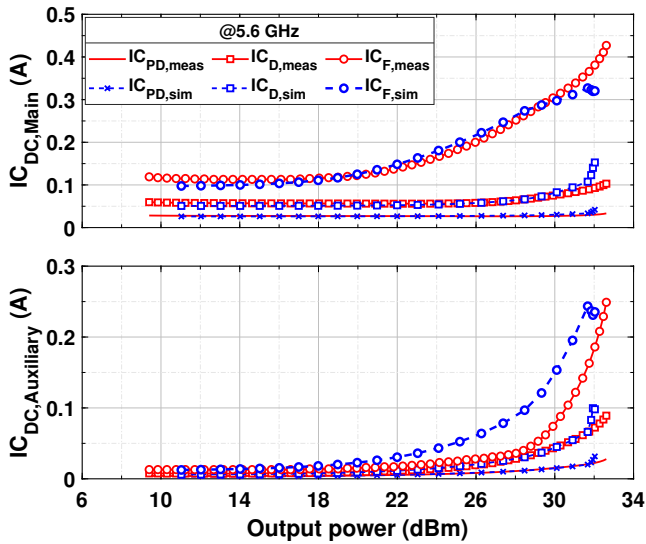


Fig. 8. Measured and simulated DC collector currents for the Main and Auxiliary devices (pre-driver, driver and final cell) at 5.6 GHz.

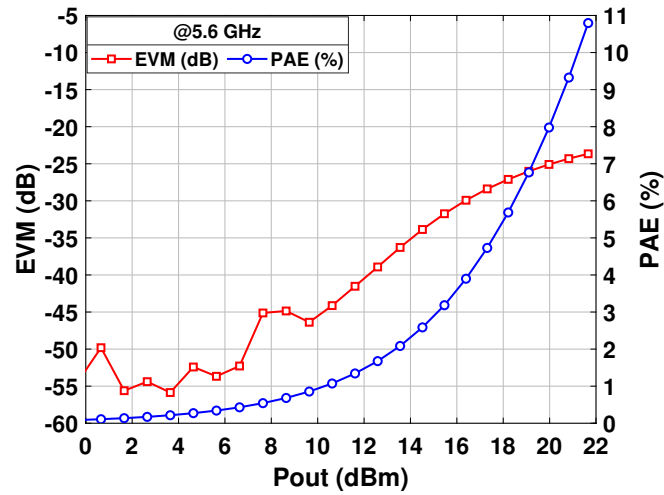


Fig. 9. Measured EVM and PAE vs. output power with 20 MHz-MCS11.

reports a comparison with the state of the art of similar realizations. Notably, this DPA shows the highest efficiency at saturation with a comparable linearity performance.

## V. CONCLUSION

This paper has presented the design process and experimental characterization of a DPA for Wi-Fi 6 communication systems in GaAs HBT technology. The fabricated MMIC achieves 32 dBm of output power with 22.5 dB of gain in the 5-6.2 GHz frequency band with a peak of 44 % of PAE. Linearity measurements with 20 MHz MCS11 standard show a maximum EVM of -24 dB with an output power of 22 dBm and PAE close to 11 % at 5.6 GHz.

## REFERENCES

- [1] A. S. George and A. George, "A review of wi-fi 6 : The revolution of 6th generation wi-fi technology," vol. 10, pp. 56-65, Oct. 2020. DOI: 10.5281/zenodo.7024625.

Table 1. Comparison with SoA

Reference	[3]	[4]	[5]	[6]	This work	
Architecture	Diff. class F	PA class AB	Diff. class AB	Doherty	Doherty	
Technology	GaAs HBT	GaAs HBT	GaAs HBT	55 nm CMOS	GaAs HBT	
Supply (V)	5	5	5.5	5.5	5	
Freq. (GHz)	5.15-6.425	2.4	5.15-7.125	5.8	5-6.2	
Pout (dBm) @Sat	29*	27.2	33	27.2	32	
PAE (%) @SAT	27*	28	34	24.5	33-44	
PAE (%) @OBO	-	-	-	22* @2.5 dB	20-26 @6 dB	
Gain (dB) @SAT	29*	24*	22*	14*	22.5	
Linearity	Modulation	802.11ax MCS11	802.11ax MCS11	802.11ax MCS11	80 MSym/s 256-QAM	802.11ax MCS11
	Pout (dBm)	20/22	16.8/18.4	19.8	17	10
	PAE (%)	9.3/13.8	5.8/8.1	4.3	5.3	1
	EVM (dB)	-40/-35	-35/-32	-40	-34.5	-45

\*Value extrapolated from graphs

- [2] S. Maas, "Ballasting hbt's for wireless power amplifier operation," in *2006 International Workshop on Integrated Nonlinear Microwave and Millimeter-Wave Circuits*, 2006, pp. 2-5. DOI: 10.1109/INMMIC.2006.283493.
- [3] J. Li, Z. Zhang, and G. Zhang, "A 5.15-6.425 ghz stagger-tuning neutralized power amplifier using a continuous-mode harmonically tuned network," *IEEE Microwave and Wireless Technology Letters*, vol. 33, no. 2, pp. 173-176, 2023. DOI: 10.1109/LMWC.2022.3168567.
- [4] X. Yang, Z. Leng, L. Chen, Z. Ge, J. Zhou, and F. Sun, "A fully integrated gaas hbt power amplifier for wlan 802.11ax applications," *Microwave and Optical Technology Letters*, vol. 66, no. 10, e70000, 2024. DOI: <https://doi.org/10.1002/mop.70000>. eprint: <https://onlinelibrary.wiley.com/doi/pdf/10.1002/mop.70000>. [Online]. Available: <https://onlinelibrary.wiley.com/doi/abs/10.1002/mop.70000>.
- [5] S. Hwang, J. Jeon, S. Bae, B. Yoon, S. Kang, and J. Kim, "A 5.15-7.125-ghz differential power amplifier with enhanced linearity of average power region using dynamic cross-coupled capacitor," *IEEE Transactions on Microwave Theory and Techniques*, vol. 72, no. 1, pp. 575-588, 2024. DOI: 10.1109/TMTT.2023.3323045.
- [6] D. Jung, H. Zhao, and H. Wang, "A cmos highly linear doherty power amplifier with multigated transistors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 5, pp. 1883-1891, 2019. DOI: 10.1109/TMTT.2019.2899596.