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19 June 2026

Reducing CM Conducted EMI in Output Filterless WBG Traction Inverters by Means of a Dummy Leg

Erica Raviola, *Member, IEEE*, Franco Fiori, *Member, IEEE*

***Abstract*—The design of traction inverters for electric vehicles poses several challenges, particularly in reducing Common Mode (CM) conducted Electromagnetic Interference (EMI) without the use of bulky input filters. This paper proposes a novel approach based on a small dummy leg, which acts as a source of canceling switching noise. By connecting the dummy leg to the motor chassis through a given impedance, CM current cancellation is achieved when active zero state modulations are employed. To this purpose, the design procedure for the impedance loading the dummy leg is proposed, together with an optimized control method of the dummy leg. Experimental results validate the effectiveness of this approach in a real-case scenario, achieving up to $30\,\mathrm{dB}$ reduction in the $150\,\mathrm{kHz}$-$1\,\mathrm{MHz}$ range, thus reducing the input filter volume and overall system cost compared to conventional solutions.**

***Index Terms*—Conducted electromagnetic interference, electromagnetic compatibility, three-phase four-leg inverter, traction inverter, dummy leg, active zero state PWM.**

I. Introduction

Integrated Motor Drives (IMDs), in which traction inverter and motor share the same housing and are connected using short busbars, are the standard in powertrains for electric vehicles. In such systems, traction motors typically feature nominal ratings in the 100–500 kW range, corresponding to phase peak currents of 100s A. A critical aspect when designing such IMDs is the conducted Common Mode (CM) Electro Magnetic Interference (EMI) they deliver. As far as two-level IMDs like that in Fig. 1 are concerned, the primary source of CM EMI is the Common Mode Voltage (CMV) at the inverter output, which results from the switching of legs between the high-voltage DC rails. Since no output filters are employed in IMDs, due to the large phase currents and short interconnections, the same CMV appears at the motor terminals. Variations of CMV results in a CM current to flow through the CM loop comprising the Artificial Networks (ANs), the inverter and the motor (see Fig. 1) [1]. As high dv/dt can be achieved using SiC and GaN power transistors, conducted EMI in the LF range, i.e., from $150\,\mathrm{kHz}$ up to a few MHz are expected to increase. To keep LF CM EMI within the strict limits imposed by standards, such as [2], bulky one-turn CM chokes are placed around the DC input busbars [3]. However, these chokes are typically the largest components in passive EMI filters, result in filters occupying up to a third of the inverter volume [4].

Several solutions have been proposed in the literature to reduce CM conducted EMI in motor drive systems. Active EMI Filters (AEFs) have been extensively investigated [5], but these have been tested with Low Voltage (LV) supplies [6], [7], employed wire-wound chokes [8], or have not been tested using a traction motor [3]. Additionally, AEFs at the inverter output have been proposed, but these solutions either require the motor chassis not to be ground connected [9], or rely on wound CM chokes for a consistent CM EMI reduction [10]. To the authors knowledge, none of the AEFs proposed thus far is suitable for a direct implementation in traction inverters.

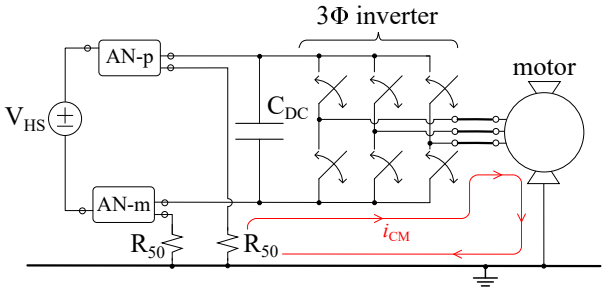

Fig. 1. Common mode current loop in a motor drive system, in which the motor is placed close to the inverter.

Beyond filtering, CM EMI can be reduced at the source. Various strategies have been proposed to this purpose, ranging from active gate drivers [11], [12] to spread-spectrum frequency modulation. Although the latter is widely employed in DC-DC converters, it has been found to provide limited EMI reduction when applied to traction inverters [13]. As far as three-phase motor drives are concerned, Active Zero State Pulse Width Modulations (AZSPWMs) can lower the CMV amplitude by one third [14], while multi-level inverters can, in principle, achieve zero CMV [15]. However, their high cost prevents them from being adopted in commercial IMDs [16]. The Delay Compensation Technique (DCT) proposed in [17], [18] reduces low-frequency CM EMI by finely aligning the commutation of opposite legs, but it was verified on LV motor drives only. Recently, [19] explored the use of DCT on HV SiC legs, but only simulation results were provided.

The CMV in motor drive systems can ideally be eliminated using a three-phase four-leg inverter, in which an additional leg is included to achieve zero CMV at the inverter output. Such a topology was first proposed in [20], later employed in [21] for CMV reduction, voltage boosting during sags, and increased reliability, and more recently combined with sigma-delta modulations to meet conducted EMI military standards [22], [23]. In all these works, an LC filter is placed between the inverter and the motor. As the motor CMV results from the combined contribution of all inverter leg voltages, the output

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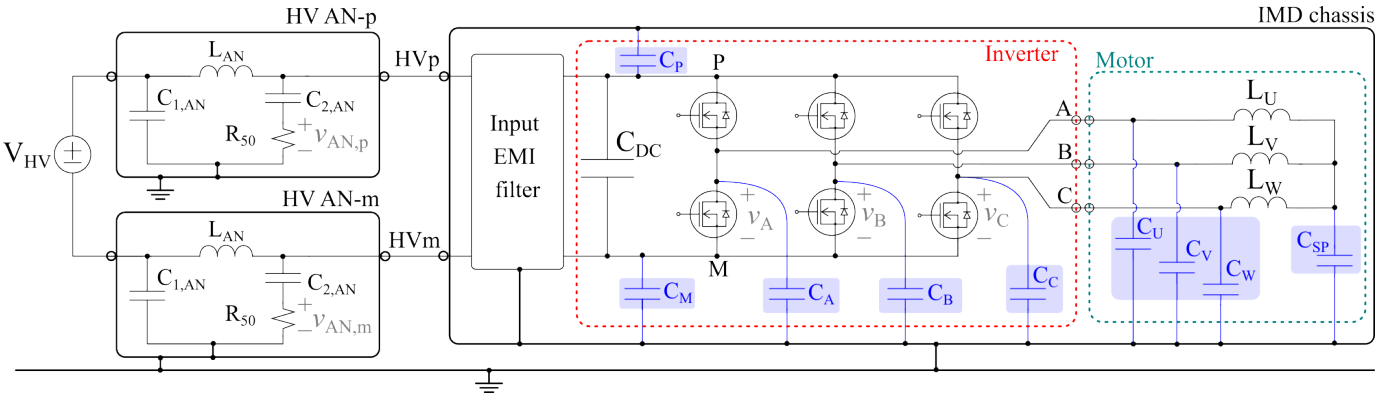

Fig. 2. Setup for the conducted EMI measurement with an Integrated Motor Drive (IMD) as equipment under test. Such an IMD comprises the input EMI filter, the DC link, the inverter itself and the motor in the same housing. Parasitic capacitances related to CM conducted EMI are enclosed in a box.

filter ensures that all legs, including the additional one, exhibit identical transfer functions for frequencies above the filter cut-off, thus contributing equally to the CMV. In such a way, the neutral voltage of the motor is kept constant [20]. Moreover, within the regulated conducted-EMI frequency range, the filter inductors increase the impedance of the common-mode loop (see Fig. 1), providing additional CM filtering at the AC side. However, due to the presence of the output filter, the practical applicability of four-leg inverters to high-current traction systems remains limited.

This work addresses the LF CM conducted EMI reduction in two-level voltage source traction inverters based on the four-leg topology, without the need for output filters. Unlike conventional approaches, the fourth leg here is directly connected to the chassis through a defined impedance to cancel CM currents directly at the source. This eliminates the need for both output filters and access to the load neutral point, thus extending four-leg three-phase inverters for CM EMI reduction to high-current traction systems. The analytical derivation and design of the required impedance are presented, along with a novel control strategy based on AZSPWM-1 and AZSPWM-3 schemes. Experimental results validate the effectiveness of the proposed technique in reducing conducted EMI, achieving an improved trade-off between filter volume and cost compared to traditional solutions.

The paper is organized as follows. Sect. II discusses the CM conducted EMI delivered by an IMD. The proposed three-phase four-leg inverter is introduced in Sect. III, with the dummy leg control strategy discussed in Sect. IV. The case study and measurement results are reported in Sect. V, and the comparison with traditional solutions presented in Sect. VI. Concluding remarks are in Sect. VII.

II. CM Conducted EMI delivered by an Integrated Motor Drive

The conducted EMI delivered by an IMD can be discussed referring to the circuit shown in Fig. 2. The motor drive system includes a passive input EMI filter, a DC link, an inverter and an electrical machine. To evaluate conducted EMI, the High Voltage (HV) DC supply V_{HV} is provided through two HV Artificial Networks (HV-ANs), as prescribed by the CISPR-25 standard [2]. A two-level three-phase inverter is considered, as those exploited in commercial EV traction drives. It is directly supplied by the DC link, which is simplified by C_{DC} in Fig. 2, and it comprises legs A, B and C. Regarding the electrical machine, a Permanent Magnet Synchronous Motor (PMSM) is typically employed. This motor is shown in Fig. 2 as three star-connected inductances ($L_{\mathrm{U-W}}$), which represent the low-frequency winding inductance. According to the voltage method, CM conducted EMI is defined as

$$v_{\mathrm{AN,CM}} \hat{=} \frac{v_{\mathrm{AN,p}} + v_{\mathrm{AN,m}}}{2}. \tag{1}$$

The parasitic components responsible for CM conducted EMI are enclosed in a boxed area in Fig. 2 for clarity. These include capacitances $C_{\mathrm{P,M}}$, which model the parasitic coupling between the HV DC bars and the ground-connected chassis, and $C_{\mathrm{A,B,C}}$, representing the coupling between the exposed tabs of power transistors and the inverter housing. These capacitances typically range from 10 to 100 pF [24]. Regarding the electric motor, the coupling between the stator windings and the slots is represented by CM parasitic capacitances C_{U-W} (C_{SC}). Using a Π model, these capacitances are connected between the motor terminals (star-center node) and ground. Previous research suggested that the overall CM capacitance of traction motors ranges from 4 to 8 nF [25]. Therefore, CM conducted EMI at low frequencies are primarily related to the current flowing through $C_{\mathrm{U-W,SC}}$. This CM current (i_{CM}) is directly related to the dv/dt of the inverter output voltages ($v_{\mathrm{A-C}}$).

An equivalent model for analyzing the Low-Frequency (LF) CM EMI is shown in Fig. 3. The HV ANs have been substituted by their CM impedance ($Z_{\mathrm{AN,CM}}$), and the CM impedance of the electrical machine ($Z_{\mathrm{EM,CM}}$) has been approximated by $C_{\mathrm{N}} = C_{\mathrm{U}} + C_{\mathrm{V}} + C_{\mathrm{W}} + C_{\mathrm{SC}}$. Such an approximation is reasonable in case of PMSMs in hairpin technology [26] as the value of $L_{\mathrm{U-W}}$ is typically in the order of tens of µH, meaning that $Z_{\mathrm{EM,CM}}$ is mainly capacitive up to frequencies of around 1 MHz for motor of this type [25]. Moreover, the impact of interconnections between the inverter and the motor is negligible at LF. The source of CM EMI is identified as the CMV at the motor terminals, i.e.,

$$v_{\mathrm{CM}}(t) = \frac{v_{\mathrm{A}}(t) + v_{\mathrm{B}}(t) + v_{\mathrm{C}}(t)}{3} - \frac{V_{\mathrm{HV}}}{2}. \tag{2}$$

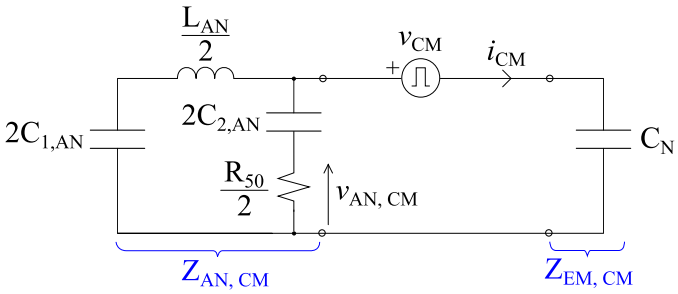

Fig. 3. Equivalent model of the circuit shown in Fig. 2 for analyzing the CM conducted EMI in the low frequency regulated range.

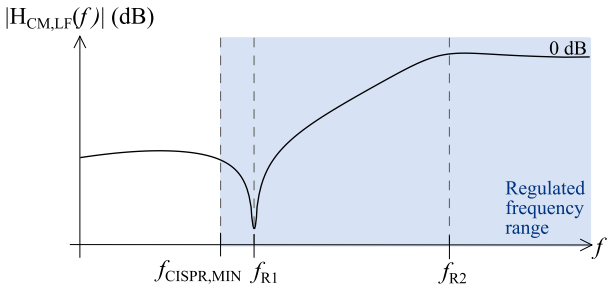

Fig. 4. Magnitude of the CM transfer function obtained from the simplified model shown in Fig. 3 in the low frequency range.

Referring to the model in Fig. 3 and recalling (1), the CM EMI can be expressed in the Laplace domain as

$$V_{\mathrm{AN,CM}}(s) = H_{\mathrm{CM,LF}}(s) V_{\mathrm{CM}}(s), \tag{3}$$

meaning that the CM EMI deals with the transfer function ($H_{\mathrm{CM,LF}}$) and the CMV frequency spectra. As far as the former is concerned, $H_{\mathrm{CM,LF}}$ is equal to

$$H_{\mathrm{CM,LF}}(s) = \frac{R_{50} C_{2,\mathrm{AN}} s}{1 + R_{50} C_{2,\mathrm{AN}} s} \cdot \frac{Z_{\mathrm{AN,CM}}}{(Z_{\mathrm{AN,CM}} + Z_{\mathrm{EM,CM}})}. \tag{4}$$

Denoting with $C_{\mathrm{AN}} = C_{1-2,\mathrm{AN}}$, (4) can be approximated as

$$H_{\mathrm{CM,LF}}(s) \approx \frac{\frac{R_{50}}{2} C_{\mathrm{N}} s (1 + C_{\mathrm{AN}} L_{\mathrm{AN}} s^2)}{R_{50} C_{\mathrm{AN}} s \left(C_{\mathrm{N}} \frac{L_{\mathrm{AN}}}{2} s^2 + \frac{L_{\mathrm{AN}}}{R_{50}} s + 1 \right) + 2}, \tag{5}$$

provided that $C_{\mathrm{N}} << 2C_{\mathrm{AN}}$. The magnitude of this transfer function is plotted in Fig. 4. For frequencies in the regulated range, i.e., above $f_{\mathrm{CISPR,MIN}}$=150 kHz, $|H_{\mathrm{CM,LF}}|$ exhibits a second-order high-pass behavior above $f_{\mathrm{R1}} = (2\pi\sqrt{C_{\mathrm{AN}} L_{\mathrm{AN}}})^{-1}$ =225 kHz given the nominal values of HV AN components (C_{AN}=100 nF and L_{AN}=5 µH). For frequencies above $f_{\mathrm{R2}} = (2\pi\sqrt{C_{\mathrm{N}} L_{\mathrm{AN}}})^{-1}$, the magnitude remains constant at 0 dB. Regarding the CMV frequency spectra, its LF content is primarily determined by the inverter switching frequency (f_{SW}) and modulation scheme. As far as Space Vector Modulation (SVM) is concerned, the CMV waveform is as that shown in Fig. 5. The period of v_{CM} is the PWM period, i.e., $1/f_{\mathrm{SW}}$, with v_{CM} changing by $V_{\mathrm{HV}}/3$ each time one of the three legs switches. A common mode current flows through C_{N} at each commutation. The frequency spectrum of an SVM-modulated CMV is bounded to that of a trapezoidal waveform with a 0.5 duty cycle [1]. Thus, the envelope of the CMV spectra is characterized by -20 dB/dec slope in the low-frequency range, which multiplied by the transfer function plotted in Fig. 4, results in CM EMI hardly attenuated in the range (150 kHz, 225 kHz). The LF CM EMI are further worsened by the increase in switching frequency when employing Wide Band Gap (WBG) power transistors, as their low switching losses enables higher f_{SW}. As a consequence, the amplitude of the first harmonics above $f_{\mathrm{CISPR,MIN}}$ is expected to increase. To sum up, LF CM EMI components pose a challenge in WBG traction inverters.

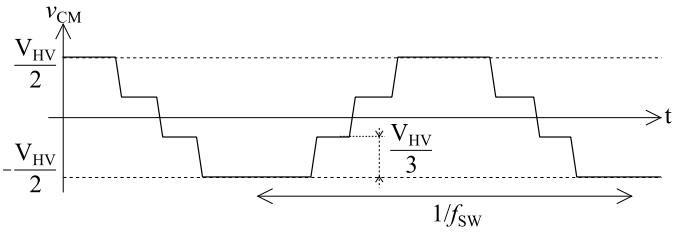

Fig. 5. Common mode voltage with SVM.

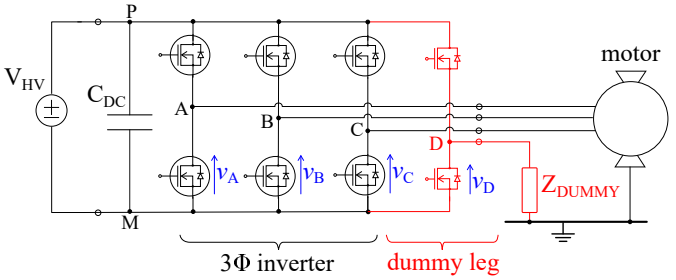

Fig. 6. Three-phase four-leg inverter with the dummy leg connected to ground through the proposed Z_{DUMMY}.

III. Proposed Three-Phase Four-Leg Inverter

Recalling (3), reduction techniques effective at the source aim to shape the CMV spectra to lower the resulting CM EMI. In case of motor drives, one could ideally achieve zero CMV by employing a three-phase four-leg inverter. In this configuration, two legs are always tied to the positive supply rail and the other two to the negative one. This requires that every time a leg switches, another must switch opposite.

To take advantage of ideally-zero CMV in four-leg topology to reduce LF CM EMI, this study investigates the connection of the fourth leg to the IMD chassis, as shown in Fig. 6. In this configuration, legs A to C remains directly connected to drive the electrical machine, as shown in Fig. 2. The fourth leg, also referred to as the dummy leg, is connected to impedance Z_{DUMMY} to the reference ground. Such an impedance is needed to load the dummy leg similarly to how the legs A-C are loaded toward ground. The remainder of this Sect. discusses the Z_{DUMMY} value and its implementation.

A. Derivation of Z_{DUMMY}

To achieve LF CM EMI reduction, the impedance Z_{DUMMY} must be carefully chosen to ensure that the CM current resulting from the commutation of a main leg is canceled out by that flowing in the dummy leg. To this purpose, the case

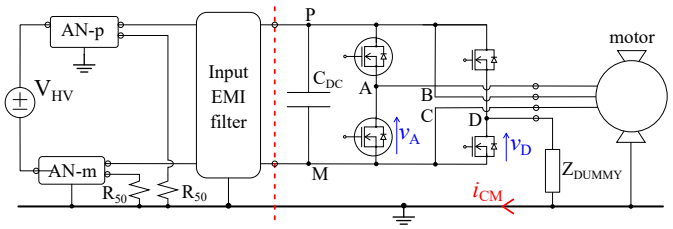

Fig. 7. Equivalent circuit of the inverter shown in Fig. 6 when the dummy leg switches complementarily to leg A. Leg B and C are either connected to nodes P or M.

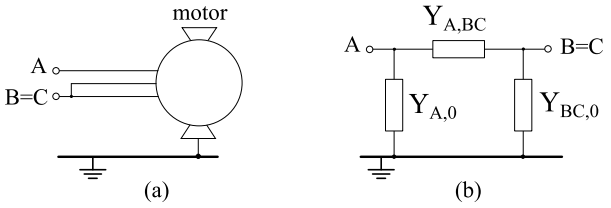

Fig. 8. In (a), the two-port motor. In (b), the corresponding Π-equivalent model in terms of shunt ($Y_{\mathrm{A},0}, Y_{\mathrm{BC},0}$) and series ($Y_{\mathrm{A,BC}}$) admittances.

where leg A and leg D switch complementarily is considered. In this scenario, the output of leg B is tied to node P, and that of leg C to node M. This ensures that, even after the commutation of legs A and D, there are always two legs high and two legs low. This simplifies the circuit shown in Fig. 6 to the model in Fig. 7. The results from this case can also be applied to the commutations of legs B and C.

To analyze the CM EMI generated by the complementary commutation of legs A and D, the differential mode component is neglected, meaning that nodes P, M, B and C are assumed to be tied together. As far as the motor is concerned, terminals B and C are short-circuited, as shown in Fig. 8(a). By considering the ground-connected chassis as reference terminal, the motor can be fully represented by a passive two port network, resulting in the Π-equivalent model shown in Fig. 8(b). Such a Π model comprises two shunt ($Y_{\mathrm{A},0}, Y_{\mathrm{BC},0}$) and a series admittance ($Y_{\mathrm{A,BC}}$). Notably, this approach enhances the generality to the proposed method, as it remains independent from the specific lumped-element model adopted for the motor.

The circuit shown in Fig. 7 can be further simplified in the model in Fig. 9. Here, the motor is represented by its two-port Π-equivalent (see Fig. 8(b)), and legs A and D by ideal voltage sources v_{A} and v_{D}. Concerning the DC side of the inverter, all elements on the left of the dotted line in Fig. 7 can be modeled by an equivalent CM admittance $Y_{\mathrm{DC,CM}}$ connected between nodes P-M and ground. In such a way, with the input EMI filter not placed, $Y_{\mathrm{DC,CM}} = (Z_{\mathrm{AN,CM}})^{-1}$ (see Fig. 3). Conversely, with the filter present, $Y_{\mathrm{DC,CM}}$ includes its effect, regardless of the specific filter topology. By applying the superposition principle to the model in Fig. 9(a), the current flowing in the CM loop i_{CM} can be expressed as

$$i_{\mathrm{CM}} = i'_{\mathrm{CM}} + i''_{\mathrm{CM}}, \tag{6}$$

where i'_{CM} (i''_{CM}) is that obtained by zeroing v_{D} (v_{A}). Based on the simplified circuits shown in Fig. 9(b) and (c), these two

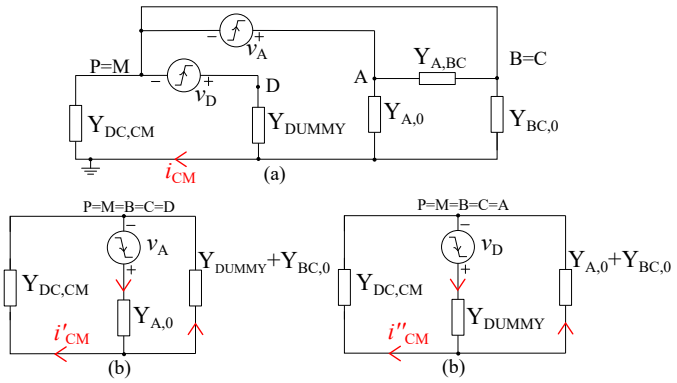

Fig. 9. In (a), simplified model of the circuit shown in Fig. 7. The equivalent circuits for evaluating (7) and (8 are shown in (b) and (c), respectively.

contributions results in

$$i'_{\mathrm{CM}} = Y_{\mathrm{DC,CM}} \frac{(Y_{\mathrm{DC,CM}} + Y_{\mathrm{BC},0} + Y_{\mathrm{DUMMY}}) \oplus Y_{\mathrm{A},0}}{Y_{\mathrm{DC,CM}} + Y_{\mathrm{BC},0} + Y_{\mathrm{DUMMY}}} v_{\mathrm{A}} \tag{7}$$

and

$$i''_{\mathrm{CM}} = Y_{\mathrm{DC,CM}} \frac{(Y_{\mathrm{DC,CM}} + Y_{\mathrm{BC},0} + Y_{\mathrm{A},0}) \oplus Y_{\mathrm{DUMMY}}}{Y_{\mathrm{DC,CM}} + Y_{\mathrm{BC},0} + Y_{\mathrm{A},0}} v_{\mathrm{D}}, \tag{8}$$

where the $\oplus$ operator denotes $Y_1 \oplus Y_2 = Y_1 Y_2/(Y_1 + Y_2)$.

Since the dummy leg should cancel the current injected by leg A at the AC-side ground, from (7) and (8) it must be $v_{\mathrm{A}} = -v_{\mathrm{D}}$ and, by inspection, Y_{DUMMY} should be equal to $Y_{\mathrm{A},0}$. As $Y_{\mathrm{A},0}$ equals one-third of the CM motor admittance, i.e., that measured between terminals A,B,C short-circuited and the chassis (see Fig. 8), the impedance loading the dummy leg should be three times the CM motor impedance ($Z_{\mathrm{EM,CM}}$), yielding

$$Z_{\mathrm{DUMMY}} = Z_{\mathrm{A},0} = 3Z_{\mathrm{EM,CM}}. \tag{9}$$

Such a result is valid provided that the dominant CM impedance on the AC side of the inverter is $Z_{\mathrm{EM,CM}}$, meaning that $C_{\mathrm{A,B,C}}$ shown in Fig. 2 and motor cables can be neglected. From what discussed in Sect. II, this assumption is reasonable up to a few MHz. Although the CM current depends on $Y_{\mathrm{DC,CM}}$, Z_{DUMMY} does not. This is because all elements on the DC side of the inverter affect the CM current injected by the four legs into the AC-side ground in the same manner.

B. Impedance matching

To achieve (9), the first step is to measure the CM impedance of the motor using an impedance or network analyzer in the frequency range of interest, i.e., up to a few MHz. This measurement is performed by disconnecting the motor from the inverter, short-circuiting its terminals, and measuring the impedance between them and the motor chassis. In the experimental validation reported in Sect. V, a 100 kW PMSM designed specifically for automotive traction in hairpin technology [25] is exploited as test case. The measured CM impedance, scaled by a factor of three, is shown in Fig. 10 by solid line in terms of magnitude (at the top) and phase (at the bottom). Such an impedance can be approximated by a 2.2 nF

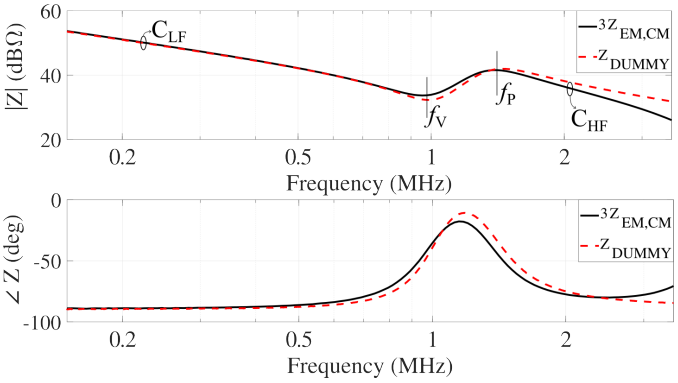

Fig. 10. Measured CM impedance of the electrical machine multiplied by a factor three (solid line) and the synthesized impedance (dashed line).

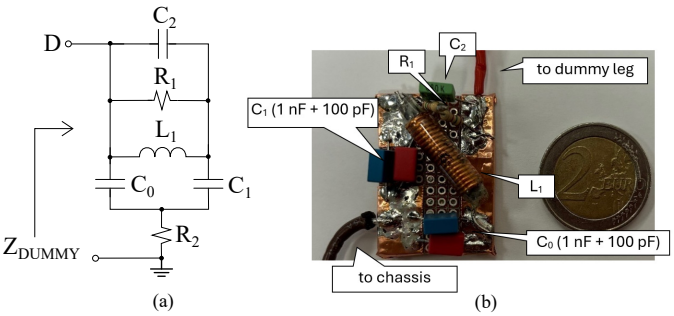

Fig. 11. In (a), the passive network exploited to synthesize $Z_{\mathrm{DUMMY}} = 3Z_{\mathrm{EM,CM}}$, in (b), a photograph of the synthesized dummy leg.

capacitance for frequencies up to 700 kHz. This value is one third of the overall low-frequency CM capacitance C_{N} shown in Fig. 2. The measured impedance exhibits a series and a parallel resonance at f_{V}=955 kHz and f_{P}=1.4 MHz. The CM impedance shown in Fig. 10 aligns well with findings from previous studies [25], allowing the following considerations to be applied to motors different from the one considered.

To synthesize such an impedance in the considered frequency range, the network shown in Fig. 11(a) was exploited. Alternative network topologies, derived from slight modifications of the selected configuration and featuring comparable complexity and component count, can also be employed. The analytical expression of the considered impedance in the Laplace domain, with $C_0 = C_1$, is

$$Z_{\mathrm{DUMMY}} = \frac{(C_0+C_2)L_1 s^2 + \frac{L_1}{R_1}s + 1}{2C_0 s\left((C_2+\frac{C_0}{2})L_1 s^2 + \frac{L_1}{R_1}s + 1\right)} + R_2. \quad (10)$$

It is characterized by a double resonance, as that measured experimentally, with the frequencies of the peak (f_{P}) and of the valley (f_{V}) equal to

$$f_{\mathrm{V}} = \frac{1}{2\pi\sqrt{L_1(C_0+C_2)}}, \quad f_{\mathrm{P}} = \frac{1}{2\pi\sqrt{L_1(\frac{C_0}{2}+C_2)}}. \quad (11)$$

The values of the equivalent capacitance for frequencies much lower than f_{V} (C_{LF}) and much higher than f_{P} (C_{LF}) can be obtained by direct inspection of the circuit shown in Fig. 11(a), resulting in

$$C_{\mathrm{LF}} = 2C_0, \quad C_{\mathrm{HF}} = C_0 + (C_0 \oplus C_2). \quad (12)$$

Solving for C_0 and C_2 yields

$$C_0 = \frac{C_{\mathrm{LF}}}{2}, \quad C_2 = \frac{C_0^2 - C_0 C_{\mathrm{HF}}}{C_{\mathrm{HF}} - 2C_0}. \quad (13)$$

With C_0 and C_2 known, the value of the L_1 inductance can be obtained (11). The value of the damping resistance R_1 can be derived from $|3Z_{\mathrm{EM,CM}}|$ at f_{P}. Finally, resistance R_2 have been included to damp the unwanted the HF resonance of C_{HF} with the parasitic inductance of interconnections. Its value should be chosen sufficiently small not to affect Z_{DUMMY} for frequencies lower than f_{P}.

Following the proposed matching procedure for the test case, the resulting component values are reported in Table I. This impedance was then assembled and measured to compare it against the target impedance, i.e., $3Z_{\mathrm{EM,CM}}$. A photograph of the network emulating Z_{DUMMY} is shown in Fig. 11(b), with the main components labeled. Plastic capacitors were employed for C_{0-2}, and an unshielded RF inductor wound on a ferrite core was used for L_1. As only the CM current injected/sunk by the dummy leg flows through Z_{DUMMY}, the passive components here used are not subject to high current stress, and their primary design constraint is the voltage rating. The Z_{DUMMY} impedance is shown in Fig. 10 by dashed lines. Solid and dashed curves are in good agreement. Although the accuracy between Z_{DUMMY} and $3Z_{\mathrm{EM,CM}}$ can be improved by increasing the model's order, this would also raise the complexity of the passive network in Fig. 11(a), with only marginal benefits in the frequency range of interest. It is worth noting that the proposed matching procedure is based solely on the motor CM impedance, as this represents the main CM current path in the low frequency range of regulated conducted EMI. Thus, the same approach can be applied to motor other the one used in the experimental validation, resulting in passive component values different from those reported in Table I. Moreover, with V_{HV}=400 V, the energy stored by Z_{DUMMY} can be approximated as $E_{\mathrm{Z}} = 0.5 C_{\mathrm{LF}} V_{\mathrm{HV}}^2 \approx 0.3$ mJ, which is significantly lower than the typical limit of 0.2 J imposed for Y-capacitors [**?**].

TABLE I
NOMINAL VALUES OF THE DUMMY IMPEDANCE

Parameter	Value	Parameter	Value
C_0	1.1 nF	C_1	1.1 nF
C_2	680 pF	L_1	12 µH
R_1	150 Ω	R_2	4 Ω

IV. Design of the Dummy Leg and Control Strategy

With the impedance of the dummy leg defined to cancel the CM current, the control algorithm of the motor drive system shown in Fig. 6 should be modified to include the control signal of the dummy leg. In traditional SVM, the binary

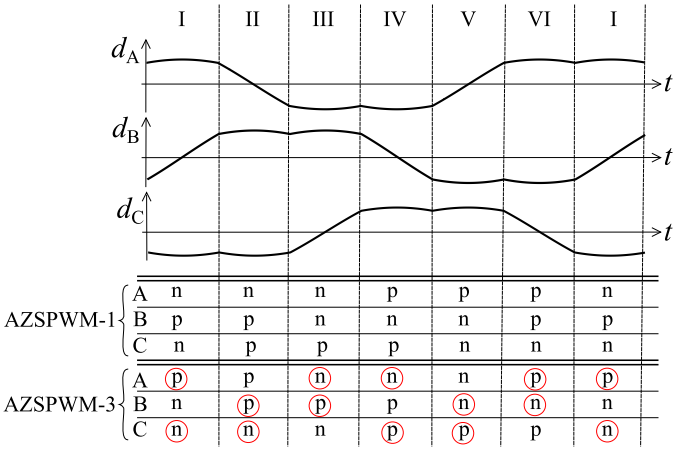

Fig. 12. Reference signals of the three legs over a modulation period at the top. The three of them are shifted by 120°. At the bottom, it is reported whether a positive ('p') or a negative ('n') triangular waveform is exploited to generate the A-C control signals according to AZSPWM-1 and AZSPWM-3 schemes.

control signals of the three main legs ($S_{\mathrm{A-C}}$) are generated from three reference signals ($d_{\mathrm{A-C}}(t)$), which are shown at the top of Fig. 12 for the six sectors. Those signals are derived from three sinusoidal waveforms with frequency f_{LOAD}, each shifted by 120°, which are fed to a pulse centering unit [27]. The control signals $S_{\mathrm{A-C}}$ are obtained by comparing the $d_{\mathrm{A-C}}$ with a triangular waveform with f_{SW} frequency. By convention, S_{i} is high (low) when the high-side (low-side) transistor of the corresponding leg is on. However, SVM can not be applied to a three-phase four-leg inverter because it exploits zero vectors, i.e., '000' and '111'. Amongst the modulations which can be adopted with the fourth leg, Active Zero State PWMs (AZSPWMs) were investigated as they do not affect the linearity range and the efficiency of inverter [28]. This Sect. briefly reviews AZSPWM modulations and proposes two optimized algorithm for the dummy leg. Hardware design guidelines regarding the dummy leg are provided at the end.

A. AZSPWM modulations

When AZSPWM modulations are employed, the control signals of legs A, B and C can obtained by comparing the reference signals $d_{\mathrm{A-C}}(t)$ with either a positive or a negative triangular waveform [14]. AZSPWM-1 and AZSPWM-3 will be considered in the following discussion as they are exploited in the experimental validation. The scheme is reported at the bottom of Fig. 12, with either a 'p' or an 'n' indicating that a positive or a negative triangular waveform is used for a given leg in a specific sector.

To gain a better understanding of AZ modulations, reference and control signals in sector I are shown in Figs. 13(a) and (b) for AZSPWM-1 and AZSPWM-3, respectively. In this sector, d_{A} (d_{C}) is approximately constant at its maximum (minimum) value, and d_{B} varies from minimum to maximum. Over a single switching period ($T_{\mathrm{SW}} = 1/f_{\mathrm{SW}}$), $d_{\mathrm{A-C}}$ are approximately constant, and they are compared against either a positive (solid) or negative (dashed) triangular waveform.

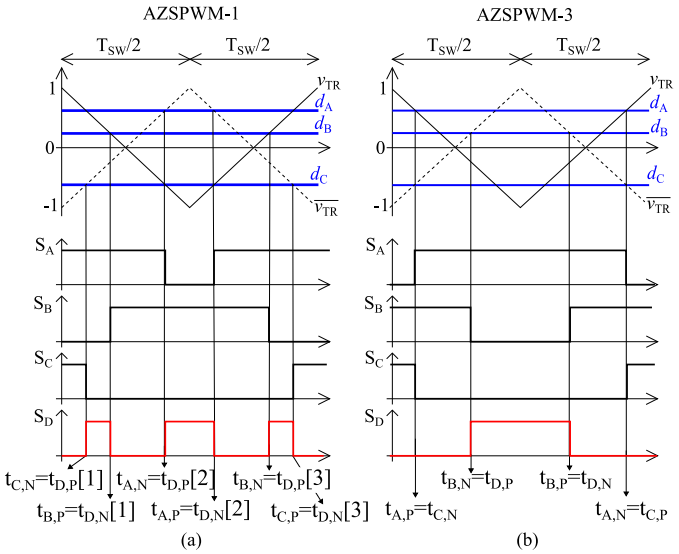

Fig. 13. Reference signals $d_{\mathrm{A-C}}$ with positive (solid) and negative (dashed) triangular waveform at the top for sector I. The resulting control signals are in the middle, and the resulting CMV is shown at the bottom for AZSPWM-1 (on the left) and AZSPWM-3 (on the right).

TABLE II
SWITCHING STATE FOR AZSPWM-1 AND AZSPWM-3.

	Leg	AZSPWM-1	AZSPWM-3		Leg	AZSPWM-1	AZSPWM-3
I	A	1-1-1-0-1-1-1	0-1-1-1-0	IV	A	0-0-0-1-0-0-0	1-0-0-0-1
	B	0-0-1-1-1-0-0	1-1-0-1-1		B	1-1-0-0-0-1-1	0-0-1-0-0
	C	1-0-0-0-0-0-1	1-0-0-0-1		C	0-1-1-1-1-1-0	0-1-1-1-0
	D	0-1-0-1-0-1-0	0-0-1-0-0		D	1-0-1-0-1-0-1	1-1-0-1-1
II	A	1-1-0-0-0-1-1	0-0-1-0-0	V	A	0-0-1-1-1-0-0	1-1-0-1-1
	B	0-1-1-1-1-1-0	0-1-1-1-0		B	1-0-0-0-0-0-1	1-0-0-0-1
	C	0-0-0-1-0-0-0	1-0-0-0-1		C	1-1-1-0-1-1-1	0-1-1-1-0
	D	1-0-1-0-1-0-1	1-1-0-1-1		D	0-1-0-1-0-1-0	0-0-1-0-0
III	A	1-0-0-0-0-0-1	1-0-0-0-1	VI	A	0-1-1-1-1-1-0	0-1-1-1-0
	B	1-1-1-0-1-1-1	0-1-1-1-0		B	0-0-0-1-0-0-0	1-0-0-0-1
	C	0-0-1-1-1-0-0	1-1-0-1-1		C	1-1-0-0-0-1-1	0-0-1-0-0
	D	0-1-0-1-0-1-0	0-0-1-0-0		D	1-0-1-0-1-0-1	1-1-0-1-1

The resulting leg control signals are reported below. The time instants in which the control signals vary from low to high (high to low) are hereinafter denoted with a P (N) subscript. With AZSPWM-1, each leg commutation corresponds to a CMV commutation. In contrast, AZSPWM-3 pairs legs with minimum and maximum d, one associated with a positive and one with a negative triangular waveform, resulting in a CMV cancellation between two legs and only two CMV commutations per period.

B. Control algorithms for the dummy leg

As far as the fourth leg is concerned, it should switch to ensure that, at every time, two out of four legs are driven high, and the remaining two are driven low. In such a way, the CMV is zeroed. Thus, the control signal of the fourth leg (S_{D}) can be expressed as [21]

$$S_{\mathrm{D}} = S_{\mathrm{A}} \ \mathtt{xor} \ S_{\mathrm{B}} \ \mathtt{xor} \ S_{\mathrm{C}}. \tag{14}$$

Referring to Fig. 13, (14) can be declined in case of AZSPWM-1 and AZSPWM-3 as follows. For AZSPWM-1, the dummy leg should commutate every time one of the main

TABLE III
LUT FOR DUMMY LEG CONTROL WHEN EMPLOYING AZSPWM-1

$t_{\mathrm{D,P}}[1] \leftarrow t_{\mathrm{A,N}}$	$t_{\mathrm{D,P}}[2] \leftarrow t_{\mathrm{B,N}}$	$t_{\mathrm{D,P}}[3] \leftarrow t_{\mathrm{C,N}}$
$t_{\mathrm{D,N}}[1] \leftarrow t_{\mathrm{A,P}}$	$t_{\mathrm{D,N}}[2] \leftarrow t_{\mathrm{B,P}}$	$t_{\mathrm{D,N}}[3] \leftarrow t_{\mathrm{C,P}}$

TABLE IV
LUT FOR DUMMY LEG CONTROL WHEN EMPLOYING AZSPWM-3

Sector	I	II	III	IV	V	VI
$t_{\mathrm{D,P}}$	$t_{\mathrm{B,N}}$	$t_{\mathrm{A,N}}$	$t_{\mathrm{C,N}}$	$t_{\mathrm{B,N}}$	$t_{\mathrm{A,N}}$	$t_{\mathrm{C,N}}$
$t_{\mathrm{D,N}}$	$t_{\mathrm{B,P}}$	$t_{\mathrm{A,P}}$	$t_{\mathrm{C,P}}$	$t_{\mathrm{B,P}}$	$t_{\mathrm{A,P}}$	$t_{\mathrm{C,P}}$

leg switches (see Fig. 13(a) at the bottom). In AZSPWM-3, two of the main legs always switch opposite, meaning that the dummy leg compensates for only one main leg per sector. As the reference vector moves to the subsequent sectors, the main leg requiring compensation changes. The detailed sequence of switching state within a PWM cycle is reported in Tab. II for all six sectors, for both AZSPWM-1 and AZSPWM-3. It can be noticed that zero vectors (0000, 1111) never occurs, and that (14) is always valid.

With the controller of the motor drive system implemented on a Field Programmable Gate Array (FPGA), one could directly implement (14) using the available on-board logic gates. However, most microcontrollers, which are typically used in commercial products, are not provided with this capability, meaning that external logic gates would be required to output S_{D}.

To allow for the direct control of S_{D} on-board the controller, the algorithms proposed below can be adopted. With the time instants related to the commutations of legs A-C ($t_{\mathrm{A-C,P}}$ and $t_{\mathrm{A-C,N}}$) already evaluated by the firmware running on the controller, the time instants for the commutations of the dummy leg can be directly evaluated by means of the Look-Up Tables (LUTs) reported in Tab. III and IV for AZSPWM-1 and AZSPWM-3, respectively. Regarding AZSPWM-1, the dummy leg should switch in a complementary way to the main legs (see Fig. 13(a) at the bottom), meaning that the three low-to-high D time instants ($t_{\mathrm{D,P}}[i]$) are equal to the high-to-low time instants of legs A-C ($t_{\mathrm{A-C,N}}$), and vice versa. This rule applies for all sector. Conversely, when employing AZSPWM-3, the control signal of the dummy leg is dependent on the sector, with the corresponding LUT directly derived from Tab. II. The proposed algorithms allow for the direct control of the dummy leg with no computational overhead, without requiring external logic gates.

C. Hardware design of the dummy leg

With the control algorithm discussed, some design guidelines regarding the dummy leg are provided in what follows. As leg D does only drives Z_{DUMMY}, and not a motor phase inductances $L_{\mathrm{A-C}}$ (see Fig. 2), then its design can be optimized in terms of cost and volume with respect to that of legs A-C. Voltage rating of power transistors included in the dummy leg should be comparable to those of the main legs, as they should withstand the same input supply voltage V_{HV}. As

TABLE V
NOMINAL PARAMETERS OF TEST CASE.

DC link	4 x 40 µF, 4 x 4 x 100 nF
Power transistors for legs A,B,C	117 A, 650 V
Power transistors for leg D	17 A, 1700 V
Estimated $C_{\mathrm{A-D}}$ (see Fig. 2)	25 pF
Switching frequency (f_{SW})	32 kHz
Modulation frequency (f_{LOAD})	500 Hz
Input supply voltage (V_{HV})	96 V
Motor	PMSM in hairpin
Power rating	100 kW
Phase inductance $L_{\mathrm{U,V,W}}$	40 µH
Motor CM capacitance	6.6 nF

the dummy leg only drives Z_{DUMMY}, the peak current flowing in Z_{DUMMY} ($I_{\mathrm{PK,D}}$) can be approximated as

$$I_{\mathrm{PK,D}} \approx C_{\mathrm{LF}} \frac{V_{\mathrm{HV}}}{t_{\mathrm{R/F,D}}}, \tag{15}$$

where C_{LF} is the LF equivalent capacitance (see Fig. 10) and $t_{\mathrm{R/F,D}}$ is the rise/fall times of the v_{D} voltage. Thus, the transistors for the dummy leg should be chosen with a maximum peak current higher than (15), which is much lower than that in the main legs when considering typical traction inverters. Regarding the losses of the dummy leg, the on-resistance of transistors included in the dummy leg is not critical, as conduction losses are zero. Concerning switching losses, they can be approximated as

$$P_{\mathrm{SW,D}} = k f_{\mathrm{SW}} C_{\mathrm{LF}} V_{\mathrm{HV}}^2, \tag{16}$$

with $k = 1$ in case of AZSPWM-3 and $k = 3$ for AZSPWM-1, provided that the output capacitance of dummy leg transistors is negligible compared to C_{LF}. With AZSPWM-1, the dummy legs switches six times over a switching period, compared to two times of AZSPWM-3, as shown in Fig. 13 and reported in Tab. II. To sum up, the design of the dummy leg differs from that of the main leg, as its driving requirements are less stringent. This allows for the use of lower-cost components, both for power transistors and auxiliary circuitry, and for a more compact design thanks to the reduced current capability and less-critical thermal dissipation compared to those of the main legs.

V. EXPERIMENTAL VALIDATION

Aiming to validate the use of the dummy leg connected to Z_{DUMMY}, and to compare the proposed solution against traditional ones, an ad-hoc prototype was designed and assembled. Experimental measurements were then conducted to assess CM EMI reduction achieved by the proposed technique under representative conditions. Measurement results for SVM, AZSPWM-1, and AZSPWM-3 modulations, both with and without employing the dummy leg are discussed in what follows.

A. Case study

The blocks the prototype is comprised of are shown in Fig. 14. These include the microcontroller (μC), high-side and

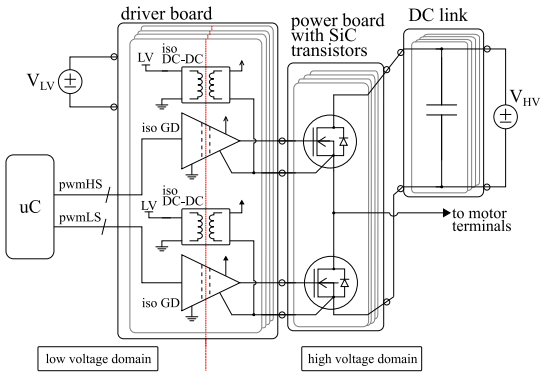

Fig. 14. Block scheme of the modular prototyped inverter, comprising the controller, a driver board, the power board and the DC link. Insulation between the low-voltage domain and the high-voltage domain is guaranteed by isolated gate drivers and power supplies.

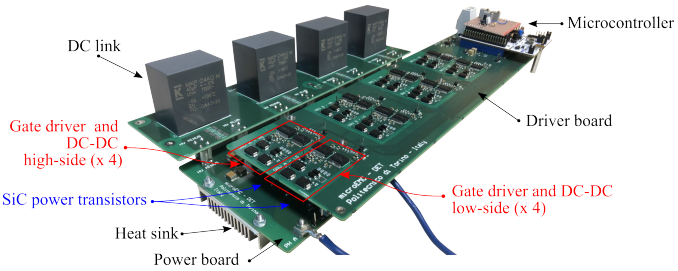

Fig. 15. Photograph of the prototyped traction inverter. The blocks in Fig. 14 have been replicated four times for legs A-D.

low-side isolated gate drivers and their power supplies, four switching legs with SiC power transistors and the DC link. The nominal values of the components are reported in Table V for reference. The microcontroller implements the standard SVM scheme, as well as the AZSPWM-1 and AZSPWM-3. The control signals for the switching legs are output by the PWM of the μC and are denoted with `pwmHS` and `pwmLS` in Fig. 14. The driver board is supplied by V_{LV}=24 V, and a dedicated isolated gate driver is employed for each power transistor in the main legs. This setup ensures galvanic isolation between the inverter (HV domain) and the controller (LV domain), as in a practical traction application. The DC link includes film capacitors as well as ceramic ones placed close to the SiC power switching transistors to minimize its impedance at high frequency. The assembly is shown in Fig. 15, where the main components have been labeled to be found at a glance. Each leg is equipped with a grounded aluminum heat sink, which is screwed on the back and faces the drain terminals of the power transistors for power dissipation. Such a mounting and grounding scheme closely mimic that of an IMD, where the grounded housing is employed as an heat sink. Power transistors of the dummy leg were chosen according to the guidelines in Sect. IV-C. The inverter layout was designed to minimize the switching loop inductance, and all four legs, including the DC link and the gate driver circuitry, have been designed to be identical. This setup allowed the testing of the fourth leg using either the same transistors as those included in the main leg, or smaller devices. This results in a 25 % volume overhead in the prototype, which can be significantly

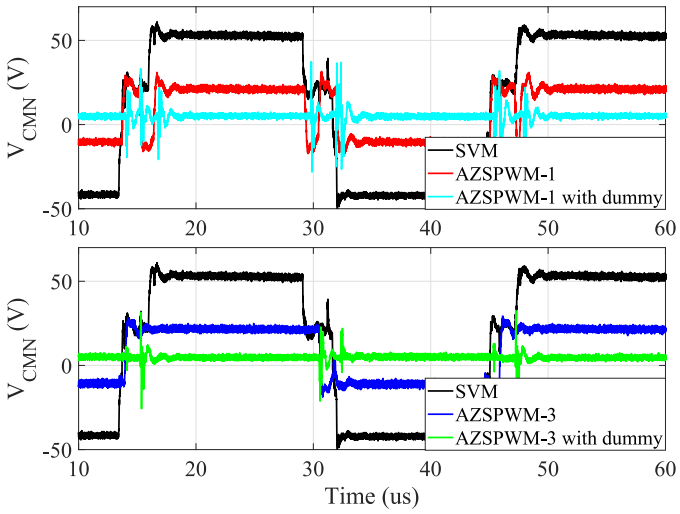

Fig. 16. Time domain waveforms of the common mode voltage at the motor terminals in case of SVM, AZSPWM-1 with and without the dummy leg (on the top) and AZSPWM-3 with and without the dummy leg (on the bottom) with V_{HV}=96 V and a 20 A phase peak current. With the use of dummy leg, the common mode voltage is constant expect for transients.

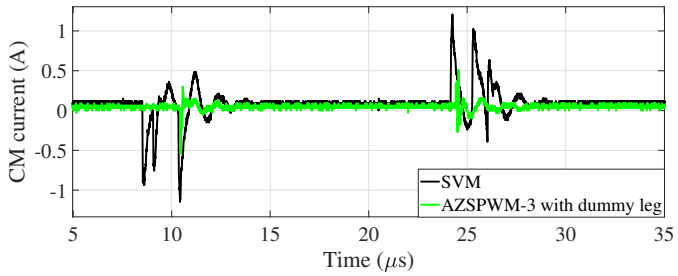

Fig. 17. Time domain waveforms of the CM current at the inverter input for SVM (black) and the proposed technique (green line). The power associated to the latter is around four times lower than that of SVM.

reduced in an engineered version.

With the four-leg three-phase inverter connected to the traction motor, whose CM impedance was previously characterized (see Fig. 10), preliminary measurements were carried out to assess the functionality of the prototype. The common mode voltage, measured directly at the terminals of the electrical machine, is reported in Fig. 16 for V_{HV}=96 V and a 10% modulation index, which corresponds to a peak phase current of 20 A. When using the classical SVM, the resulting CMV is similar to that reported in Fig. 5. Such a plot focuses on the behavior during a switching period of approximately 30 µs. Conversely, the CMV maximum amplitude is limited when employing the AZ modulations. Finally, when employing the dummy leg, the CMV remains constant except for some residual peaks during transients. The complementary commutations of the four switching leg allow for reducing the CMV, which in turn results in a reduction of the current flowing in the CM loop (see Fig. 1). To assess this point, the CM current at the DC input of the inverter was measured in the time domain, and it is reported in Fig. 17 for three-leg SVM (black) and dummy leg with AZSPWM-3 (green curve). By employing the proposed technique, oscillations at around 1 MHz, associated with $Z_{\mathrm{EM,CM}}$ resonances, are suppressed, with only residual

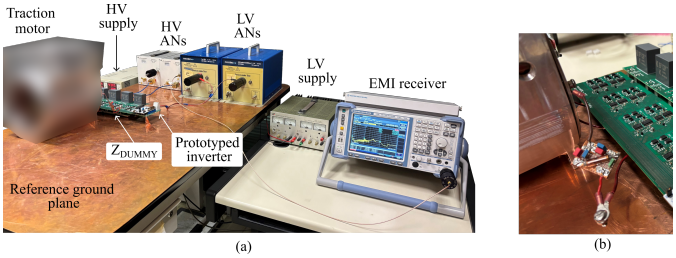

Fig. 18. In (a), the test-bench for the measurement of conducted EMI in accordance with the CISPR-25 standard for HV applications. In (b), a close-up image of the Z_{DUMMY} mounting.

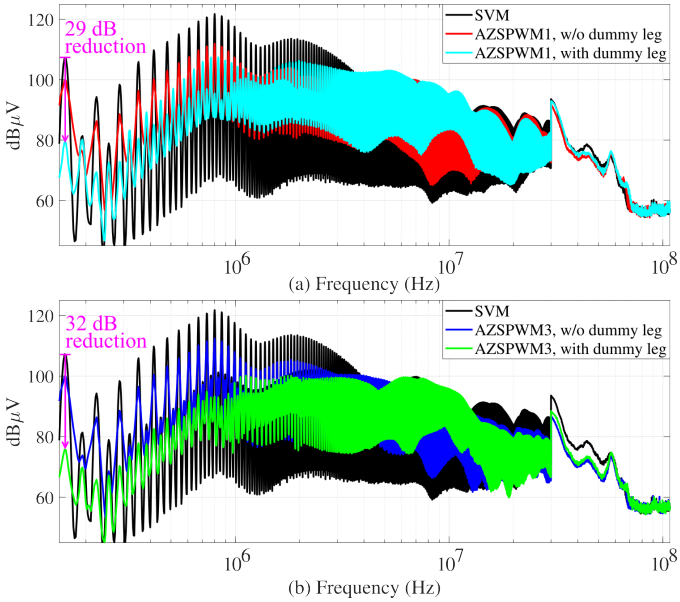

Fig. 19. Conducted EMI with f_{LOAD}=500 Hz, V_{HV}=96 V and 2.5 A peak phase current. The spectra obtained using the dummy leg are compared to that with SVM, when employing (a) AZSPWM-1 and (b) AZSPWM-3 modulation schemes.

peaks at much higher frequency visible. Although perfect CM current cancellation is not achieved, the proposed approach significantly reduces LF components compared to SVM, in accordance with results shown in Fig. 16.

B. Conducted EMI

To assess the reduction of conducted EMI at low frequency, the test bench prescribed by the CISPR-25 standard for HV application [2] was set up, and it is shown in Fig. 18(a). It comprises two sets of ANs connected to the HV power supply (V_{HV}) and the LV power supply (V_{LV}). The prototype shown in Fig. 15 was connected to the motor with unshielded cables kept as short as possible, as in an IMD. A close-up of Z_{DUMMY}, which is connected to the motor chassis through a bolt, is shown in Fig. 18(b). According to [2], conducted EMI spectra were measured in the 150 kHz-108 MHz range by an EMI receiver featuring 9 kHz (120 kHz) resolution bandwidth for frequencies lower (higher) than 30 MHz.

With the motor drive operating under nominal conditions, as detailed in Table V, conducted EMI at the HV AN connected to the negative supply rail are shown in Fig. 19. As the

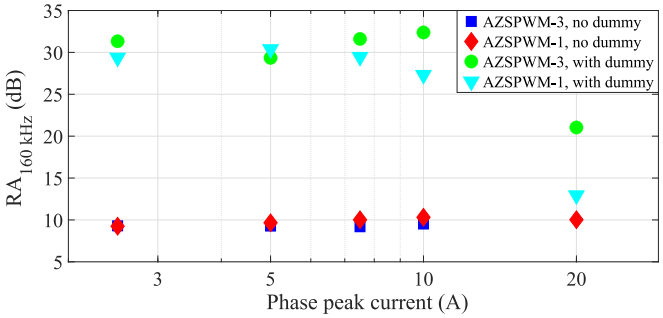

Fig. 20. Reduction of the peak around 160 kHz with respect to the SVM when applying the dummy leg with AZSPWM-1 (triangle) and AZSPWM-3 (circle) modulation schemes.

switching frequency (f_{SW}) is 32 kHz, the first harmonic in the regulated frequency range is $5f_{\mathrm{SW}}$. Recalling the CM transfer function shown in Fig. 4, the notch at 225 kHz, which is related to the resonance of the HV ANs components, is clearly visible in the measured EMI spectra in case of SVM, as shown in Fig. 19 in black. By switching the modulation scheme from SVM to AZSPWM-1 (AZSPWM-3), without switching the dummy leg and with Z_{DUMMY} disconnected, the resulting conducted EMI sprectrum is shown at the top (at the bottom) in red (in blue). In agreement with time-domain waveforms (see Fig. 16), AZ modulations result in CM conducted EMI reduced by around 10 dB compared to SVM.

With the dummy leg activated and connected to the reference ground through Z_{DUMMY} as shown in Fig. 18(b), the resulting spectra are shown in Fig. 19 when AZSPWM-1 (light blue) and AZSPWM-3 (green) are employed. The magnitude of those spectra is significantly lower than that in case of SVM up to 3 MHz. Regarding frequency components around 160 kHz, the dummy leg results in a reduction of approximately 29 dB and 32 dB when combined with AZSPWM-1 (at the top) and AZSPWM-3 (at the bottom), thus assessing the efficacy of the proposed technique. It is worth noting that the spectra shown in Fig. 19 were obtained without any control of the alignment of the output voltages of the inverter, meaning that neither dead-time compensation nor a fine alignment of the switching waveforms, as discussed in [18], were implemented.

To validate the use of the dummy leg under various load scenario, conducted EMI measurements were repeated for different values of phase current. The Relative Amplitude (RA) at frequency f_0 was defined as the ratio between the measured EMI with traditional SVM and that obtained by employing the AZSPWM with or without the dummy leg, as

$$RA_{\mathrm{f_0}} = \max_{\mathrm{f_0}\pm\Delta\mathrm{f}} |V_{\mathrm{AN,SVM}}(f)|_{\mathrm{dB}} - \max_{\mathrm{f_0}\pm\Delta\mathrm{f}} |V_{\mathrm{AN,AZS}}(f)|_{\mathrm{dB}}. \tag{17}$$

With f_0=160 kHz and Δf=10 kHz, the resulting RAs are shown in Fig. 20 for AZSPWM-1 without (diamond) and with (triangle markers) the dummy leg, as well as for AZSPWM-3 without (square) and with (circle markers) the dummy leg. With the dummy leg not activated, AZSPWM-1 and AZSPWM-3 modulations, which do not require any hard-

ware or topological modifications, achieve a similar reduction of around 10 dB compared to SVM. Conversely, reductions are more substantial, reaching 30 dB, when employing the dummy leg. AZSPWM-3 demonstrates superior performance compared to AZSPWM-1 when utilizing the dummy leg. This distinction arises because AZSPWM-3's opposite commutations of two main legs result in lower CM voltage variations compared to the scenario where the dummy leg cancels out a main leg, as shown in Fig. 16(b). Additional measurements assessed the impact of the dummy leg on DM EMI components, confirming that the proposed technique results in DM EMI levels comparable to those obtained with SVM. Further investigations will be carried out to better understand whether the proposed approach affects the CM-to-DM conversion mechanisms.

C. Sensitivity to CM motor impedance

The proposed method is based on designing Z_{DUMMY} to have the CM current injected by the dummy leg equal, in magnitude, to those of legs A-C. As discussed in Sect. III-B, the dummy impedance was synthesized using an RLC network to emulate the solid curve shown in Fig. 10. As far as PMSMs for traction application are concerned, the motor CM impedance is not expected to vary with the motor operating conditions, as it is mainly determined by the geometry of the stator windings and the slots. Aiming to assess the sensitivity of the proposed method to small variations of the motor CM impedance, $Z_{\mathrm{EM,CM}}$ was intentionally modified by adding three equal capacitors placed between the terminals and the chassis of the motor, i.e., in parallel to $C_{\mathrm{U,V,W}}$ shown in Fig. 2. In such a way, the LF CM capacitance of the motor ($3C_{\mathrm{LF}}$) can be modified, while keeping constant the dummy impedance. A 5 % deviation in C_{LF}, which is comparable to the uncertainty affecting the $Z_{\mathrm{EM,CM}}$ measurement, resulted in a negligible 4 dB reduction in RA. Conversely, when considering a 10 % variation, which is comparable with sample-to-sample variations due to fabrication tolerances, RA is reduced by 6 dB compared to that shown in Fig. 19.

D. Other figures of merit

Besides significantly reducing CM EMI at low frequency, the proposed solution makes use of AZSPWMs modulations, which in turns come with some trade-offs. More precisely, the Total Harmonic Distortion (THD) of the output phase currents is expected to increase compared to the SVM case. In the considered test case, it was found that the THD is less than 5% when employing AZ modulations, provided that the modulation index is higher than 4%. Concerning power losses under different modulation schemes, the average DC input power at the HV terminals of the prototype was measured, reflecting the overall dissipated power. The results, shown in Fig. 21, indicate that SVM has the lowest switching losses, followed by AZSPWM-3 and AZSPWM-1. Further investigations revealed that the power losses of the inverter increase from 4.5 W (SVM) to 11 W (AZSPWM-3), and those of the motor from 0.5 W (SVM) to 40 W (AZSPWM-3) for a 2.5 A peak phase current. This can be attributed to the motor

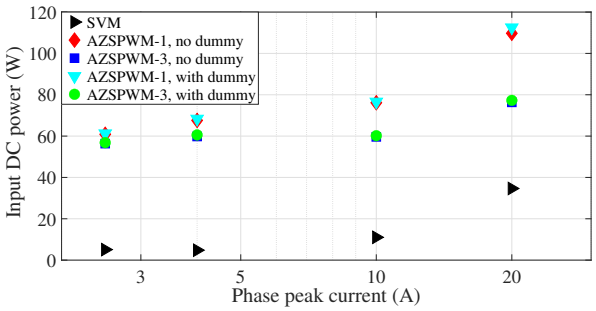

Fig. 21. Input DC power supply measured with SVM (triangle), AZSPWM-1 (diamond), and AZSPWM-3 (square markers) modulation scheme. The use of the dummy leg does not affect significantly the switching losses of the inverter.

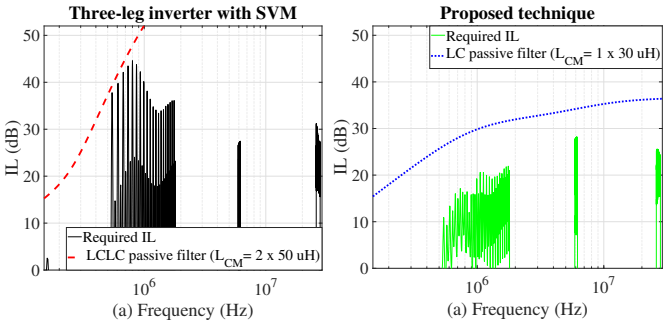

Fig. 22. Comparison of the required insertion loss for (a) SVM and (b) AZSPWM-3 with the dummy leg (green). The EMI filter was designed for both cases, resulting in the insertion loss shown in dashed (dotted) for SVM (proposed technique).

implementation in hairpin technology, which is particularly susceptible to AC losses. Conversely, the dummy leg has a minimal impact on switching losses, with similar input DC power observed for both AZSPWM-1 (diamond vs. triangle markers) and AZSPWM-3 (square vs. circle markers). Such a result is in agreement with (16), as the estimated power dissipated by the dummy leg is around 1 W.

VI. Volume and Cost Comparison

As discussed in Sect. V, the dummy leg achieves around 30 dB reduction of LF CM EMI compared to SVM. Despite this significant result, practical implementation in traction inverters requires evaluating computational, cost, and volume overheads of the proposed technique and to verify its benefits compared to traditional approaches. Referring to Sect. IV-B, commutation timing of leg D is directly derived from those of the main legs, yielding to a negligible computational overhead. Regarding the hardware components, a cost analysis was carried out, showing that the prototype cost increases by 20% when adding the dummy leg. However, by using lower-performance components for the dummy leg, the additional cost can be reduced to 5–6% of the total inverter cost. Similarly, the 25% volume overhead accounted for in the prototype shown in Fig. 15 can be significantly reduced with an optimized design.

To assess the volume reduction of the input filter when employing the proposed technique, two passive EMI filters

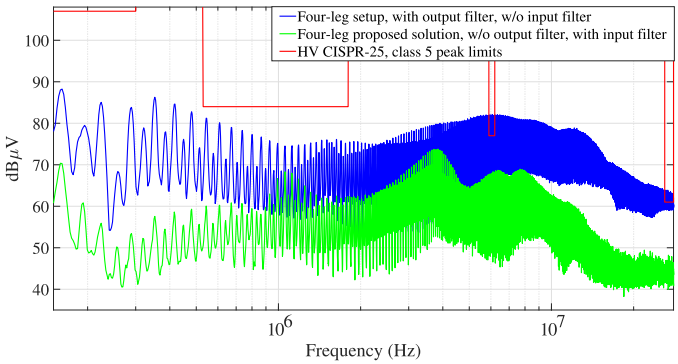

Fig. 23. Measured conducted EMI in case of the proposed technique combined with the designed input EMI filter (green) and when the four-leg inverter is connected to an output LC filter (blue spectrum). The former is compliant with CISPR-25 limits, the latter is not.

TABLE VI
COMPARISON BETWEEN DIFFERENT SOLUTIONS.

Solution	Three-leg inverter	Four-leg inverter with output filter	**Four-leg inverter with Z_{DUMMY} (proposed)**
Modulation	SVM	AZSPWM-3	**AZSPWM-3**
CM input filter	Topology: LCLC Chokes: 2x 50 µH Y-cap: 4 x 50 nF	Topology: C Y-cap: 2 x 20 nF	**Topology: LC** **Chokes: 1 x** 30 µH **Y-cap: 2 x** 100 nF
Output filter	No	LC filter with 3 x 4 x 10 µH, 4 x 40 µF	**No**
Total filter volume	365 cm^3	600 cm^3	106 cm^3
Cost overhead	0 %	+ 60%	≈ **0%**

were designed, one for the prototype operating as three-phase inverter with SVM, and one for the dummy-leg configuration. HV class-5 CISPR-25 limits [2], with an added 6 dB margin, were subtracted from the EMI spectrum shown in Fig. 19 in black for the SVM, and in green for the proposed technique. The required Insertion Losses (ILs) are shown in Fig. 22(a) for SVM and (b) for the proposed dummy leg in solid lines. In both cases, the 530 kHz-1.8 MHz is the critical band. Since the proposed solution decreases CM EMI at the source, the required IL is around 20 dB lower than that for SVM.

Based on these target ILs, two passive LC filters were designed for both cases. For the filter related to the SVM case, two stages are required, resulting in the IL shown in Fig. 22(a) in dashed line. Conversely, when employing the proposed solution, the required IL can be achieved with a single stage (dotted line in Fig. 22(b)). The component values for the two designed filters are listed in the third row of Tab. VI. The input EMI filter for the proposed technique was assembled and tested, resulting in the green spectrum shown in Fig. 23, thus confirming the CISPR-25 compliance with a compact input filter.

To compare the proposed technique with four-leg inverters for motor drives proposed thus far, an output LC filter as that in [21] was assembled using 30 µH inductors and 40 µF capacitors for each branch. When connected to the prototype in place of Z_{DUMMY} and tested under the same conditions, the resulting EMI are that shown in Fig. 23 in blue. In this case, the combined effect of fourth leg with AZSPWM-3 and of the output filter results in CISPR-25 limits almost met even without an input filter.

The three solutions, i.e., SVM with passive filter, four-leg inverter with output filter and the proposed technique, were compared in terms of filter volume and overall system cost, as summarized in Tab. VI. To ensure a fair comparison, all configurations were evaluated under CISPR-25 compliance, and selecting commercial filter components suitable for application to IMDs. As far as CM chokes for the input filter are concerned, one-turn chokes were considered, as they can be directly mounted around the input DC bus-bars. For the inductors of the output filter, they were selected with a saturation current above 100 A. What emerges from this comparison is that four-leg topology with output filter is impractical in IMDs, as it results in excessive cost and volume. Conversely, in the proposed technique, the additional inverter cost is counterbalanced by the smaller input EMI filter, while reducing significantly its volume. Although the proposed method cannot independently meet the CISPR-25 limits, the CM EMI reduction it achieves at the inverter output is directly translated into a lower IL for the input filter, thus reducing its volume and offering significant advantages over traditional solutions for IMD applications.

VII. CONCLUSION

This work investigates the use of a small dummy leg in a three-phase traction inverter to reduce CM EMI at low frequency. Unlike traditional three-phase four-leg topologies, this approach does not require output filters to achieve CM current cancellation, making it beneficial for high-current applications, such as IMDs. The method combines AZSPWM modulations, which enable the complementary commutations of all four switching legs, with a small dummy leg, loaded with a passive network emulating the CM impedance of the motor.

Experimental results show that AZSPWM-3 achieved the best performance, reducing CM EMI by 20-32 dB. The method was found to be robust against variations of the motor CM impedance related to fabrication tolerances. With an optimized design, the cost overhead is limited to 5 %. By comparing the proposed method against traditional solutions, i.e., SVM with passive input filters and four-leg topology with output filter, the proposed solution is superior in terms of both filter volume and cost. Future work will investigate the proposed technique when applied to test case different than traction motors, including a dynamic adjustment of Z_{DUMMY} if needed and the fine alignment of the switching waveforms, as discussed in [18], to increase the efficacy of the dummy leg at higher frequency.

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