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A Software-Based Control System to Reduce Conducted CM EMI in Four-Leg Three-Phase Inverters Using the Delay Compensation Technique

Erica Raviola, *Member, IEEE*, and Franco Fiori, *Member, IEEE*

***Abstract*—Common-Mode (CM) conducted Electro Magnetic Interference (EMI) is a critical issue in automotive power converters, where strict EMC regulations must be met. This paper investigates the Delay Compensation Technique (DCT) applied to traction inverters to reduce CM EMI at low-frequency. Although the four-leg topology enables complementary switching, existing works do not provide a method to finely align the commutation edges, which is required to have CM current pulses canceling out and effectively reducing CM EMI. In this work, an iterative optimization method is introduced for the two-leg case, and then extended to the four-leg inverter with sinusoidal modulation, enabling fast convergence and minimal computational overhead. Experimental validation resulted in 30 dB EMI reduction at 160 kHz and in 15-20 dB for frequencies up to a few MHz, with significant benefits in terms of volume reduction of the input EMI filter compared to state-of-the-art techniques.**

***Index Terms*—CM conducted EMI, software-based EMI control, three-phase four-leg inverter, delay compensation technique, dummy leg, active zero state modulation.**

I. Introduction

With the spread of electric vehicles, the design of traction inverters compliant to automotive EMC standards is a major concern, particularly regarding conducted Electro Magnetic Interference (EMI). Designed based on SiC and GaN power transistors can achieve high power density and switching frequency [1], but EMI in the Low-Frequency (LF) regulated range, i.e., from 150 kHz to a few MHz, also increases [2]. Conducted EMI can be analyzed by decomposing it into Differential Mode (DM) and Common Mode (CM) components. The former can be addressed at design stage by tailoring the DC link impedance. The latter is related to the parasitic coupling between high dv/dt nodes and the ground reference. To reduce LF CM EMI in traction inverters, one-turn CM chokes are typically placed around the input busbars, resulting in bulky EMI filters that impair the achievable power density [3]. To reduce the EMI filter volume, active solutions, either based on analog [4], [5], [6] or digital [7], [8] implementations, have been proposed, but their practical use in traction inverters remains limited.

Besides filtering, several EMI mitigation techniques effective at the source have been investigated [9]. Spread spectrum modulation, where the switching frequency is continuously varied, is a well-known technique for DC-DC converters [10], but its efficacy in traction inverters is limited due to the low frequency deviation allowed [11]. Amongst software-based solutions, active zero modulations can reduce CM voltage at the inverter output by one third, resulting in 10 dB lower EMI at LF [12]. Active gate drivers can control the switching transients of power transistors [13], but they are mainly effective above tens of MHz, with no advantages at LF.

A promising approach to mitigate LF CM EMI is the Delay Compensation Technique (DCT), which can be applied to power converters featuring oppositely commutated legs. By finely aligning complementary voltages, the currents injected into the parasitic capacitances between the phase nodes and the reference ground cancel each other, thus suppressing CM current [14]. This alignment can be achieved by a software control of the delays of signals driving the power transistors. The DCT has been effective in reducing LF CM EMI in low-voltage motor driver [15] and in a full-bridge DC-DC converter [16], achieving reductions of around 20 dB. Preliminary simulation-based studies [17] have already assessed the EMI reduction when applying the DCT to high-voltage power circuits. However, DCT requires pairs of complementary legs, thus it can not be directly applied to sinusoidal three-phase inverters, as their typical modulation scheme, i.e., space vector modulation, prevents complementary commutations from occurring.

To overcome this limitation, four-leg three-phase inverters, originally proposed for load balancing and CM voltage reduction, can be explored [18], [19]. In this topology, all four legs switch complementarily, thus canceling the CM current. However, this topology has always been combined with an output filter, which is unsuitable in high-current applications. Moreover, the commutation edges are not finely adjusted in practice. In this context, DCT is well suited for four-leg three-phase inverters, and, to the authors' knowledge, no previous research investigated this integration. Implementing the DCT in traction inverters requires an adaptive control of the commutation delays to account for manufacturing tolerances

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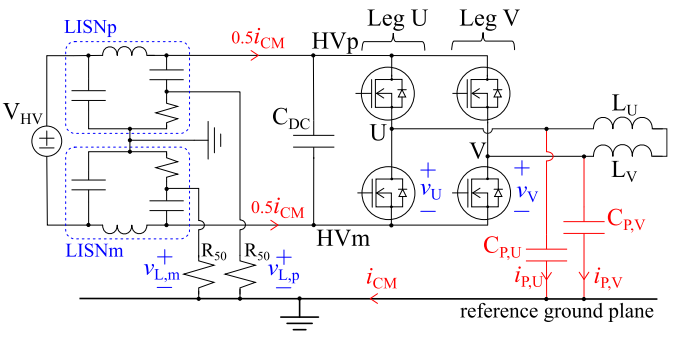

Fig. 1. Legs U and V considered to discuss CM EMI delivered by opposite switched legs. The CM current (i_{CM}) is the sum of those flowing through parasitic capacitances $C_{P,U-V}$ ($i_{P,U-V}$).

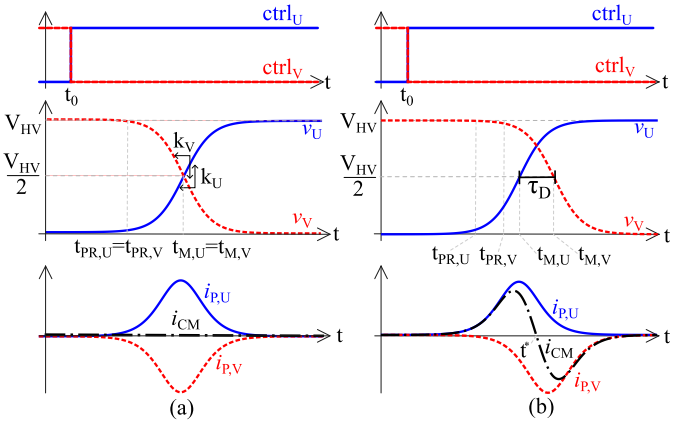

Fig. 2. Control signals ($ctrl_{U-V}$), output voltages (v_{U-V}) and CM currents ($i_{P,U-V}$) when leg U and leg V are (a) aligned, and (b) not aligned.

and sinusoidal load conditions, while introducing minimal computational burden. While advanced control strategies have been investigated for non-traditional three-phase topologies [20], [21], little attention has been paid to control strategies addressing conducted EMI.

This work proposes a control system to integrate the DCT in four-leg three-phase inverters for traction applications. The main contributions include a theoretical framework that formulates the DCT as a minimization problem, an algorithm that adaptively optimize the delays of two opposite switched legs to achieve zero CM current, and a strategy for extending this algorithm to traction inverters while reducing the total number of iterations. By demonstrating the feasibility and effectiveness of DCT in four-leg three-phase inverters, this work poses the basis for future developments in software-based EMI reduction and more compact power converters.

The paper is organized as follows. In Sect. II, CM conducted EMI delivered by two opposite switched legs is analyzed. A theoretical framework for the DCT and the minimization algorithm in case of two legs is reported in Section III. Four-leg three-phase inverters are analyzed in Section IV, and the extension of DCT algorithm to traction inverters is discussed in details in Section V. The case study and experimental results are discussed in Section VI. Concluding remarks are in Sect. VII.

II. CM Conducted EMI of Two Opposite Commutated Switching Legs

The CM conducted EMI delivered by two legs is analyzed referring to the circuit shown in Fig. 1. The legs, denoted as U and V, drive an inductive load (L_U, L_V). Power transistors are switched according to logic signals $ctrl_{U-V}$ through dedicated gate drivers (not shown in Fig. 1). With the legs switching complementarily, $ctrl_U = \overline{ctrl_V}$, meaning that when $v_U \approx V_{HV}$, then $v_V \approx 0$ V, and vice versa.

To assess CM EMI, the legs are supplied through two Line Impedance Stabilization Networks (LISNs) to decouple the device under test, i.e., legs U and V, from the power supply distribution network (V_{HV}). The measurement ports of the LISNs are terminated with 50 Ω resistances (R_{50}), as prescribed by CISPR-25 [22]. The setup also includes a reference ground plane, over which the device under test and the LISNs are placed on. According to the voltage method, CM conducted EMI is defined as the average disturbance across the R_{50} terminations, i.e.,

$$v_{LISN,CM} \hat{=} \frac{v_{L,p} + v_{L,m}}{2}. \tag{1}$$

Indeed, $v_{LISN,CM}$ is related to the CM current (i_{CM}) flowing through the reference plane. As nodes U and V experience the highest dv/dt in the circuit, they are typically identified as the primary source of CM EMI. A capacitive coupling usually exists between these nodes and the ground plane, represented in Fig. 1 by $C_{P,U-V}$. Concerning traction inverters, the dominant contribution at low frequency is the CM capacitance between the stator windings and grounded chassis of the motor, with typical values of 10 nF [23].

To further discuss CM EMI, the waveforms shown in Fig. 2 are considered. At time t_0, control signals $ctrl_{U-V}$ switch opposite. Due to the propagation delays of the gate drivers and the time required by power transistors to switch from interdiction to saturation, v_U (v_V) begins to rise (fall) at time $t_{PR,U}$ ($t_{PR,V}$). The drain-source voltages are modeled with an S-shape profile, allowing for a $\mathcal{C}^\infty$ representation [24], resulting in

$$v_U(t) = \frac{V_{HV}}{1 + e^{-k_U(t-t_{M,U})}}, \tag{2}$$

$$v_V(t) = V_{HV} - \frac{V_{HV}}{1 + e^{-k_V(t-t_{M,V})}}, \tag{3}$$

where k_{U-V} are the slopes at $t = t_{M,U-V}$

Thus, CM current i_{CM} can be approximated as

$$i_{CM}(t) = i_{P,U}(t) + i_{P,V}(t) \approx C_{P,U}\frac{dv_U(t)}{dt} + C_{P,V}\frac{dv_V(t)}{dt}, \tag{4}$$

provided that $v_{LISN,CM}$ is much lower than V_{HV}. The resulting CM current is the sum of two pulses, which are shown in Fig. 2 at the bottom in solid and dashed lines. Given (4), i_{CM} is zero only when $k_U = k_V$ and $t_{M,U} = t_{M,V}$, as shown in Fig. 2 on the left. On the contrary, when v_V leads or lags v_U, the CM current is no longer null, as shown on the right. The time difference between the midpoints of the two transitions, denoted ad τ_D, is defined as

$$\tau_D = t_{V,M} - t_{U,M} = t_{PR,U} + \frac{t_{RISE,U}}{2} - t_{PR,V} - \frac{t_{FALL,V}}{2}, \tag{5}$$

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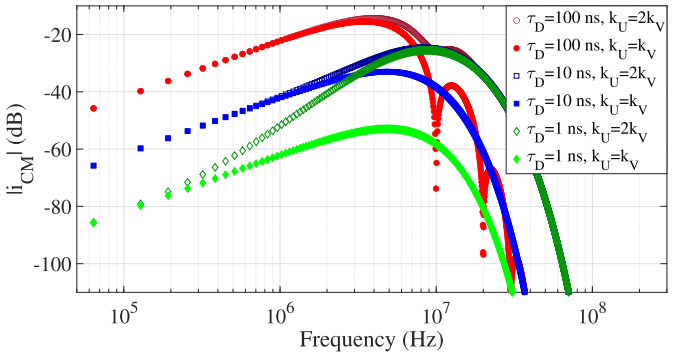

Fig. 3. Magnitude of i_{CM} frequency spectrum for $\tau_D \neq 0$ (unfilled) and $k_U \neq k_V$ (filled markers). LF components are mainly determined by τ_D.

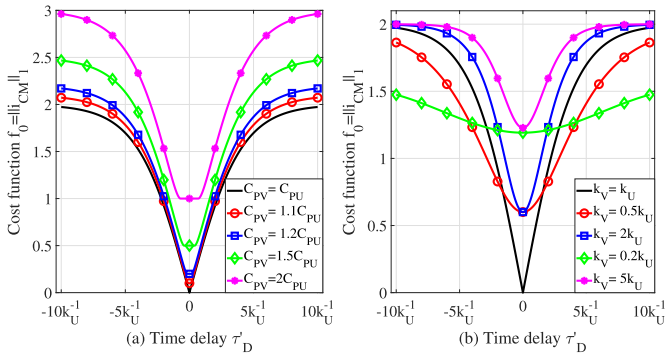

Fig. 4. Cost function in (12) as a function of the residual delay τ'_D in case of mismatch of (a) parasitic capacitance and (b) of the rise/fall times.

where $t_{RISE,U}, t_{FALL,V}$ are the 10%-90% rise/fall of legs U and V. Assuming $C_{P,U} = C_{P,V}$ and $k_U = k_V$, substituting the time derivatives of (2), (3) in (4) yields

$$i_{CM}(t) = k_U C_{P,U} V_{HV} \left(\frac{e^{-k_U t}}{(1+e^{-k_U t})^2} - \frac{e^{-k_U(t-\tau_D)}}{(1+e^{-k_U(t-\tau_D)})^2} \right). \quad (6)$$

From (6), the CM current is zeroed only if $\tau_D = 0$, in accordance with Fig. 2(a).

As far as the impact of τ_D on the i_{CM} spectrum is concerned, the frequency components of (4) are shown in Fig. 3 in case of $\tau_D \neq 0$ (unfilled) and $k_U \neq k_V$ (filled markers). A tenfold reduction of τ_D, from 100 ns (circle) to 10 ns (square), and 1 ns (diamond marker), results in a 20 dB decrease in the low-frequency components, as discussed in previous studies [11], [15]. In contrast, rise/fall time mismatches affect the high-frequency range. Thus, minimizing τ_D is the most effective strategy to reduce low-frequency CM EMI delivered by switched legs. In power circuits such as that in Fig. 1, $\tau_D \neq 0$ due to manufacturing tolerances, e.g., controller jitter, mismatched interconnection lengths, and gate driver mismatches, thus preventing CM current cancellation.

III. DCT for Two Opposite Switched Legs

Targeting the time-domain waveforms shown in Fig. 2(a), the Delay Compensation Technique (DCT) reduces i_{CM} by finely aligning the output switching voltages. Since τ_D is not under control, the key idea is to advance, or delay, the signal $ctrl_V$ with respect to $ctrl_U$ by an amount d_{DCT} to compensate for the intrinsic mismatch τ_D. After applying the DCT, the residual mismatch on the output waveforms is

$$\tau'_D = \tau_D - d_{DCT}. \quad (7)$$

To be effective, the DCT requires an adaptive approach to determine d_{DCT}. This optimization can be formalized as a minimization problem where the variable to be optimized is d_{DCT}, and the cost function f_0 is the p-norm of $i_{CM}(t, \tau'_D)$ over a time interval $[t_1, t_2]$

$$\text{Minimize } f_0(\tau'_D) = ||i_{CM}||_p = \left(\int_{t_1}^{t_2} |f_0(t, \tau'_D)|^p dt \right)^{\frac{1}{p}} \quad (8)$$

$$\text{Subject to } -|d_{DCT,MAX}| < d_{DCT} < |d_{DCT,MAX}| \quad (9)$$

A constrain on the maximum delay ($d_{DCT,MAX}$) is imposed not to alter significantly the operating point of the power converter. The properties of the cost function are analyzed in Section III-A to identify a suitable optimization algorithm. To this purpose, a single commutation, as that shown in Fig. 2, is considered. The proposed algorithm is then presented in Section III-B in the case of periodical commutated switching legs.

A. Cost Function

Concerning f_0, the p-norm is considered in (8) to remove the time dependence, meaning that $f_0 : \mathbb{R}^2 \to \mathbb{R}$. The $p = 1$ norm, i.e., the integral of the absolute value, was preferred over the $p = 2$ norm, i.e., the energy-based norm, as it is more robust to high-frequency noise [25]. When considering a single commutation, the cost function can be written as

$$f_0 = ||i_{CM}||_1 = \int_{-\infty}^{\infty} |i_{CM}(t, \tau'_D)| dt. \quad (10)$$

An analytical expression can be derived by substituting (6) into (10), and replacing τ_D with τ'_D, as introduced in (7). By defining the midpoint $t^* = \frac{1}{2}\tau'_D$, which is shown in Fig. 2(b) at the bottom, and assuming $\tau'_D \geq 0$, from (6) it can be shown that $i_{CM}(t^*) = 0$, $i_{CM}(t) \geq 0, \forall t < t^*$, and i_{CM} is odd with respect to $t = t^*$. Under these symmetries, (10) simplifies to

$$f_0 = 2\ k_U C_{P,U} V_{HV} \int_{-\infty}^{t^*} \frac{e^{-k_U t}}{(1+e^{-k_U t})^2} - \frac{e^{-k_U(t-\tau'_D)}}{(1+e^{-k_U(t-\tau'_D)})^2} dt, \quad (11)$$

yielding

$$f_0(\tau'_D) = 2C_{P,A} V_{HV} \left(\left(1 + e^{-\frac{k_U \tau'_D}{2}}\right)^{-1} + \left(1 + e^{\frac{k_U \tau'_D}{2}}\right)^{-1} \right). \quad (12)$$

A similar analysis can be performed for $\tau'_D < 0$, leading to $f_0(\tau'_D) = f_0(-\tau'_D)$. The values $f_0(\tau'_D)$ assumed are plotted in Fig. 4 normalized to $C_{P,A} V_{HV} = 1$. With $k_U = k_V$ and $C_{P,U} = C_{P,V}$, the cost function exhibits a minimum at $\tau'_D = 0$ and saturates at two for $\tau'_D \gg 1/k_U$, i.e., when the support of $i_{P,U}(t)$ does not overlap with that of $i_{P,V}(t)$. Mismatches in parasitic capacitance ($C_{P,U} \neq C_{P,V}$) and waveform slopes ($k_U \neq k_V$) are reported by markers in Fig. 4(a) and (b), respectively. Although f_0 still exhibits a minimum around τ'_D, its value is greater than zero due to the asymmetry and increases with the mismatch.

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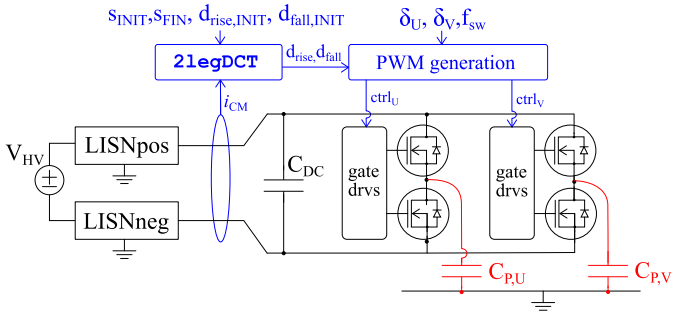

Fig. 5. Proposed setup for optimizing the $d_{\text{rise}}, d_{\text{fall}}$ delays of the complementary switching legs U and V. Based on the isolated CM current sensing, the `2legDCT` algorithm iteratively adjust the delays to achieve the lowest CM EMI.

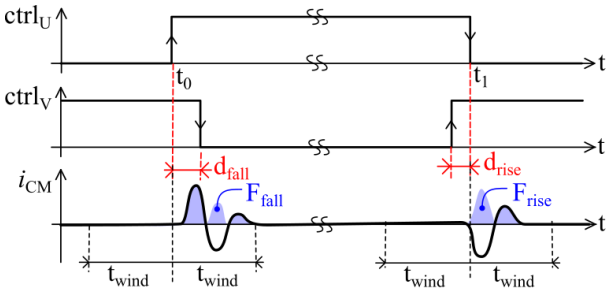

Fig. 6. Time-domain waveforms of the leg control signals ($ctrl_{\text{U-V}}$) and CM current for the circuit shown in Fig. 5. The algorithm optimizes the delays of $ctrl_{\text{V}}$ (secondary) with respect to $ctrl_{\text{U}}$ (primary leg).

B. Iterative Minimization Algorithm for Two Legs

Based on the previous analysis, f_0 is generally non-convex, as $f_0'' \not\geq 0$ from (12). However, it exhibits a unique minimum, even in case of asymmetric conditions (see Fig. 4). Thus, (8)-(9) is a non-convex constrained optimization problem. Various numerical methods can be used to solve it [26]. In this work, a bracketing-based iterative algorithm with halved step division was preferred, as it is not affected by stability issues as in gradient-based methods.

Algorithm 1 `2legDCT`

Data: $s_{\text{INIT}}, s_{\text{FIN}}, d_{\text{rise,INIT}}, d_{\text{fall,INIT}}$
Result: Optimized delays $d_{\text{rise}}, d_{\text{fall}}$.

```
1  begin
2      d_rise ← d_rise,INIT, d_fall ← d_fall,INIT;
3      N_iter ← log2 (s_INIT/s_FIN);
4      for i_iter = 1 : 1 : N_iter do
5          s ← s_INIT/2^i_iter;
6          Set the delay to d_rise and d_fall, evaluate F_rise,1, F_fall,1;
7          Set the delay to d_rise + s and d_fall + s, evaluate F_rise,2, F_fall,2;
8          Set the delay to d_rise − s and d_fall − s, evaluate F_rise,3, F_fall,3;
9          if F_rise,2 > F_rise,1 and F_rise,2 > F_rise,3 then
10             d_rise ← d_rise + s;
11         else if F_rise,3 > F_rise,1 and F_rise,3 > F_rise,2 then
12             d_rise ← d_rise − s;
13         end
14         if F_fall,2 > F_fall,1 and F_fall,2 > F_fall,3 then
15             d_fall ← d_fall + s;
16         else if F_fall,3 > F_fall,1 and F_fall,3 > F_fall,2 then
17             d_fall ← d_fall − s;
18         end
19     end
20 end
```

To adjust d_{DCT} adaptively, the circuit shown in Fig. 1 is modified as shown Fig. 5. The CM current is measured at the input through an isolated transducer. Based on this, the proposed algorithm computes the optimized delays for leg V's control signal with respect to that of leg U, and provides them to the PWM generator. Since the legs switch at frequency f_{SW} and duty cycle $\delta_{\text{V}} = 1 - \delta_{\text{U}}$, two commutations occur in each PWM period. The algorithm must thus determine two delays, one for the rising (d_{rise}) and one for the falling (d_{fall}) edges of $ctrl_{\text{V}}$, as shown in Fig. 6. Recalling (8), the cost function should be evaluated over a time window $[t_1, t_2]$ wide enough to include the support of both $i_{\text{P,U}}$ and $i_{\text{P,V}}$. As it is not know a priori whether leg V leads or lags leg U, the integration interval has been chosen symmetric, as shown in Fig. 6.

The pseudo-code of the proposed algorithm (`2legDCT`) is reported in Alg. 1. The inputs are the initial (s_{INIT}) and final (s_{FIN}) step sizes, and the initial delay values ($d_{\text{INIT,rise}}$ and $d_{\text{INIT,fall}}$). The delays are applied to the control signal of the secondary leg, which is leg V in Fig. 6, while the timing of primary one (leg U) is not affected. As the algorithm is based on a ternary search, the number of iterations is

$$N_{\text{iter}} = \left\lceil \log_2 \left(\frac{s_{\text{INIT}}}{s_{\text{FIN}}} \right) \right\rceil. \tag{13}$$

At each iteration i_{iter}, the algorithm tests three values, i.e., the central values (row 6) and the central values plus/minus the step size (rows 7-8). For both commutations, the cost function is evaluated and stored in $F_{\text{rise(fall)}}$. The delay resulting in the lowest $F_{\text{rise(fall)}}$ then is selected as next $d_{\text{rise,i+1}}$, $d_{\text{fall,i+1}}$ (rows 9-18). To sum up, the algorithm provides optimized delays for both commutations while maintaining low complexity, making it suitable for implementation in resource-limited controllers.

Design guidelines can be drawn regarding the input parameters choice. As it is initially unknown whether leg V leads or lags leg U, setting $d_{\text{rise/fall,init}} = 0$ ensures symmetry and maximizes the search range. The final step size (s_{FIN}) should be smaller than the $v_{\text{U,V}}$ rise/fall time to allow for a fine alignment. The maximum value of $d_{\text{rise,fall}}$ may reach during the algorithm execution should be bounded to (9), resulting in

$$s_{\text{INIT}} \leq \frac{d_{\text{DCT,MAX}}}{\sum_{i=1}^{N_{\text{iter}}} 2^{-i}}. \tag{14}$$

It is worth noting that the inserted delays should not affect the actual duty cycle the legs are commutated at, meaning that $d_{\text{DCT,MAX}} \ll \delta_{U-V} f_{\text{SW}}^{-1}$ should be ensured. To sum up, s_{INIT} and s_{FIN} should be selected as a trade-off between the achievable time resolution and the time required to execute the algorithm, which is proportional to N_{iter}.

C. Experimental Validation

To gain insight on `2legDCT` algorithm, experimental results for two complementary legs are shown in Fig. 7, referring to the commutation at the $ctrl_{\text{U}}$ falling edge. The setup is described in details in Section VI-A. Regarding the algorithm parameters, it was set $t_{\text{wind}} = 1\ \mu$s and $s_{\text{FIN}} = 8$ ns, as the rise/fall times of the output phases were in the (20 ns, 50 ns) range. Without delay ($d_{\text{fall}} = 0$ ns), the CM current is shown in dashed line at the top of Fig. 7. During the first iteration, the algorithm tests three d_{fall} values, i.e., −64, 0 and

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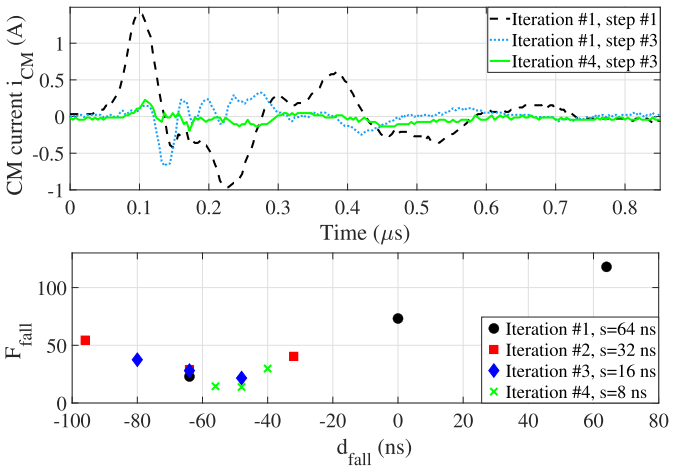

Fig. 7. At the top, CM current before (dashed), during (dotted) and after (solid line) the running of iterative algorithm (see Alg. 1). The merit factor at the falling edge (F_{fall}) is reported at the bottom during the algorithm execution.

64 ns. Amongst them, the −64 ns case yields the lowest value of cost function (F_{fall}), as shown by the dotted i_{CM} current and by the circle markers at the bottom. The next iteration refines the search around $d_{\text{fall}} = -64$ ns (square markers), and at the final iteration, the optimal d_{fall} is obtained, with the corresponding i_{CM} shown in solid line. F_{fall} decreases by a factor 5.5 during the algorithm execution, and Fig. 7 at the bottom is in good agreement with the analytical cost function (see Fig. 4), thus confirming the analysis and the delay optimization strategy.

IV. Three-Phase Four-Leg Inverter With AZSPWM-3 Modulation

The iterative algorithm discussed in Sect. III-B is effective in reducing the CM current, but it requires a pair of legs switching opposite. This condition is not met in traditional three-phase inverters, as space vector modulation does not ensure complementary leg commutations. As a result, DCT can not be applied to three-leg inverters with sinusoidal outputs. To overcome this limitation, the four-leg three-phase topology, combined with an active zero modulation, has been investigated and it is discussed in what follows.

A. Design of the Dummy Leg

The four-leg topology is shown in Fig. 8, where legs A, B and C, drive the motor, presented by three star-connected inductors. The fourth leg, referred to as the dummy leg, drives the impedance Z_{DUMMY}, connected to the motor chassis. This solution eliminates the need for passive output filters, typically employed in four-leg inverters to fix the motor star-center potential. To achieve CM EMI cancellation, Z_{DUMMY} must be such that the CM current generated by leg D matches, in magnitude, that of the other legs. Assuming complementary commutations of leg A and D as in Fig. 2(a), from the analysis of the circuit shown in Fig. 8 it can be derived

$$Z_{\text{DUMMY}} = 3Z_{\text{EM,CM}}, \tag{15}$$

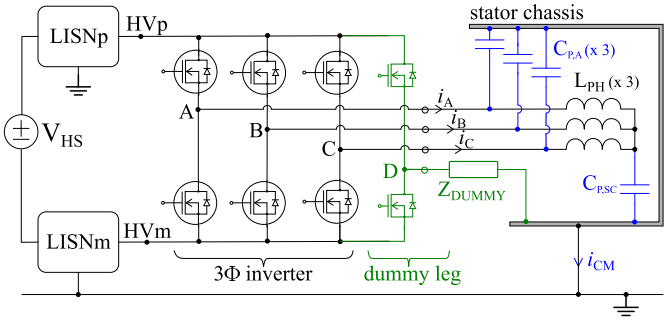

Fig. 8. Four-leg three-phase inverter, where the dummy leg is connected to the reference ground through the impedance Z_{DUMMY}.

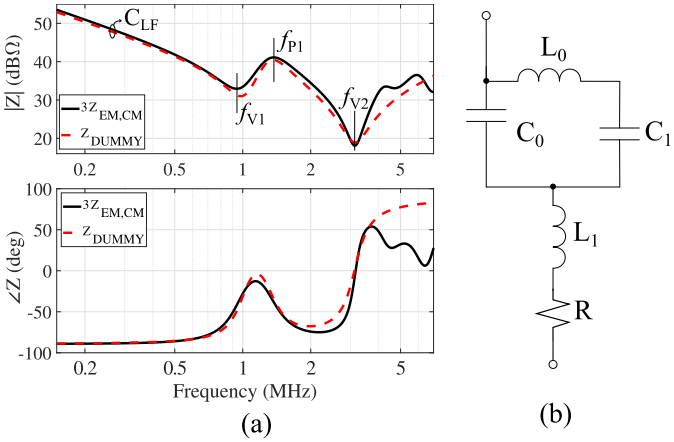

Fig. 9. In (a), measured CM impedance of the motor (solid) and of Z_{DUMMY} (dashed line) in the frequency range of interest, i.e., from 150 kHz up to a few MHzs. The passive network used to synthesize Z_{DUMMY} is in (b), with component values reported in Tab. I.

where $Z_{\text{EM,CM}}$ is the motor CM impedance. The dominant CM path for the frequency range of interest, i.e., from 150 kHz up to a few MHz, is that encompassing the stator windings and the ground-connected chassis, meaning that output interconnections can be neglected. $Z_{\text{EM,CM}}$ can be measured using an impedance or a network analyzer, connected between the shorted motor terminals and the chassis. Concerning traction motors, such an impedance is like that shown in Fig. 9(a) in solid line, which refers to the motor used in the experimental validation. $Z_{\text{EM,CM}}$ is capacitive at LF and exhibits resonances and anti-resonances in the MHz range [23].

The topology shown in Fig. 9(b) was adopted to ensure (15). The corresponding impedance in the Laplace domain is

$$Z_{\text{DUMMY}} = R + sL_1 + \frac{s^2L_0C_1 + 1}{s(C_0 + C_1) \cdot \left(s^2L_0\dfrac{C_0C_1}{C_0 + C_1} + 1 \right)}. \tag{16}$$

At low frequency, Z_{DUMMY} is primarily capacitive ($C_0 + C_1$), and designed to be equal to one third of $3C_{\text{P,A}} + C_{\text{P,SC}}$ (see Fig. 8). Then, L_0 resonates with C_1, followed by a parallel resonance of L_0 with $C_0 \oplus C_1$, and by a series resonance ($L_1 - C_0 \oplus C_1$). By fitting $3Z_{\text{EM,CM}}$, the values of the passive components have been obtained and are reported in Tab. I. The resulting impedance is in good agreement with $3Z_{\text{EM,CM}}$,

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TABLE I
DUMMY IMPEDANCE VALUES

Parameter	Value	Parameter	Value	Parameter	Value
C_0	1.5 nF	C_1	0.8 nF	R	5 Ω
L_0	30 µH	L_1	1.9 µH	C_{LF}	2.2 nF
f_{V1}	930 kHz	f_{P1}	1.4 MHz	f_{V2}	3.2 MHz

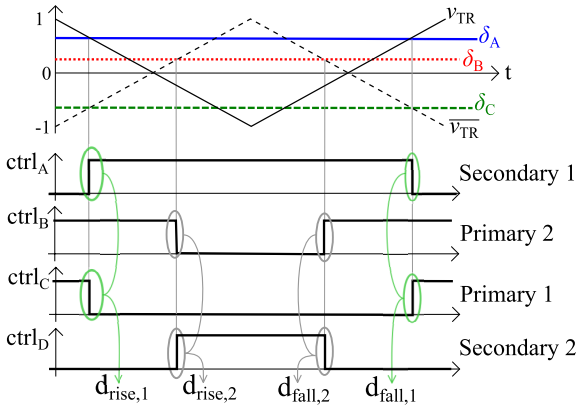

Fig. 10. Control signals of the main legs and that of the dummy leg with AZSPWM-3 modulation scheme in Sector I, resulting in opposite commutations of all four legs.

as show in Fig. 9(a) in dashed lines. Notably, Z_{DUMMY} is an open circuit at DC, keeping leg D isolated from the chassis.

As far as the transistors of the dummy leg are concerned, they can be chosen with a relaxed constrain on the maximum current they should bear, as only a fraction of the CM current flows through them. This allows for choosing smaller and less-expensive transistors compared to those in the main legs, thus minimizing the volume and cost overhead of the dummy leg.

B. AZSPWM-3 and Control of the Dummy Leg

With the four-leg three-phase topology shown in Fig. 8, the control signals ($ctrl_{A–C}$) of the four legs must ensure that load currents ($i_{A–C}$) are sinusoidal, and that only complementary commutations occur. This requires the number of legs tied to the positive supply rail always matching that of legs tied to the negative rail. The conventional Space Vector Modulation (SVM) scheme violates this condition, as it relies on zero vectors to synthesize the reference rotating vector. To overcome this issue, SVM has been replaced with Active Zero State PWM type three (AZSPWM-3) modulation, which guarantees the complementary commutation of two out of the three main legs. The AZSPWM-3 scheme can be implemented by replacing, for given sectors and legs, the triangular PWM carrier v_{TR} with its complement [27]. This point is clarified in Fig. 10, where the duty cycles of the three legs ($\delta_{A–C}$) and the triangular carriers $v_{TR}, \overline{v_{TR}}$ are shown at the top for Sector I. According to AZSPWM-3, the control signals are generated by comparing $\delta_{B–C}$ to the inverted carrier $\overline{v_{TR}}$, and δ_A to v_{TR} in the first sector. Since $\delta_A = -\delta_C$, the resulting switching waveforms are complementary, as shown at the bottom. Thus, the dummy leg must only compensate for leg B, leading to $ctrl_D = \overline{ctrl_B}$.

TABLE II
LOOK UP TABLE FOR AZSPWM-3 CARRIER SELECTION AND DUMMY LEG CONTROL SIGNAL

Sector	I	II	III	IV	V	VI
Leg A carrier	v_{TR}	v_{TR}	$\overline{v_{TR}}$	$\overline{v_{TR}}$	$\overline{v_{TR}}$	v_{TR}
Leg B carrier	$\overline{v_{TR}}$	v_{TR}	v_{TR}	v_{TR}	$\overline{v_{TR}}$	$\overline{v_{TR}}$
Leg C carrier	$\overline{v_{TR}}$	$\overline{v_{TR}}$	$\overline{v_{TR}}$	v_{TR}	v_{TR}	v_{TR}
Leg D control	$\overline{ctrl_B}$	$\overline{ctrl_A}$	$\overline{ctrl_C}$	$\overline{ctrl_B}$	$\overline{ctrl_A}$	$\overline{ctrl_C}$

To extend the example shown in Fig. 10 to all sectors, according to AZSPWM-3, the legs with maximum and minimum δ in a given sector are always associated with v_{TR} and $\overline{v_{TR}}$. As a result, two of three main legs are inherently driven to generate complementary switching waveforms.The remaining leg, whose duty cycle changes the most within the sector, must be paired to the dummy leg to ensure CM current cancellation. Hence, the generation of $ctrl_D$ can be based on the Look Up Table (LUT) reported in Tab. II.

V. DCT FOR FOUR-LEG THREE-PHASE INVERTERS

This Section presents the DCT algorithm for the four-leg three-phase inverter in Fig. 8 operating with AZSPMW-3. The adaptation of the two-leg algorithm to the four-leg topology is discussed, together with its integration with the motor controller and computational overhead.

A. Block Scheme

To apply the DCT to traction inverters, the control architecture shown in Fig. 11 is proposed. The additional components, which have been highlighted to be found at a glance, implement the AZSPMW-3 modulation, generate the control signal for the four legs, and execute the DCT algorithm.

Starting from modulation index (m) and load frequency (f_{LOAD}), which are typically provided by a higher-level control loop to achieve the target motor speed and torque, the controller generates three sinusoidal references $\delta^*_{A–C}$. These signals are processed by the pulse centering module, yielding to the duty cycles $\delta_{A–C}$, which are shown in Fig. 12 at the top for the six sectors. According to AZSPWM-3, the control signals for legs A-C are obtained by comparing their duty cycle to either v_{TR} or $\overline{v_{TR}}$, as shown in Fig. 10. This requires a selection block to provide the proper carrier to each leg comparator in accordance with Tab. II. Similarly, the control signal of the dummy leg is generated as per the last row of the same table. The four control signals are then provided to the gate drivers, which in turn switch the power transistors the inverter is comprised of.

In addition, specific blocks are included in the controller to implement the DCT. During standard operation, delays are introduced to $ctrl_{A–D}$ using the precomputed matrices $\mathbf{D}_{rise}$ and $\mathbf{D}_{fall}$, storing the rising and falling delays, respectively. Such matrices are accessed based on the sector (row index) and the

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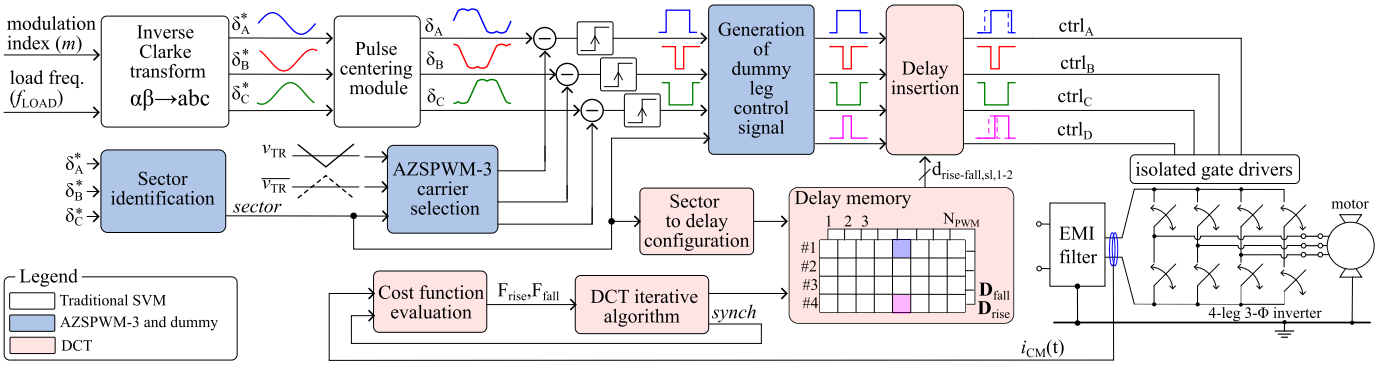
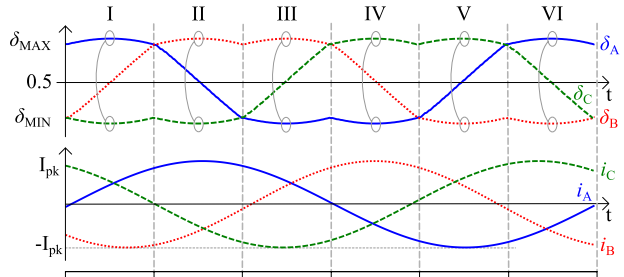


Fig. 11. Architecture of the motor drive controller including the blocks for AZSPWM-3, control of the dummy leg and the DCT.



Configuration	#1	#2	#1	#2	#1	#2
Primary	Leg C	Leg B	Leg A	Leg C	Leg B	Leg A
Secondary	Leg A	Leg C	Leg B	Leg A	Leg C	Leg B
Configuration	**#3**	**#4**	**#3**	**#4**	**#3**	**#4**
Primary	Leg B	Leg A	Leg C	Leg B	Leg A	Leg C
Secondary	Leg D	Leg D	Leg D	Leg D	Leg D	Leg D

Fig. 12. Reference signals (δ_{A-C}) and sinusoidal output currents (i_{A-C}) for the three main leg over a load period, i.e., across all six sectors. At the bottom, the four configurations for delay reusing have been reported for each sector.

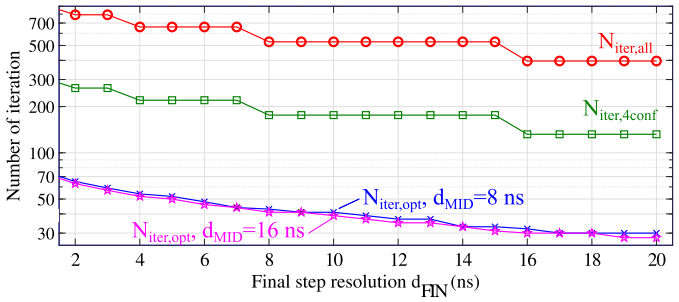


Fig. 13. Number of algorithm iterations for different strategies, i.e., brute force (circle), delay sector reuse (square) and coarse-fine strategy (star markers), when applied to the four-leg inverter.

specific PWM cycle within the sector (column index). The iterative four-leg algorithm is executed in steady state, i.e., with m and f_{LOAD} constant, and it populates $\mathbf{D}_{\mathrm{rise,fall}}$. From the scheme in Fig. 11, the DCT additional blocks do not affect the primary motor control, which is responsible for determining m and f_{LOAD}, as they only introduce small delays that are negligible compared to the duty cycles.

B. Proposed Strategy to Derive Delays in Six Sectors

To implement the DCT blocks shown in Fig. 11, a strategy is needed to extend the two-leg DCT algorithm (see Alg. 1) to the four-leg topology, while keeping the number of iterations low. As shown in Fig. 10, four complementary commutations can be identified in each PWM cycle, meaning that the DCT algorithm should optimize four delays. From Tab. II and Fig. 12, the pairs of opposite switching legs vary depending on the sector. Moreover, phase currents are not constant, meaning that the optimal delays are not expected to be constant within a sector. A first approach is to apply the `2legDCT` algorithm to each pair of complementary legs over the six sector. Given the number of PWM cycles (N_{PWM}) per sector

$$N_{\mathrm{PWM}} = \left\lfloor \frac{f_{\mathrm{SW}}}{6 f_{\mathrm{LOAD}}} \right\rfloor, \tag{17}$$

the total number of iterations becomes

$$N_{\mathrm{iter,all}} = 6 \cdot 2 \cdot N_{\mathrm{PWM}} \left\lceil \log_2 \left(\frac{s_{\mathrm{INIT}}}{s_{\mathrm{FIN}}} \right) \right\rceil, \tag{18}$$

where s_{INIT}, s_{FIN} are the initial and final step size of the two-leg DCT algorithm. For $s_{\mathrm{INIT}} = 128$ ns, $N_{\mathrm{iter,all}}$ is shown in Fig. 13 in circle markers with s_{FIN} in the 2 ns-20 ns range. This results in several hundreds iterations, leading to a large execution time.

It is worth noting that, over the six sectors, some patterns are repeated. For instance, in Sector I, leg A and C commutates complementarily, with $\delta_A \approx \delta_{MAX}$, $\delta_C \approx \delta_{MIN}$, resulting in i_A to increase from 0 to I_{PK} and i_C to decrease from I_{PK} to 0, as shown in Fig. 12. This scenario is repeated in Sector III and V, but with different legs. Conversely, in the even sectors, the currents of complementary main legs increase or decrease between 0 and $-I_{\mathrm{PK}}$. Thus, the delays found in Sector I (II) can be extended to III and V (IV and VI). These considerations allow to identify four configurations, denoted as #1-#4, which are reported at the bottom of Fig. 12. As `2legDCT` requires a primary and a secondary leg to optimize the delays, the assignment must be consistent over the sectors to allow for delay reuse. Such an approach allows to reduce the algorithm iterations to

$$N_{\mathrm{iter,4conf}} = N_{\mathrm{CONF}} \cdot N_{\mathrm{PWM}} \left\lceil \log_2 \left(\frac{s_{\mathrm{INIT}}}{s_{\mathrm{FIN}}} \right) \right\rceil, \tag{19}$$

where $N_{\mathrm{CONF}} = 4$. Although (19) is one third of (18), the number of iterations remains significant, as shown in Fig. 13 in square markers.

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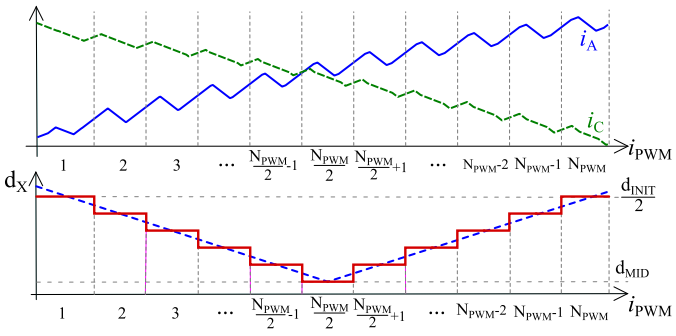

Fig. 14. At the top, load current for leg A and C in Sector I, as a function of the PWM cycle. At the bottom, the modulated initial step size for the fine phase optimization.

A further reduction in N_{iter} can be achieved using a coarse-fine approach. This strategy is discussed referring to Fig. 14, where the load i_A, i_C are shown at the top for Sector I. Although i_A increases from 0 A to around I_{PK} within the sector, much smaller load variations occur between adjacent PWM cycle, as $f_{LOAD} \ll f_{SW}$. Therefore, the rise and fall delays minimizing the CM current are not expected to vary significantly between adjacent PWM cycles. Thus, the optimization can be firstly performed on the central PWM cycle for each configuration (coarse phase), and later refined for each PWM cycle individually (fine phase). The initial step size for fine tuning (s_X) is proportional to the distance from the central PWM cycle, i.e.,

$$s_X(i) = s_{MID} + \frac{2}{N_{PWM}}\left(\frac{s_{INIT}}{2} - s_{MID}\right)\left|i - \frac{N_{PWM}}{2}\right|, \qquad (20)$$

where s_{MID} is that for $i = \frac{N_{PWM}}{2}$, and $\frac{s_{INIT}}{2}$, i.e., one half of the initial step in the coarse phase, is that at the sector boundary. The total number of iterations results in

$$N_{\text{iter,opt}} = N_{CONF}\left\lceil \log_2\left(\frac{d_{INIT}}{d_{MID}}\right)\right\rceil + N_{CONF}\sum_{i=1}^{N_{PWM}}\left\lceil \log_2\left(\frac{d_X(i)}{d_{FIN}}\right)\right\rceil, \qquad (21)$$

as shown in Fig. 13 in star markers. Compared to (18), it results in a tenfold reduction compared to the initial approach. Moreover, the sensitivity of $N_{\text{iter,opt}}$ to d_{MID} is negligible, thus simplifying its selection.

C. Iterative Algorithm to Populate the Delay Memory

With the DCT strategy defined, i.e., the reuse of four configurations and the coarse-fine approach, details on the four-leg DCT algorithm are discussed in what follows. As previously mentioned, the DCT algorithm aims at populating the delay matrices $\mathbf{D}_{\text{rise}}, \mathbf{D}_{\text{fall}}$, both sized $N_{CONF} \times N_{PWM}$, where each row corresponds to a configuration and each column to a PWM cycle within the sector. The pseudo-code is detailed in Alg. 2. The `4legDCT` procedure takes four input parameters, i.e., the initial (s_{INIT}), middle (s_{MID}) and final (s_{FIN}) step size, along with the number of PWM cycle per sector (N_{PWM}). It must be $s_{INIT} > s_{MID} > s_{FIN}$. During the initialization step (row 3), delay matrices are initialized to zero, and each configuration is associated with the sector (`sectConf`), the primary (`primLeg`) and the secondary leg (`secLeg`), according to Fig. 12. In the coarse phase (rows 4-10), the iterative two-leg DCT algorithm (`2legDCT`) is executed on the central PWM cycle of each configuration, i.e., $\frac{N_{PWM}}{2}$. A synchronization signal ensures the i_{CM} current is acquired for the PWM cycle under optimization. Then, the obtained delays are extended to all PWM cycle within the sector (rows 11-14). The last step is the fine optimization (rows 15-24), where `2legDCT` is repeated using as starting point the previously estimated delays. In such a way, all rise and fall delays for each pair of complementary switching leg are refined to minimize the CM current.

Algorithm 2 `4legDCT`

```
   Data: s_INIT, s_MID, s_FIN, N_PWM
   Result: Optimized delay matrices D_rise, D_fall.
1  begin
2      sectorConf=[1 1 2 2], primLeg=[C C A A]; secLeg=[A B D D];
3      D_rise ← 0, D_fall ← 0;
4      for i_c = 1 : 1 : N_CONF do
5          Set primary to primLeg[i_conf], secondary to secLeg[i_c]
6          Set synch at sect:sectorConf[i_c], PWM cycle: N_PWM/2;
7          (d_rise, d_fall) ← 2legDCT(s_init, s_mid,0,0);
8          D_rise(i_conf, N_PWM/2) ← d_rise;
9          D_fall(i_conf, N_PWM/2) ← d_fall;
10     end
11     for i_conf = 1 : 1 : N_CONF do
12         D_rise(i_conf, :) ← D_rise(i_conf, N_PWM/2);
13         D_fall(i_conf, :) ← D_fall(i_conf, N_PWM/2);
14     end
15     for i_c = 1 : 1 : N_CONF do
16         Set primary to primLeg[i_c], secondary to secLeg[i_c]
17         for i_PWM = 1 : 1 : N_PWM do
18             Set synch at sect:sectorConf[i_c], PWM cycle: i_PWM;
19             s_X ← (20);
20             (d_r, d_f) ← 2legDCT(s_X, s_FIN,
                 D_rise(i_c, i_PWM),D_fall(i_c, i_PWM));
21             D_rise(i_c, i_PWM) ← d_rise;
22             D_fall(i_c, i_PWM) ← d_fall;
23         end
24     end
25 end
```

D. On the Implementation of the DCT Algorithm

As shown in the block scheme in Fig. 11, the proposed DCT algorithm operates independently from the main motor controller, as it only inserts small delays to the PWM signals. To assess its suitability in a real-time implementation, the computation overhead introduced by the DCT algorithm should be compared against that of the motor controller. Assuming that addition (C_{sum}), shift (C_{shift}), and comparison (C_{comp}) require one CPU cycle, and memory read/write ($C_{\text{r/w}}$) requires two clock cycles, the execution cost in terms of CPU clock cycles of the 2-leg DCT (see Alg. 1) is

$$C_{\text{2legDCT}} \approx N_{\text{iter}}(C_{\text{shift}} + 6C_{\text{sum}} + 8C_{\text{comp}}) = 15N_{\text{iter}}. \qquad (22)$$

The computation cost of the 4-leg DCT algorithm is

$$C_{\text{4legDCT}} \approx N_{\text{conf}}(N_{\text{PWM}}(6C_{\text{rw}} + C_{\text{2legDCT}}) + C_{\text{2legDCT}}) \qquad (23)$$

Once the delay matrices have been populated, the run-time cost introduces by the DCT is that required to fetch the current delay from the memory and adding to the control signals, resulting in

$$C_{\text{DCT,running}} = 4(C_{\text{rw}} + C_{\text{sum}}) \qquad (24)$$

Therefore, $C_{\text{DCT,running}} = 12$ CPU cycles. Since motor controllers typically require more than 1000 clock cycles per PWM cycle [28], the run-time overhead of the proposed algorithm is negligible compared to that of the motor. Another

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TABLE III
NOMINAL PARAMETERS OF TEST CASE

Parameter	Value
Switching frequency (f_{SW})	32 kHz
Modulation frequency (f_{LOAD})	666 Hz
Inverter input supply voltage (V_{HS})	90 V
Phase peak current	25 A
Motor	100 kW PMSM in hairpin technology 180 N · m peak torque, max 12 000 rpm 6.6 nF CM capacitance

aspect to be addressed is that m and f_{LOAD} are not constant in practical applications, as they do depend on the mechanical load conditions. A viable approach to cope with torque and speed variations is to precompute the optimal delays over the expected operating range by repeating the proposed algorithm, and store them in lookup tables. At run-time, the delays can be retrieved directly or interpolated for conditions not mapped, ensuring a tracking speed suitable for the fast vehicle dynamics.

VI. EXPERIMENTAL VALIDATION

To assess the efficacy of the proposed technique in terms of CM EMI reduction, experimental measurements were carried out on a representative test-case. More details concerning the prototype and the EMI measurement test-bench are provided, followed by CM current measurements. Finally, the four-leg solution with DCT is compared in terms of cost and volume against state-of-the-art approaches to assess its benefits.

A. Case Study and Setup

A four-leg traction inverter was designed and prototyped to assess what proposed. It includes a DC link, four half-bridges, isolated gate drivers with dedicated DC-DC supplies, and an on-board controller. SiC power transistors were used for all four legs. As dummy leg does not carry load currents i_{A-C}, less-performing and lower-cost transistors were employed for the fourth leg. The inverter drives a PMSM motor in hairpin technology [23]. The nominal parameters of the system are reported in Tab. III. As far as the inverter controller is concerned, it implements both SVM and AZSPWM-3 modulations with dummy leg control. Referring to the architecture shown in Fig. 11, all controller blocks are included in the microcontroller firmware, except for the four-leg DCT algorithm and cost function evaluation block, which were implemented in Matlab [29]. A serial interface allows the DCT algorithm to modify, at run-time, the delay matrices stored on the microcontroller. The propagation delay from the microcontroller to the phase voltage commutation resulted in around 180 ns, while the rise/fall time ranged in (10 ns, 30 ns). To accurately align the output switching waveforms, a controller with a 700 ps PWM time resolution was selected, ensuring a resolution much lower than the minimum rise/fall time.

The test-bench is shown in Fig. 15(a), with a photograph of the experimental setup in Fig. 15(b). The HV

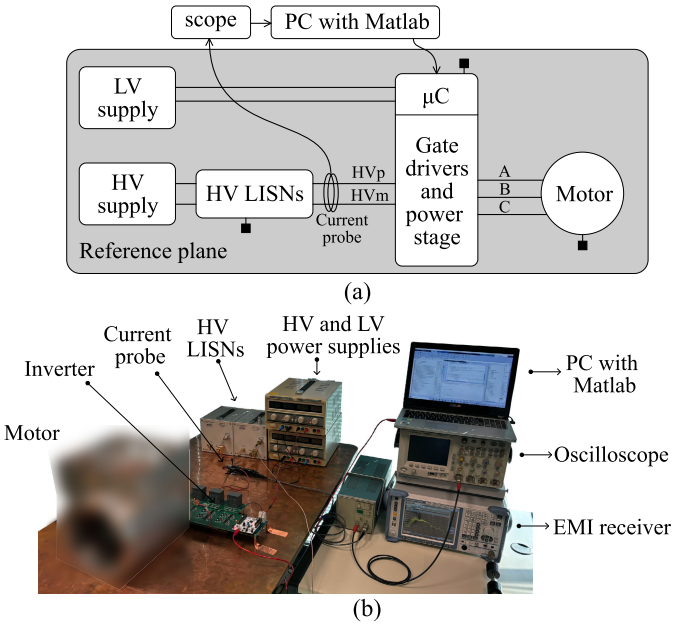

Fig. 15. (a) Block view and (b) photograph of the experimental setup for validating the proposed method.

voltage supply is provided to the inverter through two HV LISN, as prescribed by CISPR-25 [22]. A 20 MHz-bandwidth isolated current probe measures the CM current at the inverter input. Its output is connected to an oscilloscope, and the waveforms are acquired by a PC running the four-leg DCT algorithm. Once `4legsDCT` has been executed and the populated delay matrices stored in the inverter controller, conducted EMI measurement at the LISNs port can be performed, with both the PC and the oscilloscope disconnected.

B. CM Current Reduction

To gain insight on the operation of the algorithm, time-domain waveforms are shown in Fig. 16 during the different phases. These results refer to the commutation event of the second PWM cycle in Sector V, where leg A switches opposite to leg D (see Fig. 12). Before applying the DCT algorithm, the voltages of legs A and D are shown in (a) on the left. A misalignment of 64 ns exists between the two voltages, resulting in pulses in the CM current (on the right). After the coarse phase, the delay between the output waveforms is reduced to 16 ns, but the CM current peak remains significant. In the fine phase, the output waveforms are finely aligned (see Fig. 16(c) on the left), effectively achieving $\tau'_D \to 0$ (see (7)) and further reducing the CM current.

At sector level, the fall delays and the corresponding cost function (F_{fall}) for configurations #1 and #2 are shown in Fig. 17. Without applying `4legsDCT`, the cost function F_{fall} is shown at the bottom with circle markers. After the coarse optimization phase, F_{fall} significantly decreases at $\frac{N_{PWM}}{2} = 4$ (diamond markers), indicating that the algorithm successfully optimized this commutation. However, applying $D_{fall}(i, 4)$ uniformly to all PWM cycles may cause the CM current to

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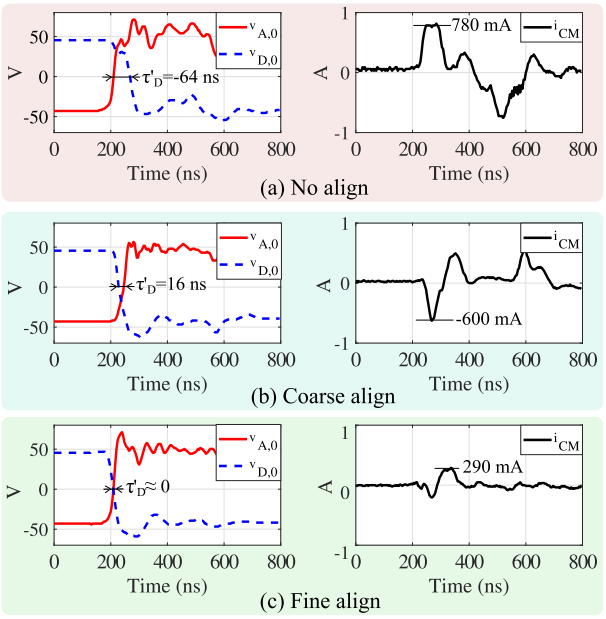

Fig. 16. Voltages at the inverter output (on the left) and corresponding CM current (on the right) when (a) the DCT algorithm is not applied, and at the end of (b) the coarse and (c) fine phase. By reducing the time misalignment from τ'_D=−64 ns to around 0 ns, i_{CM} reduces significantly.

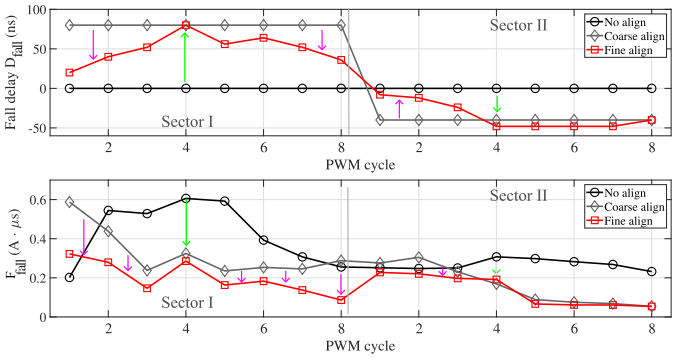

Fig. 17. Delay time (top) and cost function (bottom) for the falling edge commutations related to configuration 1 and 2.

increase, rather then decrease, particularly for PWM cycles far from the sector center. The fine phase addresses this issue by adjusting each commutation separately. The final F_{fall} values (square) are lower than those before applying the DCT (circle markers), thus confirming its effectiveness.

With the operation of proposed algorithm verified, measurement were performed on the prototype operating with traditional SVM, i.e., without the dummy leg and the DCT, to provide a reference case. The corresponding CM current i_{CM} is shown in Fig. 18 in solid line for (a) a load period and (b) with a zoomed view of one commutation. The CM current exhibits peaks as high as 2 A, with a waveform reflecting the CM impedance of the electrical machine (see Fig. 9(a)). With the dummy leg activated and the modulation switched to AZSPWM-3, the resulting CM current is that shown in dashed lines. After executing the delay optimization algorithm, the CM current exhibits peak values below 0.4 A, as shown

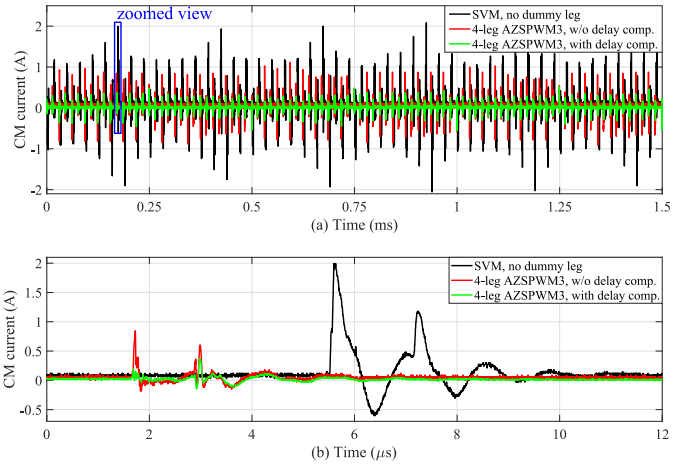

Fig. 18. CM current waveforms when the inverter drives the motor according to SVM (black), AZSPWM-3 with the dummy leg (red) and after applying the delay compensation algorithm (green).

in dotted lines. Indeed, the energy content associated with i_{CM} was significantly reduced, confirming that the proposed software-based method is effective in reducing the CM current by only adjusting the commutation edges. With the CM current waveforms acquired, their frequency spectra were evaluated to assess the reduction at the harmonics of the switching frequency. It resulted a 30 dB reduction at the fundamental and at the third harmonic when employing the proposed technique in place of the SVM case, thus assessing the efficacy of the technique at low-frequency.

C. Conducted EMI

Conducted EMI measurements were carried out to assess the effectiveness of the proposed technique. The current probe, oscilloscope and PC were thus removed from the setup not to impair EMI measurements. The spectra reported hereinafter were measured at the negative rail connected LISN, with EMI receiver configured according to CISPR-25 [22]. As a reference, traditional SVM was tested with the operating parameters reported in Tab. III, resulting in the black spectrum shown in Fig. 19. With the dummy leg activated and the modulation scheme switched to AZSPWM-3, the resulting spectrum is that shown in red. It is worth noting that this spectrum corresponds to the case without DCT, i.e., the red curves in Fig. 18. The first harmonic within the regulated frequency range, at 160 kHz, decreased by 27 dB compared to SVM. By applying the $D_{rise-fall}$ delay matrices obtained as discussed in Sect. VI-B, the conducted EMI spectrum is that shown in green in Fig. 19. The DCT further reduced conducted EMI, with a more significant impact in the 400 kHz-5 MHz range, with 15 dB to 25 dB reduction compared to SVM. Above 10 MHz, conducted EMI spectra for the three cases are nearly identical.

D. Comparison With State-of-the-Art Techniques

With the DCT algorithm assessed as shown in Fig. 19, additional investigations were carried out to highlight the benefits

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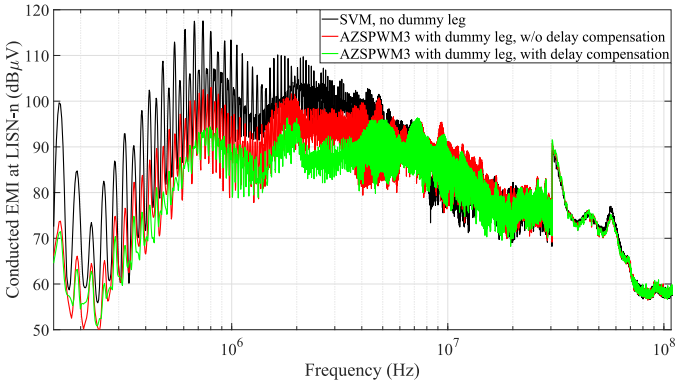

Fig. 19. Conducted EMI spectra at the measurement port of LISN connected to the negative rail for SVM (black), four-legs AZSPWM-3 without (red) and with (green) delay compensation.

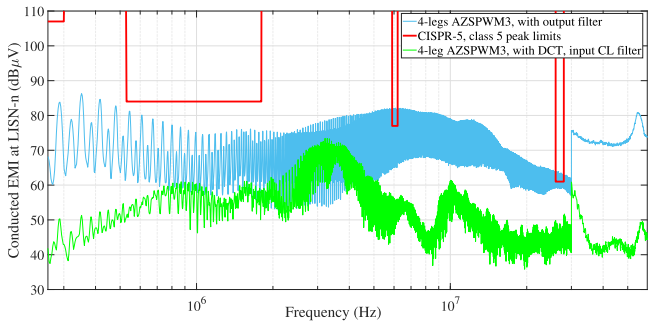

Fig. 20. Conducted EMI spectra for four-leg AZSPWM-3 with output filter (blue) and proposed technique (green).

TABLE IV
COMPARISON AMONG DIFFERENT SOLUTIONS

Solution	CM input filter	Output filter	Filter volume	Cost
Three-leg inverter with SVM	CLCL (2 x 50 µH, 4 x 50 nF)	No	365 cm^3	0%
Three-leg inverter with AZSPWM-3	CLCL (2 x 30 µH, 4 x 50 nF)	No	200 cm^3	-2%
Traditional four-leg inverter with AZSPWM-3	C (2 x 100 nF)	4 x LC	600 cm^3	+60%
Proposed technique	CL (1 x 30 µH, 2 x 100 nF)	No	106 cm^3	≈ 0%

of the proposed technique in terms of cost and volume. To this purpose, four different solutions were considered, i.e., three-leg SVM, three-leg AZSPWM-3, traditional four-leg with an output filter [19], and the proposed solution. For each of them, a filter was designed to ensure compliance with CISPR-25 class 5 limits. The main parameters of such filters, including an estimate of volume and cost, are summarized in Tab. IV. For the four-leg solutions (last two rows), the corresponding filters were assembled, and conducted EMI measured as shown in Fig. 20. What emerges is that the proposed solution, i.e., the dummy leg with the DCT, is compliant with the class 5, HV, peak CISPR-25 mask.

From Tab. IV, the conventional SVM approach requires a two-stage CL filter, while the three-leg AZSPWM-3 reduces the CM choke volume by 40%. In the traditional four-leg case, each switching leg must include a CL output branch, meaning that the output filter components introduce significant cost and volume overheads given the high-current application. In contrast, the proposed technique achieves compliance with a single-stage input filter, reducing the estimated filter volume by 70% compared to SVM. Since the dummy leg only drives Z_{DUMMY}, it can be implemented with smaller power transistors and less-performing auxiliary circuits, resulting in an cost increase of the inverter by around 6%. Such a cost overhead is counterbalanced by the reduced input-filter cost, resulting in no cost penalty compared to SVM.

Besides this analysis, the proposed technique should not alter significantly the performance of the motor drive system. To this purpose, investigations were conducted to assess the torque ripple variations under different scenario. At one half the nominal torque, the torque ripple was found to be 7.3% with SVM and 8.7% with AZSPWM-3 with or without the DCT. The difference in the motor performance can be mostly attributed to the different modulation strategy, and not to the dummy leg. To sum up, the proposed techniques offers better trade-off between CM EMI reduction, volume and cost compared to existing solutions, without impairing significantly motor performance.

VII. CONCLUSION

This paper investigated the DCT to reduce LF CM conducted EMI in four-leg traction inverters. The proposed approach is well-suited to be integrated in the motor controller, as it is only introduces small delays compared to the duty cycles and adds a negligible computation overhead. Experimental results on a high-voltage prototype demonstrated a 30 dB EMI reduction at 160 kHz and 15-20 dB reduction at higher frequencies, confirming the effectiveness of the approach.

A key benefit of the technique is the CM EMI reduction at the source, resulting in a 70% volume decreases of the input EMI filter without increasing the system cost. Future work will focus on implementing the cost-function evaluation using dedicated hardware, and embedding the four-leg DCT algorithm directly in the controller firmware to achieve real-time operation. Additional investigations will focus on a tracking phase to adapt delay values under varying load conditions, and a multi-objective optimization process to not only eliminate the delay misalignment but also match rise and fall times, further reducing high-frequency conducted EMI.

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