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Back-to-Back Testing Platform for Inverter Efficiency Mapping using Standard CAN Communication

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ABSTRACT The growing demand of power electronics for emergent applications has introduced significant challenges in testing and validation of power electronic converters. Traditional passive load-based testing approaches lack flexibility and fail to emulate realistic operating conditions, while advanced programmable setups are often prohibitively expensive and hardware-intensive. Back-to-back (B2B) testing configurations have emerged as a promising alternative, enabling internal power recirculation and dynamic control. However, existing B2B architectures suffer from key limitations, common mode circulating currents, and tightly coupled control platforms, which hinder modularity and full-power testing. This article presents a novel B2B test bench topology featuring zero common mode currents and enabling independent operation of the converter under test (CUT) with respect to the loading converter. The two converters are enabled and commanded via controller area network (CAN) bus communication, which is used exclusively to transmit the operating points to the converter control units and to allow fully independent control of each converter. The suppression of circulating common mode currents is instead ensured by the use of the transformer. The proposed solution provides high modularity and scalability, supporting flexible testing of a wide range of power converters under arbitrary load profiles without shared firmware or hardware resources. Furthermore, the platform requires an external DC source that needs to cover only for the overall system losses, and therefore, it is rated at a maximum 10% of the CUT-rated power, enabling high-power testing with low supply demand. Experimental validation demonstrates the effectiveness of the setup in achieving high-fidelity testing with minimal infrastructure requirements.

INDEX TERMS Back-to-back (B2B) converter, controller area network (CAN) bus communication, common mode (CM) current suppression, electric vehicles, modular test bench, power converter testing.

I. INTRODUCTION

The increasing demand of power converters for emergent applications, such as vehicle electrification, energy smartness, and efficient power supplies, requires proper testing and functional validation of these power converters, according to their mission profiles and specific operating points. As a result, the testing and validation of these converters have become more complex and expensive. Traditional testing approaches often rely on passive loads; however, these suffer from serious limitations in replicating realistic operating conditions. In particular, purely inductive loads allow to explore only very low power factor operating points, rendering them unsuitable for comprehensive efficiency testing. On the other hand, advanced setups involving high-power supplies and programmable load banks offer greater flexibility, but the associated costs are substantial.

A. STATE-OF-THE-ART SOLUTIONS AND THEIR LIMITATIONS

To overcome these limitations, various alternative testing methods have been explored in the literature. For instance, Wang et al. [1] proposed the emulation of an induction motor

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using a back-to-back (B2B) configuration of two converters: one regulates the three-phase voltage V_{abc}, while the other tracks the current references generated by a motor model. Despite the effectiveness of this approach in replicating realistic load conditions, the setup is affected by circulating common mode (CM) currents i_{cm} between the converters. To address this, Wang et al. [1] introduced synchronization of the fundamental waveforms via controller area network (CAN) Bus communication. A related research line exploits power-hardware-in-the-loop platforms for machine emulation. For example, Bigarelli et al. [2] evaluated *LCL* coupling networks to ensure stable and accurate emulation of permanent magnet synchronous machines. While this approach does not rely on a classical B2B configuration, it shares the goal of providing realistic converter loading conditions, but introduces additional challenges related to stability margins and coupling network design.

Moreover, the test bench in [3] is tailored for uninterruptible power supply systems and includes an additional step-up transformer. This element serves multiple functions: enabling DC-link charging, facilitating energy recirculation, and introducing leakage inductance to shape the current waveform and improve modeling accuracy. A more complex alternative is shown in [4], where circulating power is sent back to the grid using two electrical machines and additional control hardware for synchronization—an approach that further increases hardware requirements and complexity. As a result, in order to solve the problem, more focus has been investigated in the control routines. The industrial test platform proposed in [5] for end-of-line testing of industrial drives employs dual voltage-source inverters to emulate a virtual load for the converter under test (CUT). While a resonant controller enables this virtual load to function as a CM active filter, eliminating recirculating currents, its effectiveness is restricted to predefined frequencies. Consequently, this solution can only attenuate low-frequency disturbances due to bandwidth limitations in the control implementation.

Moreover, several other contributions in the literature address related aspects of coordinated control and CM mitigation. For example, Farajpour et al. [6] proposed carrier-based pulsewidth modulation (PWM) strategies to reduce CM voltage, while Liu et al. [7] introduced a coordinated control strategy between converters requiring high-speed communication links. Chen et al. [8] employed an *LCL* filter combined with coordinated control, whereas She et al. [9] explored hysteresis-based control for circulating current suppression. Moreover, a CM choke combined with carrier synchronization is demonstrated in [10]. Furthermore, Choi et al. [11] presented synchronized control routines for accelerated power cycling, and Li et al. [12] discussed zero-sequence current elimination methods in dual-inverter systems. Finally, early regenerative B2B configurations, such as in [13], highlight the potential of power recirculation, although without addressing CM suppression.

Despite the variety of existing approaches, two limitations remain recurrent in B2B-based testing platforms: 1) the need for tight synchronization or a shared controller between the two converters, which reduces modularity and prevents independent operation of the CUT; 2) the presence of circulating CM currents, especially when the converters share the same DC link, which leads to losses, electromagnetic interference (EMI) issues and accuracy degradation. In addition to the aforementioned contributions, recent literature has also highlighted the importance of accurately modeling and evaluating semiconductor losses. For example, the opposition method has been revisited in [14], where an enhanced loss estimation technique is proposed to improve the prediction accuracy of power semiconductor dissipation during testing. A practical high-power validation of the same methodology is demonstrated in [15], which applies the opposition method to a 100-kW three-phase wireless charging system, confirming its suitability for experimental characterization of converter behavior. Furthermore, the relevance of accelerated stress testing in power electronics is underlined by the early work in [16], where traction inverters are subjected to controlled overload conditions to assess their endurance and failure mechanisms. These studies collectively reinforce the need for testing platforms capable of reproducing realistic mission profiles, accurately capturing loss mechanisms, and enabling accelerated reliability evaluation.

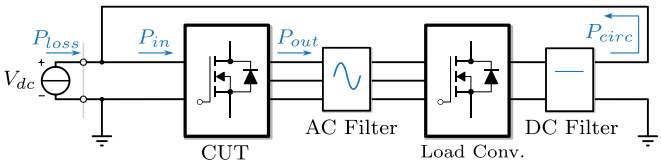


FIGURE 1. B2B converter test setup scheme.

In response to the need for simpler yet reliable testing strategies, Luo et al. [17] marked a significant milestone by proposing a topology inspired by an open-end winding motor, as presented in Fig. 1.

This configuration uses two inverters sharing the same DC link and connected through three coupling inductors that mimic motor windings. The main advantage of this topology is that it avoids the need for external load banks. Moreover, the power is internally recirculated between the converters, requiring only a small DC supply to compensate for system losses. However, several limitations emerge. First, this configuration does not allow full-power testing of the CUT, since the converters are sharing the same DC link. Second, CM circulating currents become a significant issue, especially in high-power scenarios, and mitigation strategies should be implemented. In [17], this is achieved through an external synchronization board, while in [11] and [18], a common controller board manages both converters, simplifying coordination but reducing modularity.

Although these solutions enable internal power recirculation and reduce the need for bulky passive loads, they remain limited in their ability to fully decouple the CUT from its load

TABLE 1. Summary of Literature on B2B Converter Configurations

Ref.	Regenerative setup	CM mitigation technique	Synch. requirement	Limitations
[1]	yes	None	AC voltage PLL	Emulation of induction motor, no mention about suppression of common mode currents, requires AC voltage measurement
[4]	yes	Motor-generator decoupling	None	Mechanical coupling
[6]	no	PWM modulation strategies	Tight	The reduction of the common mode voltage proposed is based on the control of the switching of both converters
[7]	yes	Coordinated control between converters and PWM synchronization	Tight	Control of both converters implemented in the same digital hardware
[8]	yes	Low frequency only by PI controller	AC voltage PLL	No high frequency CM mitigation, requires AC voltage measurement
[9]	yes	Unpredictable, switching frequency changes due to hysteresis control	Loose	Variable switching frequency and complex CM filter design
[10]	yes	CM choke + PWM synchronization	Tight	Carrier synchronization dependency
[11]	yes	Control routine + PWM synchronization	Tight	Same controller board for both converters
[13]	yes	PWM synchronization	Tight	CM current suppression not addressed
[17]	yes	Control + PWM synchronization	Tight	External additional board to synchronize the two converters
[18]	yes	Low frequency only by PI controller	AC voltage PLL	No high frequency CM mitigation, requires AC voltage measurement

in terms of both power and control. Most notably, the presence of a shared control board or tightly coupled synchronization strategy restricts system modularity and the ability to test different units independently. Moreover, the shared DC-link topology inherently introduces the risk of CM current generation, leading to EMI, increased power losses, and potential reliability issues, especially in high-voltage or high-power applications. The most relevant literature solutions on this topic are summarized and compared in Table 1. The comparison metrics focus on hardware and software requirements. First, it is important to verify whether the setup is regenerative to reduce the burden on the power supply. Then, the mitigation method for CM is compared. This is significant because it requires either a hardware solution (filters) or software modifications (typically PWM synchronization or low-frequency mitigation using proportional integral (PI) regulators only). Finally, the communication burden between the two converters in the setup is evaluated. Many solutions rely on tight PWM synchronization between the converter units, which decreases the flexibility of the solution and the ability to adapt it to other CUT.

B. PROPOSED SOLUTION

To address these limitations, this work proposes a B2B testing architecture based on two fully independent converters, each running its native control firmware, and coordinated only through a low-bandwidth CAN interface. This allows the CUT to operate exactly as in real applications—without code modification or shared controller—while the loading converter emulates arbitrary operating points. A transformer inserted between the converters suppresses circulating CM currents and enables full-voltage, full-modulation-range operation of

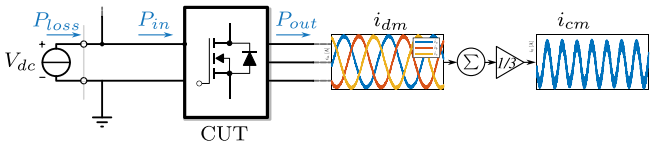


FIGURE 2. Illustration of CM i_{cm} and differential-mode i_{dm} currents in a B2B configuration.

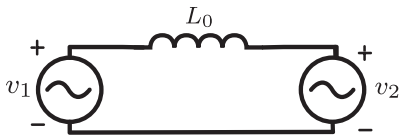


FIGURE 3. Simplified CM equivalent circuit of the B2B test configuration.

the CUT, allowing complete efficiency mapping with minimal external power consumption.

Since the configuration relies on a low-frequency transformer, the minimum achievable fundamental frequency is bounded by its magnetization current and core characteristics.

The resulting setup allows comprehensive, high-fidelity testing with minimal hardware complexity and strong flexibility in integrating converters of different architectures, control schemes, or power levels.

The rest of this article is organized as follows. Section II analyzes the main challenges of CM and differential-mode currents in B2B configurations and reviews existing mitigation strategies. Section III introduces the proposed test bench architecture and discusses its control implementation. Section IV presents the experimental validation, including both CM current suppression tests and efficiency mapping of a high-power converter. Finally, Section V concludes this article by highlighting the advantages and potential applications of the proposed solution.

II. CM AND DIFFERENTIAL MODE EQUIVALENT AND FILTERING CONFIGURATIONS

As previously introduced, the use of a shared DC link between two converters in a B2B test configuration provides clear benefits in terms of reduced power demand from the external supply. However, this architecture introduces a number of critical challenges. The main challenge is the presence of undesired low-frequency and high-frequency current components, particularly CM i_{cm} and differential-mode i_{dm} currents, as shown in Fig. 2. The differential-mode current, i_{dm}, is the output load current generated by the differential-mode voltage, defined as the voltage difference between any two phase terminals. It contains the fundamental output frequency f_0, as well as harmonic components arising from the PWM switching process and the interaction with the load. In contrast, the CM current, calculated as their mathematical average values, is related to the CM voltage generation of the inverter. This voltage can be deliberately injected, for instance, to achieve higher modulation indices or to implement zero-sequence voltage injection techniques. Especially in the case of a B2B configuration, the presence of a shared DC bus creates a natural return path for CM currents that can reach significant values. Such currents can cause increased conduction and switching losses, generate unwanted electromagnetic emissions, and ultimately degrade the accuracy and reliability of the test results. This issue is particularly severe when testing complete power converters that include EMI filters at their input stage. Indeed, these EMI filters are typically designed to tolerate only limited levels of i_{cm}, and may be damaged or operate improperly when subjected to the higher currents typically observed in this configuration. Moreover, the interaction between converters through the shared DC link leads to the generation of both i_{cm} and i_{dm} ripples, both of which must be minimized to ensure robust operation and reliable test data. As mentioned in the literature, a significant source of i_{cm} is related to the lack of synchronization of the carriers of the two converters and the dead-time for power switches belonging to the same leg [19], [20]. Furthermore, the third harmonic injection naturally generates a CM recirculating current.

To clarify the mechanism behind the generation and suppression of the CM circulating current in the adopted B2B configuration, a simple CM equivalent circuit can be derived. The proposed model, as shown in Fig. 3, consists of two CM voltage sources, representing the CM voltages generated by each inverter (the CUT and the load converter), and an equivalent CM inductance L_0 of the loop. The inductance L_0 accounts for all the elements that contribute to the impedance seen by the CM current (coupling inductors, L or LCL filters, transformer leakage inductance, and possible CM chokes). The CM capacitances are neglected in this analysis, since their values are difficult to estimate or to measure accurately. Moreover, they do not significantly affect the first-harmonic behavior, which is the focus of this model.

If only the first harmonics of the CM voltages v_1 and v_2 are considered, then they can be expressed as

$$v_1 = V_{\mathrm{CM}} \sin(\omega_1 t + \varphi_1) \tag{1}$$

$$v_2 = V_{\mathrm{CM}} \sin(\omega_1 t + \varphi_2) \tag{2}$$

where V_{CM} is the amplitude of the first harmonic of the CM voltage generated by each inverter and ω_1 is the fundamental frequency of the CM voltage ($\omega_1 = \omega_{\mathrm{sw}}$ for three-phase two-level inverters).

The amplitudes are assumed to be equal, since the DC-link voltage, modulation index, and switching frequency of the two converters are the same or at least very similar. Without loss of generality, the phase of the first converter CM voltage is set to $\varphi_1 = 0$. The resulting CM voltage stress across the loop is then given by

$$v_{\mathrm{CM}}(t) = v_1 - v_2 = V_{\mathrm{CM}} [\sin(\omega_1 t) - \sin(\omega_1 t + \varphi_2)]. \tag{3}$$

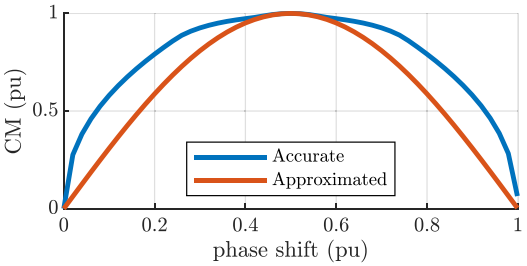


FIGURE 4. Comparison between normalized CM voltage stress obtained from detailed numerical evaluation and from the simplified first-harmonic model as a function of the phase shift between the voltages generated by the two converters.

By applying trigonometric identities, (3) can be rewritten as

$$v_{\mathrm{CM}}(t) = 2V_{\mathrm{CM}} \cos\left(\omega_1 t + \frac{\varphi_2}{2}\right) \sin\left(-\frac{\varphi_2}{2}\right). \tag{4}$$

Therefore, the magnitude of the CM voltage stress in the loop is proportional to $\left|\sin(\varphi_2/2)\right|$ and depends directly on the phase shift φ_2, which is ultimately dictated by the converters' PWM carriers and switching patterns.

By neglecting the CM capacitances, the circulating CM current can be approximated as

$$i_{\mathrm{CM}}(t) \approx \frac{v_{\mathrm{CM}}(t)}{j\omega_1 L_0} \tag{5}$$

so that its peak value is

$$I_{\mathrm{CM,pk}} \approx \frac{2V_{\mathrm{CM}} \left|\sin\left(\frac{\varphi_2}{2}\right)\right|}{\omega_1 L_0}. \tag{6}$$

This design-oriented expression makes it possible to estimate a priori the circulating current amplitude from the setup parameters. Given a maximum acceptable CM current $I_{\mathrm{CM,max}}$, the required equivalent inductance can be directly obtained as

$$L_0 \geq \frac{2V_{\mathrm{CM}} \left|\sin\left(\frac{\varphi_2}{2}\right)\right|}{\omega_1 I_{\mathrm{CM,max}}}. \tag{7}$$

In the proposed setup, this constraint is satisfied by the combination of the coupling inductors, the AC and DC filters, and the transformer leakage inductance, ensuring that the CM current remains well below the admissible limit across the operating range.

Although the model is intentionally simple and only considers the first harmonic of the CM voltage, it matches well the numerically obtained results when the actual switching waveforms of both converters are used. This is illustrated in Fig. 4, which compares the normalized CM voltage stress predicted by the proposed model with the one obtained from a detailed numerical evaluation. The simplified model accurately captures the minima and maxima of the CM stress as a function of the phase shift, which is sufficient to identify the phase shifts leading to the worst common mode conditions and to guide the design of the mitigation techniques discussed in the remainder of this section.

From (3) and (4), it is evident that mitigation can be achieved either by reducing the CM voltage term $V_{\mathrm{CM}}|\sin(\varphi_2/2)|$ (through appropriate PWM and carrier synchronization) or by increasing the equivalent inductance L_0 of the CM path (through suitable passive filtering and transformer design). The filtering configurations analyzed in the following subsections implement these two design levers in different ways.

To address these challenges, several filtering strategies and control routines have been investigated, aiming to suppress or decouple the effects of these disturbances. This chapter presents and analyzes four main suppressing solutions, selected for their relevance in B2B converter test systems.

1) *Inductive filter:* A basic configuration using three-phase inductors on the AC side to attenuate high frequency i_{dm} disturbances, as shown in Fig. 5(a).
2) *LCL filter:* It provides a more effective alternative to the simple inductive filter that has better high-frequency attenuation and achieve the decoupling between the two converters avoiding a direct interaction of the two PWMs, as shown in Fig. 5(b).
3) *AC and DC common mode choke (CMC) filters:* A supplementary filter that can be combined with the above strategies to further suppress the i_{cm} current, as shown in Fig. 5(c) and (d).
4) *Active filtering:* Additional inner control routine can be implemented to suppress the recirculating low-frequency CM current, based on the introduction of a resonant controller at the i_{cm} current frequency.
5) *Transformer:* The most robust solution in terms of electrical isolation, capable of fully blocking CM currents and attenuating differential-mode noise via leakage inductance, as shown in Fig. 5(e). Nonetheless, practical limitations, such as saturation, bulkiness, and limited low-frequency performance, must be carefully considered.

A. INDUCTIVE FILTER AND LCL FILTER

The implementation of an inductive filter in a B2B configuration offers a simple and practical solution. As illustrated in Fig. 5(a), the proposed design aims at enhancing the power quality by attenuating current ripple, preventing direct connection between the converters.

Despite its simplicity, this configuration delivers limited harmonic attenuation due to the impedance of $Z_L = sL$ with an attenuation rate of -20 dB/dec [21], and therefore requires high switching frequencies to mitigate high-frequency harmonics [22]. Furthermore, substantial control effort is required to suppress undesired CM currents.

Since the use of a simple L filter is not achievable to remove the high-frequency harmonics, multiple filter stages are usually required. A solution that became the standard in voltage source converter (VSC) applications is the *LCL* third-order filter [21], [23], [24]. Furthermore, the design of this kind of filters has been widely investigated in the literature [25], [26]. In a B2B configuration, it can be easily included in the

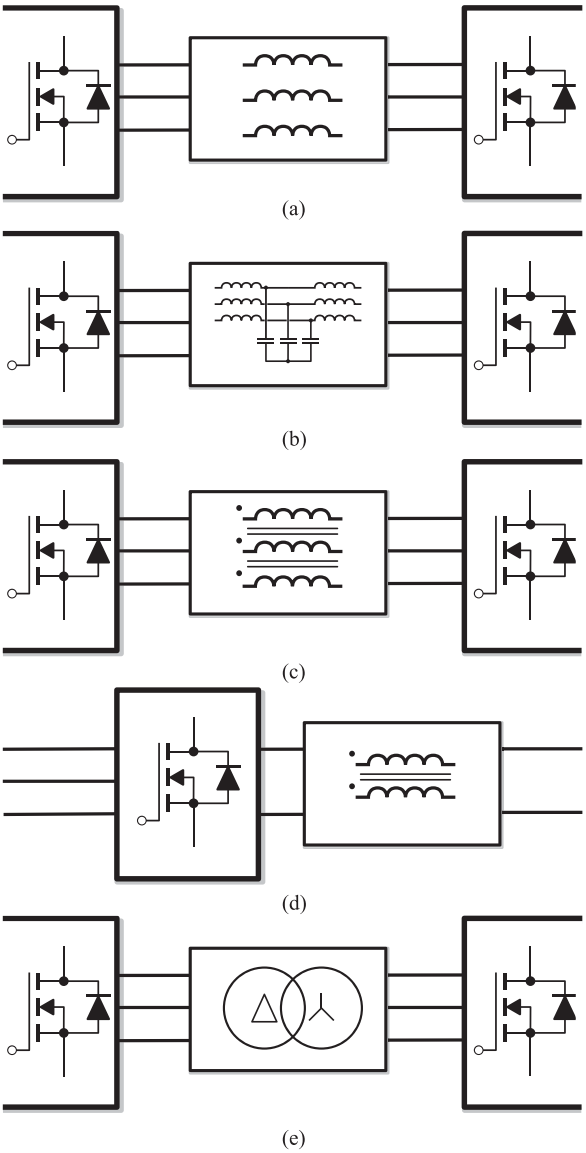


FIGURE 5. Presented filter configurations. (a) *L* filter. (b) *LCL* filter. (c) CM choke on the AC side. (d) CM choke on the DC side. (e) Transformer.

system, as presented in Fig. 5(b). Compared to the simpler *L* filter, it requires a passive component design, but is able to filter higher order harmonics [27]. However, the use of an *LCL* filter may generate stability problems due to resonances [28]. Consequently, an additional control routine is included in the system.

As a summary, *L* and *LCL* filters represent a good solution to suppress the undesired high-frequency differential circulating current i_{dm} and to decouple the PWM of both converters, but do not represent a valuable option to mitigate the i_{cm} current.

B. CM CHOKE IMPLEMENTATION

The implementation of a CM choke represents an effective solution to mitigate the impact of CM circulating currents in a B2B converter configuration [29]. In [30], an accurate design and specifications for CM filters is presented. As illustrated in Fig. 5(c) and (d), this choke can be inserted either on the AC side, between the two AC converter's side, or on the DC side, between the recirculating path of the two. When placed on the AC side, the CM choke attenuates low-frequency and high-frequency CM currents propagating toward the three-phase lines.

Over the years, the literature has proposed various integrated choke designs capable of attenuating both CM (i_{cm}) and differential mode (i_{dm}) current components [31], [32], [33], [34], aiming to improve EMI performance without significantly increasing the system footprint.

C. ACTIVE FILTERING

In order to mitigate the CM current i_{cm}, several control schemes have been proposed [7], [9], [11], [17], [18], mostly derived from the need to suppress zero-sequence current recirculation in open-winding machines [35], [36], [37], [38]. In [35], three modulation techniques for CM current suppression are analyzed. Compared to the case without any compensation, the implementation of an additional PI control loop can significantly reduce the total harmonic distortion, while the best performance is achieved using a dead-time technique.

However, dead-time compensation has practical limitations, especially in a B2B configuration. As an open-loop strategy, it lacks feedback to adapt the compensation to changing load conditions, making accurate zero sequence voltage cancellation difficult [35]. Furthermore, it requires a direct high speed communication between the two converter (i.e., a common control board) that is not always feasible while testing a converter. In [5], the suppression of the i_{cm} current is performed through the implementation of a resonant controller. Its effectiveness is similar to the introduction of a CM choke in the system, while it is extremely dependent on the fundamental frequency of the converter. Furthermore, it is strongly dependent on the tuning of the resonant controller.

For clarity, the resonant controller later on used in this work is detailed here. The controller operates on the measured CM current and is designed to attenuate the low-frequency component that appears when the two converters switch at the same frequency but with an uncontrolled PWM phase shift.

The tuning frequency of the resonant controller is selected as three times the fundamental frequency, $f_{\mathrm{res}} = 3f_0$, since this harmonic represents the dominant low-frequency component of the circulating CM current in a B2B configuration without synchronization.

The controller adopts the standard ideal resonant structure

$$G_{\mathrm{res}}(s) = K_{\mathrm{res}} \frac{2\omega_{\mathrm{res}} s}{s^2 + \omega_{\mathrm{res}}^2} \tag{8}$$

where $\omega_{\mathrm{res}} = 2\pi f_{\mathrm{res}}$.

This transfer function provides a very high gain at ω_{res} and negligible gain at DC, which is suitable for selectively suppressing the targeted harmonic of the CM current. The

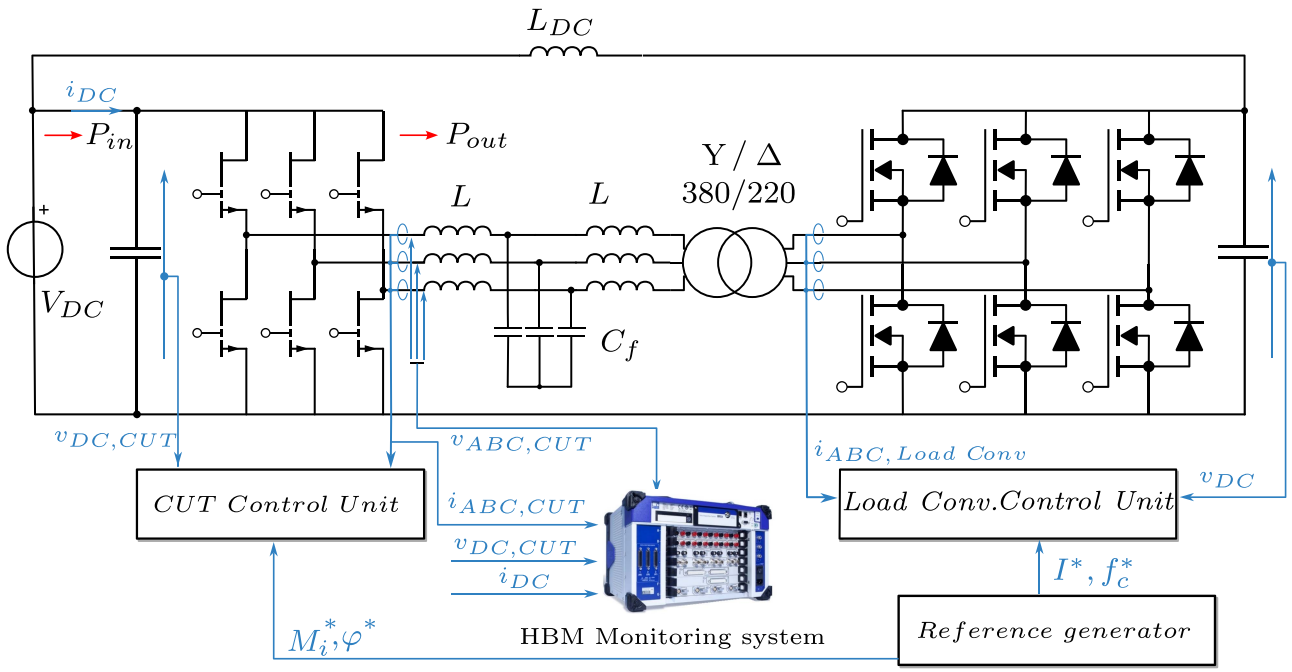


FIGURE 6. Schematic of the B2B testing configuration with the CUT [with gallium nitride (GaN) devices] and the load converter (with SiC devices).

continuous-time controller (8) is then discretized and implemented following the same sinusoidal–integrator methodology adopted in [5].

III. PROPOSED B2B TESTING SOLUTION

The proposed approach for testing power converters is presented in Fig. 6. The proposed solution uses the B2B configuration with common DC link to exploit the main advantage of this solution in terms of reduced power consumption. The primary elements consist of the CUT and a load converter operating as an active load. These converters are interconnected through a network of three coupling inductors (L) and a three-phase delta-wye (Δ–Y) transformer, establishing a controlled power recirculation path. Furthermore, the setup aims to achieve a full test of the converter by minimizing the implementation of additional hardware, avoiding the modification of the control scheme of the power converter and allowing the user the choice of any power converter as a load. Indeed, to achieve this goal, the full setup communication is performed through a CAN line communication between the two converters.

A fundamental advantage of this configuration resides in the minimized DC-link power supply requirements. The DC voltage source (V_{dc}) must provide only the aggregate system losses (P_{loss}), which constitute a minor fraction of the total recirculated power (P_{rec}). Consequently, the experimental setup achieves high-power testing capability without commensurate grid power consumption, enhancing energy efficiency, and reducing operational costs.

The inclusion of a Δ–Y transformer allows complete cancellation of the i_{cm} current recirculation between the inverters, providing significant additional benefits, such as reduced conducted emissions [39]. Any residual circulation inside the delta connection of the transformer is not relevant for the CUT operation and does not affect the accuracy or safety of the tests.

A second advantage of the introduction of the Δ–Y transformer is the possibility of increasing the effective modulation range of the CUT. In a conventional B2B configuration with direct connection, both converters generate approximately the same line-to-line voltage for a given DC link and therefore they have the same modulation index limit. By contrast, the voltage transformation introduced by the transformer allows the CUT to operate at a higher modulation index (i.e., up to 1.15), while the load converter operates within its nominal modulation range.

In three-phase power systems, transformers with a Δ–Y configuration are widely employed for stepping voltages up or down. In such a configuration, the primary winding is connected in a Δ arrangement, while the secondary is connected in a Y arrangement. If $N = \dfrac{N_\Delta}{N_Y}$ denotes the turns ratio, where N_Δ and N_Y are the number of turns per phase on the delta and wye sides, respectively, then the relation between the line currents and line voltages is expressed as in the following:

$$I_{\text{line},Y} = \frac{N}{\sqrt{3}} I_{\text{line},\Delta} \tag{9}$$

$$V_{\text{line},Y} = \frac{\sqrt{3}}{N} V_{\text{line},\Delta}. \tag{10}$$

Therefore, the overall voltage and current transformation from the Δ to the Y side includes both the turns ratio N and the $\sqrt{3}$ factor due to the differing phase-to-line relationships.

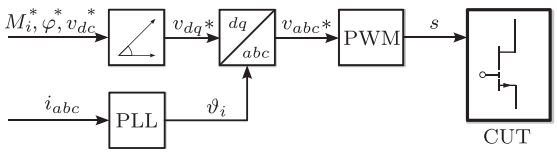


FIGURE 7. CUT converter control scheme.

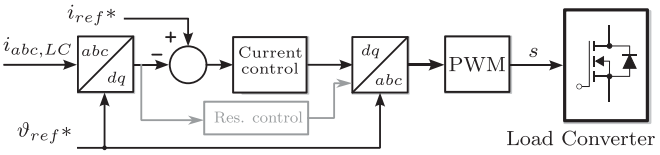


FIGURE 8. Load converter control scheme.

As the two converters are supplied by the same DC-link voltage V_{dc} and use a standard three-phase carrier-based PWM, the fundamental line-to-line voltage can be written as

$$V_{\text{line},Y} = k\, M_{\text{CUT}} V_{\text{dc}} \qquad V_{\text{line},\Delta} = k\, M_{\text{Load Conv.}} V_{\text{dc}} \tag{11}$$

where $M_{\text{Load Conv.}}$ and M_{CUT} are the modulation indices of the load converter and the CUT, respectively, and k is the PWM gain factor. Combining these expressions with (10), and assuming $N = 1$ as in our case, gives

$$k\, M_{\text{CUT}} V_{\text{dc}} = \sqrt{3}\, k\, M_{\text{Load Conv.}} V_{\text{dc}} \tag{12}$$

$$M_{\text{CUT}} = \sqrt{3}\, M_{\text{Load Conv.}} \tag{13}$$

In the experimental prototype, the adopted Δ–Y transformer has a nominal 380/220 V rating with $N = 1$, resulting in an approximately $\sqrt{3}:1$ line-to-line voltage ratio between the two sides; hence, the above equations mainly provide a design guideline for future implementations with nonunity transformer ratios. It must be noted that the transformer is a conventional low-frequency transformer, designed to sustain the fundamental frequency output of the CUT.

A. CONTROL IMPLEMENTATION

As mentioned before, another interesting aspect of this implementation is that no complex control loop scheme needs to be implemented in the controller, as the i_{cm} current is completely suppressed by the transformer and no resonant or active CM controller is required. The two converters are operating independently, using two current control schemes that are shown in Figs. 7 and 8, respectively.

The CUT control is based on an open-loop voltage control strategy, as illustrated in Fig. 7. The converter operates at a constant switching frequency of 50 kHz, with the control implemented in the synchronous rotating reference frame (d–q axes). Through CAN line communication, the CUT receives the desired modulation index and phase, which are used to generate the reference voltage vector v_{dq}^* by means of a polar transformation.

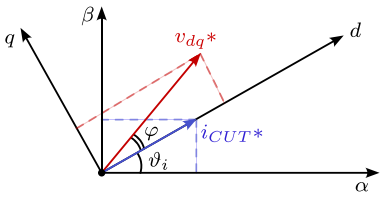


FIGURE 9. Rotating d–q vector control scheme.

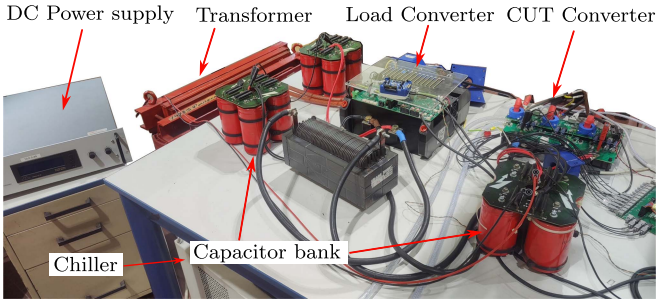


FIGURE 10. Experimental setup.

A phase-locked loop (PLL) synchronization scheme is employed to extract the reference angle ϑ_i from the measured inverter currents i_{abc}. This angle is then used to perform the inverse Park transformation, enabling the computation of the voltage vector that is provided to the PWM block implementing the modulation technique. For this work, the PWM block implements a carrier-based space vector modulation solution.

On the load side, the converter receives, via CAN communication, the reference current i_{ref}^* and the angle ϑ_{ref}^*, which is the same PLL-based angle generated previously. The reference current is then processed within a closed-loop current control strategy, as depicted in Fig. 8. Fig. 9 summarizes the involved vectors presented in the control scheme.

The d-axis is phase-locked to the rotating current vector imposed by the loading converter through a PLL subsystem.

The reference and measured current vectors are used in a closed control loop scheme by the load converter, which will provide the desired currents for the CUT.

The controller of the load converter uses a simple closed-loop current control scheme, as presented in Fig. 8. It is important to note that the CUT should have a switching frequency higher or equal to the load converter. If not, the dimensioning of the filters could be compromised, resulting in a higher current ripple.

IV. EXPERIMENTAL VALIDATION

The following two experimental verifications have been performed on a 30-kW GaN inverter prototype.

1) Evaluation of all presented CM suppression strategies, without the use of a transformer.
2) Efficiency mapping for the CUT full operating range, using the proposed testing configuration with a transformer. Both experimental campaigns were conducted

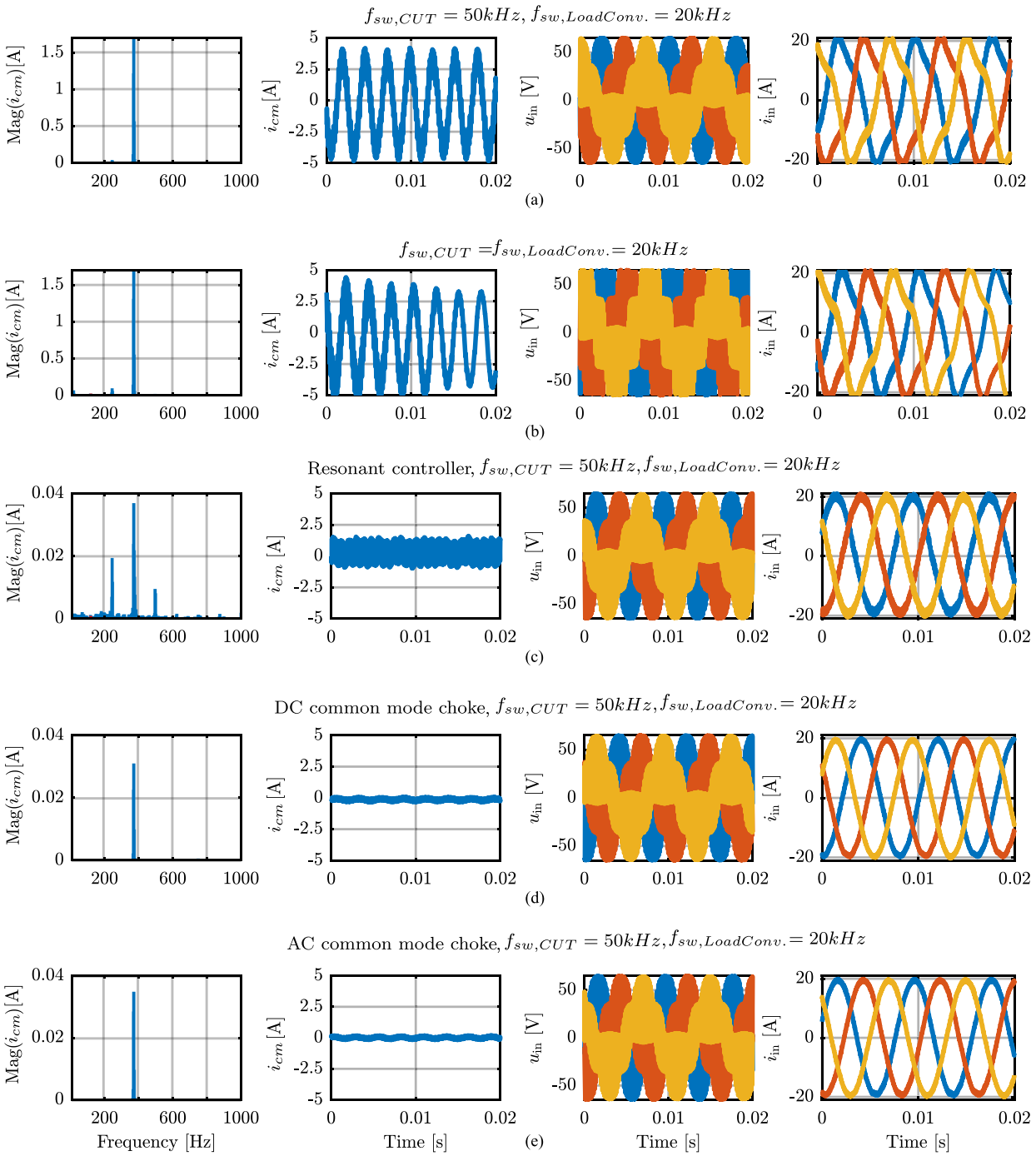


FIGURE 11. Experimental data comparison for different CM mitigation techniques. From left to right: Fast Fourier Transform (FFT) of icm, time-domain icm, CUT phase voltages $v_{a,b,c,CUT}$, and CUT phase currents $i_{a,b,c,CUT}$. (a) Experimental results with different switching frequencies ($f_{sw,CUT} = 50$ kHz, $f_{sw,Load} = 20$ kHz). (b) Experimental results with identical switching frequencies ($f_{sw,CUT} = f_{sw,Load} = 20$ kHz). (c) Resonant controller, ($f_{sw,CUT} = 50$ kHz, $f_{sw,Load} = 20$kHz). (d) DC-side common-mode choke, ($f_{sw,CUT} = 50$ kHz, $f_{sw,Load} = 20$ kHz). (e) AC-side common-mode choke ($f_{sw,CUT} = 50$ kHz, $f_{sw,Load} = 20$ kHz).

using a dedicated test setup, described in the following section.

A. EXPERIMENTAL SETUP

A comprehensive test setup has been implemented to support both experimental tasks. An overview of the complete laboratory setup is provided in Fig. 10. This setup includes the CUT and the load inverter. Depending on the experiment, the interconnection and filtering components change, as detailed below. The control schemes described in Section III for the CUT and the load inverter have been implemented during all tests.

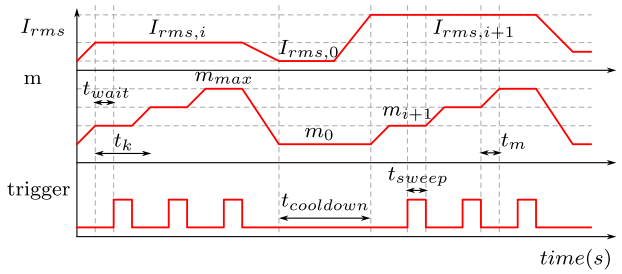
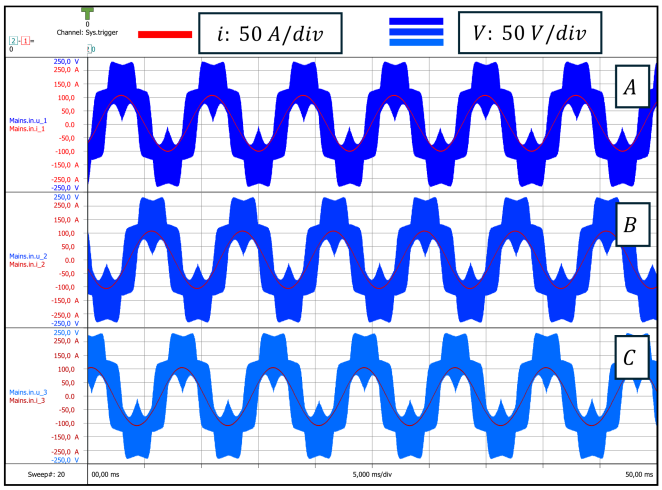
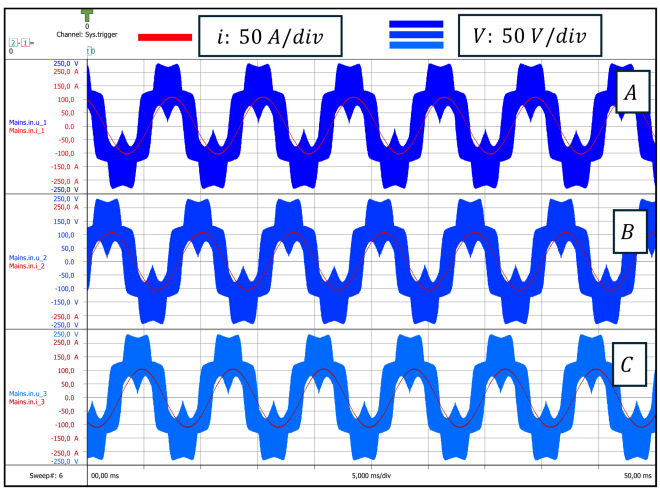


FIGURE 12. Test map including cool-down periods between different target points.



(a)



(b)

FIGURE 13. Measured line-to-phase voltage and current waveforms from the CUT. (a) $\varphi = 0°$. (b) $\varphi = 20°$.

In the first test (see Section IV-B), focusing on CM current suppression strategies, the CUT is connected directly to the load inverter through an *LC* output filter and, optionally, a CM choke. In this case, the transformer is not included in the setup, to allow clearer observation of circulating current phenomena and their mitigation.

In the second test (see Section IV-C), aimed at mapping the efficiency of a high-power converter, the CUT and the load inverter are connected through a transformer, as presented in Fig. 6, enabling safe and accurate measurements at higher power levels. The efficiency map is obtained at variable power factor, as the proposed CUT control scheme allows synchronization with the load current through a PLL, as presented in Fig. 7.

To ensure consistency in the communication layer, any CAN-compatible device can be used to transmit references and acquire measurements, which represents one of the advantages of the proposed architecture. For the experiments, both a dSPACE unit (for the first test) and a PC running MATLAB equipped with a PEAK USB–CAN interface (for the second test) have been employed. The adoption of a standard CAN protocol confirms the flexibility and portability of the proposed solution across different control and communication hardware.

Table 2 summarizes the key components involved in both test configurations.

TABLE 2. Main Components of the Experimental Setup for the Two Test Campaigns

Test 1 – CM suppression	
CUT	GaN-based converter rated for 30 kW $V_{dc} = 400$ V
Load converter	SiC-based 175 kW inverter operating as active load
LC filter	Output filter with L and C_f per phase
CMC	Ferrite-core three-phase choke, optionally placed on AC or DC side
Acquisition system	HBM high-precision logger for voltage and current
Communication interface	CAN-based communication
Test 2 – Efficiency mapping	
CUT	GaN-based converter rated for 30 kW
Load converter	SiC-based 175 kW converter operating as active load
Transformer	50 kVA transformer
Acquisition system	HBM high-precision logger for voltage and current
Communication interface	CAN-based communication
Control synchronization	PLL-based phase alignment and power factor control

B. EVALUATION OF CM MITIGATION TECHNIQUES

In the first set of experiments, the focus is on the characterization and mitigation of CM currents (i_{cm}). Several strategies are implemented and compared, including the following:

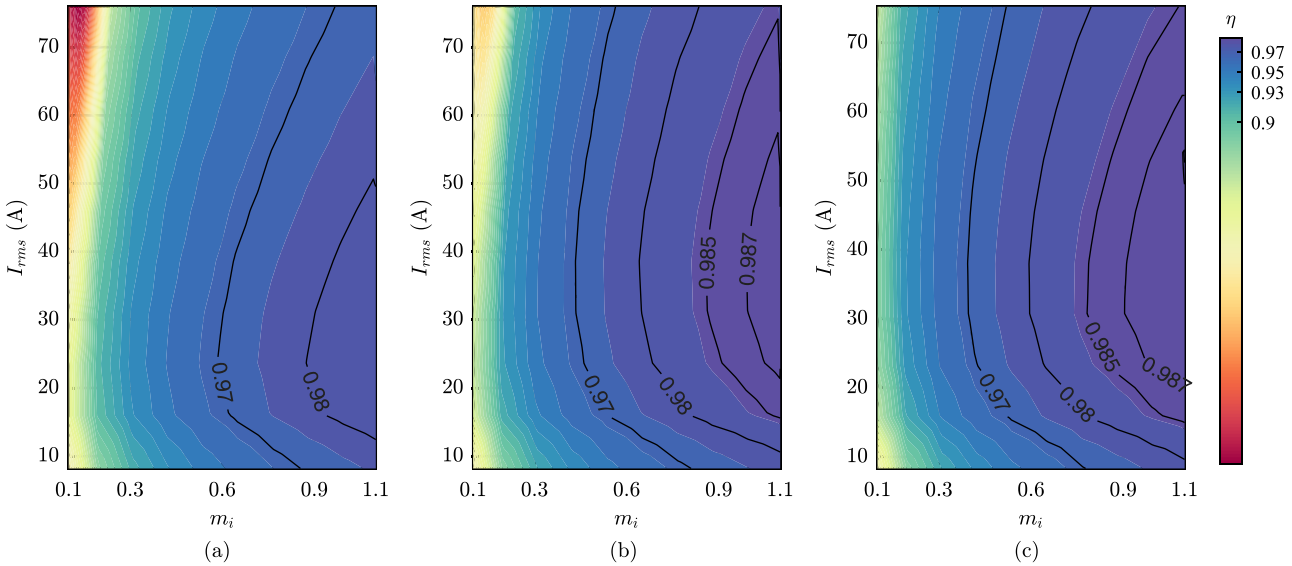


FIGURE 14. **Efficiency mapping of the 30-kW CUT at $V_{in} = 400$ V under varying modulation index and output current. (a) Converter efficiency, including losses introduced by the test-bench *LCL* filter and connecting cables (voltage measured across filter capacitors). (b) Partially compensated efficiency: same measurement as (a) but with I^2R losses of the filter inductors and cables analytically subtracted. (c) True CUT-only efficiency, measured directly at the converter output terminals, excluding all test-bench-related losses. *Only (c) represents the intrinsic converter performance; (a) and (b) illustrate the impact of the measurement setup on the perceived efficiency.***

TABLE 3. **Component Values Used in the CM Mitigation Experiments**

Component	Value
Inductance L	300 μH
LCL inductance L	300 μH
LCL capacitor C_f	40 μF
AC CMC inductance $L_{\mathrm{CM,AC}}$	1.48 mH
DC CMC inductance $L_{\mathrm{CM,DC}}$	1.48 mH
Resonant gain K_{res}	100

1) Baseline operation without any suppression technique with different switching frequencies of the two converters $f_{\mathrm{sw,CUT}} = 50\,\mathrm{kHz}$, $f_{\mathrm{sw,LoadConv.}} = 20\,\mathrm{kHz}$.
2) Baseline operation without any suppression technique with equal switching frequencies of the two converters $f_{\mathrm{sw,CUT}} = f_{\mathrm{sw,LoadConv.}} = 20\,\mathrm{kHz}$.
3) Implementation of a resonant controller.
4) Addition of CMC on the AC and DC side.

The tests are conducted at a specific operating point characterized by a modulation index $M_i = 0.5$, an rms load current of $I_{\mathrm{rms}} = 15$ A, and a fundamental frequency $f_0 = 125$ Hz.

The experimental setup employs the passive filters discussed in Section II. In particular, when the LCL filter configuration is used, the values are: $L = 300$ μH and $C_f = 40$ μF, resulting in a resonant frequency of $f_{\mathrm{res,LCL}} = 2054$ Hz. This value is far from both the fundamental and from the converters' switching frequencies.

The AC-side CM choke used in Fig. 11(d) has a CM inductance of $L_{\mathrm{CM,AC}} = 1.48$ mH, while the DC-side choke in Fig. 11(e) provides $L_{\mathrm{CM,DC}} = 1.48$ mH. A detailed list of component values is reported in Table 3.

The resonant controller is implemented with the same structure described in Section II. For completeness, the specific parameters used in the experiments are reported in the following.

1) *Resonant frequency:* $f_{\mathrm{res}} = 3 \cdot f_0 = 150\,\mathrm{Hz}$.
2) *Resonant gain:* $K_{\mathrm{res}} = 100$.

These values were tuned to maximize attenuation of the dominant low-frequency component of the circulating current without affecting the stability of the current control loops of the CUT or the load converter.

The experimental results are summarized in Fig. 11.

As illustrated in Fig. 11(a), the baseline configuration exhibits a significant circulating i_{cm} in the system. As expected, when the two converters are switching at the same frequency [see Fig. 11(b)], the CM current presents a pulsating behavior related to the uncontrolled shifting of the PWM. Indeed, the implementation of a resonant controller drastically reduces this recirculating current, reducing the low-frequency harmonics of it, as shown in Fig. 11(c). Furthermore, the introduction of CM chokes, either on the AC or DC side, contributes to the attenuation of both i_{cm} and differential-mode current (i_{dm}) ripple components, as presented in Fig. 11(d) and (e).

C. EFFICIENCY MAPPING

In the second set of experiments, a full efficiency map of a 30-kW GaN converter prototype is generated. To ensure precision and repeatability, a dedicated acquisition routine is implemented using an HBM data logger and automated reference generation via MATLAB.

A predefined test pattern, as shown in Fig. 12, is employed to explore the operating envelope of the CUT. For each operating point, the following procedure is executed.

1) The reference values for current and modulation index are generated and transmitted via CAN.
2) A waiting time of $t_{\text{wait}} = 400$ ms is enforced to ensure steady-state conditions.
3) Data acquisition is triggered using the HBM system.
4) A cool-down period is applied before the next operating point.

This systematic approach ensures consistent thermal conditions across measurements and improves the reliability of the resulting map. Fig. 13 is included to demonstrate the correct operation of the control architecture during the efficiency-mapping procedure. In particular, the measured voltages and currents confirm that the PLL ensures a stable and accurate synchronization between the CUT and the load converter, and that the phase shift commanded via CAN is properly tracked. This validates the correctness of the operating conditions for each measurement point in the efficiency map.

During the efficiency mapping campaign, the CUT reached its full rated power of 30 kW. Under these conditions, the external DC source supplied only a small amount of power, corresponding to few percentage points of the CUT rated power.

The final efficiency map is reported in Fig. 14, where three cases are presented. In the first case [see Fig. 14(a)], the efficiency of the CUT is evaluated by measuring the voltage after the filtering LC stage, across the output filter capacitor C_f, as presented in Fig. 6. The second case [see Fig. 14(b)] refers to the same measurement approach, but with the I^2R losses of the cables and inductors subtracted from the estimation, where $R = 13$ mΩ. As can be observed, the resulting map in Fig. 14(b) exhibits a shape that closely matches the one obtained in the third case [see Fig. 14(c)], where the voltages are directly measured at the output terminals of the CUT converter.

V. CONCLUSION

This article presented a novel B2B converter testing platform designed to overcome key limitations found in conventional approaches, CM circulating currents, and lack of modularity. By introducing a Δ–Y transformer and independent CAN-based control platforms, the proposed architecture enables fully decoupled power and control paths between the CUT and the active load. The operations of the CUT and of the load converter are fully independent, with no need of communication between them.

The CUT is operated in open-loop mode, with a voltage vector that is synchronized with the load current vector that is controlled by the load converter. The proposed testing structure allows full-power testing under arbitrary load conditions, to get the CUT efficiency mapping across a wide range of operating conditions: modulation index, output frequency, output current, and power factor. This efficiency mapping is mandatory for characterizing the inverter to create accurate system models of powertrains or high-efficiency industrial drives. The CUT can be used without access to its firmware, allowing the proposed solution to be applied with any CUT that provides CAN bus communication to receive only the modulation index and the output frequency. Furthermore, the proposed test bench allows full-power characterization of the CUT using an external power source covering only the overall losses of the system, significantly reducing the infrastructure cost. Therefore, the proposed testing solution is extremely flexible and versatile, as demonstrated by the experimental verification.

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