Design Guidelines for Active Power Filters Operating in Disturbed Industrial Environments

IEEE Open Journal of
Industry Applications

Received 24 September 2025; revised 9 December 2025; accepted 23 January 2026. Date of publication 6 February 2026;
date of current version 11 February 2026.

Digital Object Identifier 10.1109/OJIA.2026.3658742

Design Guidelines for Active Power Filters Operating in Disturbed Industrial Environments

ALESSANDRO ROVERI [1] (Graduate Student Member, IEEE), VINCENZO MALLEMACI [2] (Member, IEEE), FABIO MANDRILE [2] (Member, IEEE), AND RADU BOJOI [2] (Fellow, IEEE)

[1]Prima Electro S.P.A., 10024 Moncalieri, Italy
[2]Dipartimento Energia, Politecnico di Torino, 10129 Torino, Italy

CORRESPONDING AUTHOR: FABIO MANDRILE (e-mail: fabio.mandrile@polito.it).

This work was supported in part by Project ROCKET (Reliable pOwer to Cloud multiKilowatt ElecTronics), in part by the Piedmont Region, in the framework Programma Pluriennale Attività Produttive 2018/2020 Misura "Contratto di Insediamento."

ABSTRACT Regenerative testing systems of AC–AC industrial power converters (diode or thyristor rectifier and inverter) at the end of the production line are common solutions to reduce the energy drawn from the grid during the testing. However, they inherently introduce severe harmonic distortion, causing disturbances for all local loads. Shunt-type active power filters (APFs) are widely adopted to mitigate these issues. Since the APF is an add-on for the testing system in mass production facilities, it must be cost effective and with high efficiency for not affecting the overall losses for the testing. Moreover, higher switching frequencies are often used to reduce grid-interfacing filter size, further impacting APF efficiency. As the industrial environments are highly disturbed, the APF operation must be extremely robust against these disturbances. In light of the aforementioned issues, this article provides guidelines for the design of an APF intended to operate in an industrial environment characterized by significant electrical disturbances. In particular, the article demonstrates how the adoption of a dedicated discontinuous pulsewidth modulation (DPWM) technique for APFs, namely APFGDPWM, allows minimizing the impact of the APF on power line consumption and reducing the stress on the APF semiconductors and on the filters for grid interfacing. Unlike other DPWM strategies in the literature designed for APFs, APFGDPWM proves to be robust against high frequency disturbances circulating on the power lines. Moreover, a design procedure for the differential mode (DM) *LCL* filter is proposed and used to build two distinct prototypes: an APF implementing space vector pulsewidth modulation (SVPWM) and an APF using APF-GDPWM. Experimental tests are conducted on an industrial prototype (TRL 9), 100 kVA two-level APF interfaced to the grid through the previously designed DM *LCL* filters, while compensating for the distorted input current of a regenerative system testing 260 kVA power converters.

INDEX TERMS Active power filters (APFs), discontinuous pulsewidth modulation (PWM), disturbed environments, inverter losses, *LCL* filter design, power converters testing, power quality, PWM waveform quality, regenerative systems.

I. INTRODUCTION

A. BACKGROUND AND CONTEXT: REGENERATIVE TESTING SYSTEMS WITH ACTIVE POWER FILTERS (APFS)

With the rising complexity of electronic equipment, the requirements for efficiency and reliability in power electronic systems and their manufacturing processes are becoming increasingly stringent. To meet these requirements, manufacturers of power converters typically integrate regenerative testing systems into their production lines. These systems allow the testing at the end of production line, thereby reducing the probability of early failures while simultaneously minimizing power consumption from the grid and, consequently, the overall operating costs of the production facility [1], [2].

A possible regenerative approach is to test the power converter with a target motor that is mechanically coupled with a braking motor (acting as mechanical load emulator), using a back-to-back configuration [3]. The power absorbed by the braking motor is fed back into the grid only if it is powered by a bidirectional power converter. However, if the power rating of the converter under test (CUT) is high, this type of testing becomes problematic. Indeed, the test bench, which includes two motors and additional power electronic, results bulky and expensive [1]. Moreover, a mechanical testing system poses additional safety procedures and required maintenance, especially when the power and/or speed levels are high.

Due to the limitations of this approach, a more recent regenerative testing method, known as virtual load [2], or virtual machine [4], was proposed to reduce the testing cost. With this solution, the electrical machines in the regenerative system are replaced by a single power electronic converter with bidirectional power flow, consisting of two back-to-back voltage source inverters. The virtual load is flexibly controllable, allowing the testing of the CUT under any operating condition in terms of output current, voltage, and frequency.

An alternative regenerative solution, suitable when space constraints are not critical, involves the use of a transformer within the regenerative loop with an appropriate transformation ratio. This solution minimizes maintenance costs and does not require the control of additional converters beyond the CUT. However, it only allows testing the CUT at the fixed grid voltage and frequency. This approach is well suited for testing converters that operate in the field at nearly constant operating points, such as applications in compressed air systems and vacuum pumps.

The CUT analyzed in this article is a power converter with an uncontrolled AC/DC input stage (such as thyristor or diode rectifier) and a DC/AC voltage source inverter at the output stage. Regardless of the adopted regenerative configuration, during testing the active power recirculates within the regenerative system. The current drawn from the grid is therefore a small amount of active current to compensate for system losses, plus the distorted current generated by the CUT grid front-end rectifier. Typically, the distorted current is much higher than the fundamental current drawn from the grid, making the regenerative system a highly distorted nonlinear load for the grid. Its distorted current component leads to an overall increase of the current drawn from the grid with subsequent overheating of the supplying line cables, increasing risk of triggering of the line protection devices, and interference with neighboring sensitive electronic components in the production facility. Indeed, international standards [5] provide harmonic distortion limitations to compensate for the negative effects of distorted currents on power systems and, due to their intrinsic characteristics, regenerative systems inherently fail to comply with these requirements.

An effective solution to mitigate the issue of distorted currents injected by the CUT and to comply with harmonic distortion regulations consists in installing APFs on the supply lines of the regenerative systems (see Fig. 1). The APFs are

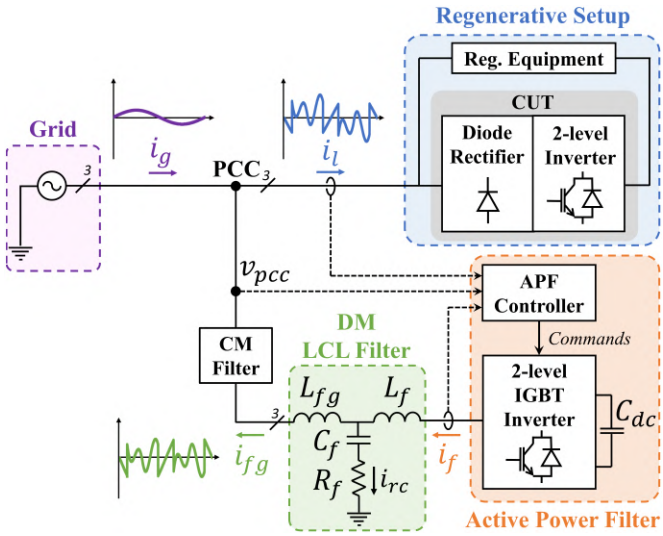

FIGURE 1. Principle scheme of a shunt-type APF compensating for the distorted current injected by the passive front-end rectifier of the CUT during its final functional test in the regenerative system.

power converters specifically designed to limit the low frequency current harmonics injected into the grid by nonlinear loads, such as diode or thyristor front-end rectifiers [6], [7], [8]. As shown in Fig. 1, a shunt-type APF [9], connected in parallel to the regenerative system at the point of common coupling (PCC), can inject nonsinusoidal currents to make the overall grid current sinusoidal at unity power factor, thus reducing the RMS current absorbed at the PCC and yielding significant benefits for the sizing and efficiency of the power line.

B. MOTIVATION: DESIGN OF ACTIVE POWER FILTERS OPERATING IN DISTURBED ENVIRONMENTS

As an APF is essentially an inverter connected to the grid, a company that manufactures industrial converters can easily develop a customized APF, using parts that are already available for their products. Indeed, several hardware sections, such as the power switches, their gate drivers, and the cooling systems, can be directly reused from the inverters already produced for the market. Therefore, the goal of the APF design can focus on maximizing the use of existing hardware to achieve the desired harmonic compensation performance and the highest possible efficiency, while minimizing the size and cost of the remaining hardware components to be designed, such as the differential mode (DM) *LCL* filters required for the APF grid interfacing (see Fig. 1).

While improving the power quality, the installation of the APF inherently leads to an increase of the active power absorption at the PCC due to the power converter losses. Therefore, for APFs installed in production facilities running in mass-production mode, maximizing efficiency is particularly crucial to reduce the operating costs. On the other hand, the APF switching frequency is typically set as high as possible, at the cost of efficiency reduction, to minimize

the size and cost of the grid connection filters [10] and to increase the converter control bandwidth, thus improving the APF harmonic compensation capability [11].

The selection of the inverter pulsewidth modulation (PWM) technique significantly affects converter losses and the stress on grid-interfacing filters, thus influencing the overall APF design. Indeed, the use of discontinuous pulsewidth modulation techniques (DPWMs) in two-level three-phase inverters [12] is a well-known solution in the literature to reduce the switching losses, or alternatively increase the switching frequency up to 50% without affecting the power converter thermal behavior [13]. However, under the same operating conditions (i.e., switching frequency and modulation index), compared to continuous pulsewidth modulation methods (CPWMs), DPWMs typically yield a higher switching frequency current ripple component, which must be properly attenuated by oversizing the DM grid-side filters [13].

Different DPWMs have been designed for standard applications, such as electrical drives [12], [13], [14], [15] or active front-end (AFE) power converters [16], [17], [18], [19], where the current low order harmonic content mainly consists of the fundamental frequency. For all cases, an appropriate zero sequence voltage is injected to perform the desired DPWM [13].

Meanwhile, a generalized DPWM specifically designed for APFs was presented in [20], which has the the key advantage of theoretically ensuring the minimization of switching losses in APF applications, but it proves to be particularly sensitive to the noise on line currents [21]. Such noise can circulate in a disturbed environment, as in the case study of this article. i.e., a production plant of industrial inverters with regenerative testing systems. The main drawback of the method in [20], due to its sensitivity to noise, lies in unwanted APF switching events in the fundamental period [21].

The limits of the method in [20] were overcome by the solution from [21] through the introduction of a hysteresis selector into the zero sequence computation algorithm. The new generalized DPWM method for APFs proposed in [21], named APF-GDPWM, is thus robust against line noise circulating in disturbed environments, such as industrial plants.

C. NOVEL CONTRIBUTIONS OF THIS ARTICLE

The goal of this article is to extend the work from [21], by proposing a design guideline for APFs operating in disturbed environments by leveraging the advantages achievable through the implementation of APF-GDPWM. The primary objective of the design is maximizing converter efficiency and minimizing both the physical footprint and operational stresses on the grid interfacing filters, under the constraints imposed by preselected hardware components, i.e., the power semiconductors and the cooling system.

The main contributions of the presented article are as follows:

1) The conduction and switching losses for a two-level three-phase APF are analytically computed in the case of CPWMs and APF-GDPWM as a function of the total harmonic distortion (THD_i) of the load current. The calculations are reported in the Appendix.
2) The PWM waveform quality of an APF implementing space vector pulsewidth modulation (SVPWM) and APF-GDPWM is investigated. The analysis is performed in case of the APF compensating for distorted line currents with different values of THD_i. Furthermore, waveform quality indices related to the PWM techniques are defined, which will be used in the design stage of the DM *LCL* filter.
3) The authors propose an analytical straightforward design procedure for the DM *LCL* filter, only depending on the load current base value and its THD_i, the adopted PWM technique and the switching frequency. The presented procedure limits the DM *LCL* filter size and cost, while meeting the regulatory requirements of harmonic distortion at the PCC [5].
4) Experimental tests are carried out to compare the performance of APFs implementing APF-GDPWM, SVPWM and the DPWM solution for APFs from [20], for different operating conditions of the CUT in the regenerative system, various APF switching frequencies, and by interchanging the DM *LCL* filters designed through the proposed procedure.

The designed APF can be classified as a TRL 9 technology, since a number of prototypes are already used in a production facility and operate continuously. They are installed in parallel with regenerative systems used for the final functional testing of 260 kVA industrial power converters for electric drives.

The rest of this article is organized as follows. The operation of a two-level three-phase APF implementing APF-GDPWM is investigated in Section II. In Section III, the power devices losses of the APF are evaluated according to the THD_i of the current drawn by the nonlinear load. The effectiveness of the APF-GDPWM in improving the converter efficiency is thus demonstrated. The PWM waveform quality for an APF implementing the SVPWM and APF-GDPWM is investigated in Section IV. The description of the analytical design procedure for the APF DM LCL filter is provided in Section V. The experimental results for an APF connected in parallel to a production line with circulating high frequency disturbances are reported in Section VI. Finally, Section VII concludes this article.

II. IMPLEMENTATION OF APE MODULATION STRATEGY

The adopted modulation strategy for the APF described in this work is the APF-GDPWM that was presented in detail in [21]. The computation of the zero sequence voltage v^*_{cm} through the APF-GDPWM solution is outlined in the flowchart of Fig. 2. The inputs of the algorithm consist of the reference voltages v^*_{abc} and currents i^*_{abc}. The reference voltages v^*_{abc} are obtained as output of the current control regulators, while the reference currents i^*_{abc} are computed by removing the active current component at the fundamental frequency from the line current measurement (i_l in Fig. 1).

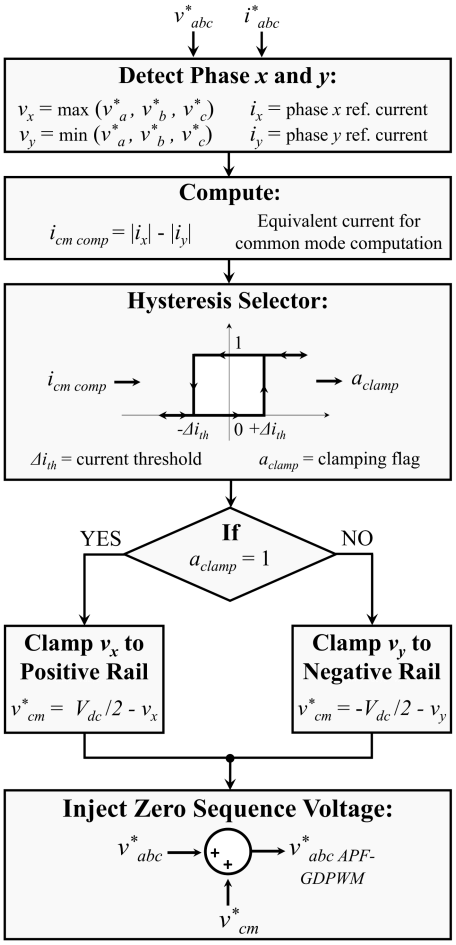

FIGURE 2. Flowchart of the zero sequence voltage v^*_{cm} computation with the proposed APF-GDPWM algorithm.

For simplicity, the operation of APF-GDPWM is briefly summarized below, emphasizing the differences with respect the original DPWM solution proposed for APF in [20] and the conventional SVPWM [22], [23]. The differences are related to the computation of the zero sequence voltage v^*_{cm} that is added to the voltage references.

The computation of v^*_{cm} with both the APF-GDPWM algorithm and the method from [20] consists of first detecting which phases are applying the maximum voltage v_x and the minimum voltage v_y; then clamping the phase v_x or v_y, respectively, to the positive $(\frac{V_{\text{dc}}}{2})$ or negative $(-\frac{V_{\text{dc}}}{2})$ DC-link rail, depending on which of the two phases is operating with the highest reference current i^* in term of absolute value. The APF-GDPWM method differs from the dedicated DPWM solution for APFs proposed in [20] for the implementation of an additional hysteresis selector into the v^*_{cm} computation algorithm (see Fig. 2), which makes the technique robust against high frequency noise that may propagate along the power lines in disturbed environments, such as in a production facility of industrial inverters. Such high frequencies current disturbances may be due to the switching of other grid-tied power converters in the surroundings, e.g., the CUTs in the regenerative systems. The high frequencies current perturbations, combined with a nonnegligible sensitivity of the line current sensors, may affect the calculation of the current references i^*_{abc} and consequently the v^*_{cm} computation, thus resulting in a repetitive change of the clamped phase. Therefore, the main drawbacks of the method in [20], due to the unwanted APF switching events in the fundamental period, lie in the following:

1) Reduction of APF efficiency caused by the increased number of switching transitions.
2) Worsening of the high frequency waveform quality of the APF output current, leading to an increase in THD_i of the current drawn at the PCC.
3) Shift toward higher frequencies (above the kHz threshold) in the common mode (CM) voltage harmonic spectrum of the components associated with zero sequence voltage injection. The occurrence of CM voltage harmonics at higher frequencies makes the system more sensitive to CM current circulation, which can cause grid current distortion, safety issues, increase of the system losses, and electromagnetic interference with other equipment connected to the grid [24], [25], [26].

As will be demonstrated by the experimental tests, the implementation of the hysteresis selector in APF-GDPWM avoids the occurrence of the negative effects described above. A change of the clamped phase is executed only if the difference between the absolute values of current references for phases v_x and v_y (i.e., $i_{\text{cm comp}}$ in Fig. 2) exceeds a threshold $\pm\Delta i_{\text{th}}$, which is tuned considering the current sensors sensitivity and the disturbance amplitude.

The noise effect on the zero sequence voltage computation is illustrated in Fig. 3 with an example. A constant 4 kHz disturbance with a 5% amplitude of the peak reference current is injected into the power line while the APF compensates for the 5th and 7th current harmonic orders provided by a nonlinear load with $\text{THD}_i = 102\%$. The sampling frequency of the power converter is 16 kHz. The zero sequence voltage and the phase reference voltage are provided in the case of SVPWM and APF-GDPWM with the hysteresis selector enabled and disabled. Bypassing the hysteresis selector, the APF-GDPWM algorithm would be equivalent to the generalized DPWM technique for APFs proposed in [20]. The fundamental component of the APF reference voltage is dominant, since the APF must balance the grid voltage, that can be considered as sinusoidal, while only a small amount of voltage is provided to compensate for the higher current frequencies proportionally to the line impedance.

The case study of Fig. 3 demonstrates that the integration of the hysteresis selector into the APF-GDPWM improves the robustness of the algorithm to disturbances on the line currents, thus avoiding unnecessary changes of clamping phase and a consequent injection of high frequency CM voltage related to the zero sequence computation. The side effect is completely eliminated by setting Δi_{th} to a comparable value with the noise amplitude (e.g., $\Delta i_{\text{th}} = 0.05$ p · u· in the example shown in Fig. 3).

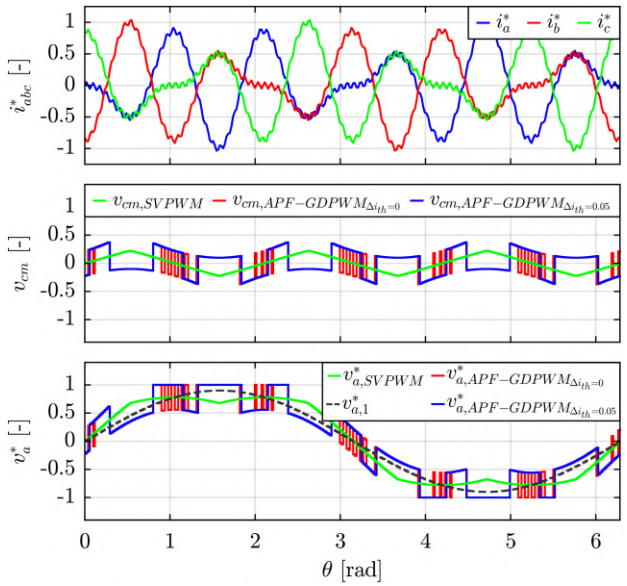

FIGURE 3. APF operation with the SVPWM and APF-GDPWM, with hysteresis selector enabled ($\Delta i_{th} = 0.05$) and disabled ($\Delta i_{th} = 0$), in presence of disturbances on the power lines. Currents and voltages are normalized. From top to bottom: reference currents, zero sequence voltage and phase *a* reference voltage.

III. APF CONDUCTION AND SWITCHING LOSSES

The conduction and switching losses for two-level three-phase PWM inverters for electrical drives have been exhaustively investigated in [12] and [13]. However, the results are not a priori extendable to an APF, where multiple harmonic currents are provided. The mean values of the conduction (P_c) and switching (P_{sw}) losses for a power device (switch or freewheeling diode) of an APF are obtained by integrating the instantaneous values over the fundamental period and the results are reported, respectively, as follows:

$$P_c = \frac{R_{\text{on}}}{2} \cdot I^2_{\text{cell},x,\text{rms}} + \frac{V_{\text{th}}}{2} \cdot I_{\text{cell},x,m} \tag{1}$$

$$P_{\text{sw}} = \frac{E_{\text{sw}}}{V_{\text{dc},n} \cdot I_n} \cdot f_{\text{sw}} \cdot V_{\text{dc}} \cdot k_{\text{sw}} \cdot I_{\text{cell},x,m} \tag{2}$$

where R_{on} and V_{th} are the power device on-resistance and threshold voltage; E_{sw}, $V_{\text{dc},n}$, I_n are the reference (provided by datasheet) total energy loss, DC-link voltage and output current; f_{sw} is the switching frequency; V_{dc} is the actual DC-link voltage; $I_{\text{cell},x,rmas}$ and $I_{\text{cell},x,m}$ are the RMS and mean currents in one of the two unidirectional switching cells into which an inverter leg can be subdivided. Particularly, $x = \text{pos}$ or $x = \text{neg}$ depending on whether the positive or negative unidirectional switching cell is considered, respectively (see Fig. 4). The full derivation of (1)–(2) is provided in the Appendix.

The k_{sw} is the switching loss factor [13] and relates the switching losses obtained with the APF-GDPWM and standard CPWMs, such as SVPWM

$$k_{\text{sw}} = \frac{P_{\text{sw,APF-GDPWM}}}{P_{\text{sw,CPWM}}}. \tag{3}$$

Differently from electric drives applications [12], P_c depends only on the current in the power devices. Indeed, neither the power factor, that is null, nor the output voltage (or the modulation index) affect the conduction losses. Instead, the P_{sw} formula remains unchanged. However, the relationship between $I_{\text{cell},x,\text{rms}}$ and $I_{\text{cell},x,m}$ is not unique (as in case of single harmonic control) and it is strictly dependent on the type of nonlinear load to be compensated.

The form factor that relates the switching cell mean and RMS current is defined as follows:

$$k_f = \frac{I_{\text{cell},x,m}}{I_{\text{cell},x,\text{rms}}}. \tag{4}$$

Instead, the relationship between the APF RMS output current $I_{\text{cell,rms}}$ and the RMS current in the unidirectional switching cell $I_{\text{cell},x,\text{rms}}$ does not depend on the load to be compensated

$$I_{\text{cell,rms}} = \sqrt{2} \cdot I_{\text{cell},x,\text{rms}}. \tag{5}$$

Thus, P_c and P_{sw} can be expressed as a function of the APF operating current $I_{\text{cell,rms}}$, the nonlinear load type, which affects k_f, and the selected modulation technique, that impacts on k_{sw}

$$P_c = \frac{R_{\text{on}}}{4} \cdot I^2_{\text{cell,rms}} + \frac{V_{\text{th}}}{2\sqrt{2}} \cdot k_f \cdot I_{\text{cell},rams} \tag{6}$$

$$P_{saw} = \frac{E_{\text{sw}}}{\sqrt{2} \cdot V_{\text{dc},n} \cdot I_n} \cdot f_{\text{sw}} \cdot V_{\text{dc}} \cdot k_{\text{sw}} \cdot k_f \cdot I_{\text{cell,rms}}. \tag{7}$$

A common case of three-phase nonlinear load connected to the grid is the full-bridge diode front-end rectifier [27], [28]. The modeling of the current behaviour of a diode rectifier is not unique, since the current distortion caused by the load is influenced in both magnitude and shape by the type of output filter [9], [27], [29] and the ratio between the inductive and capacitive values of the installed output inductor L and capacitor C (see Fig. 5). Therefore, as a standardized case study, an ideal diode rectifier is introduced, which is described as follows:

$$i_{\text{load}}(n, \theta, \tau) = \sum_{n=1}^{\infty} \frac{4\sqrt{3}}{n\pi} \cdot \sin\left(n \cdot \frac{\tau}{2}\right) \cdot \sin(n \cdot \theta) \cdot K(n) \tag{8}$$

$$K(n) = \begin{cases} -1, & n = 6k - 1 \\ +1, & n = 6k + 1 \\ 0, & \text{otherwise} \end{cases}, \forall k \in \mathbb{N} \tag{9}$$

where $\tau \in [0, \frac{\pi}{3}]$. Nonlinear capacitive and inductive behaviors are obtained, respectively, for $\tau \to 0$ and $\tau \to \frac{\pi}{3}$ (see Fig. 6).

The benefits of the APF-GDPWM on the switching losses are thus analysed for an APF compensating for the 5th and 7th current harmonics provided by (8). As shown in Fig. 6, for the same fundamental current $i_{l,1}$ absorbed by the ideal rectifier, the load current THD_i and the resulting APF effort to compensate for the distortion increase in case of a capacitive output (i.e., as τ reduces). The relationship between k_f and k_{sw} with the input THD_i of the ideal rectifier is shown in Fig. 7. The

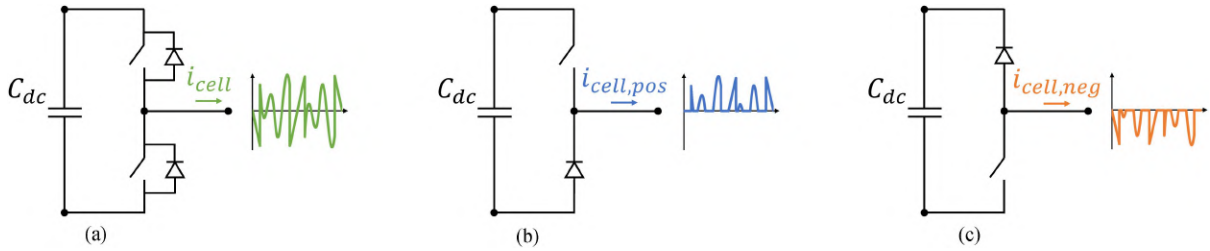

FIGURE 4. Inverter leg of a two-level three-phase APF (a) is a bidirectional switching cell, which can be subdivided into two unidirectional cells. Each cell consists of a power switch (e.g., IGBT or MOSFET) with the related freewheeling diode. The unidirectional cells conduct, respectively, positive $i_{\text{cell,pos}}$ (b) and negative $i_{\text{cell,neg}}$ (c) currents. Instantaneously, the APF output current is $i_{\text{cell}} = i_{\text{cell,pos}} + i_{\text{cell,neg}}$.

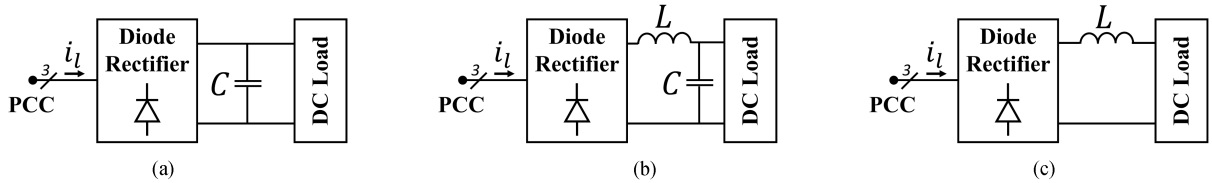

FIGURE 5. Different examples of nonlinear loads. Diode front-end rectifier with capacitive (a) inductive–capacitive, (b) and inductive (c) output and supplying a generic DC load.

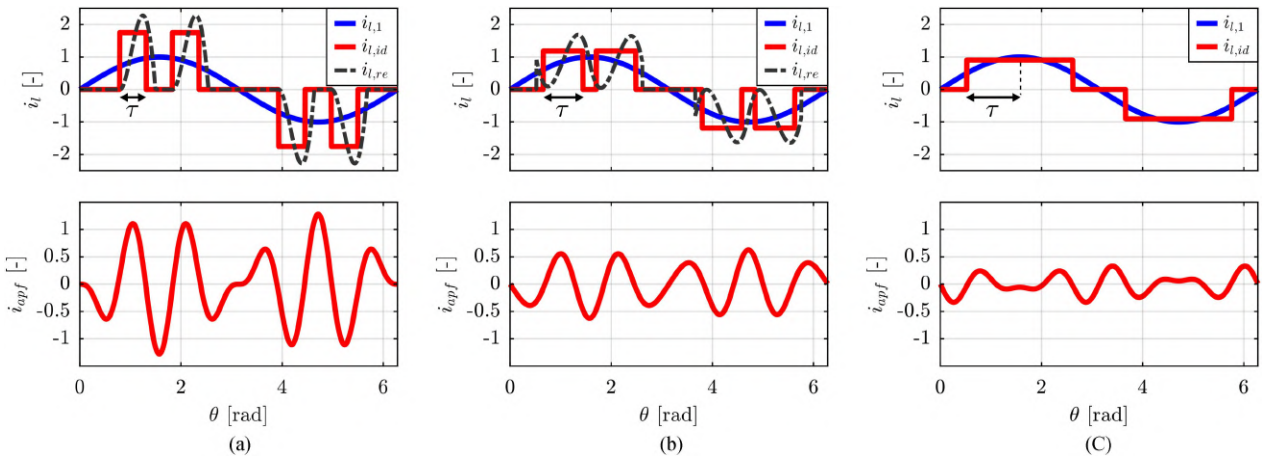

FIGURE 6. Fifth and seventh harmonic compensation of a diode front-end rectifier. From top to bottom: ideal load current ($i_{l,\text{id}}$) and its fundamental component ($i_{l,1}$), APF output current (i_{apf}). The currents are normalized with respect to the peak of $i_{l,1}$. (a) Rectifier with capacitive output ($\tau = \frac{\pi}{6}$) and input $\text{THD}_i = 102\%$. (b) Rectifier with *LC* output ($\tau = \frac{\pi}{4}$) and input $\text{THD}_i = 63\%$. (c) Rectifier with inductive output ($\tau = \frac{\pi}{3}$) and input $\text{THD}_i = 31\%$. A real rectifier input current $i_{l,re}$ with the same THD_i and RMS of $i_{l,\text{id}}$ is also reported for (a) and (b).

form factor k_f is approximately constant ($\simeq 0.6$) as the load THD_i varies, with a maximum value of 0.64 for $\text{THD}_i \simeq 50\%$. The maximum switching loss reduction of 50% ($k_{\text{sw}} = 0.5$) is obtained for capacitive loads (i.e., for high values of THD_i). Similarly, a considerable switching loss reduction (37%) is obtained in case of inductive loads. Indeed, k_{sw} is equal to 0.63 in case of a $\text{THD}_i = 31\%$.

The power devices losses computation are performed according to (6) and (7) for the commercial CM450DX-24T1 IGBT module, to demonstrate the effectiveness of APF-GDPWM in reducing the overall inverter losses. Both IGBT and diode electrical characteristics are taken from the module datasheet [30] and are reported in Table 1 with the other system data. As illustrated in Fig. 8, P_{sw} is the main contribution for the IGBT losses [see Fig. 8(a)]. Instead, P_c is dominant for the diode [see Fig. 8(b)]. Therefore, the use of APF-GDPWM instead of a CPWM is more beneficial for the IGBT than for the diode, with a total loss reduction of 28.2%–37.9% versus 16.8%–22.4% [see Fig. 8(c)]. Since the IGBT losses have a greater impact than those of the diode, the switching losses minimization with APF-GDPWM results in a significant total loss reduction for the switching cell and the entire inverter of 25.0%–33.5%, with better performance in the case of diode rectifier with capacitive output.

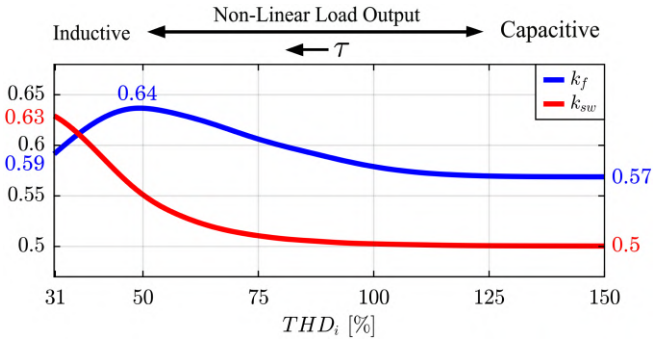

FIGURE 7. Form factor k_f and the switching loss factor k_{sw} of an APF compensating for the 5th and 7th harmonic currents absorbed by an ideal diode rectifier. k_f and k_{sw} are expressed as a function of the nonlinear load THD_i.

TABLE 1. CM450DX-24T1 Data and System Parameters for Power Losses Computation

IGBT Module Data[a]				System Parameters	
$R_{on,IGBT}$	3.0 mΩ	$R_{on,diode}$	2.7 mΩ	$I_{apf,rms}$	150 A_{rms}
$V_{th,IGBT}$	0.84 V	$V_{th,diode}$	0.75 V	V_{dc}	750 V
$E_{sw,IGBT}$	98.5 mJ	$E_{sw,diode}$	23.0 mJ	f_{sw}	8 kHz
$V_{dc,n}$	600 V	I_n	450 A		

[a] Data for junction temperature $T_{v,j}$ = 150 °C and gate-emitter voltage $V_{g,e}$ = 15 V

The ability of APF-GDPWM to reduce switching losses compared to CPWMs can be used either to improve the converter's efficiency or to increase its switching frequency, with benefits on the *LCL* filter design [10], [31], [32], [33] and increase in its harmonic compensation capability [11]. Indeed, for equal losses, f_{sw} can be increased according to the following relation:

$$f_{sw,APF-GDPWM} = \frac{f_{sw,CPWM}}{k_{sw}}. \tag{10}$$

IV. ANALYSIS OF APF OUTPUT CURRENT DISTORTION

The APF current ripple injected into the grid $i_{fg,h}$ is strictly related to the flux ripple λ_h, obtainable by integrating the high frequency component of the APF phase output voltage v_h due to the inverter switching:

$$\lambda_h = \int_0^t v_h \, dt \tag{11}$$

$$i_{fg,h} = L_{eq} \cdot \lambda_h \tag{12}$$

where L_{eq} is the equivalent output inductance, that varies with the frequency and depends on the *LCL* filter and the grid impedance.

The analysis of λ_h instead of $i_{fg,h}$ standardizes the discussion, making it independent of the system electrical parameters. An indicator used in the literature to evaluate the flux quality is the harmonic distortion factor (HDF) [23], that can be defined as follows:

$$HDF = 9 \cdot \frac{\lambda_{h,rms}^2}{\lambda_{b,rms}^2} \tag{13}$$

where $\lambda_{h,rms}$ is the RMS value of flux ripple; $\lambda_{h,b,rms}$ is a base value, that is defined as follows.

$$\lambda_{b,rms} = \frac{V_{dc}}{8 \cdot f_{sw}}. \tag{14}$$

The analytical computation of $\lambda_{h,rms}^2/\lambda_{b,rms}^2$ for different modulation techniques, including SVPWM and DPWM solutions, is provided in [12] for two-level inverter applications with single frequency output voltage, such as the electric drives. The obtained results are also valid for APFs by assuming as purely sinusoidal their low frequency output voltage.

The HDF for APF-GDPWM is computed as a function of the modulation index M through MATLAB scripts, considering an APF that compensates for the 5th and 7th current harmonics drawn by the ideal diode rectifier described in (8). The obtained results are shown in Fig. 9 for different values of nonlinear load THD_i. The HDF curves for APF-GDPWM lie between those of DPWM1 and DPWM3, which are, respectively, the DPWM techniques with highest and lowest harmonic distortion characteristics [12], [13], [20], [23]. Particularly, in the case of rectifier with inductive output (THD_i = 31%), the waveform matches that of DPWM3. The HDF for APF-GDPWM rises accordingly with increasing THD_i. Fig. 9 shows that, at the same switching frequency, APF-GDPWM is disadvantageous compared to SVPWM from the perspective of harmonic distortion.

However, the HDF analysis can be performed in the case of equal power losses. In this regard, the switching frequency can be increased with APF-GDPWM according to (10). The HDF under equal inverter efficiency HDF^{η} is thus introduced

$$HDF^{\eta} = k_{sw}^2 \cdot HDF. \tag{15}$$

As depicted in Fig. 10, under equal inverter losses APF-GDPWM has better distortion performance with respect to SVPWM regardless of load THD_i. This holds true especially for $M \in [0.8, 1]$, which are typical values of the modulation index during APF steady-state operation, as they guarantee a sufficient voltage margin to control the output current while simultaneously limiting the required DC-link voltage [20].

The HDF is useful for evaluating the RMS value of current (flux) ripple injected into the grid by the APF. However, it does not provide any information on the peak value of λ_h, which is a critical parameter for the proper design of the *LCL* filter inductors. Indeed, its knowledge is essential to prevent their flux density saturation. Therefore, the peak to peak maximum value of flux ripple over a switching period $\lambda_{h,pp\,max}$ is computed as a function of M by means of MATLAB scripts, as in [34], [35]. The results obtained both with SVPWM and APF-GDPWM are reported in per unit in Fig. 11

$$\lambda_{h,pp\,max,pu} = \frac{\lambda_{h,pp\,max}}{\lambda_{b,pp\,max}} \tag{16}$$

$$\lambda_{b,pp\,max} = \frac{V_{dc}}{6 \cdot f_{sw}} \tag{17}$$

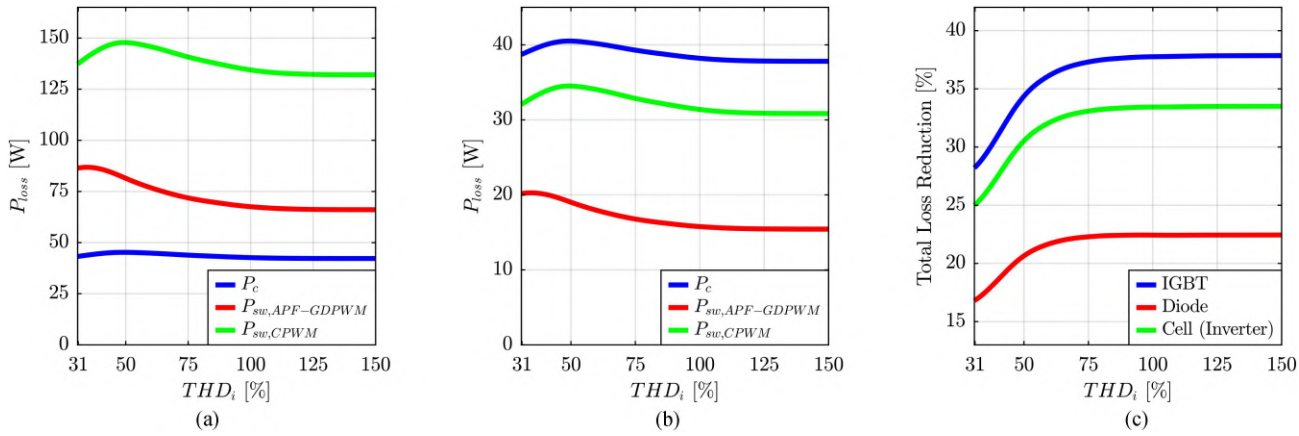

FIGURE 8. Power devices losses for CM450DX-24T1 IGBT module according to the input THD_i of the ideal diode rectifier. The inverter is operating under the conditions described in Table I. IGBT (a) and diode (b) conduction losses (P_c), switching losses with CPMWs ($P_{sw,CPWM}$) and APF-GDPWM ($P_{sw,APF-GDPWM}$). (c) IGBT, diode and switching cell total loss reduction obtained with APF-GDPWM with respect to CPWMs. The loss reduction for the switching cell also corresponds to the overall inverter loss reduction.

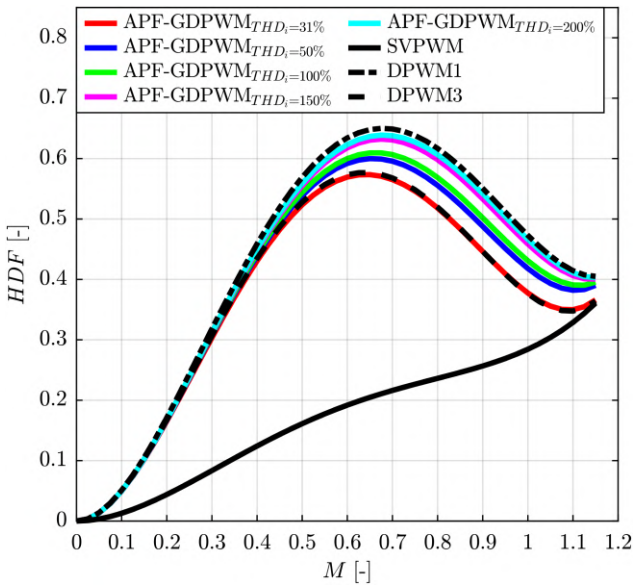

FIGURE 9. HDF under equal switching frequency (HDF) of an APF compensating for the 5th and 7th current harmonics drawn by an ideal diode rectifier (8).

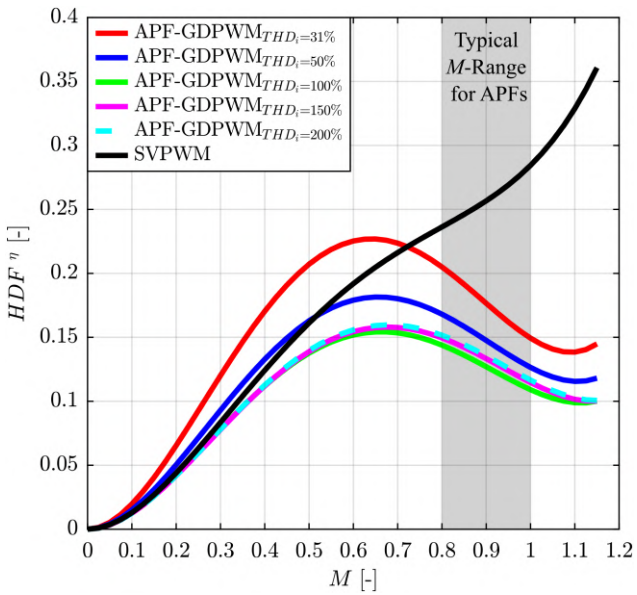

FIGURE 10. HDF under equal inverter efficiency (HDF^{η}) of an APF compensating for the 5th and 7th current harmonics drawn by an ideal diode rectifier (8).

where $\lambda_{h,pp\,\max,\mathrm{pu}}$ and $\lambda_{b,pp\,\max}$ are, respectively, the per unit and base values.

Differently from HDF, $\lambda_{h,pp\,\max,\mathrm{pu}}$ obtained with APF-GDPWM is independent of the nonlinear load current THD_i. Moreover, the corresponding curve lies above that of SVPWM for $M < 0.95$, while the curves coincide for $M \in \left[0.95, \frac{2}{\sqrt{3}}\right]$.

Similarly to HDF, a study of $\lambda_{h,\mathrm{pp}\,\max,\mathrm{pu}}$ can be performed also under equal inverter efficiency. For this purpose, the equivalent indicator $\lambda^{\eta}_{h,pp\,\max,\mathrm{pu}}$ is introduced

$$\lambda^{\eta}_{h,pp\,\max,\mathrm{pu}} = k_{\mathrm{sw}} \cdot \lambda_{h,pp\,\max,\mathrm{pu}}. \tag{18}$$

As outlined in Fig. 12, under equal inverter losses, APF-GDPWM and SVPWM exhibit comparable results of peak to peak maximum flux ripple for low values of M. Instead, for high M, particularly within the typical operating range ($M \in [0.8, 1]$), APF-GDPWM guarantees a lower $\lambda^{\eta}_{h,pp\,\max,\mathrm{pu}}$.

V. LCL FILTER DESIGN

As demonstrated in literature, the *LCL* filter is the most adopted topology for applications above several kilowatts [10], [36]. Indeed, compared to a simple *L* filter and for the same installed inductance, the *LCL* offers up to three times the attenuation capability at high frequencies [32], [33], [36], thus resulting a more cost-effective and compact solution.

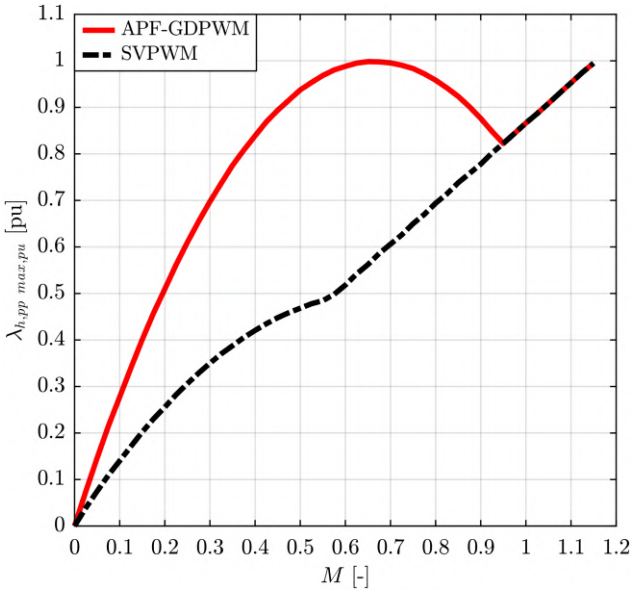

FIGURE 11. Peak to peak maximum value of flux ripple under equal switching frequency ($\lambda_{h,pp\ \mathrm{max,pu}}$) of an APF compensating for the 5th and 7th current harmonics drawn by an ideal diode rectifier (8).

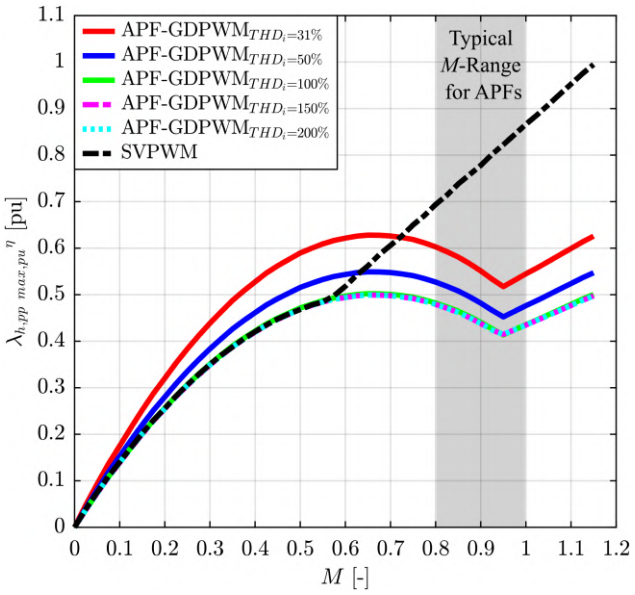

FIGURE 12. Peak to peak maximum value of flux ripple under equal inverter efficiency ($\lambda^{\eta}_{h,pp\ \mathrm{max,pu}}$) of an APF compensating for the 5th and 7th current harmonics drawn by an ideal diode rectifier (8).

Due to the critical role of the input filter, several design methodologies have been proposed in the literature for grid-connected inverters [10], [31], [32], [33], [36] and specifically for APFs [37], [38], [39], [40]. The criteria defined for inverters and rectifiers result too stringent when applied to APFs, particularly regarding resonant frequency constraints [39]. Indeed, the design procedures dedicated to APFs focus particularly on the placement of the resonance frequency, aiming to simultaneously achieve accurate low harmonic order

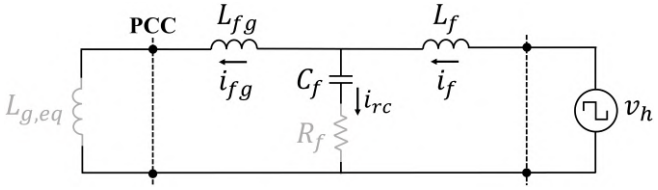

FIGURE 13. High frequency single-phase equivalent circuit of the *LCL* filter interfacing the APF to the grid. The equivalent grid inductance $L_{g,\mathrm{eq}}$ and the damping resistance R_f are neglected and are thus shown in gray.

compensation by APF control and efficient suppression of switching-induced ripple components. The methods in [37], [39], [40] do not consider that APF switching ripple has to be evaluated on the total current drawn by the system at the PCC (i_g in Fig. 1), which depends both on APF and nonlinear load current absorption. Instead, the proposed design procedures limit the ripple respect to the APF compensation current (i_{fg}), leading to a filter oversizing with a significant impact on cost and volume. The method in [38] properly sizes the APF *LCL* filter based on the line current at the PCC. However it lacks detailed criteria for determining the specific values of inductances and capacitance.

Motivated by the limits of the solutions in the literature, this section proposes a straightforward step-by-step procedure for designing the *LCL* filter of an APF. The outcomes of the design procedure depend both on the following:

1) The APF nominal operating conditions, i.e., the adopted PWM technique, the modulation index M, the switching frequncy f_{sw} and the highest order harmonic that needs to be compensated h.
2) The nonlinear load characteristics, i.e., the rated power P_l, the input current fundamental component $i_{l,1}$ and THD_i.

This section is structured as follows. First, preliminary considerations on the *LCL* filter are carried out to obtain the relations to be used in the design phase. Then, the proposed procedure is outlined, describing in detail the computation of the filter parameters, as well as the final validation checks, that are performed to ensure at the same time good filtering performance and the proper APF operation. Finally, two design examples are provided for a two-level APF implementing, in one case, SVPWM with $f_{\mathrm{sw}} = 8$ kHz and in the other, APF-GDPWM with $f_{\mathrm{sw}} = 16$ kHz.

A. PRELIMINARY CONSIDERATIONS

The high frequency single-phase equivalent circuit of the *LCL* filter interfacing the APF to the grid is shown in Fig. 13. In the preliminary design stages, the damping resistance R_f is neglected. The grid equivalent inductance $L_{g,\mathrm{eq}}$ can be considered as an additive inductor in series with the *LCL* filter, that enhances its high-frequency attenuation performance. However, it is generally not known a priori, since it depends on the APF installation location. Moreover, it can widely change during operating conditions [41]. Therefore, in order to adopt

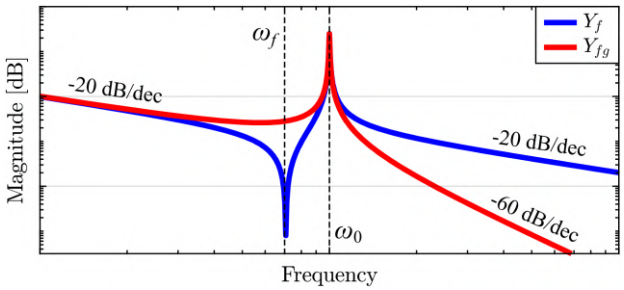

FIGURE 14. Qualitative representation in the logarithmic scale of the magnitude of the admittances $Y_f(s)$ and $Y_{fg}(s)$ in case of negligible damping resistance R_f. The resonance frequency ω_0 and antiresonance frequency ω_f are reported in the graph with the attenuation characteristics of the *LCL* filter.

a conservative approach, $L_{g,\text{eq}}$ is neglected in the design procedure. The system transfer functions used for the filter design are listed as follows.

$$Y_f(s) = \frac{i_f(s)}{v_h(s)} = \frac{1}{sL_f} \cdot \frac{s^2 + \omega_f^2}{s^2 + \omega_0^2} \tag{19}$$

$$Y_{fg}(s) = \frac{i_{fg}(s)}{v_h(s)} = \frac{1}{s(L_f + L_{fg})} \cdot \frac{\omega_0^2}{s^2 + \omega_0^2} \tag{20}$$

$$\omega_f^2 = \frac{1}{C_f L_{fg}} \tag{21}$$

$$\omega_0^2 = \frac{L_f + L_{fg}}{C_f L_f L_{fg}} \tag{22}$$

where the admittances Y_f and Y_{fg}, respectively, relate the APF-side (i_f) and grid-side (i_{fg}) currents with the ripple voltage (v_h) and their qualitative trends are reported in Fig. 14; ω_0 and ω_f are the system resonance and antiresonance frequencies, respectively, which depend on the filter APF-side inductance L_f, grid-side inductance L_{fg}, and capacitance C_f.

The procedure is expressed in per-unit to facilitate the design scalability. The base values are thus defined as follows:

$$L_b = \frac{Z_b}{\omega_b} \tag{23}$$

$$C_b = \frac{1}{\omega_b \cdot Z_b} \tag{24}$$

where ω_b is the grid base frequency and Z_b is the base impedance, which is obtained by dividing the square of the grid rated voltage by P_n.

B. DESIGN PROCEDURE

The grid is assumed to operate under nominal grid voltage and frequency (i.e., $\omega_g = V_g = 1\ \text{p} \cdot \text{u}\cdot$), while the nonlinear load is operating at full power (i.e., $P_l = 1\ \text{p} \cdot \text{u}\cdot$). The step-by-step procedure consists of the following computations, to be performed in the order here presented.

1) *APF-Side Inductance* L_f: The parameter is chosen to reduce the current stress on the semiconductor devices, thus limiting the peak current in accordance with the power switches nominal data. The maximum peak to peak current ripple $i_{f,h,pp\,\max}$ is thus constrained as follows:

$$i_{f,h,pp\,\max} = k_{L_f} \cdot I_{l,1} \tag{25}$$

where $I_{l,1}$ is the load peak fundamental current, k_{L_f} is an attenuation factor suggested to be in the range 20%–30%.

Similarly to (12), $i_{f,h,pp\max}$ depends both on L_f and $\lambda_{h,pp\,\max}$, the latter being a function of the modulation index M and the PWM technique, as shown in Fig. 11. Therefore, the following per-unit expression for the inductance L_f can be derived by combining (16), (17), (23), and (25).

$$L_f = \frac{2\pi}{3} \cdot \frac{\lambda_{h,\text{pp max}}}{\omega_{\text{sw}} \cdot M \cdot k_{L_f}}. \tag{26}$$

2) *Capacitance* C_f: When the APF is connected to the grid and it is not operating, the reactive power generated by C_f (Q_c) must not reduce the power factor measured at the PCC beyond a certain limit. Therefore, the following constraint is imposed:

$$Q_{c,\text{max OFF}} = k_{C_{f,\text{OFF}}} \cdot P_l = k_{C_{f,\text{OFF}}} \tag{27}$$

where $Q_{c,\text{max OFF}}$ is the maximum admitted value of Q_c generated by C_f, while APF is in idle state; $k_{C_{f,\text{OFF}}}$ is a percentage index suggested in the range 3%–5%, relating $Q_{c,\text{max OFF}}$ to P_l.

Instead, during its operation, the APF can perform feedforward compensation for Q_c. However, the required power effort must be limited, since the larger amount of the APF installed power S_{apf} has to be reserved for line current compensation. Assuming the APF rated current I_{apf} is equal to the load distorted current $I_{l,d} = I_{l,1} \cdot \text{THD}_i$, a second constraint for Q_c is imposed

$$Q_{c,\text{max ON}} = k_{C_{f,\text{ON}}} \cdot S_{\text{apf}} = k_{C_{f,\text{ON}}} \cdot \text{THD}_i \tag{28}$$

where $Q_{c,\text{max ON}}$ is the maximum admitted value of Q_c compensable in feedforward mode by the APF; $k_{C_{f,\text{ON}}}$ is a percentage index suggested in the range %–5%, relating $Q_{c,\text{max ON}}$ to S_{apf}.

Since $C_f \simeq Q_c$ in per-unit, a formula for computing C_f is obtained by combining (27)–(28)

$$C_f = \min\left(k_{C_{f,\text{OFF}}}, k_{C_{f,\text{ON}}} \cdot \text{THD}_i\right). \tag{29}$$

In practice, $k_{C_{f,\text{OFF}}}$ and $k_{C_{f,\text{ON}}}$ are equally set. Therefore, the most limiting constraints between (27) and (28) only depends on load input THD_i.

3) *Grid-Side Inductance* L_{fg}: Once L_f and C_f are known, L_{fg} can be determined as in [10], by combining (19)–(20) and imposing the desired current ripple attenuation $k_{L_{fg}} = |i_{fg}(s)/i_f(s)|$ at f_{sw}. The following per-unit expression is thus derived:

$$L_{fg} = \frac{\left(1 + \frac{1}{k_{L_{fg}}}\right) \cdot L_f}{L_f \cdot C_f \cdot \omega_{\text{sw}}^2 - 1}. \tag{30}$$

The attenuation coefficient $k_{L_{fg}}$ is suggested to be in the range 10%–20% and the selected value depends on

the implemented PWM technique. Indeed, as shown in Fig. 9, different PWM solutions differs for HDF and consequently for RMS current ripple $I_{fg,h}$ injected into the grid. For the same impact on THD_i at the PCC, a PWM technique with a higher HDF requires a lower $k_{L_{fg}}$. For instance, since HDF $\propto I_{fg,h}^2$, the attenuation factors of APF-GDPWM and SVPWM can be related as follows:

$$k_{L_{fg,\text{APF-GDPWM}}} = k_{L_{fg,\text{SVPWM}}} \cdot \sqrt{\frac{\text{HDF}_{\text{SVPWM}}}{\text{HDF}_{\text{APF-GDPWM}}}}. \quad (31)$$

4) *Damping Resistance R_f:* The insertion of a resistive component R_f into the *LCL* filter is required to damp the current oscillation at the resonance frequency, due to the null value of the filter impedance at ω_0. An R_f value proportional to the capacitive reactance is typically selected [32], [33], such as

$$R_f = \frac{1}{3\omega_0 C_f}. \quad (32)$$

The mitigation of resonant fluctuations can be achieved either by physically installing a resistor or by implementing into the APF current control one of the active damping algorithms proposed in the literature [38], [42], [43], [44], thus emulating the desired resistive behavior with a virtual resistance. In this latter case, the installation of a passive component is avoided, with the benefit of significant overall filter losses reduction. However, a passive damping solution is adopted herein to avoid the APF current control from being involved in the filter design, thus simplifying the discussion.

Once the values of the filter inductive (L_f and L_{fg}), capacitive (C_f) and resistive (R_f) components have been defined, the following constraints are verified to avoid resonant behavior, ensure the desired low frequency current compensation capability, minimize the impact on power line consumption, and ensure the system compliance with regulatory limits on harmonic distortion at PCC.

1) *Resonance Frequency ω_0*: The upper limit defined for ω_0 in the literature [10], [31], [32], [33], [36], [37], [38], [39], [40] is one-half of ω_{sw} to avoid unwanted amplification of switching harmonics

$$\omega_0 \leq \frac{\omega_{\text{sw}}}{2}. \quad (33)$$

In the event that (33) is not satisfied, ω_0 can be lowered by increasing L_f, C_f, or L_{fg}, according to (22).

2) *Antiresonance Frequency ω_f*: The APF harmonic compensation capability can be compromised if ω_f is so low as to interact with the highest harmonic frequency $h \cdot \omega_g$ the APF has to mitigate. Specifically, when ω_f is too close to $h \cdot \omega_g$, the *LCL* filter output current i_{fg} may experience magnitude amplification and phase delay compared to the controlled input current i_f, resulting in i_{fg} deviating from the desired value required to compensate for the distortion of i_l. In order to avoid current control limitation, the following constraint is proposed:

$$\omega_f \geq 2h \cdot \omega_g. \quad (34)$$

When the constraint in (34) is violated, C_f or L_{fg} have to be reduced according to (21).

3) *Damping Resistors Losses P_d*: The *LCL* filter losses must be limited to minimize the impact on overall power line consumption. To this end, P_d must not exceed a defined percentage amount $k_{P_d,l}$ of the load rated power P_l. At the same time, P_d must not excessively affect the design of the APF cooling system (i.e., heatsink and fans). Therefore, P_d must also remain below a specified percentage $k_{P_d,\text{apf}}$ of the APF nominal power S_{apf}. Based on the considerations above, the following constraint is imposed:

$$P_d \leq \min\left(k_{P_d,l}, k_{P_d,\text{apf}} \cdot \text{THD}_i\right) \quad (35)$$

where $P_d = 3R_f I_{rc}$, with I_{rc} the RMS current in the capacitor C_f.
A suggested value both for $k_{P_d,l}$ and $k_{P_d,\text{apf}}$ is 1%. In the event that condition (35) is not met, R_f has to be reduced by increasing either ω_0 or C_f according to (32). Alternatively, I_{rc} can be limited by increasing L_f, thus enhancing the high frequency current filtering provided by the converter-side inductor.

4) *Current Ripple $I_{fg,h}$*: The residual APF current ripple injected at the PCC must not exessively impact the THD_i of the overall current drawn from the grid (i_g in Fig. 1). Indeed, the high frequency attenuation provided by the *LCL* filter must ensure the system compliance with harmonic distortion standards [5], which require the strictest limit of $\text{THD}_i \leq 5\%$ in the case of weak grids (short-circuit ratio SCR < 20). Since the APF installation is not predetermined, $I_{fg,h}$ has to meet the worst-case constraint with a 50% additional margin, thus accounting partial low frequency current compensation provided by the APF, unmodeled factors and component tolerances

$$I_{fg,h} \leq 2.5\%. \quad (36)$$

In case constraint (36) is not satisfied, L_f, C_f, or L_{fg} must be increased to improve the filter attenuation at high frequencies.

C. DESIGN EXAMPLES

The procedure previously illustrated is used for the design of the *LCL* filter for a two-level APF, respectively, in the case of implementation of SVPWM with $f_{\text{sw}} = 8$ kHz (Filter 1) and APF-GDPWM with $f_{\text{sw}} = 16$ kHz (Filter 2). The system base values, the operating characteristics of both the APF and the nonlinear load, as well as the indices used for the design of the *LCL* filters are reported in Table 2. Once the modulation index is defined (i.e., $M = 0.9$), the values of HDF and $\lambda_{h,pp\,\text{max,pu}}$ to use during the design stage can be obtained respectively from Figs. 9 and 11, according to the selected modulation technique.

TABLE 2. System Main Data and Coefficients for the *LCL* Filter Design

Base Values		Non-Linear Load		Active Power Filter		LCL Filter Design Factors	
S_b	260 kVA	P_l	1.0 pu	S_{apf}	0.33 pu	k_{L_f}	25 %
V_b	400 V_{rms}	$I_{l,l}$	1.0 pu	M	0.9	$k_{C_{f,OFF}}$	4 %
ω_b	314 rd/s	THD_i	33 %	h	25	$k_{C_{f,ON}}$	4 %
Z_b	0.62 Ω					$k_{L_{fg,SVPWM}}$	15 %
L_b	1.96 mH					$k_{L_{fg,APF\text{-}GDPWM}}$	11 %
C_b	5.17 mF					$k_{P_{d,l}}$	1 %
						$k_{P_{d,apf}}$	1 %

TABLE 3. *LCL* Filter Design Results

Parameter	Filter 1	Filter 2	Constraint
Modulation	SVPWM	APF-GDPWM	-
f_{sw} [kHz]	8	16	-
$\lambda_{h,pp,max}$ [pu]	0.78	0.88	-
HDF [-]	0.26	0.45	-
L_f [μH]	**89**	**50**	**-**
C_f [μF]	**68**	**68**	**-**
L_{fg} [μH]	**48**	**15**	**-**
R_f [mΩ]	**225**	**136**	**-**
ω_0 [rad/s]	21745	-	$\leq$ 25133
	-	36007	$\leq$ 50266
ω_f [rad/s]	17552	31694	$\geq$ 15708
P_d [%]	0.21	0.15	$\leq$ 0.33
$I_{fg,h}$ [%]	1.00	1.54	$\leq$ 2.5

The computed parameters (i.e., L_f, C_f, L_{fg}, and R_f) of both Filter 1 and 2 are reported in Table 3, where f_{sw}, the adopted modulation technique and the related PWM waveform quality indices HDF and $\lambda_{h,pp\,max}$ are also specified for each filter. Moreover, Table 3 presents the corresponding values of ω_0, ω_f, P_d, and $I_{fg,h}$, which satisfy their respective constraints (33)–(36).

While ω_f and ω_0 are computed from (21) to (22), P_d and $I_{fg,h}$ are evaluated by implementing a simple and straightforward model of the system in MATLAB environment. The behaviors obtained in simulation of i_{rc} (from which P_d is calculated), $i_{f,h}$ and $i_{fg,h}$ are reported in Fig. 15.

The procedure design led to the prototyping of L_f and L_{fg} with a toroidal-core in powder-type magnetic material and wound with Litz wire. The same technology was used for the realization of the inductors in both Filter 1 and 2. The views of realized L_f and L_{fg} inductors are reported in Figs. 16 and 17, respectively.

Since the requested capacitance value C_f and the current i_{rc} are expected to be similar for Filter 1 and 2, the same PCB-mounted film capacitors were used to realize the capacitor branch for both prototypes. A picture of the capacitive element is presented in Fig. 18.

The designed *LCL* filters have been assembled, and for both, the real admittance curve $Y_f(s)$ has been measured using a IM3536 Hioki LCR meter. The comparison between the expected and the experimentally measured admittances are provided in Fig. 19. While slightly differing in resonance and anti-resonance frequencies, as well as in resonance damping due to component tolerances, the real curves closely match the ideal ones for $\omega \leq h\omega_g$ and $\omega \geq \omega_{sw}$, thus guaranteeing the desired filters behavior within the control frequency range and the required high frequency attenuation capability.

Both filters designed with the proposed procedure were employed during the experimental testing phase to compare the performance of APF-GDPWM with SVPWM.

VI. EXPERIMENTAL RESULTS

The case study for the nonlinear load used for experimental tests is a regenerative system employed for the final functional testing of the CUT at the end of the production line, as shown in Fig. 20. The active power recirculates in the regenerative system through a line transformer. The CUT is a 260 kVA power converter for electrical drives consisting of a diode three-phase rectifier with output *LC* filter in the AC/DC stage [see Fig. 5(b)] and a two-level three-phase IGBT inverter in the DC/AC stage. The THD_i of the current absorbed by the diode rectifier during the full-power operation is 34.3%.

A two-level APF is connected in parallel to the regenerative system (see Fig. 20) to compensate for the current harmonics produced by the CUT grid rectifier. The adopted APF control method is the one proposed in [29] and depicted in Fig. 21. A 50 Hz proportional resonant regulator (P-RES) operating in stationary (α, β) reference frame is implemented to perform the fundamental current control and the d bus voltage regulation. Instead, RESs operating in synchronous (d, q) reference frame and rotating at the grid frequency are tuned at the harmonic orders $6k$, with $k = 1, 2\ldots$. Each RES compensates for the $6k-1$ and $6k+1$ harmonics of negative and positive sequence, collapsing on the $6k$ harmonic in synchronous (d, q) reference frame. The controller computational effort to reach the desired harmonic compensation is thus minimized. The APF is tuned to compensate for the current distortion up to the 25^{th} harmonic, while the DC bus voltage is regulated to achieve $M \simeq 0.9$ during APF operation. The P-RES and RESs gains are reported in Table 4.

The APF-GDPWM algorithm and SVPWM have been implemented on the APF, which can be alternatively interfaced to the grid through the *LCL* Filter 1 or 2 (as designed in Section V), according to which modulation technique is used. A HBM Genesis data recorder is connected between the *LCL* filter and the grid to evaluate the overall power converter losses, consisting in both the inverter and *LCL* filter losses (see Fig. 20).

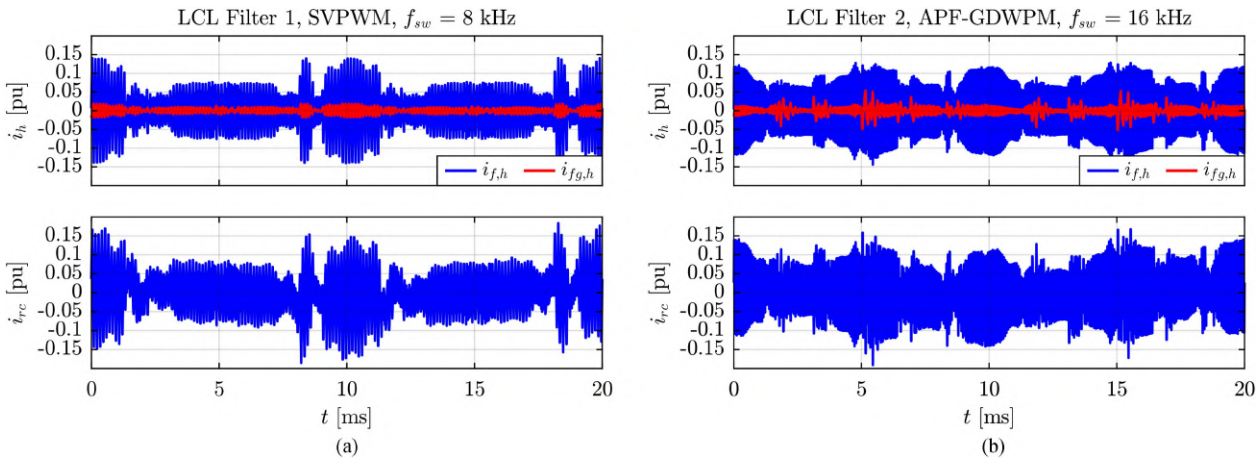

FIGURE 15. Simulation results: current ripple in the APF-side inductor L_f ($i_{f,h}$) and grid-side inductor $L_{f,g}$ ($i_{fg,h}$) and capacitor current (i_{rc}) obtained respectively with *LCL* Filter 1, SVPWM, $f_{sw} = 8$ kHz (a) and *LCL* Filter 2, APF-GDPWM, $f_{sw} = 16$ kHz (b).

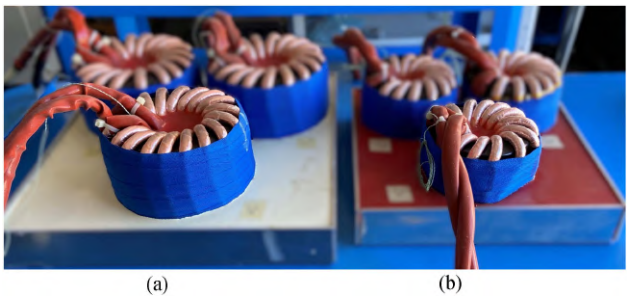

FIGURE 16. View of the APF-side inductor L_f of Filter 1 (a) and 2 (b). The inductors are encapsulated in thermally conductive resin. The volume and weight of each inductor are respectively 2.39l and 9.6 kg for Filter 1 and 1.30l and 5.8 kg for Filter 2.

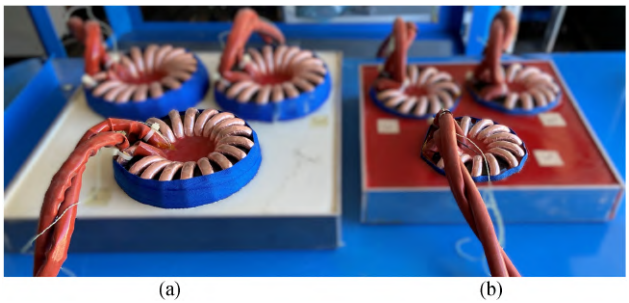

FIGURE 17. View of the APF-side inductor L_{fg} of Filter 1 (a) and 2 (b). The inductors are encapsulated in thermally conductive resin. The volume and weight of each inductor are, respectively, 1.59l and 6.5 kg for Filter 1 and 0.74l and 2.6 kg for Filter 2.

FIGURE 18. View of the capacitor board used both in Filter 1 and 2.

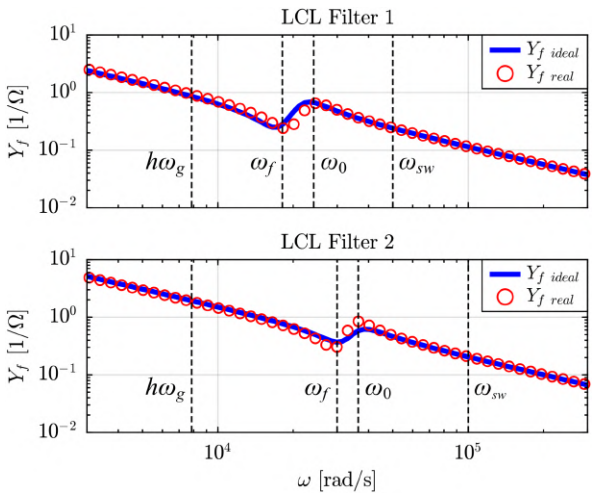

FIGURE 19. Expected (i.e., ideal) and measured (i.e., real) curves of Y_f for *LCL* Filter 1 and 2. The ideal curves are obtained from (19).

TABLE 4. APF Current Control Parameters

P-RES & RESs					
k_p	$0.7\ \frac{V}{A}$	k_1	$500\ \frac{V}{A \cdot s}$	k_6	$350\ \frac{V}{A \cdot s}$
k_{12}	$140\ \frac{V}{A \cdot s}$	k_{18}	$11\ \frac{V}{A \cdot s}$	k_{24}	$7\ \frac{V}{A \cdot s}$

The nonlinear load, APF and power system main data are the same of Table 2, while the system setup is shown in Fig. 22.

The full-power steady-state operation of the system is illustrated in Fig. 23, when the APF is connected to the PCC through the *LCL* Filter 2 and is using APF-GDPWM at $f_{sw} = 16$ kHz. Without the installation of the APF, the current

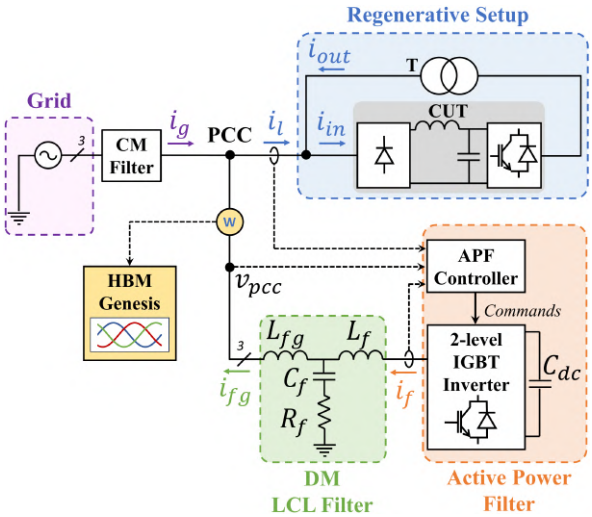

FIGURE 20. Scheme of the shunt-type APF in parallel to a regenerative system used for the final functional tests of industrial inverters.

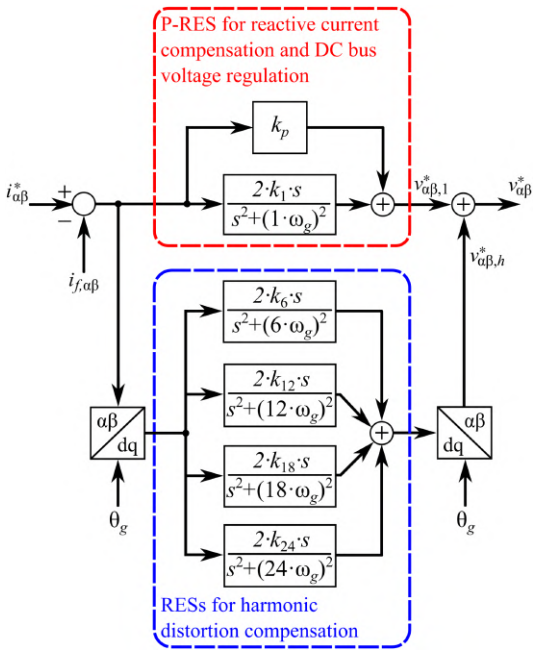

FIGURE 21. Block diagram of the implemented APF current control. θ_g is the PCC voltage vector position.

drawn from the grid would be $i_g = i_l = 170.0\ \mathrm{A_{rms}}$. Instead, with the compensation performed by the APF, i_g drastically reduces to 32.8 $\mathrm{A_{rms}}$ (-80.7%). The current reinjected at the PCC by the CUT (i_{out}) leads in phase the CUT absorbed current at the fundamental frequency ($i_{in,1}$). This phase shift is indicative of a reactive current injected by the regenerative system at ω_g, which is compensated by the APF, along with the distorted current, to make i_g at unity power factor. As can be observed in Fig. 23, i_{out} exhibits a high frequency current ripple due to the switching of the CUT ($f_{\mathrm{sw,CUT}} = 4$ kHz). This high frequency component propagates towards

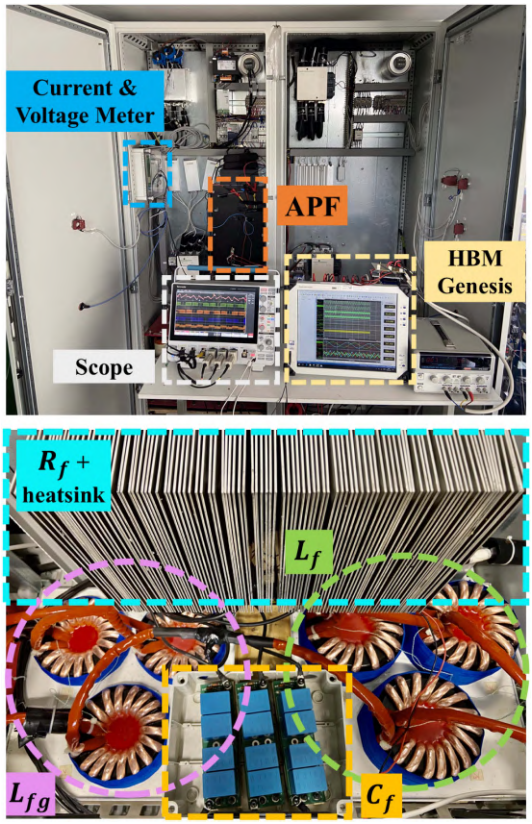

FIGURE 22. System setup: APF cabinet with measuring equipment (top) and assembled DM *LCL* filter (bottom).

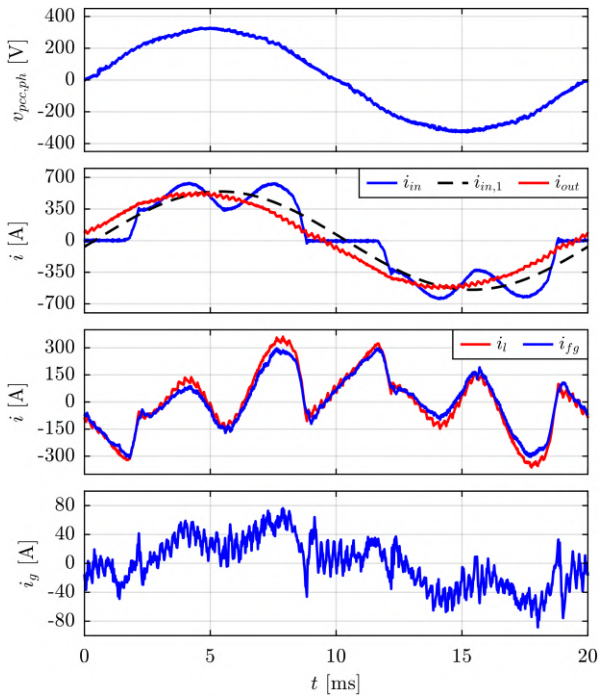

FIGURE 23. Full-power operation of the regenerative system with connected in parallel the APF. From top to bottom: phase PCC voltage $v_{\mathrm{pcc},ph}$, CUT input current i_{in} and its fundamental component $i_{\mathrm{in},1}$, CUT output current i_{out}, current absorbed by the regenerative system i_l, current injected by the APF at the PCC i_{fg}, grid current i_g.

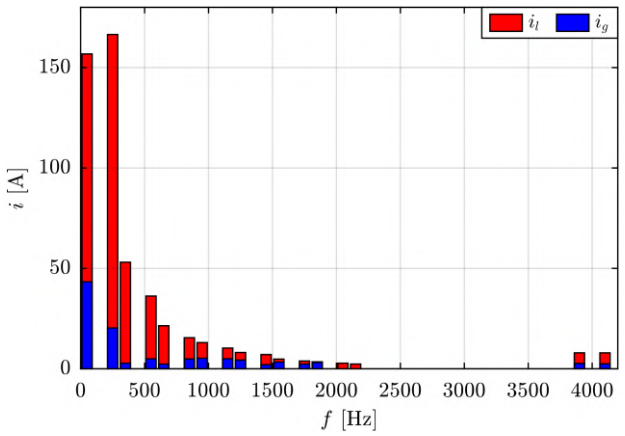

FIGURE 24. Compensation capability of the APF, while the regenerative system is full-power operating. The currents i_l and i_g are shown in the frequency domain. A 4 kHz disturbance can be observed on i_l and, more attenuated, on i_g.

the PCC and is measurable on i_l by the APF controller. As theoretically explained in Section II (see Fig. 3) and as will be also shown with the experimental tests, this noise can affect the computation of the zero sequence voltage in the case of an APF implementing APF-GDPWM. The APF compensation capability and the circulation of 4 kHz current noise on the power line are further demonstrated in Fig. 24, which shows i_l and i_g in the frequency domain.

Different tests are performed to evaluate the performance of the APF-GDPWM in comparison with SVPWM and the generalized DPWM technique for APFs presented in [20] as follows:

1) *Tests 1–2:* The performance of the APF using the APF-GDPWM technique and connected to the grid through the *LCL* Filter 2 is evaluated both in the case of bypass and proper tuning of the hysteresis selector, i.e., $\Delta i_{\text{th}} = 30$ A, approximately twice the amplitude of the circulating high frequency current disturbance shown in Fig. 24, thus also accounting for possible measurement noise. The disabling of the hysteresis selector is equivalent to using the method presented in [20]. Tests are performed with the system operating at full-power (Test 1) and at reduced power (1/10 of full power, Test 2).
2) *Test 3:* The APF current ripple injected into the grid $i_{fg,h}$ and the overall APF efficiency are analyzed in the case of three different configurations: implementation of SVPWM with $f_{\text{sw}} = 8$ kHz and grid connection through *LCL* Filter 1 (*Case 1*), implementation of APF-GDPWM with $f_{\text{sw}} = 16$ kHz and grid-interfacing through *LCL* Filter 1 (*Case 2*) or *LCL* Filter 2 (*Case 3*).

A. TESTS 1–2: IMPACT OF APF-GDPWM

The steady-state operation of the APF connected to the grid through the designed *LCL* filter 2 and implementing APF-GDPWM at $f_{\text{sw}} = 16$ kHz is illustrated in Figs. 25 and 27, respectively, in the case of CUT operating at full-power ($P_{\text{CUT}} = 260$ kW) in Test 1 and one-tenth-power ($P_{\text{CUT}} = 28$ kW) in Test 2, to demonstrate the effectiveness of the hysteresis selector. By reducing P_{CUT}, the behaviour of the CUT diode rectifier becomes more capacitive, resulting in a higher THD_i for the absorbed current i_{in}, which is, respectively, 34.3% in Test 1 and 106.7% in Test 2. In addition, the current reduces in magnitude and the current sensors sensitivity worsens, with a significant impact on the zero sequence voltage computation in the case of hysteresis selector disabled (i.e., null Δi_{th}). Indeed, when the hysteresis selector is bypassed, the unwanted repetitive changes of the clamped phase occur many times in a fundamental period, especially at low power in Test 2. Instead, the side effect is completely eliminated by setting $\Delta i_{\text{th}} = 30$ A for all system operating conditions, with the zero sequence modulation index $m_c = \frac{v^*_{\text{cm}}}{V_{\text{dc}}/2}$ and the phase modulation index $m = \frac{v^*}{V_{\text{dc}}/2}$ both exhibiting a trend without repetitive abrupt variations at the switching frequency. The main beneficial effect of implementing the hysteresis selector is the reduction of $i_{fg,h}$, thus limiting the impact of the APF high frequency ripple on the THD_i of the overall current absorbed at the PCC. In particular, the $i_{fg,h}$ RMS value is reduced by 12.7% in Test 1 and significantly by 41.5% in Test 2.

The benefits of the hysteresis selection on the CM voltage are highlighted in Fig. 26 for Test 1 and Fig. 28 for Test 2. The harmonic spectrum is divided into following three ranges.

1) *Low frequency*: it consists of the frequency components with $f \leq 1$ kHz, which are associated with the zero sequence voltage injection;
2) *Mid frequency*: it corresponds to the frequency range $f \in (1,12]$ kHz, an intermediate region of the harmonic spectrum, that normally has low harmonic content, since it is little affected by zero sequence injection and lies below the switching frequency ($f_{\text{sw}} = 16$ kHz).
3) *High frequency*: it contains all the harmonics related to the inverter switching, corresponding to $f > 12$ kHz.

While the implementation of the hysteresis selector does not impact on the overall CM RMS voltage V_{cm}, or the high frequency CM RMS voltage $V_{\text{cm},hf}$, it influences the harmonic distribution in the low and mid frequency ranges. In particular, without the hysteresis selector, the low frequency RMS content ($V_{\text{cm},lf}$) decreases, as part of the harmonics associated with the zero sequence injection shift into the mid frequency range. The enabling of the hysteresis selector confines these harmonics to the low frequency range, thus making the system less prone to the circulation of CM currents. The mid frequency CM RMS voltage $V_{\text{cm},mf}$ is thus reduced by 38.3 % in Test 1 and 72.9 % in Test 2.

The results of Tests 1–2 are summarized in Table 5, where all the relevant data for comparison are reported in absolute and relative values.

B. TEST 3: APF-GDPWM AND SVPWM COMPARISON

The power measurements and the APF high frequency current distortion analysis have been performed for the APF operating under three different configurations, while the regenerative

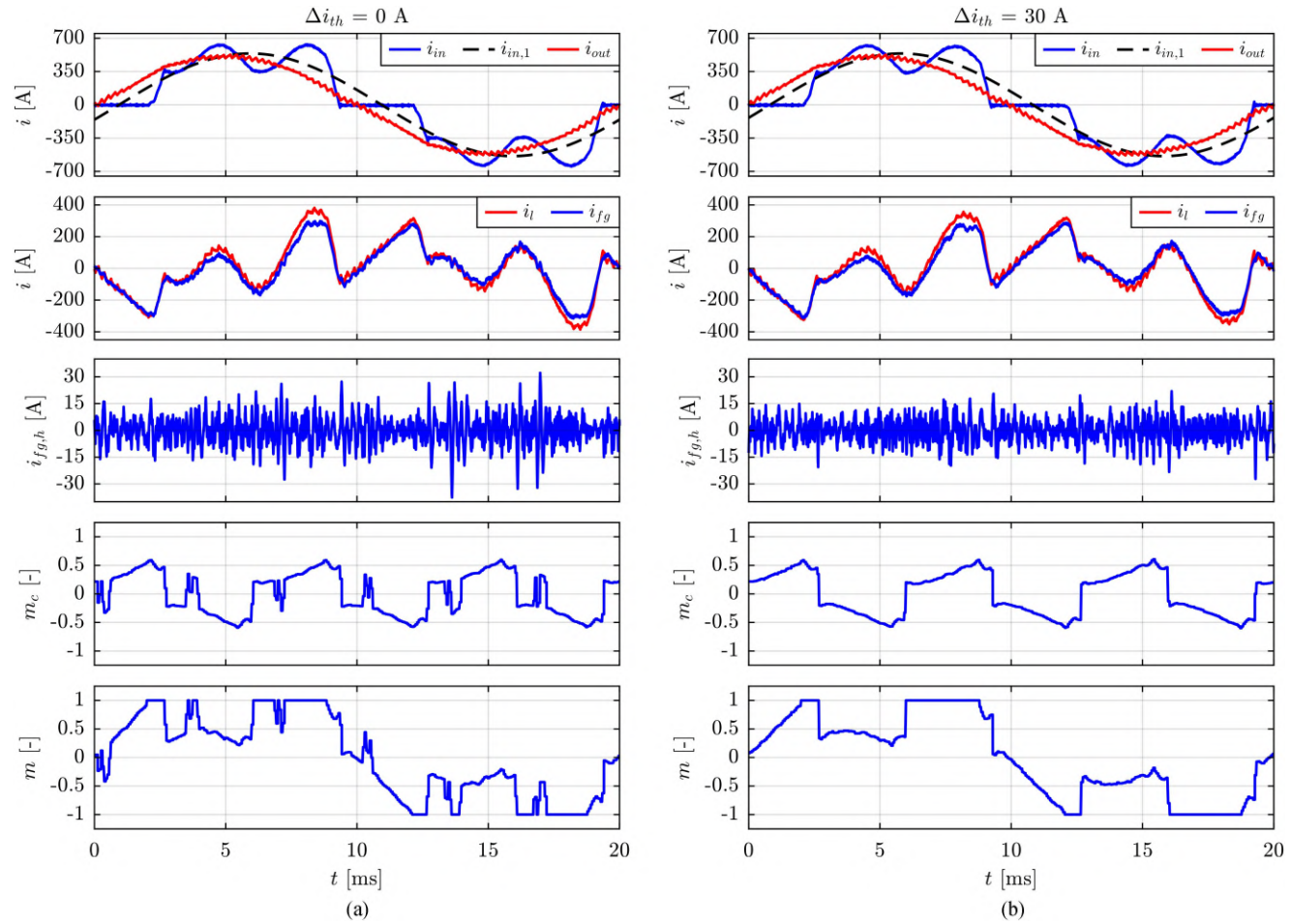

FIGURE 25. Test 1: system steady-state operation while the CUT is providing full-power (P_{CUT} = 260 kW). The APF is implementing APF-GDPWM with f_{sw} = 16 kHz in the case of hysteresis selector disabled (a) and enabled with Δi_{th} = 30 A (b). From top to bottom: CUT input current i_{in} and its fundamental component $i_{in,1}$, CUT output current i_{out}, current absorbed by the regenerative system i_l, current injected by the APF at the PCC i_{fg}, residual APF current ripple injected at the PCC $i_{fg,h}$, zero sequence modulation index m_c and phase modulation index m.

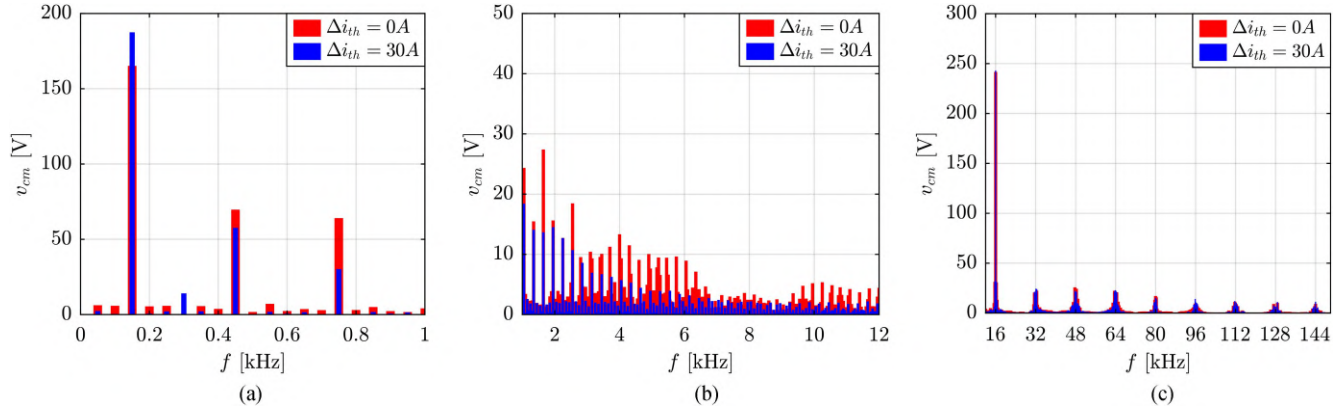

FIGURE 26. Test 1: system steady-state operation while the CUT is providing full-power (P_{CUT} =260 kW). CM voltage v_{cm} harmonic spectrum in the low frequency (a) mid frequency, (b) and high frequency (c) ranges.

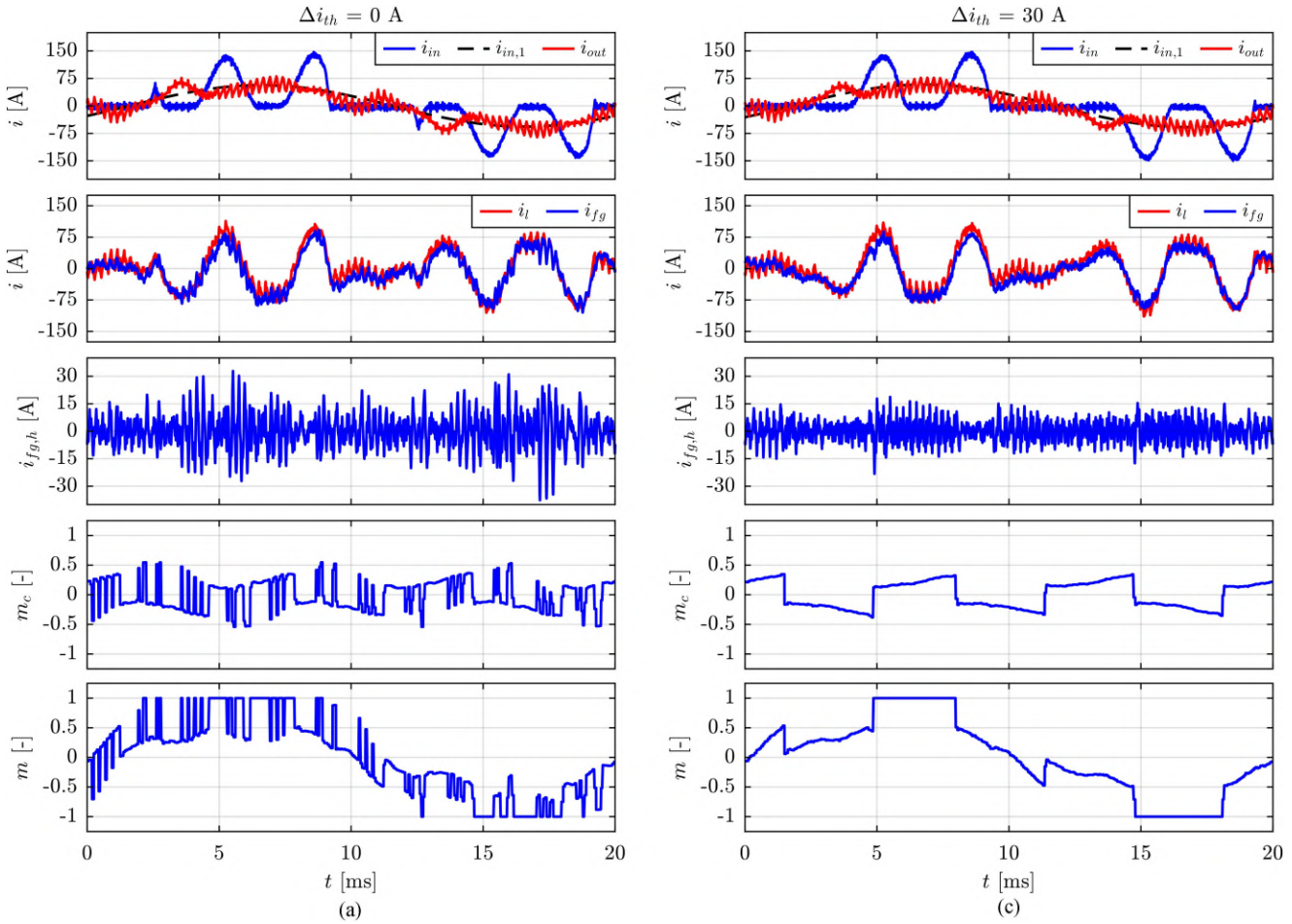

FIGURE 27. Test 2: system steady-state operation while the CUT is providing one-tenth-power (P_{CUT} =28 kW). The APF is implementing APF-GDPWM with f_{sw} = 16 kHz in the case of hysteresis selector disabled (a) and enabled with Δi_{th} = 30 A (b). From top to bottom: CUT input current i_{in} and its fundamental component $i_{in,1}$, CUT output current i_{out}, current absorbed by the regenerative system i_l, current injected by the APF at the PCC i_{fg}, residual APF current ripple injected at the PCC $i_{fg,h}$, zero sequence modulation index m_c and phase modulation index m.

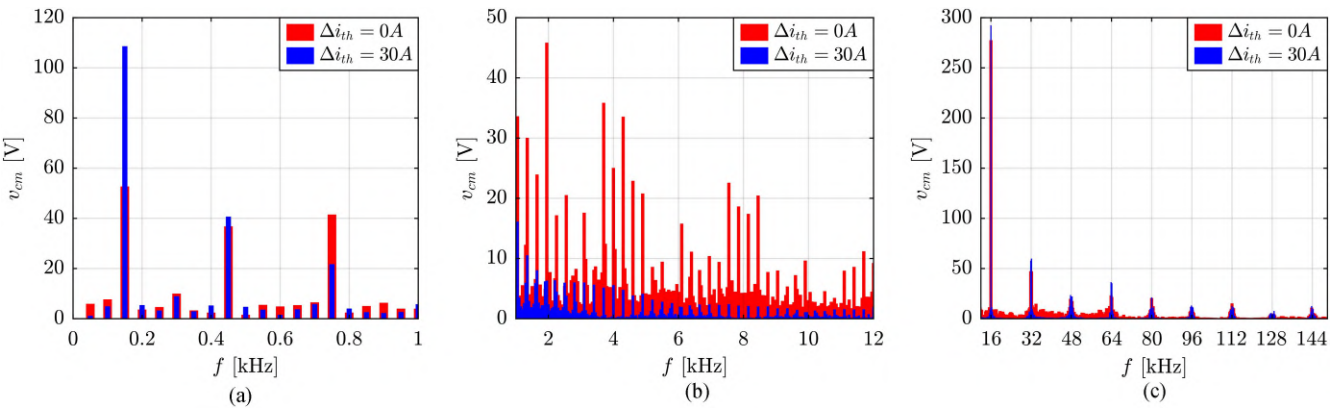

FIGURE 28. Test 2: system steady-state operation while the CUT is providing one-tenth-power (P_{CUT} = 28 kW). CM voltage v_{cm} harmonic spectrum in the low frequency (a) mid frequency, (b) and high frequency (c) ranges.

TABLE 5. EXPERIMENTAL RESULTS OF TESTS 1–2

Test	Notes	Quantity	Δi_{th} = 0 A	Δi_{th} = 30 A	
1	P_{CUT} =	**$I_{fg,h}$**	**7.9 A_{rms}**	**6.9 A_{rms}**	**-12.7 %**
	260 kW	$V_{cm,lf}$	137.9 V_{rms}	140.7 V_{rms}	+2.0 %
	THD_i =	**$V_{cm,mf}$**	**49.3 V_{rms}**	**30.4 V_{rms}**	**-38.3 %**
	34.3 %	$V_{cm,hf}$	193.4 V_{rms}	192.6 V_{rms}	-0.4 %
		V_{cm}	242.6 V_{rms}	240.5 V_{rms}	-0.9 %
2	P_{CUT} =	**$I_{fg,h}$**	**9.4 A_{rms}**	**5.5 A_{rms}**	**-41.5 %**
	28 kW	$V_{cm,lf}$	56.3 V_{rms}	84.5 V_{rms}	+50.1 %
	THD_i =	**$V_{cm,mf}$**	**89.4 V_{rms}**	**24.2 V_{rms}**	**-72.9 %**
	106.7 %	$V_{cm,hf}$	221.9 V_{rms}	227.7 V_{rms}	+2.6 %
		V_{cm}	245.8 V_{rms}	242.2 V_{rms}	-1.5 %

TABLE 6. EXPERIMENTAL RESULTS OF TEST 3

Quantity	Unit	Case 1	Case 2	Case 3
LCL Filter	-	1	1	2
Modulation	-	SVPWM	APF-GDPWM	APF-GDPWM
f_{sw}	kHz	8	16	16
$I_{fg,h}$	%	1.63	1.33	1.86
P_d*	%	0.22	0.10	0.16
P_{loss}	%	0.94	0.83	1.07

* P_d is not directly measured, but estimated by considering the damping resistance R_f and the capacitor current i_{rc}, while neglecting the skin effect.

system is full-power operating (P_{CUT} = 260 kW). In *Case 1*, the APF uses the SVPWM with f_{sw} = 8 kHz and it is connected to the grid through the *LCL* Filter 1. In *Case 2*, the *LCL* Filter 1 is installed and the APF-GDPWM with f_{sw} = 16 kHz is implemented. Instead, In *Case 3* APF-GDPWM with f_{sw} = 16 kHz is used, while the APF is grid-interfaced with the *LCL* Filter 2. The APF steady-state operation for the three test conditions is illustrated in Fig. 29, while the obtained results are reported in Table 6.

By comparing *Case 1* and *Case 2*, it emerges that APF-GDPWM allows the doubling of switching frequency from 8 to 16 kHz, without increasing the total losses. Indeed, without modifying the existing hardware (i.e., power switches and *LCL* filter), the measured losses for the converter operating at f_{sw} = 8 kHz using SVPWM (0.94% of P_{CUT}) are slightly higher than the losses obtained with the converter operating at f_{sw} = 16 kHz with APF-GDPWM (0.83% of P_{CUT}). An overall converter loss reduction is obtained although the regenerative system is an inductive nonlinear load (THD_i = 34.3%) and the switching losses reduction is less effective in this case, as demonstrated in Section III. Notably, the application of APF-GDPWM reduces also the capacitor current i_{rc} and consequently the estimated damping resistor losses P_d are 0.22% in case of SVPWM at f_{sw} = 8 kHz, while it is reduced to 0.10% with APF-GDPWM at f_{sw} = 16 kHz. The filter losses were not considered in the theoretical discussion and their reduction further validates the effectiveness of APF-GDPWM. Nevertheless, the doubling of the switching frequency in *Case 2* allows the reduction of the current ripple $i_{fg,h}$ injected into the grid by the APF (from 1.63% to 1.33% of $i_{in,1}$).

Finally, the comparison between *Case 1* and *Case 3* highlights that the implementation of APF-GDPWM with the doubling of the switching frequency allows for a more compact filter design, with reduced inductance, volume, and weight, while preserving similar results in terms of current ripple $i_{fg,h}$, overall power converter losses P_{loss} and damping resistor losses P_d.

Specifically, the *LCL* Filter 2, compared to *LCL* Filter 1, features a total inductance reduced by 53% (137 vs. 65 μ H), a single-phase L_f inductor with 46% less volume (2.39 vs. 1.30l) and 40% less weight (9.6 vs. 5.8 kg), a single-phase L_{fg} inductor with 54% less volume (1.59 vs. 0.74l) and 60% less weight (6.5 vs. 2.6 kg). Meanwhile, the obtained values of $i_{fg,h}$ and P_d respects the constraints imposed in (35) and (36) both in *Case 1* ($i_{fg,h}$ = 1.63% and P_d = 0.22%) and *Case 3* ($i_{fg,h}$ = 1.86% and P_d = 0.16%). Instead, the overall APF power losses P_{loss} account for approximately 1% of P_{CUT} (0.94 % in *Case 1* and 1.07 % in *Case 3*), ensuring a minimal impact of the APF on the overall power line consumption.

VII. CONCLUSION

This work proposes a design methodology of APFs operating in industrial disturbed environments, such as regenerative converter testing systems at the end of production lines. Starting from the selection of main hardware components, the proposed design methodology includes the proper selection of modulation strategy (APF-GDPWM), the computation of APF losses, the analysis of APF output current distortion and the design of the APF output DM *LCL* filter. To simplify the theoretical treatment, the analyses were performed assuming an APF compensating for the current distortion caused by an ideal nonlinear load. However, the results also apply to real cases, such as an APF compensating the distorted current drawn by a diode rectifier.

The experimental validation has been carried out on a TRL 9 industrial two-level IGBT APF compensating a regenerative testing system of 400 V, 260 kVA industrial AC–AC power converters. The experimental tests, performed in a real disturbed industrial environment, demonstrate the effectiveness of integrating a hysteresis selector within the APFGDPWM scheme, in contrast to the approach described in [20], which omits this functionality. Indeed, APF-GDPWM, compared to the solution in [20], reduces the current ripple injected into the grid and the applied high frequency CM voltage components

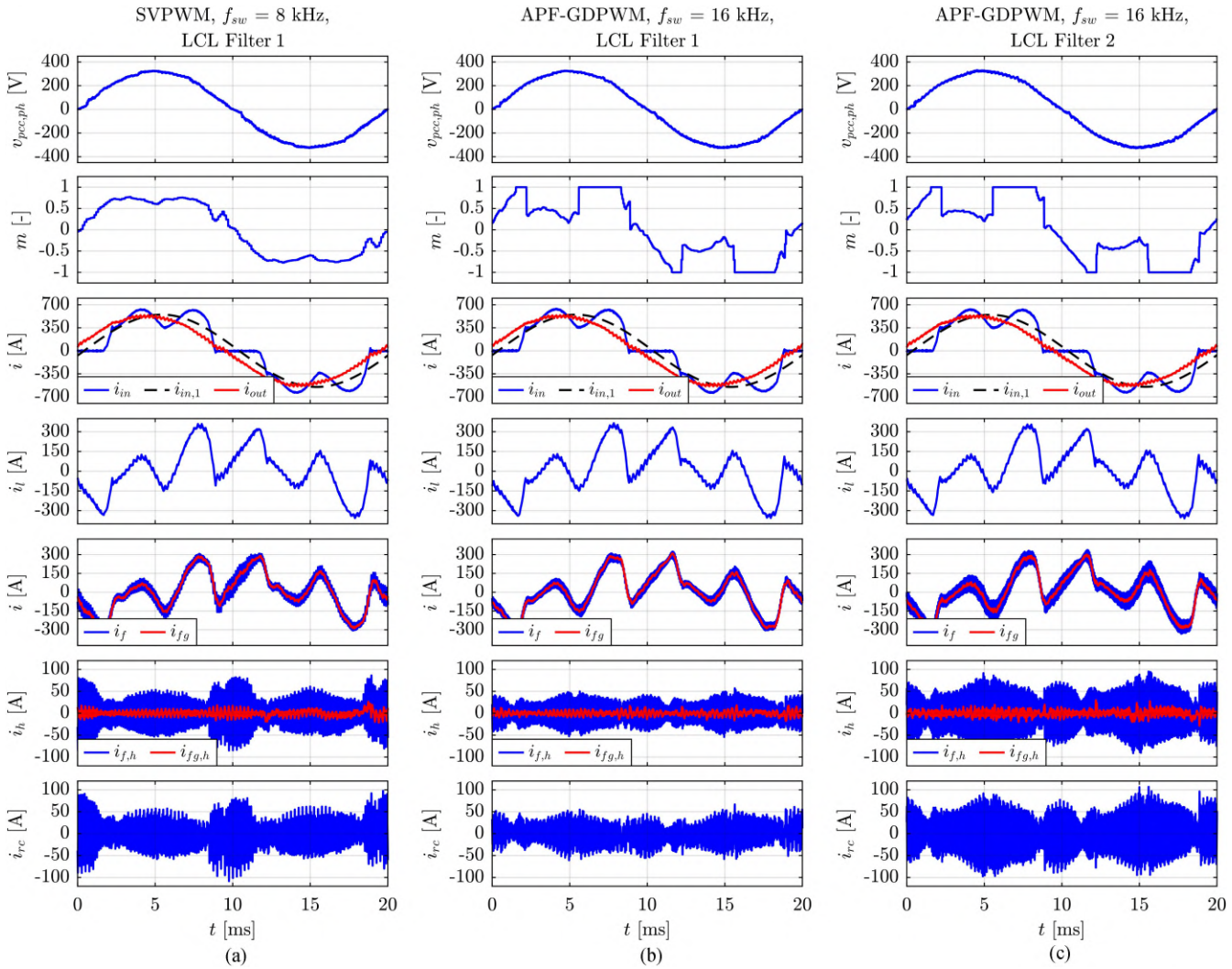

FIGURE 29. Test 3: APF steady state operation in case of SVPWM at f_{sw} = 8 kHz and installation of *LCL* Filter 1 (a) APF-GDPWM at f_{sw} = 16 kHz and installation of *LCL* Filter 1, (b) and APF-GDPWM at f_{sw} = 16 kHz and installation of *LCL* Filter 2. The CUT is providing full-power (P_{CUT} =260 kW). From top to bottom: phase PCC voltage $v_{pcc,ph}$, phase modulation index m, CUT input current i_{in} and its fundamental component $i_{in,1}$, CUT output current i_{out}, current absorbed by the regenerative system i_l, inverter-side APF current i_f, current injected by the APF at the PCC i_{fg}, high frequency current ripple $i_{f,h}$ and $i_{fg,h}$, capacitor current i_{rc}.

associated with the zero sequence voltage, thus limiting the risk of circulating CM currents.

Nevertheless, the results of the tests have shown that, compared to SVPWM, the APF-GDPWM provides a better exploitation of the existing hardware (i.e., inverter and DM *LCL* filter) by doubling the switching frequency from 8 to 16 kHz, with the benefit of current ripple (−18%) and power losses (−12%) reduction. Moreover, the control bandwidth may be increased, thus resulting in a better dynamic performance and higher harmonic orders compensation. Alternatively, implementing APF-GDPWM in combination with a doubled switching frequency enables the use of a reduced size and lower cost DM *LCL* filter, achieving a 46% reduction in volume and 40% in weight for the converter-side inductor L_f, and a 54% reduction in volume and 60% in weight for the grid-side inductor L_{fg}, while maintaining the same APF compensation performance and efficiency as with SVPWM.

Therefore, a two-level APF using APF-GDPWM can match the performance of more expensive hardware solutions, including three-level inverters implementing standard SVPWM, while offering significant cost advantages.

VII. APPENDIX

This section presents the computation of both conduction and switching losses for the power devices of a two-level three-phase APF.

B. CONDUCTION LOSSES

The mean value of conduction losses for a generic power switch (e.g., IGBT, MOSFET, etc.) over a switching period can

be expressed as follows [12]:

$$p_c = (R_{\text{on}} \cdot i_{\text{cell},x} + V_{\text{th}}) \cdot i_{\text{cell},x} \cdot d \tag{37}$$

where $i_{\text{cell},x}$ is the current flowing through the positive ($x = \text{pos}$) or negative ($x = \text{neg}$) unidirectional switching cell that includes the power switch (see Fig. 4); d is the duty cycle.

The current $i_{\text{cell},x}$ is assumed constant during a switching period. Instead, the term d is defined as follows:

$$d = \frac{v^* + v^*_{\text{cm}}}{V_{\text{dc}}} + \frac{1}{2} \tag{38}$$

where v^* is the leg reference voltage, while the zero sequence voltage v^*_{cm} depends on the adopted PWM strategy.

The mean value of the conduction losses over a fundamental period is thus obtained by combining (37) and (38) and performing the following integration:

$$P_c = \frac{1}{2\pi}\int_0^{2\pi} p_c \, d\theta \; = A + B + C \tag{39}$$

$$A = \frac{1}{2\pi}\int_0^{2\pi} \frac{R_{on} \cdot i^2_{\text{cell},x} \cdot v^*}{V_{\text{dc}}} + \frac{V_{th} \cdot i_{\text{cell},x} \cdot v^*}{V_{\text{dc}}} \, d\theta \tag{40}$$

$$B = \frac{1}{2\pi}\int_0^{2\pi} \frac{R_{\text{on}} \cdot i^2_{\text{cell},x} \cdot v^*_{\text{cm}}}{V_{\text{dc}}} + \frac{V_{\text{th}} \cdot i_{\text{cell},x} \cdot v^*_{\text{cm}}}{V_{\text{dc}}} \, d\theta \tag{41}$$

$$C = \frac{1}{2\pi}\int_0^{2\pi} \frac{R_{\text{on}} \cdot i^2_{\text{cell},x}}{2} + \frac{V_{\text{th}} \cdot i_{\text{cell},x}}{2} \, d\theta. \tag{42}$$

Term A (40) depends on the relationship between $i_{\text{cell},x}$ and v^*. It is a contribution related to the provision of active power (P_{apf}) by the converter. An APF injects only reactive (Q_{apf}) and deformed (D_{apf}) powers to counteract the nonlinear load current distortion, while drawing a small amount of P_{apf} to compensate for the converter losses. Therefore, term A is negligible for an APF.

Term B (41) is related to the interaction between $i_{\text{cell},x}$ and v^*_{cm}. As demonstrated in [12] for the case, where the output current consists only of the fundamental frequency, the zero sequence voltage does not influence the conduction losses, even in the case of multiharmonic injection. The value of B is thus null.

As a result, (39) depends only on term C (42), that can be detailed as follows:

$$C = \frac{R_{\text{on}}}{2} \cdot \frac{1}{2\pi}\int_0^{2\pi} i^2_{\text{cell},x} \, d\theta + \frac{V_{\text{th}}}{2} \cdot \frac{1}{2\pi}\int_0^{2\pi} i_{\text{cell},x} \, d\theta$$

$$P_c = C = \frac{R_{\text{on}}}{2} \cdot I^2_{\text{cell},x,\text{rms}} + \frac{V_{\text{th}}}{2} \cdot I_{\text{cell},x,m}. \tag{43}$$

C. SWITCHING LOSSES

By assuming a linear dependency of the switching energy loss on the switched current [12], the mean value of switching losses for a generic power switch over a switching period can be expressed as follows:

$$p_{\text{sw}} = \frac{E_{\text{sw}}}{V_{\text{dc},n} \cdot I_n} \cdot f_{\text{sw}} \cdot V_{\text{dc}} \cdot i_{\text{cell},x,\text{sw}} \tag{44}$$

where $i_{\text{cell},x,\text{sw}}$ is the unidirectional cell switched current.

As proposed in [12], [13], [45], under the assumption of constant junction temperature, E_{sw} can be assumed approximately linear dependent on V_{dc} and $i_{\text{cell},x,\text{sw}}$. This assumption is supported by the application manuals provided by power modules manufacturers [46]. Moreover, the hypothesis of a linear dependence of E_{sw} on V_{dc} is experimentally validated in [47], while the linear relationship between E_{sw} and $i_{\text{cell},x,\text{sw}}$ is confirmed by the experimental curves typically reported in the datasheets of power switches modules, e.g., in [30].

The current $i_{\text{cell},x,\text{sw}}$ is null when the inverter leg is clamped to the positive or negative DC rail, otherwise it equals i_{cell} [13]

$$i_{\text{cell},x,\text{sw}} = \begin{cases} 0, & d = 0 \vee d = 1 \\ i_{cell,x} & 0 < d < 1 \end{cases}. \tag{45}$$

In the case of using a CPWM, $i_{\text{cell},x,\text{sw}} = i_{\text{cell},x}$ at all times. The mean value of the switching losses obtained with standard CPWMs over a fundamental period is given by the following:

$$P_{\text{sw,CPWM}} = \frac{1}{2\pi}\int_0^{2\pi} p_{\text{sw,CPWM}} \, d\theta$$

$$P_{\text{sw,CPWM}} = \frac{E_{\text{sw}}}{V_{\text{dc},n} \cdot I_n} \cdot f_{\text{sw}} \cdot V_{\text{dc}} \cdot \frac{1}{2\pi}\int_0^{2\pi} i_{\text{cell},x} \, d\theta$$

$$P_{\text{sw,CPWM}} = \frac{E_{\text{sw}}}{V_{\text{dc},n} \cdot I_n} \cdot f_{\text{sw}} \cdot V_{\text{dc}} \cdot I_{\text{cell},x,m}. \tag{46}$$

By definition, the switching loss factor relates the switching losses obtained with a specific PWM technique, such as APF-GDPWM, and standard CPWMs (3). A generalized formulation of the switching losses for any modulation technique is thus obtained by combining (3) with (46)

$$P_{\text{sw}} = \frac{E_{\text{sw}}}{V_{\text{dc},n} \cdot I_n} \cdot f_{\text{sw}} \cdot V_{\text{dc}} \cdot k_{\text{sw}} \cdot I_{\text{cell},x,m}. \tag{47}$$

The calculation of P_c and P_{sw} has been carried out for the power switch. However, identical results to those in (43) and (47) would be obtained in the analysis of power losses for the freewheeling diode.

REFERENCES

[1] K. Ma, S. Xia, Y. Qi, X. Cai, Y. Song, and F. Blaabjerg, "Power-electronics-based mission profile emulation and test for electric machine drive system—concepts, features, and challenges," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8526–8542, Jul. 2022.

[2] R. Bojoi, E. Armando, S. G. Rosu, S. Vaschetto, and P. Soccio, "Virtual load with common mode active filtering for power hardware-in-the-loop testing of power electronic converters," in *Proc. 40th Annu. Conf. IEEE Ind. Electron. Soc.*, 2014, pp. 1875–1881.

[3] P. Sandholdt, E. Ritchie, J. K. Pedersen, and R. E. Betz, "A dynamometer performing dynamical emulation of loads with nonlinear friction," in *Proc. IEEE Int. Symp. Ind. Electron.*, 1996, pp. 873–878.

[4] T. Boller and R. M. Kennel, "Virtual machine — A hardware in the loop test for drive inverters," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–5.

[5] *IEEE Standard for Harmonic Control in Electric Power Systems*. IEEE Std 519-2022 (Revision of IEEE Std 519-2014), 2022, pp. 1–31.

[6] W. M. Grady, M. J. Samotyj, and A. H. Noyola, "Survey of active power line conditioning methodologies," *IEEE Trans. Power Del.*, vol. 5, no. 3, pp. 1536–1542, Jul. 1990.

[7] H. Akagi, "New trends in active filters for power conditioning," *IEEE Trans. Ind. Appl.*, vol. 32, no. 6, pp. 1312–1322, Nov./Dec. 1996.

[8] B. Singh, K. Al-Haddad, and A. Chandra, "A new control approach to three-phase active filter for harmonics and reactive power compensation," *IEEE Trans. Power Syst.*, vol. 13, no. 1, pp. 133–138, Feb. 1998.

[9] D. Li, T. Wang, W. Pan, X. Ding, and J. Gong, "A comprehensive review of improving power quality using active power filters," *Electric Power Syst. Res.*, vol. 199, 2021, Art. no 107389.
[10] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1281–1291, Sep./Oct. 2005.
[11] C. Lascu, L. Asiminoaei, I. Boldea, and F. Blaabjerg, "High performance current controller for selective harmonic compensation in active power filters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1826–1835, Sep. 2007.
[12] J. W. Kolar, H. Ertl, and F. C. Zach, "Influence of the modulation method on the conduction and switching losses of a PWM converter system," *IEEE Trans. Ind. Appl.*, vol. 27, no. 6, pp. 1063–1075, Nov./Dec. 1991.
[13] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "A high-performance generalized discontinuous PWM algorithm," *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1059–1071, Sep./Oct. 1998.
[14] T. D. Nguyen, J. Hobraiche, N. Patin, G. Friedrich, and J.-P. Vilain, "A direct digital technique implementation of general discontinuous pulse width modulation strategy," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4445–4454, Sep. 2011.
[15] J. Lee, M.-W. Kim, and J.-W. Park, "Carrier selection strategy of generalized discontinuous PWM method for current reduction in DC-link capacitors of VSI," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10428–10442, Sep. 2022.
[16] B. Ciftci and A. M. Hava, "Performance evaluation and selection of PWM switching and control methods for grid connected modular multilevel converters," in *Proc. 2015 IEEE Energy Convers. Congr. Expo.*, 2015, pp. 3622–3629.
[17] H. Xu, L. Xu, K. Wang, Z. Zheng, and Y. Li, "Switching losses reduction of grid-tied inverters with variable switching frequency discontinuous PWM," in *Proc. 2019 IEEE Energy Convers. Congr. Expo.*, 2019, pp. 1567–1573.
[18] Z. Jankovic, P. Murthy, L. Wei, and A. Nasiri, "Dynamic discontinuous PWM for grid-tied inverter applications," in *Proc. 2020 IEEE Energy Convers. Congr. Expo.*, 2020, pp. 5032–5039.
[19] P. Karamanakos, M. Nahalparvari, and T. Geyer, "Fixed switching frequency direct model predictive control with continuous and discontinuous modulation for grid-tied converters with LCL filters," *IEEE Trans. Control Syst. Technol.*, vol. 29, no. 4, pp. 1503–1518, Jul. 2021.
[20] L. Asiminoaei, P. Rodriguez, and F. Blaabjerg, "Application of discontinuous PWMModulation in active power filters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1692–1706, Jul. 2008.
[21] A. Roveri, F. Mandrile, V. Mallemaci, and R. Bojoi, "Discontinuous PWM modulation for active power filters operating in disturbed environments," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2023, pp. 6429–6436.
[22] H. W. van der Broeck, H.-C. Skudelny, and G. V. Stanke, "Analysis and realization of a pulsewidth modulator based on voltage space vectors," *IEEE Trans. Ind. Appl.*, vol. 24, no. 1, pp. 142–150, Jan./Feb. 1988.
[23] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "Simple analytical and graphical methods for carrier-based PWM-VSI drives," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 49–61, Jan. 1999.
[24] O. Lopez et al., "Eliminating ground current in a transformerless photovoltaic application," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 140–147, Mar. 2010.
[25] M. C. Cavalcanti et al., "Modulation techniques to eliminate leakage currents in transformerless three-phase photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 4, pp. 1360–1368, Apr. 2010.
[26] E. Un and A. M. Hava, "A near-state PWM method with reduced switching losses and reduced common-mode voltage for three-phase voltage source inverters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 2, pp. 782–793, Mar./Apr. 2009.
[27] A. W. Kelley and W. F. Yadusky, "Rectifier for minimum line-current harmonics and maximum power factor," *IEEE Trans. Power Electron.*, vol. 7, no. 2, pp. 332–341, Apr. 1992.
[28] P. Pejovic and J. W. Kolar, "Exact analysis of three-phase rectifiers with constant voltage loads," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 8, pp. 743–747, Aug. 2008.
[29] R. I. Bojoi, G. Griva, V. Bostan, M. Guerriero, F. Farina, and F. Profumo, "Current control strategy for power conditioners using sinusoidal signal integrators in synchronous reference frame," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1402–1412, Nov. 2005.
[30] Mitsubishi Electric, "CM450DX-24T1/CM450DXP-24T1 Datasheet", Jan. 2025.
[31] E. Kantar and A. M. Hava, "Optimal design of grid-connected voltage-source converters considering cost and operating factors," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5336–5347, Sep. 2016.
[32] S. Jayalath and M. Hanif, "Generalized LCL-filter design algorithm for grid-connected voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 1905–1915, Mar. 2017.
[33] D. Cittanti, F. Mandrile, M. Gregorio, and R. Bojoi, "Design space optimization of a three-phase LCL filter for electric vehicle ultra-fast battery charging," *Energies*, vol. 14 no. 5, 2021, Art. no. 1303.
[34] S. Rubino, "Advanced electric drives: Modeling, design, and implementation - Part I," University Lecture–PhD Program in Electrical, Electronics and Communications Engineering, Politecnico di Torino, 2025, doi: 10.13140/RG.2.2.20222.70722.
[35] S. Rubino, "Advanced electric drives: Modeling, design, and implementation - Part II," University Lecture–PhD Program in Electrical, Electronics and Communications Engineering, Politecnico di Torino, 2025, doi: 10.13140/RG.2.2.33644.48004.
[36] R. N. Beres, X. Wang, M. Liserre, F. Blaabjerg, and C. L. Bak, "A review of passive power filters for three-phase grid-connected voltage-source converters," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 54–69, Mar. 2016.
[37] M. T. Bina and E. Pashajavid, "An efficient procedure to design passive LCL-filters for active power filters," *Electric Power Syst. Res.*, vol. 79, no. 4, pp. 606–614, 2009.
[38] Y. Tang, P. C. Loh, P. Wang, F. H. Choo, F. Gao, and F. Blaabjerg, "Generalized design of high performance shunt active power filter with output LCL filter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1443–1452, Mar. 2012.
[39] Q. Liu, L. Peng, Y. Kang, S. Tang, D. Wu, and Y. Qi, "A novel design and optimization method of an LCL filter for a shunt active power filter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 4000–4010, Aug. 2014.
[40] L. Zhou, Z. Liu, Y. Ji, D. Ma, J. Wang, and L. Li, "A improved parameter design method of LCL APF interface filter," in *Proc. IEEE Int. Conf. Artif. Intell. Comput. Appl.*, 2020, pp. 948–952.
[41] M. K. De Meerendre, E. Prieto-Araujo, K. H. Ahmed, O. Gomis-Bellmunt, L. Xu, and A. Egea-Álvarez, "Review of local network impedance estimation techniques," *IEEE Access*, vol. 8, pp. 213647–213661, 2020.
[42] J. Dannehl, F. W. Fuchs, S. Hansen, and P. B. Thøgersen, "Investigation of active damping approaches for PI-based current control of grid-connected pulse width modulation converters with LCL filters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 4, pp. 1509–1517, Jul./Aug. 2010.
[43] R. Peña-Alzola, M. Liserre, F. Blaabjerg, M. Ordonez, and Y. Yang, "LCL-filter design for robust active damping in grid-connected converters," *IEEE Trans. Ind. Informat.*, vol. 10, no. 4, pp. 2192–2203, Nov. 2014.
[44] A. Camboni, A. Roveri, F. Mandrile, and R. Bojoi, "Simple active damping solution for industrial grid-tied inverters using LCL filters," in *Proc. IEEE Energy Convers. Conf. Congr. Expo.*, 2025, pp. 1–7.
[45] Y. Zhu, M. Xiao, X. Su, G. Yang, K. Lu, and Z. Wu, "Modeling of conduction and switching losses for IGBT and FWD based on SVPWM in automobile electric drives," *Appl. Sci.*, vol. 10 no. 13, 2020, Art. no. 4539.
[46] S. Danfoss. *Application Manual Power Semiconductors*. Nuremberg, Germany: SEMIKRON International GmbH, Feb. 2025.
[47] S. C. Das, G. Narayanan, and A. Tiwari, "Experimental study on the dependence of igbt switching energy loss on DC link voltage," in *Proc. IEEE Int. Conf. Power Electron. Drives Energy Syst.*, 2014, pp. 1–5.

ALESSANDRO ROVERI (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degree in electrical engineering in 2016 and 2019, respectively, from Politecnico di Torino, Turin, Italy, where he is working toward the Ph.D. degree in electrical engineering.

He has been an R&D Engineer of the company Prima Electro S.p.A., Moncalieri (TO), Italy, since 2018. He is focusing his research activity on the control of grid-connected power converters, virtual synchronous machines and ultra-fast charging systems.

VINCENZO MALLEMACI (Member, IEEE) was born in Messina, Italy, in 1996. He received the bachelor's and master's degrees both in electrical engineering from Politecnico di Torino, Italy, in 2018 and 2020, respectively. He received the Ph.D. degree in electrical engineering with Dipartimento Energia "G. Ferraris", Politecnico di Torino, in 2024.

His Ph.D. activity focused on virtual synchronous machines and control for power electronic grid–connected converters.

FABIO MANDRILE (Member, IEEE) received the M.Sc. and Ph.D. degrees in electrical engineering from Politecnico di Torino, Torino, Italy, in 2017 and 2021, respectively.

His main research interests include virtual synchronous generators, power electronics for grid-connected applications, the experimental characterization of converters, and motor drives.

RADU BOJOI (Fellow, IEEE) received the M.Sc. degree in electrical engineering from the Technical University of Iasi, Iasi, Romania, in 1993, and the Ph.D. degree in electrical engineering from the Politecnico di Torino, Turin, Italy, in 2002.

He is currently a Full Professor of power electronics and electrical drives with the Energy Department "G. Ferraris" and the Chairman of the Power Electronics Innovation Center, Politecnico di Torino. He has authored or coauthored more than 200 papers covering electrical drives and power electronics for industrial applications, transportation electrification, power quality, and home appliances.

Dr. Bojoi is past Co-Editor-In-Chief of IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS. He is the recipient of six IEEE paper awards. He is involved in many research projects with industry aiming at obtaining new products involving emerging technologies.