A versatile readout system for front-end ASICs with HLS-based hardware-accelerated processing capabilities

A versatile readout system for front-end ASICs with HLS-based hardware-accelerated processing capabilities

Published by IOP Publishing for Sissa Medialab

Received: *November 6, 2025*
Accepted: *January 6, 2026*
Published: *January 28, 2026*

Topical Workshop on Electronics for Particle Physics
Rethymno, Crete, Greece
6–10 October 2025

A versatile readout system for front-end ASICs with HLS-based hardware-accelerated processing capabilities

Valerio Pagliarino[a,b,*] **Alberto Bortone**[b] **Davide Falchieri**[c] **Umberto Follo**[a,b] **Emanuela Petrini**[d] **Angelo Rivetti**[b] **Manuel Dionisio Da Rocha Rolo**[b] **and Stefan Cristi Zugravel**[b]

[a] *Dipartimento di Elettronica e Telecomunicazioni, Politecnico di Torino, Corso Duca degli Abruzzi 24, 10129 Torino, Italy*
[b] *Sezione di Torino, INFN, Via Giuria 1, 10125 Torino, Italy*
[c] *Sezione di Bologna, INFN, Viale Carlo Berti Pichat 6/2, 40127 Bologna, Italy*
[d] *Dipartimento di Informatica, Università degli Studi di Torino, Corso Svizzera 185, 10149 Torino, Italy*

E-mail: valerio.pagliarino@polito.it

Abstract: This paper presents a versatile readout system for particle detector front-end ASICs based on the AMD Zynq Ultrascale+ System-on-Chips. The system is suitable for both extensive laboratory characterization and for data acquisition at test beam facilities. Its software-level scripting of the test procedure reduces the firmware development effort, maximizing the system reusability among different DUTs. At the same time, the integration with High-Level Synthesis flows allows the deployment of real-time data processing algorithms in hardware, offloading the ARM processor. The system has been tested in different use cases, including the mixed-signal data acquisition from monolithic CMOS sensors for timing applications at test beam facilities and the readout of CMOS sensors for tracking and tomographic imaging.

Keywords: Data acquisition circuits; Data acquisition concepts; Digital electronic circuits

*Corresponding author.

https://doi.org/10.1088/1748-0221/21/01/C01047

Contents

2026 JINST 21 C01047

1 Introduction

The continuous evolution of detector front-end electronics for particle physics experiments demands increasingly sophisticated and flexible testing and data acquisition systems. Within this context, the INFN Torino VLSI group has been developing a broad portfolio of custom ASICs optimized for different detector technologies and experimental environments, ranging from high-channel-count devices such as DENEB [1] to precision timing and photon-counting chips such as ALCOR [2].

Each of these ASICs presents distinct requirements in terms of analog front-end performance, data throughput, configuration interfaces, and operating conditions, but they share a common need for a flexible data-acquisition and testing system to be used both for extensive characterization in the lab and during test beams. Traditional DAQ systems, often tailored to a single ASIC or detector prototype, tend to require significant firmware redevelopment and hardware adaptation when changing the Device Under Test (DUT), resulting in long deployment times and limited reuse of existing components.

To overcome these limitations, this work introduces a versatile, software-defined, SoC-based test and readout system capable of supporting multiple generations and families of front-end ASICs thanks to its modular architecture. Therefore, the design of this DAQ system has been driven by three main requirements:

- *A Software-Oriented System.* A Software Defined DAQ is required in order to reduce the firmware development effort when changing the DUT, thus reducing the time-to-operation and allowing the involvement of personnel without a strong background in digital design. The High-Level Synthesis tools are introduced for implementing high-throughput signal processing on the incoming stream from the DUT with software languages such as C and C++.

- *Ensuring High Data Bandwidth.* Firmware components are still essential because the data throughput of the new ASICs is continuously growing, asking for readout capabilities beyond 10 Gbps also during laboratory characterization and test beam campaigns.

- *Scalable and Modular.* The System must be easy to scale to a large number of DUTs, to a large number of interconnected SoC-boards and to a production-grade system on a custom DAQ card. The System must be easy to use not only for testing, but also during the ASIC DFT/verification flow.

2 System architecture

The SoC-based Test System (STS) is built around a central unit featuring an AMD Xilinx UltraScale+ MPSoC (ZU9EG series) device, which integrates on a single chip a 16 nm FinFET FPGA fabric, a quad-core 64-bit ARM processor, a real-time processing unit, and a high-performance memory and I/O subsystem. The platform, described in figure 1, provides multiple multi-gigabit transceivers supporting data rates up to 12 Gbps [3]. Two ANSI/VITA 57.1 FMC HPC connectors allow direct interfacing with the DUT, providing digital connectivity. The system also includes a SATA III interface linked to an external SSD, which hosts the custom Linux operating system, while four additional multi-gigabit transceivers are routed to SFP+ cages that can be configured either as a 10 Gbps Ethernet interface or as a 12 Gbps AXI Stream over Aurora link for high-speed data transmission to external storage servers.

A 4 GB SoDIMM DDR4 memory module is attached to the Processing System (PS), complemented by an additional DDR4 memory bank connected to the Programmable Logic (PL).

The STS is embedded within a dedicated 1–10 Gbps Ethernet network interconnecting auxiliary components required for mixed-signal ASIC characterization. These include:

- A *4-channel, 25 GSa/s, 8 GHz digitizer* with 12-bit resolution, used to acquire high-bandwidth analog signals generated by the DUT.

- A *2-channel, 10 GSa/s, 4 GHz arbitrary waveform generator (AWG)* with 16-bit resolution, employed as a programmable detector emulator connected through a custom coupling board that reproduces the sensor capacitance.

- A *networking and computing infrastructure* comprising optical and copper Ethernet switches, a DHCP-enabled router, network-attached storage units, and dedicated computing servers for online data processing and analysis.

- *External power supplies, clock generators, moving stages and laser drivers* with Ethernet connectivity that can be easily integrated inside the testing flow using a Python library that wraps SPCI commands into higher level classes.

While the Ethernet network is sufficient for slow control and data transfer, the timing-critical synchronization between the arbitrary waveform generator, the digitizer and the central unit is guaranteed by distributing a common clock and trigger signals on dedicated coaxial cables that are interconnected with the MPSoC board using a custom coaxial-to-FMC fixture.

The architecture is based on a tight integration between the software level (running on PS) and the synthesized hardware in the programmable logic (PL) using the AXI protocols. A middle layer of firmware and software provides slow control, data transfer and ancillary functionalities, reducing

2026 JINST 21 C01047

the amount of ASIC-dependent code, the software stack runs on the top of a custom Linux image generated using the *Petalinux* Flow. In the software stack, the full set of Linux tools is available as well as SSH remote access data analysis tools and packet managers.

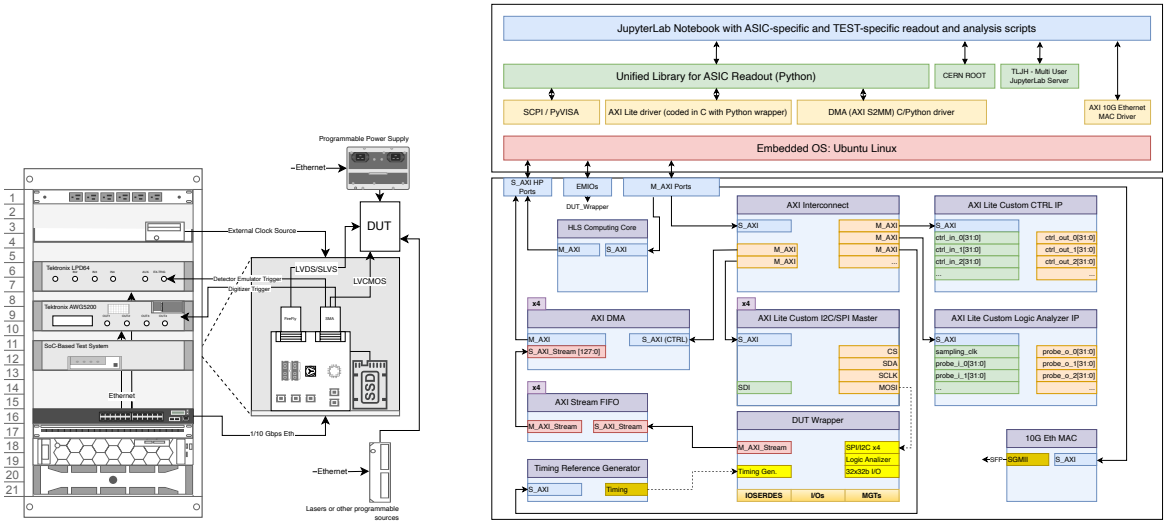

Figure 1. Hardware and Architecture Diagram of the System.

2.1 Firmware components

The primary objective in developing the firmware was to implement a modular and reusable architecture in which the DUT-dependent IP cores are encapsulated within a dedicated block, referred to as the *DUT Wrapper*. This structure allows the user to easily modify or redesign the DUT-specific logic starting from a predefined template. The DUT Wrapper communicates with a middle layer of firmware components responsible for managing the interfaces with the MPSoC programmable system, including the DUT slow-control interfaces, data paths, and high-speed connectivity.

This middle layer provides the designer of the DUT-specific RTL code with a set of standardized services, controlled through a unified software library integrated into the ASIC-specific testing framework. Sixteen CPU-to-DUT and sixteen DUT-to-CPU AXI-Lite buses (32-bit wide) can be accessed from the software to handle hardware reset signals, general-purpose I/O, and enable lines. Two high-speed AXI Stream interfaces (128-bit wide) are connected to a pair of DMA controllers that stream incoming data to the DDR4 memory linked to the Processing System. Data-word polling and DMA channel arbitration are managed by dedicated AXI-Lite registers controlled through the DMA driver, ensuring a theoretical maximum data throughput of the PL-PS interface of 42.6 Gbps. The system is typically operated with the AXI logic clocked at 200 MHz and the maximum achieved global throughput is 7.5 Gbps using the PL optical link, from the PL to the external storage server.

The firmware also includes four slow-control IP cores implementing I^2C, SPI, and JTAG master interfaces. A custom logic analyzer IP, accessible via an AXI-Lite interface, provides functionality analogous to the Xilinx Integrated Logic Analyzer (ILA) [4], but can be directly operated by the software running on the Processing System instead of through an external JTAG connection. Additional modules include a timing-reference generator, a 10 Gbps Ethernet or AXI-over-Aurora transmission IP for high-speed data transfer, and a wrapping logic for real-time data-processing IP cores generated

2026 JINST 21 C01047

through the High-Level Synthesis (HLS) flow. Firmware sources implementing data links management, 8b/10b decoding, data word alignment and eye-diagram sampling point optimization are available as RTL modules that are instantiated inside the DUT wrapper.

2.2 Back-end software components

At the core of the back-end software architecture, there is a low-level driver written in C creates a virtual device interface that enables controlled access to the specific region of the CPU address space where the firmware-mapped registers are located. This mechanism allows the higher-level software to communicate seamlessly with the hardware without requiring direct memory manipulation. A Python library operates on top of this driver, providing unified control over both the DUT and the overall test system, as well as managing data transfer operations. To optimize throughput, the data-word polling and arbitration routines associated with the AXI DMA channels are implemented in C++. The configuration parameters of the DUT and the test system are encoded in JSON-like data structures.

2.3 Front-end software components

The front-end software provides the user-level control interface for the DUT and is implemented in Python on top of the unified back-end library. Interactive operation is enabled through a *Jupyter Lab* environment with an automated widget generator that parses the JSON-like configuration structures defining the DUT parameters and creates the corresponding input fields. Alternatively, a Python REST API based on the *Flask* framework exposes read and write methods for these parameters, allowing remote configuration and control. This solution is more effective when several DAQ units operate in parallel under the supervision of a central system.

3 The Verification IPs flow

The synthesizable SystemVerilog RTL within the DUT Wrapper, implementing functions such as 8b/10b decoding, data alignment, and slow control, can be reused prior to ASIC fabrication as a suite of Verification IPs (VIPs) integrated into the chip verification environment. This approach provides a realistic model of the DAQ logic, reducing testbench development time and ensuring consistency between simulation and experimental validation.

A dedicated export flow generates the required verification IPs, adapters, and virtual interfaces for use in class-based or UVM SystemVerilog environments, enabling early verification of communication protocols and readout paths. Although this methodology enhances design reuse and coherence between firmware and ASIC verification, it does not inherently test malformed configuration packets; such cases require a specific interface for payload overriding during simulation.

4 On-board processing capabilities with HLS

While the software-centric architecture with reusable firmware greatly simplifies adaptation of the DAQ system to different DUTs, certain applications still require real-time data processing within the FPGA fabric to achieve high performance. Tasks such as data compression, zero suppression, data-word filtering, and on-the-fly calibration are more efficiently executed through dedicated logic operating directly on the incoming data stream from the ASIC. To address this need, the system includes a predefined design template for generating custom data-processing IP cores with AXI

2026 JINST 21 C01047

Stream interfaces, these modules can be seamlessly inserted between the ASIC readout FIFO and the DMA engine. The IPs are generated from C++ algorithmic descriptions using the AMD Vitis High-Level Synthesis (HLS) tool.

5 Scaling-up to multiple devices and to custom hardware

A major limitation of the initial implementation, based on the AMD ZCU102 evaluation board, was its high cost and limited scalability, which hindered simultaneous testing of multiple ASICs. To overcome these constraints, the DAQ system is being ported to a custom-designed board, the *Supernova* in figure 2, featuring the AMD Kria production System-on-Module, which retains the same MPSoC architecture while offering a more compact and cost-effective platform.

The new hardware provides up to 80 differential pairs through an FMC HPC connector, along with Ethernet, SFP+ (up to 10 Gbps), USB, and DisplayPort interfaces. Coaxial connectors are also integrated for clock distribution and synchronization across multiple boards. For system-level timing alignment, an FPGA-based Time-to-Digital Converter (TDC) has been implemented to automatically measure the propagation delays of reset and synchronization signals between boards, ensuring precise and deterministic multi-board operation.

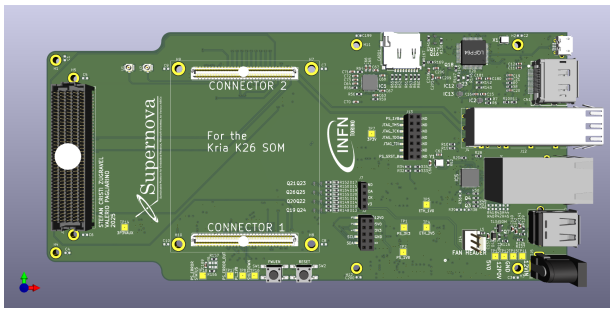

Figure 2. Custom board *Supernova*, implementing the SoC-based Test System.

6 Case studies

The SoC-based test system presented in this work has already been employed in several experimental contexts. In March 2025, it was used at the DESY Test Beam Facility [5] to characterize the MADPIX [6] monolithic CMOS sensor with internal gain optimized for sub-100 ps time resolution. The objective was to evaluate the time resolution and correlate it with the hit position of the particle inside each pixel of MADPIX. This was achieved by digitizing the signals from the CMOS sensor and an LGAD timing reference, while tracking the incident particles with a MIMOSA telescope connected to the AIDA readout system. The SoC-based DAQ managed the entire acquisition sequence: it controlled the digitizer via Ethernet, received trigger signals from the LGAD, initiated the AIDA tracker readout, acquired event identifiers from AIDA through digital links connected to the FMC interface, and associated these identifiers with the digitized waveform events before writing the data to disk and authorizing subsequent acquisitions. Additional case studies include the DENEB ASIC [1], currently in the design phase and being verified using the aforementioned Verification IP flow, and the ARCADIA MD3 [7] monolithic CMOS sensor, tested for high-resolution tracking and imaging. In

2026 JINST 21 C01047

the latter setup, the DAQ was integrated with a microfocus X-ray source for tomographic imaging. The same setup with the MD3 sensor has been used also at the LIUTO ion implantation facility in Torino [8] for beam imaging and diagnostics.

7 Conclusions and outlooks

A versatile SoC-based readout system has been developed to support the characterization of a wide range of front-end ASICs. Its modular architecture, combining reusable firmware, software-defined control, and HLS-based hardware acceleration, enables efficient adaptation to different DUTs while maintaining high data throughput and low development time. The system has demonstrated its flexibility in different use cases. Future developments will focus on three main directions: the refactoring source code to enhance ease of use; the optimization of the DMA control software to further improve data transfer performance; and the commissioning of the newly developed board.

References

[1] A. Montanari, *Scintillation imaging in GRAIN Liquid Argon detector of DUNE experiment*, 2025 *JINST* **20** C05008.

[2] R. Kugathasan, *A low-power mixed-signal ASIC for readout of SiPM at cryogenic temperature*, *PoS* **TWEPP2019** (2020) 011.

[3] V. Boppana et al., *UltraScale+ MPSoC and FPGA families*, in the proceedings of the *2015 IEEE Hot Chips 27 Symposium (HCS)*, Cupertino, CA, U.S.A. (2015), p. 1–37 [DOI:10.1109/hotchips.2015.7477457].

[4] K. Arshak, E. Jafer and C. Ibala, *Testing FPGA based digital system using XILINX ChipScope logic analyzer*, in the proceedings of the *2006 29th International Spring Seminar on Electronics Technology*, St. Marienthal, Germany (2006), p. 355–360 [DOI:10.1109/isse.2006.365129].

[5] R. Diener et al., *The DESY II Test Beam Facility*, *Nucl. Instrum. Meth. A* **922** (2019) 265 [arXiv:1807.09328].

[6] U. Follo et al., *First results on monolithic CMOS detector with internal gain*, 2024 *JINST* **19** P07033 [arXiv:2406.19906].

[7] M. Da Rocha Rolo et al., *ARCADIA fully depleted CMOS MAPS development with LFoundry 110 nm CIS*, *Front. Sens.* **6** (2025) 1603755.

[8] E. Corte et al., *The development of IBIC microscopy at the 100 kV ion implanter of the University of Torino (LIUTo) and the application for the assessment of the radiation hardness of a silicon photodiode*, *Eur. Phys. J. Plus* **140** (2025) 609 [arXiv:2501.19021].

2026 JINST 21 C01047