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A Novel Layout–Circuit Co-Design Framework for Radiation Hardening in Nanoscale Technology

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Abstract— Electronic components in space are vulnerable to radiation-induced Single-Event Effects (SEEs). This work proposes a mitigation methodology combining layout- and circuit-level analysis with targeted hardening. First, radiation-induced charge deposition through the device stack is characterized and converted into equivalent transient current pulses, yielding Single-Event Transient (SET) profiles for the given technology and topology. These profiles drive circuit-level fault injection to identify sensitive nodes, which are selectively hardened via layout modifications. Applied to a 15 nm 2:1 multiplexer, the approach improves SEE resilience with minimal delay, power, and area penalties. The hardened design increases the error threshold current by 5.69× and reduces SET duration by ~39%.

Keywords—Radiation Effect, Single Event Effect, RHBD, MUX, FinFET, Guard Rings

I. INTRODUCTION

The reliability of electronic systems in harsh radiation environments, such as space, remains a critical challenge. With continued scaling, reduced transistor pitch, current, and node capacitance have increased circuit sensitivity to radiation effects [1]. Components in such settings are persistently exposed to ionizing radiation, which can induce functional errors. A major failure mechanism is the Single Event Effect (SEE), where charged particles traverse semiconductor devices, generating transient electron–hole pairs and potentially disrupting operation [2].

In combinational circuits, SEE mainly refers to Single Event Transients (SETs). A SET is a brief, unintended voltage or current pulse in a microelectronic circuit, triggered by a high-energy particle striking a sensitive node. At the cell level, this can cause temporary erroneous outputs. If the SET persists long enough, it may propagate to downstream sequential elements and evolve into a Single Event Upset (SEU), potentially corrupting system functionality. To enhance SET immunity in combinational modules, numerous Radiation Hardening by Design (RHBD) methodologies have been proposed, spanning device, layout, and architectural levels—e.g., Triple Modular Redundancy (TMR) [3], transistor resizing [4,5], guard rings [6], and well separation [7]. However, many established techniques were conceived for earlier technology nodes. When applied to modern sub-65 nm processes, designers must meticulously balance hardening effectiveness against stringent constraints on area overhead and power consumption.

This work introduces a layout–circuit co-design framework for radiation-induced fault analysis and mitigation in nanoscale technologies. The methodology combines layout-aware particle energy deposition modeling using TRIM and RAD-RAY, a custom 3D layout-aware radiation simulation tool [8], with circuit-level fault injection in LTspice. Specifically, given a radiation profile, we combine the particle distribution and energies with the circuit's physical geometry to obtain detailed energy deposition through the stack of layers of the cell layout. Then, we provide this information, together with the cell layout, to RAD-RAY, which simulates the transient pulses generated by charged particles traversing the circuit and identifies radiation-sensitive regions. Using the extracted pulse data, we perform fault injection into the circuit netlist using LTspice to identify the most vulnerable nodes. In the optimization phase, the sensitive nodes derived from the combination of the layout and circuit-level analyses are hardened by incorporating guard ring structures, modeled and analyzed for both electrical behavior and layout-level feasibility. This integrated approach enables precise vulnerability mapping and targeted mitigation, supporting robust design in nanoscale technologies.

The developed flow has been applied to a 15nm CMOS 2:1 multiplexer (MUX), derived from the 15nm Open-Cell Library (Silvaco/Si2) [9]. Since MUX serves as a fundamental data-routing element in nearly all digital and mixed-signal systems, it is a valuable case study to validate the effectiveness of the proposed method. The experimental results indicate that, with the proposed methodology, the pulse amplitude induced by radiation–silicon interactions must be 5.69 times higher in the hardened MUX compared to its non-hardened counterpart for an error to propagate to the output. Additionally, the pulse width is reduced to approximately 39% of its original value, thereby further decreasing the likelihood of being captured by a sequential element. The delay and power overheads introduced by the approach are negligible. To the best of our knowledge, this work represents the first demonstration of such a technique implemented in a state-of-the-art 15 nm process technology.

The paper is organized as follows. Section II presents previous works related to analysis and mitigation methods for SEE effects, and Section III deeply describes our proposed methodology for the analysis and mitigation of SET. The

experimental results are reported in Section IV. Finally, Section V draws some conclusions.

II. Related Works

Extensive research has focused on developing methods to mitigate radiation effects, with RHBD currently being the most widely adopted approach. Unlike Radiation Hardening by Process (RHBP) or Radiation Hardening by Software (RHBS), RHBD does not require changes to the manufacturing process. Instead, it enhances radiation tolerance at the circuit structure or layout level, offering a better balance between compatibility, flexibility and stability. When applying RHBD techniques to address SET, reinforcement methods generally fall into three categories: transistor or gate sizing adjustments, redundant design, and protection of critical transistors.

The methodology introduced in [4,5] identifies nodes exhibiting the highest soft-error susceptibility and subsequently hardens them through transistor resizing—specifically by modifying width-to-length (W/L) ratios. Such geometric adjustments increase the critical charge (Q_{crit}) at vulnerable nodes, where Q_{crit} denotes the minimum charge deposition from an ionizing particle strike required to induce a SEU [10]. Node hardening is achieved through capacitance augmentation (elevating Q_{crit}) drive strength enhancement (accelerating charge dissipation), or hybrid implementations. Furthermore, [11] developed an optimization methodology to determine minimal transistor widths for SET attenuation in combinational circuits, achieving superior area-performance tradeoffs.

Regarding redundancy-based techniques, TMR remains among the most widely adopted approaches. TMR mitigates radiation effects by triplicating critical circuit modules and employing majority voters for output comparison. The voter determines the final output based on a "two-out-of-three" rule—if one of the modules is affected by a transient fault due to radiation, the other two (assuming they remain error-free) will outvote the corrupted result, thereby preserving the correct system behavior. Through TMR implementation, [12] realized a radiation-hardened flip-flop design with enhanced SEU immunity. Alternatively, [13] proposed a sequential circuit fault-tolerance technique that introduces redundant equivalent states for high-probability system states.

A third category of radiation-hardening solutions incorporates protective structures around susceptible transistors. The authors in [14] analyzed the latch-up phenomena with the use of guard ring structures, which mitigate radiation effects by surrounding sensitive components, such as transistors or logic cells, with a ring of diffused or implanted material connected to a stable voltage potential. The result showed that, with a higher area consumption, the guard rings are an efficient technique to reduce the parasitic effect. In [15], a new type of guard ring was proposed and analyzed in 0.18 µm CMOS technology, experimentally confirming that elevated doping concentrations in the protective layer enhance radiation hardness.

While existing techniques provide measurable radiation tolerance, their underlying principles present divergent trade-offs in modern integrated circuits. Redundancy addition and transistor resizing primarily strengthen the circuit architecture; however, as fabrication processes advance toward higher integration densities, radiation-induced malfunctions can no longer be comprehensively analyzed solely at the circuit level. Reduced junction volumes, diminished inter-cell spacing, and lower critical charge values increasingly compromise SoC reliability under radiation exposure. Conversely, guard rings, applied at the layout level, directly mitigate process-scale vulnerabilities but incur a substantial area overhead when applied indiscriminately.

This work addresses the area overhead limitation of guard rings by introducing a selective application strategy. Instead of uniformly placing guard rings across the design, we propose an analysis flow that integrates layout and circuit-level analysis to identify and protect only the most radiation-sensitive nodes. Therefore, achieving radiation sensitivity improvement with minimal area overhead.

III. The Layout-Oriented Analysis and Mitigation Methodology

The complete methodology is illustrated in Fig. 1. The framework takes as input both the GDSII layout file and the corresponding SPICE netlist. The GDSII file provides detailed physical information—including cell geometry, metal layer stack, and port locations—which is used for modeling energy deposition from ionizing particles. The SPICE netlist, on the other hand, allows for circuit-level simulation of transient fault propagation, with radiation-induced effects modeled as injected current glitches.

By combining physical and electrical domains, the methodology enables precise vulnerability mapping of internal nodes within the logic cell. Once sensitive nodes are identified through systematic fault injection, they are hardened at the layout level by inserting guard ring structures. These structures are also modeled in LTspice to evaluate their effectiveness in suppressing transient faults, as well as to assess potential trade-offs in terms of power, performance, and area. This integrated approach ensures that both physical feasibility and electrical robustness are considered in the mitigation strategy.

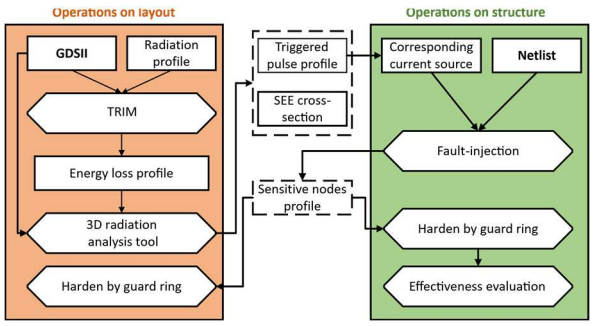


Fig. 1. The proposed analysis and mitigation workflow.

A. Layout-Level Radiation Analysis

The radiation analysis process begins with the calculation of energy deposition within the target cell regions, caused by ionizing particles traversing the device layers. This step is performed using the Transport of Ions in Matter (TRIM) tool, which takes as inputs the GDSII layout of the target cell and the characteristics of the radiation sources. In this work, the radiation sources are modeled using the energy profiles of eight heavy ions corresponding to the irradiation conditions of the UCL facility [16]. Using the geometric dimensions and material

composition extracted from the GDSII, along with the defined radiation profile, TRIM simulates the passage of each ion species through the various layers of the target cell. This simulation accounts for all physical interactions and secondary particle generation, producing as output the energy loss distribution along the ion track within the device stack.

The TRIM output, containing detailed particle energy loss data, is combined with the physical layout description of the target cell and passed as input to RAD-RAY [8], a Monte Carlo–based, three-dimensional radiation simulation framework. RAD-RAY first constructs a 3D mesh representation of the cell from the GDSII geometry, then simulates the interactions between incident heavy ions and the device's semiconductor junctions. The tool computes the total energy deposited in the silicon substrate (in electron-volts) and generates the corresponding transient voltage profiles induced by particle strikes. The simulation results obtained from RAD-RAY are employed to estimate the SEE cross-section of the logic cell, which serves as a quantitative metric for assessing the system's susceptibility to radiation-induced faults. Additionally, RAD-RAY produces a vulnerability heat map, highlighting the regions within the cell most susceptible to radiation-induced effects.

B. *Circuit-Level Sensitive Node Identification*

The transient voltage profiles generated by RAD-RAY are used as inputs for the circuit-level fault analysis to identify the most sensitive nodes of the target cell. The LTspice netlist of the cell is employed, and each transient pulse—characterized by its peak amplitude and duration—is converted into an equivalent current source according to:

$$I = \frac{C_{node} \cdot V}{\mathrm{t}} \tag{1}$$

where C_{node} is the node capacitance, V is the estimated pulse peak voltage, and t is the pulse duration. The node capacitance is a technology information retrieved by the process library, while V and t depend on the ion-matter interaction.

These equivalent current sources, which replicate the charge deposition mechanisms of energetic particles, are sequentially injected into each internal node—excluding primary inputs and outputs—during a fault-injection campaign in LTspice. For each injection, the circuit output is monitored and compared against the fault-free reference. If the output remains unchanged, the fault is classified as masked due to electrical attenuation, logical masking, or timing constraints. If the output deviates from the expected value, the corresponding node is labeled as faulty.

After injecting a statistically meaningful number of faults into each node and evaluating the probability of generating propagatable soft errors, nodes exhibiting significantly higher error rates are identified as the most vulnerable, hence requiring a mitigation strategy.

This methodology enables a detailed characterization of the temporal and spatial propagation of particle-induced transients within the circuit and provides a vulnerability map of the most critical nodes. The results offer precise guidance for the targeted placement of hardening structures, thereby enhancing the overall robustness of the design, while limiting the power and area overhead that typically affect standard mitigation strategies.

C. *Selective SET Mitigation*

The most vulnerable nodes identified through LTspice fault injection are selected for radiation hardening using guard rings. A guard ring is a doped semiconductor region placed around a transistor or logic cell and connected to either the power supply or ground, while also being tied to the substrate or well to collect stray charge. During a high-energy particle strike, the guard ring acts as a charge-absorption region: carriers generated by ionizing radiation—electrons or holes—are intercepted and redirected into the power or ground rails through junction diffusion. This prevents the collected charge from reaching sensitive internal nodes, thereby reducing the probability of transient-induced faults.

To assess the effectiveness of this mitigation, we modeled the guard ring as a network of passive and active components—including capacitors, resistors, inductors, and diodes—(Fig. 2) to emulate its electrical behavior. This model allows us to quantify not only the reduction in fault susceptibility but also potential trade-offs, such as increased power consumption and signal delay.

In parallel with circuit-level evaluation, we performed a layout-level analysis to verify the physical feasibility and measure the area overhead of guard ring insertion. The process begins by locating the transistors corresponding to the sensitive nodes identified during fault injection. Since the foundry's Process Design Kit (PDK) does not provide explicit physical coordinates for each node, transistor-level mapping is used instead. Once the target transistors are identified, guard rings are inserted using diffusion layers, contacts, and metal interconnects. This step requires compliance with the design rules and constraints of the target technology, as specified in the Library Exchange Format (LEF) file. In particular, the minimum spacing between standard cells and the minimum width and spacing of metal lines are strictly respected to ensure manufacturability.

Although the PDK does not include a complete Design Rule Check (DRC) file for automated layout verification, we manually ensured that the modified layout adheres to all routing and geometric constraints defined in the LEF.

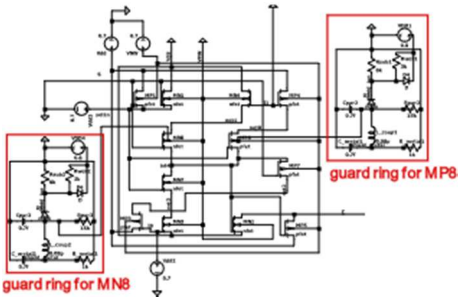


Fig. 2. Selective insertion of the equivalent guard ring network in Ltspice netlist.

IV. Experimental Results and Analysis

To validate the proposed methodology, we applied the complete analysis and mitigation flow to a 15 nm 2:1 MUX. This circuit represents a highly relevant case study, as the 2:1 MUX, thanks to its minimal logic complexity and high reusability, plays a central role in data path control, logic synthesis, and interconnect optimization, selecting between two

input signals based on a control input. In nanoscale Systems-on-Chip (SoCs), the exponential increase in the number of 2:1 MUX instances makes their reliability critical to maintaining overall system functionality. Thus, analyzing and hardening this structure offers practical insight into improving the resilience of modern digital designs under radiation-induced effects.

Radiation analysis and fault injection experiments were conducted on the MUX to identify critical nodes, which were then hardened based on the fault injection results. This chapter presents the experimental results, along with a comparison of SEE resilience, performance, and overhead before and after hardening.

A. Radiation Analysis

The radiation analysis was performed by evaluating SEEs induced by heavy-ion interactions with the MUX. To this end, we adopted a radiation profile representative of the heavy ions available at the UCL irradiation facility, which was consistently used in both TRIM and RAD-RAY simulations. The characteristics of the selected ions, including species, energy, penetration depth, and Linear Energy Transfer (LET), are summarized in Table I, forming a radiation profile compliant with radiation hardness assurance (RHA) standards.

Using the heavy-ion parameters described above, along with the GDSII layout of the 15 nm 2:1 MUX, we first conducted a depth-dependent energy deposition analysis using the TRIM tool. TRIM calculates the energy loss of each ion as it traverses the material stack of the MUX, producing a profile of energy deposition as a function of depth.

TABLE I. RADIATION PARTICLE CHARACTERISTICS [16]

Ion	DUT Energy [MeV]	Range [μmSi]	LET at surface [μm/mg/cm^2]
$^{13}C^{4+}$	131	269.3	1.3
$^{22}Ne^{7+}$	238	202.0	3.3
$^{27}Al^{18+}$	250	131.2	5.7
$^{40}Ar^{12+}$	379	120.5	10.0
$^{52}Cr^{16+}$	513	107.6	16.0
$^{58}Ni^{18+}$	582	100.5	20.4
$^{84}Kr^{26+}$	769	94.2	32.4
$^{124}Xe^{35+}$	995	73.1	62.5

This output is then used as input for RAD-RAY, which extends the analysis by incorporating the 3D physical geometry extracted from the MUX layout. While TRIM provides energy deposition relative to material layers, RAD-RAY maps this information onto the actual spatial layout, enabling a localized evaluation of SEE susceptibility within the circuit. RAD-RAY performs a Monte Carlo simulation, where 3,000 particles per ion species are simulated as they interact with the 3D structure of the MUX. Fig. 3 shows examples of pulses triggered by different ion species traversing the MUX layout. For each ion type, the tool generates a vulnerability heatmap, highlighting the regions of the layout most affected by radiation-induced charge deposition. An example is shown in Fig. 4, where Xenon, the ion with the highest LET, is used to visualize the worst-case scenario. Fig. 4(a) shows the annotated layout of the MUX with labeled transistors, while Fig. 4(b) presents the corresponding vulnerability distribution under Xenon strikes. This visualization enables intuitive identification of the most radiation-sensitive regions in the cell.

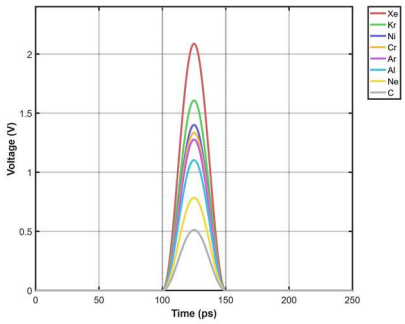
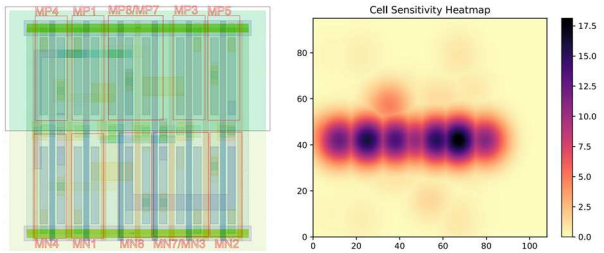


Fig. 3. Examples of pulses triggered by different particles

In addition to the spatial analysis, RAD-RAY also outputs the SEE cross-section as a function of LET, allowing for a quantitative assessment of radiation susceptibility across different ion species. Fig. 5 presents the SEE cross-section of the MUX.



(a) (b)

Fig. 4. The 15nm 2:1 MUX layout (a) and the vulnerability region reporting for the Xenon energy analysis (b).

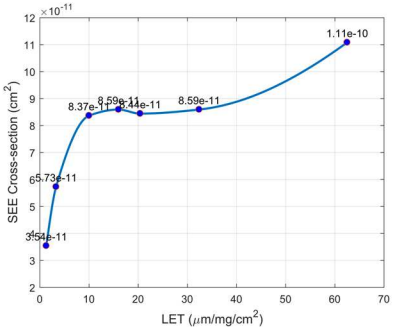


Fig. 5. The SEE cross-section of the 15nm 2:1 MUX.

B. Fault Injection

Through radiation analysis, we have characterized the transient pulses induced by particle impacts. To evaluate their potential effect on the circuit's electrical performance, we employ fault injection. The pulses are modeled as equivalent current sources and applied to each node of the MUX. By comparing the MUX output after fault injection with the ideal output, we can identify whether the transient pulses induce

propagatable errors. For each node, the minimum pulse amplitude required to cause an error serves as a measure of its radiation sensitivity—the lower the threshold, the more susceptible the node is to radiation effects.

The 15 nm 2:1 MUX structure provided by Silvaco/Si2[9] is designed with a CMOS architecture and its external ports include a data select port S, a data output port Z, and data configuration ports I1 and I0, where I1 and I0 are connected via an inverter. The Boolean equation for this 2:1 MUX is shown in (2).

$$Z = \overline{S} \cdot I0 + S \cdot I1 \tag{2}$$

Given that the function of a 2:1 MUX is to select one of the two stored input signals based on a select signal, an inverter built with the same 15 nm process transistors is connected to the output port to monitor logical correctness. If the inverter produces an output that is logically opposite to the expected value, the injected pulse is considered to have caused a propagatable soft error.

To accurately determine the voltage thresholds for logic transitions in the 15 nm process, the inverter Voltage Transfer Characteristic (VTC) method is applied. A sweep of input voltages from 0 to 0.7 volts (the nominal supply voltage for the 15nm MUX) is applied to an inverter. The critical transition voltage is defined as the point where the input and output voltages intersect. Fig. 6 shows the resulting VTC curve, from which a critical voltage of approximately 335 millivolts is identified and adopted as the threshold for logic state evaluation in subsequent analyses.

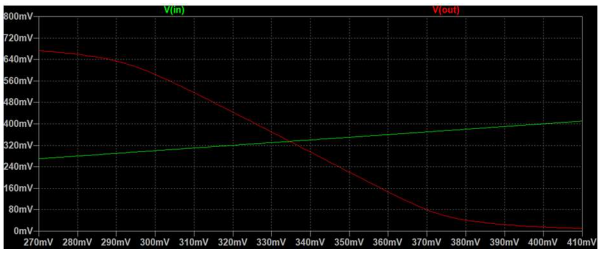


Fig. 6. The wave plot of VTC.

Given that the two data configuration ports are always complementary, the 2:1 MUX has four possible initial states. Fault injection tests were conducted for all four to cover every operating condition. Using the pulse profiles from the radiation analysis, 3,000 equivalent current sources were generated using the formula (1) in Section 3.B and injected into each of the six cell nodes. The C_{node} for the 15nm process, as shown in the process library, is 1ff under normal operating conditions. We found that the failure rate of sensitive nodes in the circuit under fault injection can reach approximately 4%, while the failure rate of other nodes remains below 1%. Table II shows the performance of the MUX cell under Xenon particle fault injection. Since the logical values of I1 and I0 are always opposite, only the logical values of I1 are listed in the table, while the names of internal nodes can be found in Fig. 2.

Simulation results show that the MUX is more vulnerable to fault injection when the output is logic high (Z=1), where even low-amplitude pulses at sensitive nodes can trigger a SET.

TABLE II. MUX CELL FAULT INJECTION RESULTS

S	I1	Most sensitive nodes	SEE threshold current [A]
0	0	Int04	8.055e-05
		Net2	8.323e-05
0	1	None	\
1	0	None	\
1	1	Int04	8.055e-05
		Net0	8.323e-05

Node int04, bridging multiple NFETs and PFETs, is the most sensitive, consistent with the heat map in Fig. 4(b). Net0 (MP4–MP8 connection) and net2 (MP7–MP3 connection) also exhibit high sensitivity under Z=1. In contrast, when Z=0, the circuit resists fault propagation—among 3000 injections, the maximum peak current (9.342×10^{-3} A) caused no errors. This behavior stems from charge-transfer dynamics: for S=0, I1=0, net2 controls the pull-up path to VDD and couples to int04 via MP7, while MP3 conduction (I0=1) makes the region highly susceptible to positive charge injection. For S=1, I1=1, net0 dominates int04 through MP8, and with MP4 conducting, it becomes the sole low-resistance path from VDD to the output.

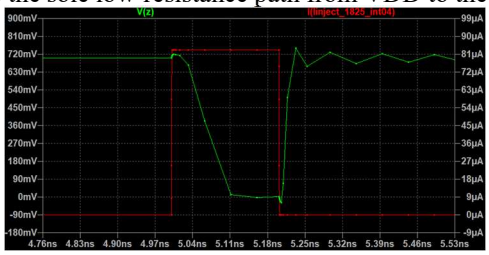


Fig. 7. An example of the injected pulse and triggered upset.

This fault sensitivity raises reliability concerns in radiation-prone environments. For example, under S=0 and I1=0, 129 of 3000 Xenon particle injections produced output-visible soft errors. As shown in Fig. 7, the weakest event caused a 0.14 ns transient inversion during a 0.2 ns pulse, which, at modern clock rates, could be latched and lead to functional errors. To mitigate this, the guard ring structure mentioned in Section 3.C was applied to the sensitive node, and a second fault injection campaign was conducted using the same pulse sources as the plain MUX. The experimental results are shown in Table III, and again, we only list the performance of the cell under Xenon injection, as the most critical one.

TABLE III. HARDENED MUX CELL FAULT INJECTION RESULTS

S	I1	Most sensitive nodes	SEE threshold current [A]
0	0	Int04	4.582e-04
		Net2	2.337e-03
0	1	None	\
1	0	None	\
1	1	Int04	4.582e-04
		Net0	2.337e-03

For the sensitive node int04, adding a guard ring increases the threshold current for propagatable soft errors by ~5.69×, while for net0 and net2, which can be critical under certain conditions, the increase is ~29×. Additionally, we measured the optimization of the guard ring on flip duration. Considering also the minimum flip-inducing pulse as an example, Fig. 8 shows that a 0.2 ns pulse with over 8× the amplitude of that in Fig. 7 produces only a 0.055 ns transient. This substantial reduction in SET duration greatly lowers the likelihood of capture and propagation, thereby enhancing reliability. Notably, the level of radiation protection can be tuned according to the allowable design overhead.

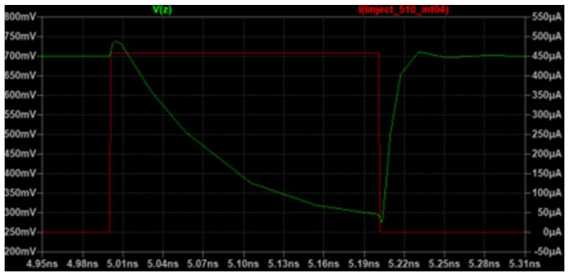


Fig. 8. An example of the injected pulse and triggered upset after hardening.

C. *Comparative Analysis*

An example of the hardened MUX layout is shown in Fig. 9. In this case, three transistors were protected using guard rings. Visually, each guard ring appears as a rectangular enclosure surrounding the original transistor geometry, forming a well-defined boundary that helps prevent charge spreading.

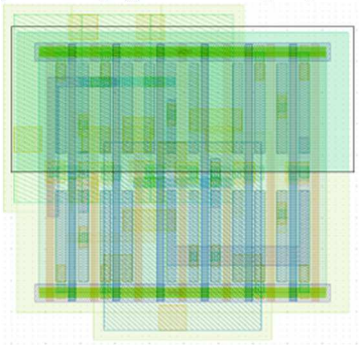


Fig. 9. The 15nm 2:1 MUX layout after hardening.

We also conducted the comparative analysis of the time delay, static power consumption, and dynamic power consumption of the 15nm 2:1 MUX cell before and after the insertion of the guard rings. The comparative results can be seen in Table IV.

TABLE IV. MUX CELL CHARACTERISTICS COMPARISON

Characteristics	Original cell	Hardened cell
Time delay [ps]	5.267	6.918
Statisic power consumption [W]	2.532e-05	2.534e-05
Dynamic power consumption [J]	2.531e-13	2.537e-13
Area overhead [μm^2]	0.226	0.257

Results show that integrating guard rings has a negligible impact on delay and power, with an area increase of ~13%. This is acceptable given that the evaluation used Xenon—a high-LET particle—as the target. In actual space missions, exposure to such particles strongly depends on the spacecraft's orbit. In Fig. 10, we plot the differential flux for the Xenon ion for different radiation environments estimated using the OMERE tool. We adopted the GCR ISO 15390 model, as established by the Space Engineering branch of the European Cooperation for Space Standardization (ECSS 10-04 Standard) and evaluated the Xenon contribution in Low-Earth Orbit (LEO), taking as reference the coordinates of the International Space Station (ISS) and in Geostationary Orbit (GEO), where typically telecommunication satellites operate. As can be seen from the plots, the flux of Xenon is reducing in LEO due to the Earth's magnetosphere, which acts as a shield for heavy ions generated outside our solar system. This suggests that guard ring dimensions can be reduced (or increased) according to specific operating environments. This adaptability enables a balanced trade-off between radiation tolerance and design overhead. Comparing our proposed method with the state of the art, it requires less additional overhead. Specifically, in [18] the proposed guard ring-based method to harden circuits, introduce 54.04% additional area overhead and 38% additional power consumption. Authors of [19] achieved radiation hardening through transistor resizing, which introduced 18.42% area overhead and 13% additional power consumption. In contrast, exploiting selective hardening through combined layout and circuit analysis, our proposed method introduces an area overhead of approximately 13%, and only approximately 0.2% of additional power consumption, while effectively increasing the overall circuit reliability.

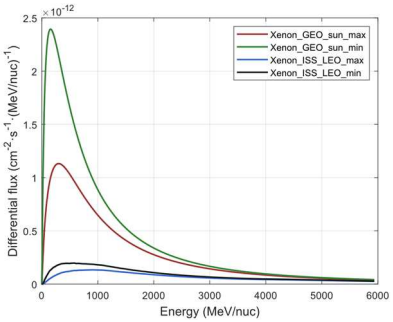


Fig. 10. Distribution of Xenon in different task enviroments.

V. CONCLUSION

This paper presents a guard ring–based radiation mitigation technique for 15 nm MUX cells, integrating 3D layout analysis with electrical evaluation to identify and harden radiation-sensitive nodes. By accurately characterizing particle–layout interactions, the method enables targeted reinforcement of vulnerable transistors and represents, to our knowledge, the first joint optimization of cell structure and physical layout in a 15 nm process. Experimental results show that the hardened MUX requires at least 5.69× higher pulse amplitude to induce a fault, with significantly shorter transient durations, while introducing negligible delay and power overhead.

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